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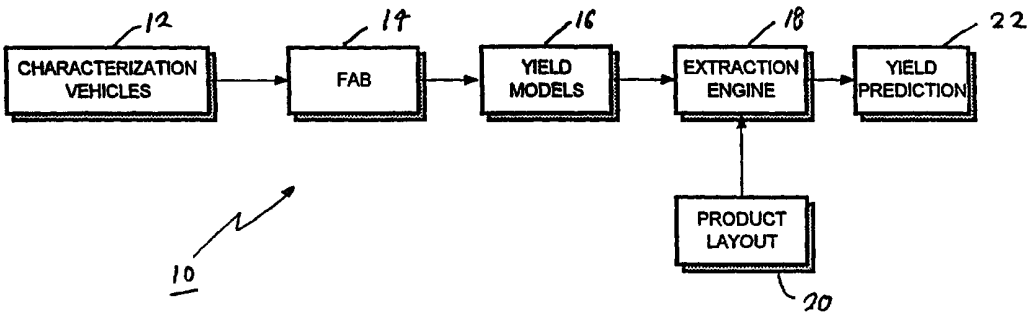
(54) Title: SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION



(57) Abstract: A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the caracterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype section at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

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SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION

Background of the Invention

The present invention pertains to fabrication of integrated circuits and more particularly to systems and methods for improving fabrication yields.

The fabrication of integrated circuits is an extremely complex process that may involve hundreds of individual operations. Basically, the process includes the diffusion of precisely predetermined amounts of dopant material into precisely predetermined areas of a silicon wafer to produce active devices such as transistors. This is typically done by forming a layer of silicon dioxide on the wafer, then utilizing a photomask and photoresist to define a pattern of areas into which diffusion is to occur through a silicon dioxide mask. Openings are then etched through the silicon dioxide layer to define the pattern of precisely sized and located openings through which diffusion will take place. After a predetermined number of such diffusion operations have been carried out to produce the desired number of transistors in the wafer, they are interconnected as required by interconnection lines. These interconnection lines, or interconnects as they are also known, are typically formed by deposition of an electrically conductive material which is defined into the desired interconnect pattern by a photomask, photoresist and etching process. A typical completed integrated circuit may have millions of transistors contained with a 0.1 inch by 0.1 inch silicon chip and interconnects of submicron dimensions.

In view of the device and interconnect densities required in present day integrated circuits, it is imperative that the manufacturing processes be carried out with utmost precision and in a way that minimizes defects. For reliable operation, the electrical characteristics of the circuits must be kept within carefully controlled limits, which implies a high degree of control over the myriad of operations and fabrication processes. For example, in the photoresist and photomask operations, the presence of contaminants such as dust, minute scratches and other imperfections in the patterns on the photomasks can produce defective patterns on the semiconductor wafers, resulting in defective integrated circuits. Further, defects can be introduced in the circuits during the diffusion operations themselves. Defective circuits may be identified both by visual inspection under high magnification and by electrical tests. Once defective integrated circuits have been identified, it is desired to take steps to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield of the integrated circuits meeting specifications.

In the past, many of the defects which caused poor yield in integrated circuits were caused by particulate contaminants or other random sources. Increasingly, many of the defects seen in modern integrated circuit processes are not sourced from particulates or random contaminants, especially in the earlier stages of process development or yield ramping, but rather stem from very systematic sources. Examples of these systematic defect sources include printability problems from using aggressive lithography tools, poly stringers from poorly formed silicides, gate length variation from density driven and optical proximity effects.

In attempting to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield, one is faced with the fact that any one or more of possibly several hundred processing steps may have caused a particular circuit to be defective. With such a large number of variables to work with, it can be extremely difficult to determine the exact cause or causes of the defect or defects in a particular circuit thereby making it extraordinarily difficult to identify and correct the yield detracting process operations. Detailed inspection of the completed integrated circuits may provide some indication of which process operation may have caused the circuits to be defective. However, inspection equipment often does not capture many of the systematic defect sources and/or the tools can be difficult to tune, optimize, or use effectively and reliably. Furthermore, inspection equipment, especially in recent technologies is often plagued with many false alarms or nuisance defects, as they are known, which serve to frustrate any attempts to reliably observe true defects or sources of defects.

It is typically discovered that, once a particular problem has been identified at final test after completion of the fabrication cycle, it can be confirmed that a problem in a particular process operation did exist at the time that operation was carried out, which could have been weeks or even months earlier. Thus the problem might be corrected well after the fact. At this time, different process operations may be causing problems. Thus, after the fact analysis of defective integrated circuits and identification of process operations causing these defective products is severely limited as a means for improving the overall yield of integrated circuits.

A number of attempts to predict yields instead of conducting unsatisfactory after the fact analysis have been made with varying degrees of success. Thus, there is a need for an improved system and method for integrated circuit product yield prediction.

SUMMARY OF THE INVENTION

A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the characterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype sections at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram depicting the steps performed by a preferred embodiment of the system of the present invention.

FIGURE 2 is a block diagram depicting additional steps performed by the system of the present invention to effect a feedback loop.

FIGURE 3 is an image of an illustrative short flow mask comprising a single lithographic layer.

FIGURE 4 depicts pad frames on an exemplary metal short flow chip.

FIGURE 5 depicts pads within each pad frame depicted in FIGURE 4.

FIGURE 6 depicts two types of pad frame structures which contain van der Pauw structures.

FIGURE 7 depicts locations, on the exemplary chip, of the pad frames containing the van der Pauw structures.

FIGURE 8 depicts an exemplary van der Pauw structure.

FIGURE 9 depicts exemplary locations of nest defect size distribution structures on an exemplary metal short flow chip.

FIGURE 10 depicts an exemplary nest defect size distribution structure.

FIGURE 11 depicts an exemplary Kelvin critical dimension structure.

FIGURE 12 depicts exemplary locations of Kelvin structures on an exemplary metal short flow chip.

FIGURE 13 depicts exemplary locations of snakes and combs on an exemplary metal short flow chip.

FIGURE 14 depicts exemplary snake and comb structures used in an exemplary metal short flow chip.

FIGURE 15 depicts examples of variations of border structures used in an exemplary metal short flow chip.

FIGURE 16 depicts exemplary locations of border structures on an exemplary metal short flow chip.

FIGURE 17 depicts exemplary locations of scanning electron microscope structures on an exemplary metal short flow chip.

FIGURE 18 depicts an exemplary test structure illustrating a shortable area.

FIGURE 19 depicts an exemplary test pattern for examining the yield of T-shaped endings at the ends of lines.

FIGURE 20 depicts an exemplary nest structure for extracting defect size distributions.

FIGURE 21 depicts a plot for determining the rate at which defects decay over size.

FIGURE 22(a), 22(b) and 22(c) depict, respectively, linewidth, linespace and pattern density distributions for a metal-1 layer of a sample product layout.

DETAILED DESCRIPTION

Referring now to Figure 1, there is shown a block diagram depicting the steps performed by a system, generally designated 10, for predicting integrated circuit yields in accordance with the present invention. The system 10 utilizes at least one type of characterization vehicle 12. The characterization vehicle 12 preferably is in the form of software containing information required to build an integrated circuit structure which incorporates at least one specific feature

representative of at least one type of feature to be incorporated into the final product. For example, the characterization vehicle 12 might define a short flow test vehicle of a single lithographic layer for probing the health and manufacturability of the metal interconnection module of the process flow under consideration. The structures need to be large enough and similar enough to the actual product or type of products running in the fabrication process to enable a reliable capture or fingerprint of the various maladies that are likely to affect the product during the manufacturing. More specific examples and descriptions of short flows and the structures embodied in them are described below.

Short flow is defined as encompassing only a specific subset of the total number of process steps in the integrated circuit fabrication cycle. For example, while the total fabrication cycle might contain up to 450 or more process steps, a characterization vehicle such as one designed to investigate manufacturability of a single interconnection layer would only need to include a small number, for example 10 to 25 process steps, since active devices and multiple interconnection layers are not required to obtain a yield model or allow accurate diagnosis of the maladies afflicting these steps associated with a single interconnection layer in the process flows.

The characterization vehicle 12 defines features which match one or more attributes of the proposed product layout. For example, the characterization vehicle 12 might define a short flow test vehicle having a partial layout which includes features which are representative of the proposed product layout (e.g. examples of line size, spacing and periodicity; line bends and runs;

etc.) in order to determine the maladies likely afflicting those specific design types and causing yield loss.

The characterization vehicle 12 might also define one or more active regions and neighboring features of the proposed design in order to explore impact of layout neighborhood on device performance and process parameters; model device parameters as a function of layout attributes; and determine which device correlate best with product performance. Furthermore, by constructing and analyzing a sufficient number of short flow vehicles such that the range of all possible or a major subset of all the modular components of the entire process is exercised, a full evaluation of many if not all of the yield problems which will afflict the specific product manufactured can be uncovered, modeled, and/or diagnosed.

In addition to providing information for assessing and diagnosing yield problems likely to be seen by the product(s) under manufacture, the characterization vehicle is designed to produce yield models 16 which can be used for accurate yield prediction. These yield models 16 can be used for purposes including, but not limited to, product planning, prioritizing yield improvement activities across the entire process, and modifying the original design of the product itself to make it more manufacturable.

The majority of the test structures in the characterization vehicle 12 contemplated in the invention are designed for electrical testing. To this end, the reliability of detecting faults and defects in the modules evaluated by each characterization vehicle is very high. Inspection

equipment cannot deliver or promise this high degree of reliability. Furthermore, the speed and volume of data collection is very fast and large respectively since electrical testing is fast and cheap. In this way, statistically valid diagnosis and/or yield models can be realized.

The characterization vehicle 12 is preferably in the form of a GDS 2 layout on a tape or disc which is then used to produce a reticle set. The reticle set is used during the selected portions of the fabrication cycle 14 to produce the yield model 16. Thus the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12.

The yield model 16 not only embodies the layout as defined by the characterization vehicle, it also includes artifacts introduced by the fabrication process operations themselves. The yield model 16 may also include prototype architecture and layout patterns as well as features which facilitate the gathering of electrical test data and testing prototype sections at operating speeds which enhances the accuracy and reliability of yield predictions.

An extraction engine 18 is a tool for extracting layout attributes from a proposed product layout 20 and plugging this information into the yield model 16 to obtain a product yield prediction 22. Such layout attributes might include, for example, via redundancy, critical area, net length distribution, and line width/space distribution. Then, given layout attributes from the proposed product layout 20 and data from yield models 16 which have been fabricated based

upon information from the characterization vehicles 12, product yield 22 is predicted. Using the system and method of the present invention, the predictable product yield obtainable can be that associated with each defined attribute, functional block, or layer, or the resultant yield prediction for the entire product layout.

Referring now to Figure 2, there is shown a block diagram of the system for predicting integrated circuit yields 10 in accordance with the present invention additionally comprising a feedback loop, generally designated 24, for extracting design attributes 26 from product layout 20 by means of extraction engine 28. In accordance with this feature of the present invention, the characterization vehicle 12 is developed using attributes of the product layout 20. In this case, attributes of the product layout are extracted, making sure that the range of attributes are spanned in the characterization vehicle 12. For example, the product layout is analyzed to determine line space distribution, width distribution, density distribution, the number of island patterns, in effect developing a subset of the entire set of design rules of the fabrication process, which subset is applicable to the particular product layout under consideration. With respect to patterns, the product layout analysis would determine the most common pattern, the second most common pattern, and so forth. These would be extracted by the extraction engine 28 yielding design attributes 26 encompassing all of these patterns for inclusion into the characterization vehicle 12. With respect to densities, if the analysis of the product layout reveals that the density of a first metal is from 10% to 50%, then the characterization vehicle would include the entire range of 10% to 50% for the first metal.

One type of characterization vehicle is a metal short flow characterization vehicle. The purpose of the metal short flow characterization vehicle is to quantify the printability and manufacturability of a single interconnect layer. Usually a metal short flow is run very early in the process since metal yield is crucial for high product yield, is often very difficult to obtain, and consists of only a few independent processing steps. Conducting short flow experiments using a metal short flow mask, enables experiments and analysis to be carried out in rapid succession to eliminate or minimize any systematic yield or random defect yield issue that is detected without having to wait for complete flow runs to finish.

Referring to Figure 3, there is shown an image of a typical and illustrative metal short flow mask, generally designated 30, which consists of a single lithographic layer. The mask 30 is used to define a single metal layer on a chip, and the exemplary chip 32 depicted in Figure 3 is as large as the stepper can accomodate which is, in this example, approximately 22 mm x 22 mm in size. It is divided into four quadrants, 42, 4, 46 and 48 as shown in Figure 4, each containing one or more of six basic structures: (i) Kelvin metal critical dimension structures; (ii) snake and comb structures; (iii) nest defect size distribution structures; (iv) van der Pauw structures; (v) OPC evaluation structures; and (vi) classical scanning electron microscopy (SEM) structures.

Approximately 50% of the chip area is devoted to nest structures for extraction of defect size distribution while 40% of the chip area is devoted to detecting systematic yield loss mechanisms and measuring parametric variation. Figure 3 also depicts the location of pad frames 34 on the chip. In the embodiment described herein, there are 131 pad frames on the chip, with

each pad frame 34 comprising thirty-two pads as shown in Figure 5. The pads within each pad frame 34 provide electrical connection points which are contacted by external test equipment as required by a test program to be described later.

The van der Pauw test structures 82 used in this chip (see Figure 8) are four terminal square structures which take advantage of the symmetry of the structure for direct determination of the sheet resistance. Accurate determination of sheet resistance is a requirement for measurement of linewidth variation. The van der Pauw structures 82 are arranged in two different frame types: mixed 62 (see Figure 6A) and VDP 1 64 (see Figure 6 B). Figure 7 depicts the location of the pad frames 72 containing the van der Pauw structures in the exemplary metal short flow chip described herein. In this exemplary chip, the van der Pauw structures occupy less than 1% of the chip area. In the van der Pauw structures the line width (LW) and the LW tap (see Figure 8) are the parameters that are varied. Table I shows the variations in the van der Pauw structures in the exemplary metal short flow chip described herein.

TABLE I

LW (μm)	LW tap (μm)
1 (DR)	1 (DR)
1.1	1.1
5	1
10	2
25	5
35	7
35	3.5
50	5

The nest defect size distribution structures are arrays of nested continuous lines designed for opens and shorts detection and for the extraction of defect size distribution. Line width and space between the line are the parameters that are varied to facilitate the extraction of defect size distribution. In the embodiment described herein, these structures occupy 50% of the chip area at locations 92 and 94 shown in Figure 9 and have fourteen variants in a total of ten cells 96. The amount of area these structures can occupy needs to be large enough to accurately detect less than 0.25 defects/cm^2 for one wafer. The number of variants typically include the design rule (DR), slightly below DR, slightly above DR and substantially above DR. Therefore, for example, if DR is 1.0 μm for line spacing, the plots might be for 0.9, 1.1, 1.3 and 2.5 as shown in Table II.

TABLE II

Line Width = Space (μm)	Length (cm)
0.9	39.6
1.0 (DR)	36
1.1	33
1.3	28.2
2.5	24.6

Each cell is split into six sub-cells to reduce the line resistance to reasonable levels (less than 250 kΩ) and to minimize the incidence of multiple defects per cell. In this embodiment, there are sixteen snakes per cell. An exemplary nest defect size distribution structure itself, generaly designated 1002, is depicted in Figure 10. The nest defect size distribution structures are designed such that the line width (LW) is equal to the spacing (S) between the lines to simplify subsequent analysis of data.

The Kelvin metal critical dimension (CD) structures are made up of a continuous straight line with terminal connections at each end. These structures allow for precise line resistance measurements which, in conjunction with the sheet resistance determined from the van der Pauw structures, allow for the determination of Kelvin line width. These structures are designed primarily to determine the variation in the electrical critical dimension. An exemplary Kelvin critical dimension structure, generally designated 110, is depicted in Figure 11. To study the impact of optical proximity effect on the variability in the electrical critical dimension, local neighborhood structures are varied. The parameters varied for the local neighborhood are the

number 112, line width 114 and space 116 of the lines. The global environment 118 around the Kelvin structures is also varied, primarily to study etch related effects on the electrical critical dimension (see Figure 11). Parameters varied for global neighborhood are the density and area. The global neighborhood structures can also serve other electrical measurement needs. For example, the yield of these structures can be measured so that not only metal critical dimension as a function of environment is obtained, but also yield as a function of environment. Figure 12 depicts the location of Kelvin structures 122 in the metal short flow chip described herein. These locations are chosen to cover available area. Tables III through IX describe the variations in the Kelvin structures used in the metal short flow chip described herein. These values were chosen as to cover the space identified in Figure 22(a) through 22(b). For example, the pattern density is centered around 45% and the line width and spaces are in the range of 1.0 to 3.3 μm since this is where most of an exemplary product layout is centered.

TABLE III

Line Width (μm)	Spacing (μm)	Number of Local Lines	Fixed Parameters
0.75	0.75	6	Local line width = 1μm
0.9	0.9		Density = 45%
1μm (DR)	1.0 (DR)		Line width of comb = 1.3μm
1.1	1.1		Dx max = 400 (μm)
1.3	1.3		Dy max = 400 (μm)
2.5	2.5		
3.3	3.0		
10	3.3		
	10		
	50		

TABLE IV

Line Width (μm)	Space ratio	Number of Local Lines	Fixed Parameters
0.75	2 to 1	6	Local line width = 1μm
0.9	3 to1	2	Density = 45%
1 (DR)			Line width of comb = 1.3μm
1.1			Dx max = 400 (μm)
1.3			Dy max = 400 (μm)
2.5			
3.3			
10			

TABLE V

Line Width (μm)	Number of Local lines	Local Line Width (μm)	Spacing (μm)	Fixed Parameters
0.75	1	1 (DR)	1 (DR)	Density = 0.45
0.9	2	1.3	1.3	Line width of comb = 1.3μm
1 (DR)	4			Dx max = 400 (μm)
1.1				Dy max = 400 (μm)
1.3				
2.5				
3.3				
10				

TABLE VI

Line Width (μm)	Spacing (μm)	Number of local lines	Density	LW comb (μm)	Fixed Parameters
1.0 (DR)	1.0(DR)	6	0	1.3	Dx max = 400 (μm)
1.3	1.3	2	0.2	10	Dy max = 400 (μm)
			0.40		
			0.45		
			0.50		

TABLE VII

Line Width (μm)	Spacing (μm)	Line width local (μm)	Fixed Parameters
0.9	1.0 (DR)	10	Number of local lines 2
1.0 (DR)	1.1	30	Density 0.45
1.1	1.3	100	Line width comb 1.3
1.3	2.5		Dx max = 400 (μm)
2.5	3.3		Dy max = 400 (μm)
3.3	10		
10			

TABLE VIII

Line Width (μm)	Spacing (μm)	Fixed Parameters
1.0 (DR)	1.0 (DR)	Number of local lines 6
1.1	1.1	Density - 0.45
1.3	1.3	Line width comb 1.3
2.5	2.5	Dx_max = 400(μm)
10	3.0	Dy_max = 400(μm)
	5.3	Line width local 1.3

TABLE IX

Line Width (μm)	Spacing (μm)	Local density	Dx_max	Fixed Parameters	Comments
0.75				Number of local lines 0	Isolated Kelvins
0.9				Density 0	
1.0 (DR)				Line width comb 0	
1.1				Line width local 0	
1.3				Dx_max = 400(μm)	
2.5				Dy_max = 400 (μm)	
3.3					
10					
	10	2.5		Line width = 1.0 (μm)	Local
	20	3.5		Local line width = 1.0 (μm)	neighborhood
	30	4.5		Number of local lines 2	size
	40	5.5		Density 0.45	
	50	6.5		Comb line width 1.3	
	60	7.5		Dx_max = 400(μm)	
	70	8.5		Dy_max = 400 (μm)	
	80	9.5			
			25	Line width 1.0	Global
			50	Line width local 1.0	neighborhood
			100	Space 1.0	size
			150	Number of local lines 6	
			200	Density 0.45	
			250	Line width comb 1.3	
			300	Dy_max 400 (μm)	
Line Width	Spacing	N_local	Dx_max	Fixed Parameters	Comments
1.0 (DR)	1.0 (DR)	6		D_local 5	Standards
1.3	1.3	6		Line width comb 1.3	
1.0	40	2		0.45	
1.3	40	2			

The snake, comb and snake & comb structures are designed primarily for the detection of shorts and opens across a wide variety of patterns. Snakes are used primarily for the detection of

opens and can also be used for monitoring resistance variation. Combs are used for monitoring shorts. Shorts and opens are fundamental yield loss mechanisms and both need to be minimized to obtain high product yield. Figure 13 shows the location of snakes and combs 1302 in the metal short flow chip described herein. Quadrant one 1304 also contains snakes 1402 and combs 1404 nested within the Kelvin structures asshown, for example in Figure 14. Line width (LW) and space (S), see Figure 14, are the parameters varied on these structures to study their impact on shorts and opens. Tables X through XIII describe the variations of snake and comb structures used in the metal short flow chip described herein. Again, the parameters were chosen such that the space covered in line width, line space, and density is similar to that seen in the example product layout, as shown in Figure 22(a) through 22(c).

TABLE X

LW_comb (μm)	Space (μm)	LW_snake (μm)	Fixed Parameters
20	0.9	1.0 (DR)	Dx_max = 200 μm
50	1.0 (DR)		Dy_max = 400 μm
100	1.1		
200	1.3		
300	2.5		
	3.0		
	3.3		
	10		
20	1.3	1.3	
50	3.1		
100	3.3		
200	3.5		
300	10		

TABLE XI

LW_comb (μm)	Space (μm)	Fixed Parameters
0.75	0.75	Dx_max = 200 μm
0.9	0.9	Dy_max = 400 μm
1.0 (DR)	1.0 (DR)	
1.1	1.1	
1.3	1.2	
2.0	1.3	
3.3	2.5	
10	3.0	
	3.3	
	10	

TABLE XII

Line Width (μm)	Fixed Parameters
0.75	Dx_max = 200 μm
0.9	Dy_max = 400 μm
1.0 (DR)	10 μm
1.1	
1.3	
2.5	
3.3	
1.0	

TABLE XIII

LW (μm)	Space (μm)	Fixed Parameters
20	0.7	Dx_max = 400 μm
50	1.0 (DR)	Dy_max = 200 μm
100	1.1	
200	1.3	
500	2.5	
	2.7	
	3.0	
	3.3	
	5	
	10	

Border and fringe structures are designed to study the impact of optical proximity correction (OPC) structures on shorts. These optical proximity corrections are usually added to improve via yields. However, it is necessary to check metal short yield with and without these borders to ensure that there is no detrimental impact to short yield. Borders 1502 are placed both at the end of the comb lines and in the interior of comb structures, generally designated 1504, as shown in Figure 15. Figure 16 shows the location of border structures, generally designated 1602, in the metal short flow chip described herein.

Scanning electron microscopy (SEM) structures are used for non-electrical measurements of line width through top down or cross sectional SEM. For the SEM bars in the metal short flow

chip described herein the line width is the same as the spacing between the lines in accordance with traditional SEM techniques. Figure 17 depicts the location of the SEM structures 1702 in the metal short flow chip described herein. The structures are placed at the bottom of each quadrant 1704, 1706, 1708 and 1710 of the embodiment depicted since this is where space was available.

In Figures 3 through 17, and accompanying text, an example characterization vehicle for metal yield improvement has been described. Other characterization vehicles for via, device, silicides, poly, el al, are often designed and utilized. However, the procedure and techniques for designing them are the same. For purposes of illustration, the example metal characterization vehicle will be carried through on extraction engines and yield models.

The extraction engine 18 has two main purposes: (1) it is used in determining the range of levels (e.g. linewidth, linespace, density) to use when designing a characterization vehicle. (2) It is used to extract the attributes of a product layout which are then subsequently used in the yield models to predict yield. (1) has already been described above with reference to how the line width, space and density of the snake, comb and Kelvin structures were chosen in the example characterization vehicle. Thus, most of the following discussion focuses on (2).

Since there are nearly infinite numbers of attributes that can be extracted from the product layout, it is impossible to list or extract all of them for each product. Thus, a procedure is

required to guide which attributes should be extracted. Usually, the characterization vehicle drives which attributes to extract. The process consists of:

1. List all structures in the characterization vehicle

2. Classify each structure into groups or families such that all structures in the family form an experiment over a particular attribute. For example, in the metal characterization vehicle discussed above, a table of family classifications might be:

Family	Attributes Explored
Nest structures	Basic defectivity over a few linewidths and spaces
Snakes and Combs	Yield over wide range of linewidths and spaces including very large widths next to small spaces and very large spaces next to small widths.
Kelvin-CD + van der Pauws	CD variation across density, linewidth, and linespace.
Border structures	Effect of different OPC schemes on yield.

3. For each family, determine which attributes must be extracted from the product layout. The exact attributes to choose are driven from which attributes are explored. For example, if a particular family explores yield over different ranges of space, then either a

histogram of spaces or the shortable area for each space must be extracted. For the above example, the required list of attributes might be:

Family	Attributes Explored	Attributes to Extract from Product Layout
(A) Nest structures	Basic defectivity over a few linewidths and spaces.	Critical area curves.
(B) Snakes and combs	Yield over wide range of linewidths and spaces including...	Shortable area and/or instance counts for each line width and space explored in the characterization vehicle.
(C) Kelvin-CD and van der Pauws	CD variation across density, linewidth, and space	Histograms of pattern density, linewidth, and linespace (similar to example shown in Figure 22)
(D) Border structures	Effect of different OPC schemes on yield	For each OPC scheme selected to use on product layout, the shortable area or instance count.

4. Use the attributes extracted in the appropriate yield models as previously described.

For other characterization vehicles, the families and required attributes will obviously be different. However, the procedure and implementation is similar to the example described above.

As previously stated, the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12. In the preferred embodiment, the yield is modeled as a product of random and systematic components:

$$Y = \left(\prod_{i=1}^{n} Ys_i \right) \left(\prod_{j=1}^{m} Yr_j \right)$$

The methods and techniques for determining Ys_i and Yr_j are as follows.

SYSTEMATIC YIELD MODELING

Since there are so many types of systematic yield loss mechanisms and they vary from fab to fab, it is not practicable to list every possible systematic yield model. However, the following describes two very general techniques and gives an example of their use especially within the context of characterization vehicles and the methodology described herein.

AREA BASED MODELS

The area based model can be written as:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)} \right]^{A(q)/A_o(q)}$$

Where q is a design factor explored in the characterization vehicle such as line width, line space, length, ratio of width/space, density, etc. $Y_o(q)$ is the yield of a structure with design factor q from the characterization vehicle. $A_o(q)$ is the shortable area of this structure and A(q) is the shortable area of all instances of type q on the product layout. $Y_r(q)$ is the predicted yield of this structure assuming random defects were the only yield loss mechanism. The procedure for calculating this quantity is described below in connection with random yield modeling.

The definition of shortable area is best illustrated with the example shown in Figure 18. This type of test structure can be used to determine if the fab is capable of yielding wide lines that have a bend with a spacing of s. In this sample test structure, a short is measured by applying a voltage between terminal (1) and (2) and measuring the current flowing from terminal (1) to (2). If this current is larger than a specified threshold (usually 1-100nA), a short is detected. The shortable area is defined to be the area where if a bridging occurs, a short will be measured. In the example of Figure 18, the shortable area is approximately x*s). The A(q) term is the shortable area of all occurrences of the exact or nearly exact patten (i.e. a large line with a spacing of s and a bend of 45 degrees) shown in Figure 18 in a product layout. The Yr(q) term is extracted by predicting the random yield limit of this particular structure using the critical area method described below.

It is important to realize that the effectiveness of this model is only as good as the number of structures and size of structures placed on the characterization vehicle. For example, if the angled bend test structure shown in Figure 18 were never put on the characterization vehicle or was not placed frequently enough to get a meaningful yield number, then there would be no hope of modeling the yield loss of wide line bends on the product layout. While it is difficult to define exactly how many of how big the test structure should be on the characterization vehicle, practical experience has shown that the total shortable area of each test structure on the characterization vehicle should ideally be such that $A(q)/Ao(q)<10$.

The above discussion has concentrated on shorts since they generally tend to dominate over open yield loss mechanisms. However, open yield loss mechanisms can be modeled equally well with this yield model so long as shortable area is replaced by open causing area.

INSTANCE BASED YIELD MODEL

The general form of the instance based yield model is:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)}\right]^{N_i(q)/N_o(q)}$$

Where Yo(q) and Yr(q) are exactly the same as in the area based yield model. Ni(q) is the number of times the unit cell pattern or very similar unit cell pattern to the test pattern on the characterization vehicle appears on the product layout. No(q) is the number of times the unit cell pattern appears on the characterization vehicle.

For example, Figure 19 shows a simple test pattern for examining the yield of T-shaped endings at the ends of lines near a space of s. This test pattern is measured by applying a voltage across terminals (1) and (2) and measuring the shorting current. If this pattern was repeated 25 times somewhere on the characterization vehicle, then No(q) would be 25x5=125 since there are five unit cells per each test structure.

If the number of times this unit cell occurs with a spacing of s near it is extracted from the product layout, the systematic yield of this type of structure can be predicted. For example, if there are five structures with 500 unit cells in each structure then No(q)=2500. If Ni(q) from some product was 10,000 and a yield of the test structures on the characterization vehicle of 98.20% was measured. Using the techniques described below, Yr(q) can be estimated as 99.67%. Using these numbers in the equation:

$$Ys_i = \left[\frac{0.9820}{0.9967}\right]^{10000/2500} = 92.84\%$$

RANDOM YIELD MODELING

The random component can be written as:

$$Y_r = e^{-\int_{x_0}^{\infty} CA(x) \times DSD(x)\,dx}$$

Where CA(x) is the critical area of defect size x and DSD(x) is the defective size distribution, as also described in"Modeling of Lithography Related Yield Losses for CAD of VSLI Circuits", W. Maly, IEEE Trans. on CAD, July 1985, pp161-177, which is incorporated by reference as if fully

set forth herein. Xo is the smallest defect size which can be confidently observed or measured. This is usually set at the minimum line space design rule. The critical area is the area where if a defect of size x landed, a short would occur. For very small x, the critical area is near 0 while very large defect sizes have a critical area approaching the entire area of the chip. Additional description of critical area and extraction techniques can be found in P. K. Nag and W. Maly, "Yield Estimation of VLSI Circuits," Techcon90, Oct. 16-18, 1990. San Jose; P. K. Nag and W. Maly, "Hierarchical Extraction of Critical Area for Shorts in Very Large ICs," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 10-18; I. Bubel, W. Maly, T. Waas, P. K. Nag, H. Hartmann, D. Schmitt-Landsiedel and S. Griep, "AFFCCA: A Tool for Critical Area Analysis with Circular Defects and Lithography Deformed Layout," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 19-27; C. Ouyang and W. Maly, "Efficient Extraction of Critical Area in Large VlSI ICs," Proc. IEEE International Symposium on Semiconductor Manufacturing, 1996, pp. 301-304; C. Ouyang, W. Pleskacz, and W. Maly, "Extraction of Critical Area for Opens in Large VLSI Circuits," Proc. IEEE International Workshop on Defect and Fault Tolerance of VLSI Systems, 1996, pp. 21-29, all of which references are incorporated in this detailed description as if fully set forth herein.

The defect size distribution represents the defect density of defects of size x. There are many proposed models for defect size distributions (see, for example, "Yield Models - Comparative Study", W. Maly, Defect and Fault Tolerance in VLSI Systems, Ed. by C. Stapper, et al, Plenum Press, New York, 1990; and "Modeling of Integrated Circuit Defect Sensitivities", C.H. Stapper, IBM J. Res. Develop., Vol. 27, No. 6, November, 1983, both of which are incorporated by reference as if fully set forth herein), but for purposes of illustrations, the most common distribution:

$$DSD(x) = \frac{D_o \times k}{x^p}$$

will be used where Do represents the total number of defects/cm^2 greater than x_0 observed. P is a unitless value which represents the rate at which defects decay over size. Typically, p is between 2 and 4. K is a normalization factor such that

$$\int_{x_o}^{\infty} \frac{k}{x^p} dx = 1$$

The following two sections describe techniques for extracting defect size distributions from characterization vehicles.

THE NEST STRUCTURE TECHNIQUE

The nest structure is designed for extracting defect size distributions. It is composed of N lines of width w and space s as shown in Figure 20. This structure is tested by measuring the shorting current between lines 1 and 2, 2 and 3, 3 and 4, ..., and N-1 and N. Any current above a given spec limit is deemed a short. In addition, opens can be testing by measuring the resistance of lines 1, 2, 3, ..., N-1, and N. Any resistance above a certain spec limit is deemed to be an open line. By examining how many lines are shorted together the defect size distribution can be determined.

If only two lines are shorted then the defect size must be greater than s and no larger than 3w + 2s. Any defects smaller than s will not cause a short at all while defects larger than 3w+2s are guaranteed to cause a short of at least 3 lines. For each number of lines shorted, an interval of sizes can be created:

Number Lines Shorted	Size Interval
2	s to 3w+2s
3	2s+w to 3s+4w
4	3s+2w to 4s+5w
...	...
N	(N-1)s+(N-2)w to (N)s+(N+1)w

It should be noted that the intervals overlap; thus, a defect size distribution cannot be directly computed. This restriction only places a limit on p extraction. Thus, in order to estimate p, a p estimate is computed from the distribution from all the even number lines and then from all the odd number lines. Finally, the two values are averaged together to estimate p. To extract p, the ln (number of faults for x lines shorted) vs log ([x-1]s + [x-2]w) is plotted. It can be shown that the slope of this line is -p. The Do term is extracted by counting the number of failures at each grouping of lines and dividing by the area of the structure. However, for very large Do, this estimate will be too optimistic. Additional information on extracing defect size distribution from structures similar to the test structures can be found, for example, in "Extraction of Defect Size Distribution in an IC Layer Using Test Structure Data", J. Khare, W. Maly and M.E. Thomas, IEEE Transactions on Semiconductor Manufacturing, pp. 354-368, Vol. 7, No. 3, August, 1994, which is incorporated by reference as if fully set forth herein.

As an example, consider the following data taken from 1 wafer of 100 dies:

Number Lines Shorted	Number of Failures
2	98
3	11
4	4
5	2
6	1
7	0
8	0

If the structure size is $1cm^2$ then the Do would be 98 + 11 +4 + 2 +1 = 133 / (100 * 1) = 1.33 defects/cm^2. Also, the plot of log (number of failures) vs log ([x-1]s + [x-2]w) (see Figure 21) shows that p=2.05.

THE COMB STRUCTURE TECHNIQUE

Assuming a comb of width = space = s, it can be shown that the yield of this structure can be written as:

$$\ln[|\ln(Y)|] = \ln[-\int_{x_0}^{\infty} DSD(x) \times CA(x) dx] \propto (1-p) \times \ln(s)$$

Thus, from the slope of the plot of ln[|ln(Y)|] vs. ln(s), p can be estimated. The Do extraction technique is the same technique as mentioned above.

YIELD IMPACT AND ASSESSMENT

Once a sufficient number of characterization vehicles has been run and yield estimates are made for each characterization vehicle, the results are placed in a spread sheet to enable prioritization of yield activities. Tables XIV through XVI are examples of information contained in such a spread sheet. It has been divided into sections of metal yield, poly and active area (AA) yield (Table XIV), contact and via yield (Table XV), and device yield (Table XVI). The columns on the left indicate systematic yield loss mechanisms while the columns on the right indicate random yield loss mechanisms. Although the exact type of systematic failure mechanisms vary from product to product, and technology by technology, examples are shown in Tables XIV through XVI.

Usually, targets are ascribed to each module listed in the spread sheet. The further a module yield is away from a target, the more emphasis and resources are devoted to fixing the problem. For example, if the target was set artificially at 95 percent for each module in the example shown in Tables XIV through XVI, then clearly ($M_2 \Rightarrow M_3$) vias (75.12%) followed by similar vias ($M_1 \Rightarrow M_2$) (81.92%), M_1 shorts (82.25%), and contacts to poly (87.22%) are below target and, with vias ($M_2 \Rightarrow M_3$) needing the most amount of work and contacts to poly needing the least amount of work.

Within each module, it is also possible to tell where the greatest yield loss is situated. That is, is it one particular systematic mechanism being the yield down or is it merely a random defectivity problem, or is it some combination of the two? For example, as shown in Table XV, via ($M_2 \Rightarrow M_3$) yield loss is clearly dominated by a systematic problem affecting vias connected to

long metal runners on the M_3 level (77.40%). Vias from (M_1 ⇨ M_2) are affected by the same problems (91.52%) in addition to a random defectivity problem (92.49%). Solving vias (M_1 ⇨ M_2) yield problems would require fixing both of these problems.

As shown in Table XIV, M_1 yield loss is also dominated by a random defectivity issue (85.23%) in addition to a systematic problem affecting wide lines near small spaces (96.66%). Fixing both of these problems would be required for improving Metal 1. Similar conclusions can be made for other modules in the spread sheet.

For the worst yielding modules, frequent running of further characterization vehicles for this module would be required. Usually, splits will be done on these characterization vehicles to try and improve and validate those improvements in module yield. For the modules which are within target, routine monitoring of short flow characterization vehicles would still be required to validate that there has been no down turn or other movement in module yield. However, these characterization vehicles can be run less frequently than for those modules with known problems.

TABLE XIV

Opens and Shorts (Metal Layers)

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Do	P	Estimated Yield	
Metal-1	Random Yield				0.7 defects/cm^2	2.3	85.23%	
	Wide lines near small space	0.034		96.66%				
	Wide space near small lines	0.00014		99.99%				
	Yield for OPC structures		72,341	99.86%				
	Bent lines		492	100.00%				
	Total for M1						82.25%	
Metal-2	Random Yield				0.35 defects/cm^:	1.92	97.45%	
	Wide lines near small space	0.00079		99.92%				
	Wide space near small lines	0.000042		100.00%				
	Yield for OPC structures		1040372	97.94%				
	Bent lines		103	100.00%				
	Total for M2						95.36%	
Metal-3	Random Yield				0.25 defects/cm^:	2.02	96.92%	
	Wide lines near small space	0.0000034		100.00%				
	Wide space near small lines	0		100.00%				
	Yield for OPC structures		352	100.00%				
	Bent lines		7942	99.92%				
	Total for M3						96.84%	
	Open and Shorts (Poly and AA Layer)							
Poly	Random Yield (without silicide)				0.17 defects/cm^:	2.03	99.81%	
	Random Yield (with silicide)				4.34defects/cm^:	4.56	89.54%	89.71%
	Wide lines near small space	0		100.00%				from silicide
	Wide space near small lines	0.01203		98.80%				
	Yield for OPC structures		0	100.00%				
	Bent lines		786541	92.44%				
	Over wide AA	0.034		96.66%				
	Over narrow AA	0.101		99.00%				
	Total for Poly						87.22%	
AA	Random Yield (without silicide)				1.3	3.45	99.12%	
	Random Yield (with silicide)				1.7	3.02	98.72%	99.60%
	Wide lines near small space		10952	99.96%				from silicide
	Wide space near small lines		0	100.00%				
	Total for AA						98.70	

TABLE XV

Contacts and Vias

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield	
Contact to Poly	Random Yield (without silicide)				2.20E-09	3270432	99.28%	
	Random Yield (with silicide)				3.10E-09	3270432	98.99%	99.71%
	Yield for Long Runners (on M1)		11,921	100.00%				
	Yield for Long Runners (on Poly)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	96.46%				
	Total for Contact to Poly						94.80%	
Contact to n+AA	Random Yield (without silicide)				2.20E-09	5270432	98.85%	
	Random Yield (with silicide)				3.10E-09	5270532	98.38%	99.53%
	Yield for Long Runners (on M1)		75,324	99.99%				
	Yield for Long Runners (on n+AA)		0	100.00%				
	Yield for Redundant Vias		4032007	99.60%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (n+)						96.78%	
Contact to p+AA	Random Yield (without silicide)				2.20E-09	6093450	98.67%	
	Random Yield (with silicide)				3.10E-09	6093450	98.13%	
	Yield for Long Runners (on M1)		96,732	99.99%				
	Yield for Long Runners (on p+AA)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (p+)						96.74%	
Vias M1->M2	Random Yield (single vias)				1.10E-08	7093210	92.49%	
	Yield for Long Runners (M2)		88640	91.52%				
	Yield for Long Runners (M1)		97645	99.03%				
	Yield for Redundant Vias		11003456	96.91%				
	Yield for Isolated Vias		119582	96.81%				
	Total for Via M1-M2						81.92%	
Vias M2->M3	Random Yield (single vias)				3.10E-09	4002063	98.77%	
	Yield for Long Runners (M3)		256128	77.40%				
	Yield for Long Runners (M2)		103432	96.97%				
	Yield for Redundant Vias		7096230	99.29%				
	Yield for Isolated Vias		1024	99.99%				
	Total for Via M2-M3						75.12%	

TABLE XVI

	Devices	Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism		
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield
NMOS	Random Yield (Logic Xtor)				2.90E-09	1395228	99.60%
	Random Yield (SRAM Xtor)				2.80E-09	2226720	99.38%
	S/D Shorts				1.00E-09	3621948	99.64%
	Bent Transistors		1113360	99.89%			
	Near Large AA		754000	99.92%			
	Near Small AA		1023452	99.90%			
	Total for NMOS Transistors						98.33%
PMOS	Random Yield (Logic Xtor)				1.80E-09	1491003	99.73%
	Random Yield (SRAM Xtor)				3.10E-09	1113360	99.66%
	S/D Shorts				9.00E.10	2604363	99.77%
	Bent Transistors		556680	99.94%			
	Near Large AA		789092	99.92%			
	Near Small AA		1309970	99.87%			
	Total for PMOS Transistors						98.89%

I claim:

I claim:

1. A system for predicting yield of integrated circuits comprising:

a) at least one type of characterization vehicle including at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) a yield model which embodies a layout as defined by the characterization vehicle, said yield model having been subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) a product layout; and

d) an extraction engine for extracting predetermined layout characteristics from the product layout, which characteristics are used in connection with the yield model to produce a yield prediction.

2. A system in accordance with claim 1 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

3. A system in accordance with claim 2 wherein the characterization vehicle comprises a short flow test vehicle.

4. A system in accordance with claim 3 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

5. A system in accordance with claim 4 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

6. A system in accordance with claim 3 wherein the characterization vehicle comprises a metal short flow test vehicle.

7. A system in accordance with claim 6 wherein the metal short flow test vehicle includes at least one basic structure.

8. A system in accordance with claim 7 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;

b) snake structure;

c) comb structure;

d) snake and comb structures;

e) nest defect size distribution structure;

f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

9. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

10. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

11. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one via or contact.

12. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one active device.

13. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one silicide region.

14. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

15. A system in accordance with claim 1 wherein the extraction engine is also used to determine a range of layout feature levels for use when designing a characterization vehicle.

16. A system in accordance with claim 15 wherein the layout feature range of levels includes line width, line space and line density.

17. A method for predicting a yield for an integrated circuits comprising:

a) providing information for fabricating at least one type of characterization vehicle having at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) fabricating a characterization vehicle which embodies a yield model and layout features representative of the product employing at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) providing a product layout;

d) extracting predetermined layout characteristics from the product layout; and

e) using the extracted layout characteristics in connection with the yield model to produce a yield prediction.

18. A method in accordance with claim 17 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

19. A method in accordance with claim 18 wherein the characterization vehicle comprises a short flow test vehicle.

20. A method in accordance with claim 19 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

21. A method in accordance with claim 20 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

22. A method in accordance with claim 19 wherein the characterization vehicle comprises a metal short flow test vehicle.

23. A method in accordance with claim 22 wherein the metal short flow test vehicle includes at least one basic structure.

24. A method in accordance with claim 23 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;

b) snake structure;

c) comb structure;

d) snake and comb structures;

e) nest defect size distribution structure;

f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

25. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

26. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

27. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one via or contact.

28. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one active device.

29. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one silicide region.

30. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

31. A method in accordance with claim 17 wherein the extraction engine is also used to determine a range of levels for use when designing a characterization vehicle.

32. A method in accordance with claim 31 wherein the range of levels includes line width, line space and line density.

33. A method in accordance with claim 17 wherein the predetermined layout characteristics are extracted from the product layout using a process which includes the steps of:

a) listing all structures in the characterization vehicle;

b) classifying each structure into families such that all structures in each family form an experiment over a particular attribute; and

c) for each family, determine which attributes are to be extracted forr the product layout.

34. A method in accordance with claim 33 wherein the families include a family comprising nest structures for exploring basic defectivity over a selected number of line widths and spaces.

35. A method in accordance with claim 33 wherein the families include a family comprising snake and comb structures for exploring yield over a predetermined range of line widths and spaces.

36. A method in accordance with claim 35 wherein the predetermined range of line widths and spaces include relatively large line widths next to relatively small spaces and relatively large interline spaces next to relatively small line widths.

37. A method in accordance with claim 33 wherein the families include a family comprising Kelvin critical dimension and van der Pauw structures for exploring critical dimension variation across line density, width and spacing.

38. A method in accordance with claim 33 wherein the families include a family comprising border structures for exploring the effect of various optical proximity correction schemes on yield.

39. A system for determining and ranking yield loss mechanisms given characterization vehicle data and extracted layout attributes.

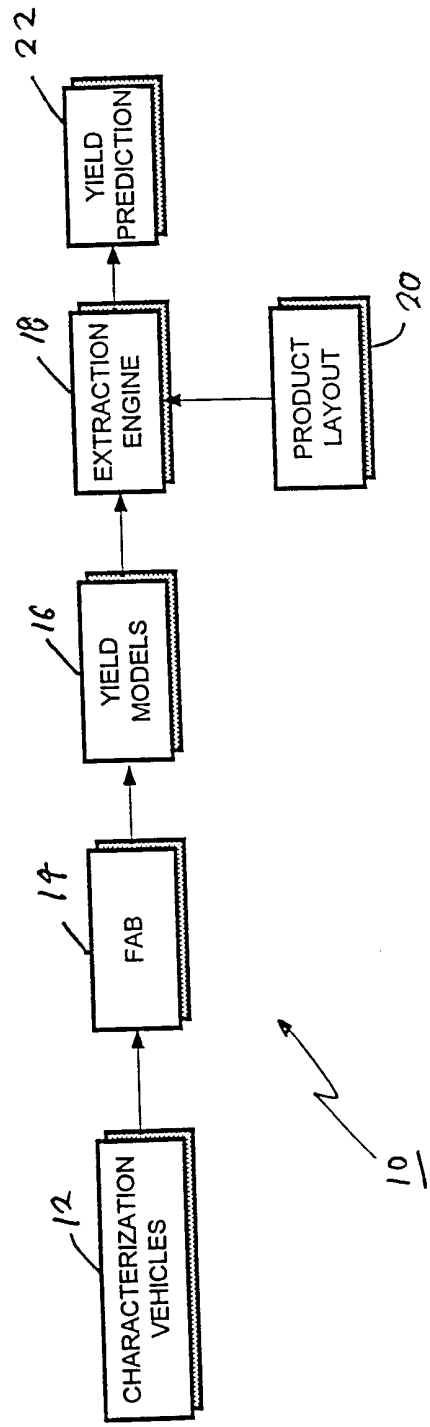
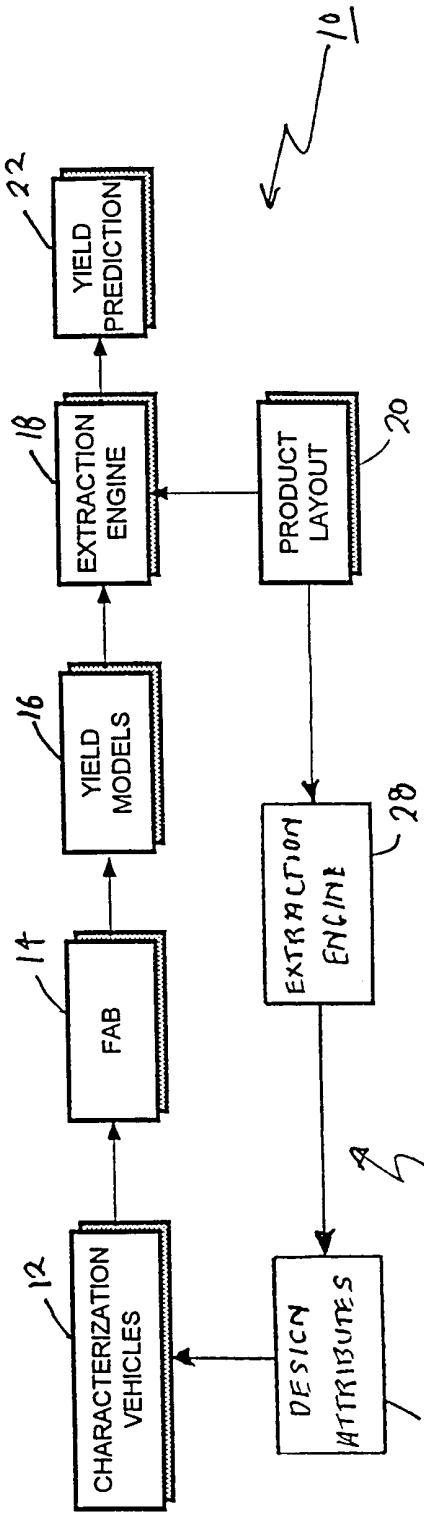

22
YIELD PREDICTION
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
16
YIELD MODELS
14
FAB
12
CHARACTERIZATION VEHICLES
10

FIGURE 1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YIELD PREDICTION
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
16
YIELD MODELS
14
FAB
28
EXTRACTION ENGINE
12
CHARACTERIZATION VEHICLES
DESIGN ATTRIBUTES
26
24

FIGURE 2

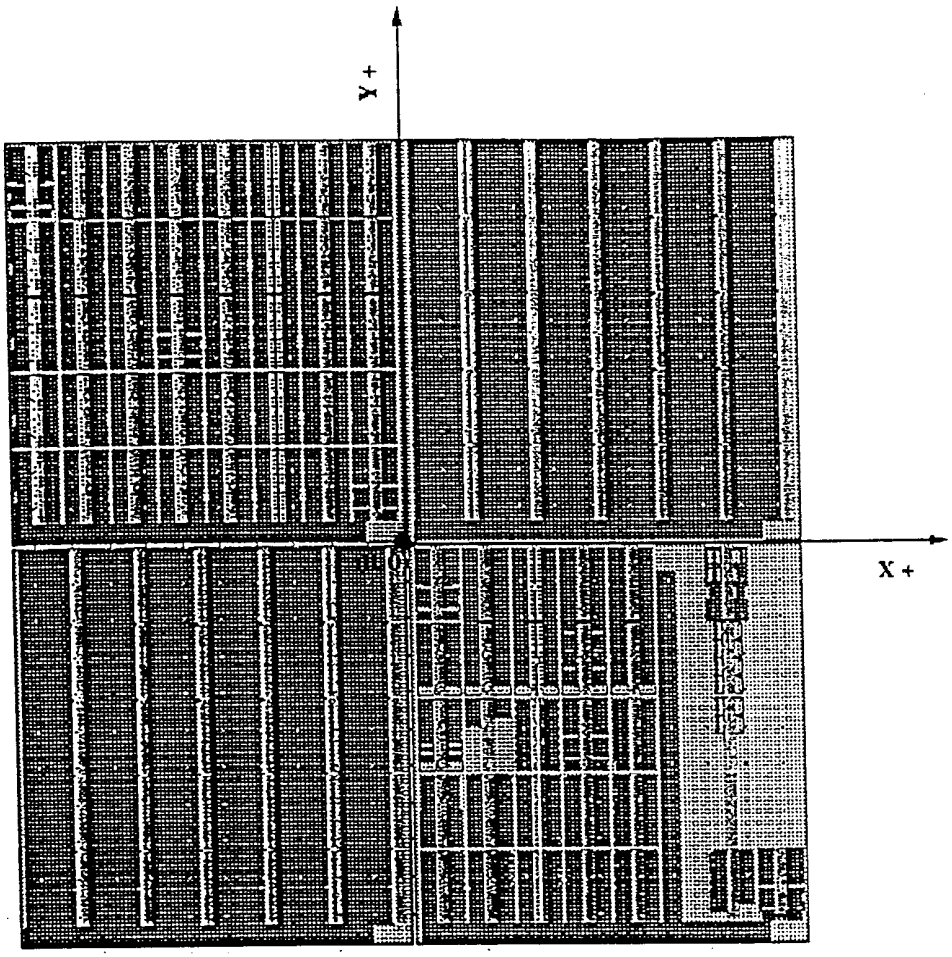


FIGURE 3

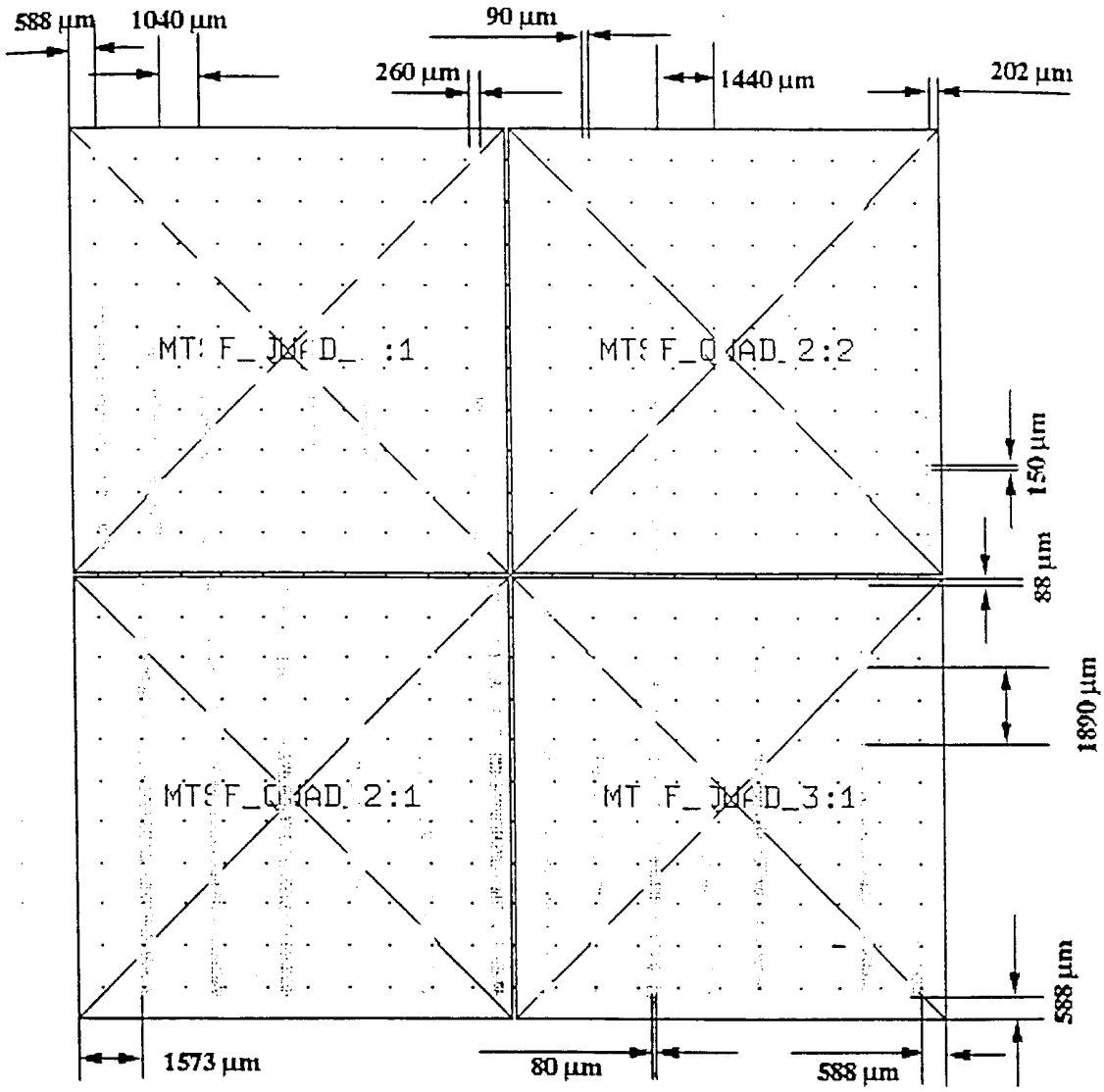

588 µm
1040 µm
90 µm
260 µm
1440 µm
202 µm
150 µm
88 µm
1890 µm
588 µm
1573 µm
80 µm
588 µm

FIGURE 4

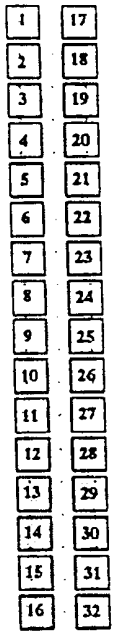
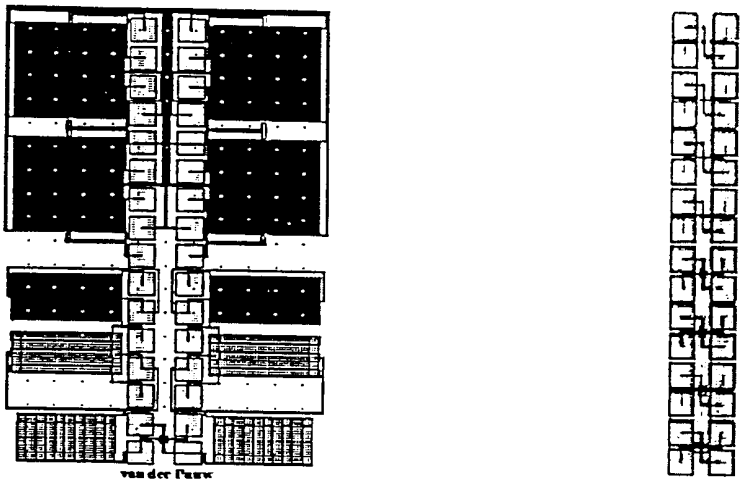


FIGURE 5



A B

FIGURE 6

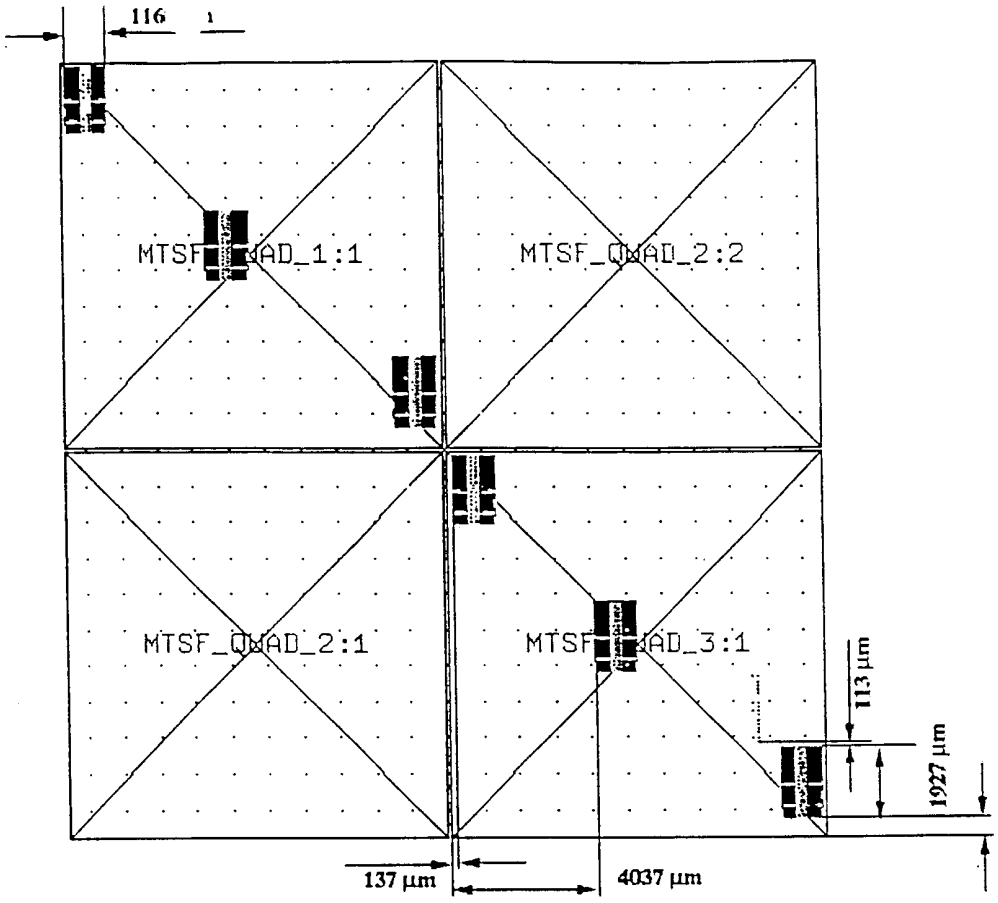


FIGURE 7

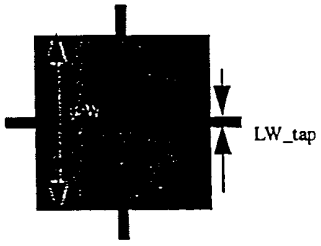


FIGURE 8

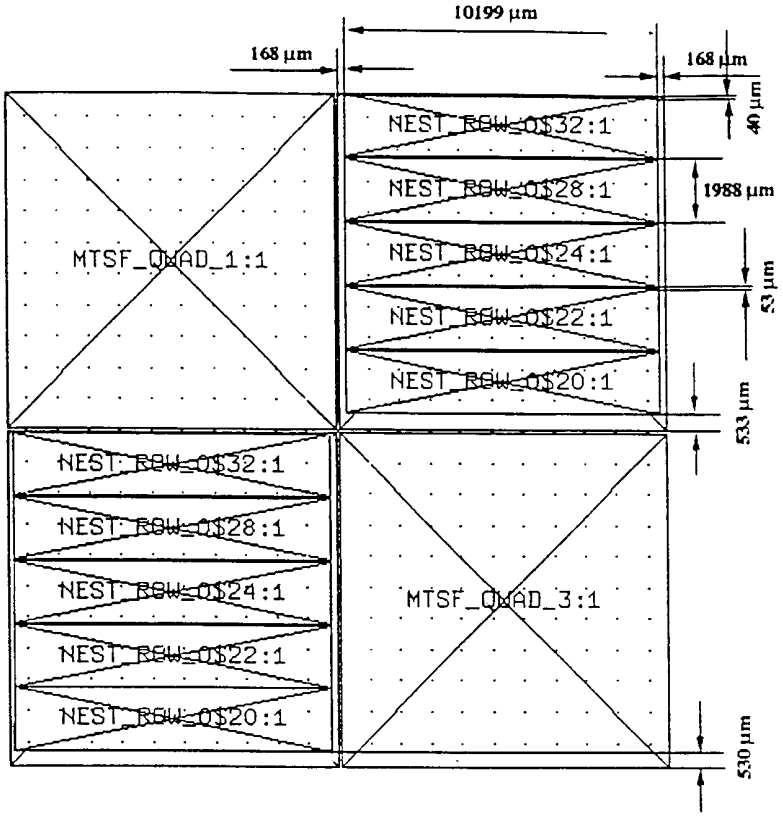


FIGURE 9

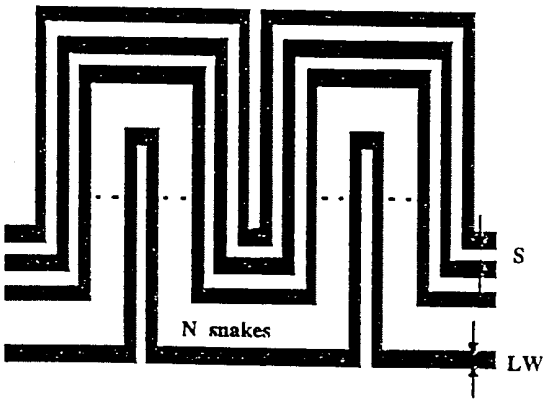


FIGURE 10

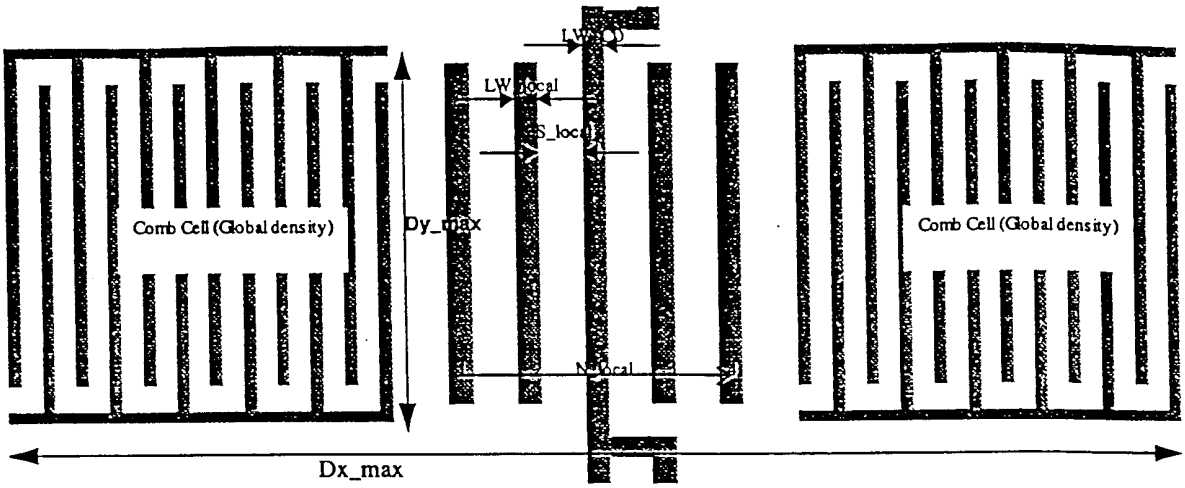


FIGURE 11

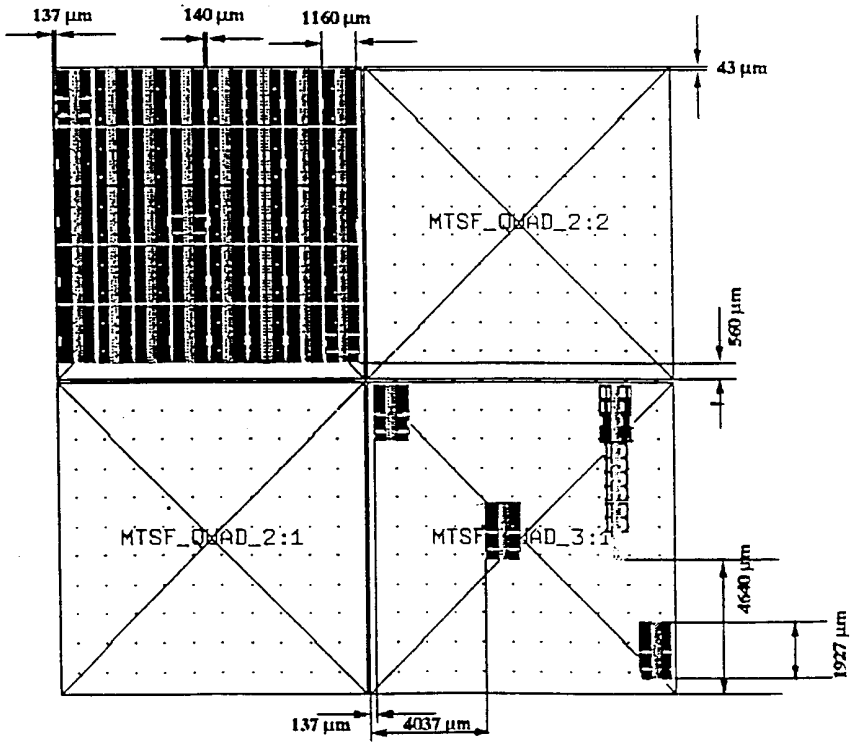


FIGURE 12

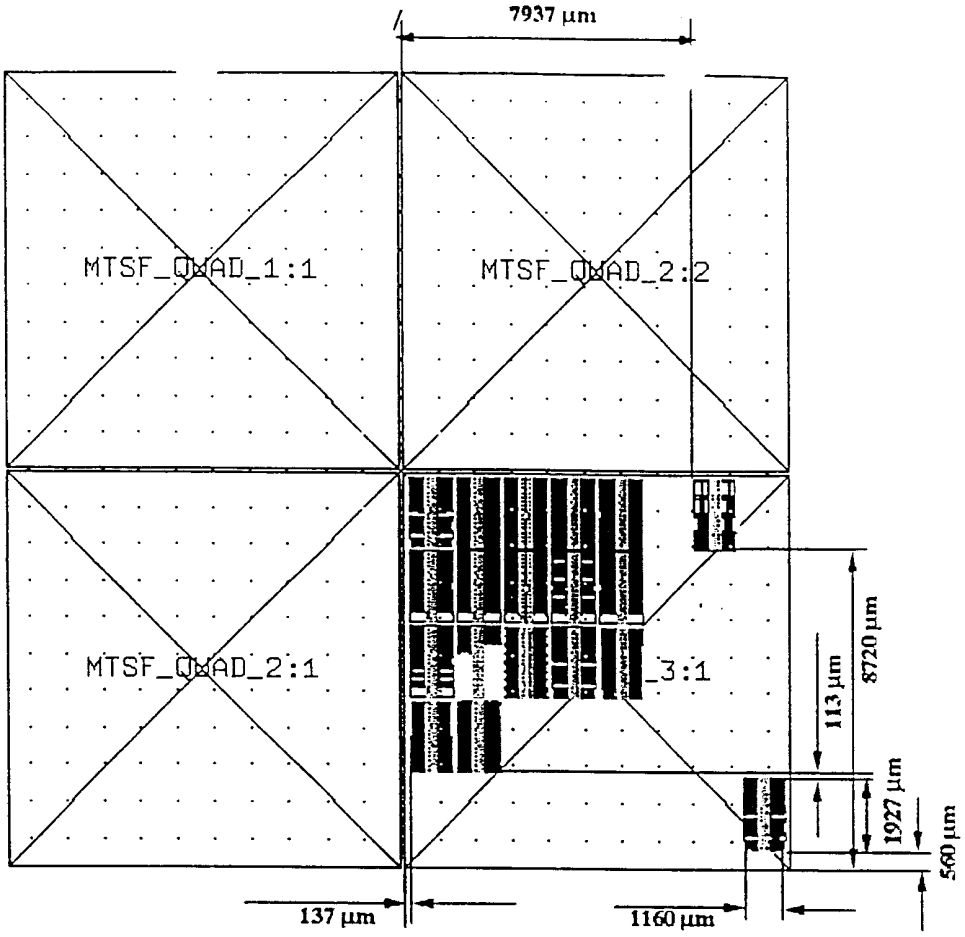


FIGURE 13

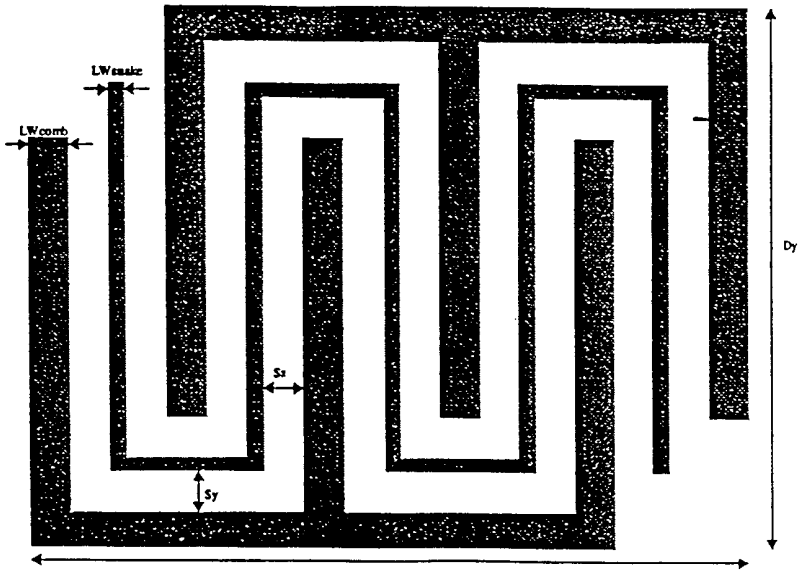


FIGURE 14

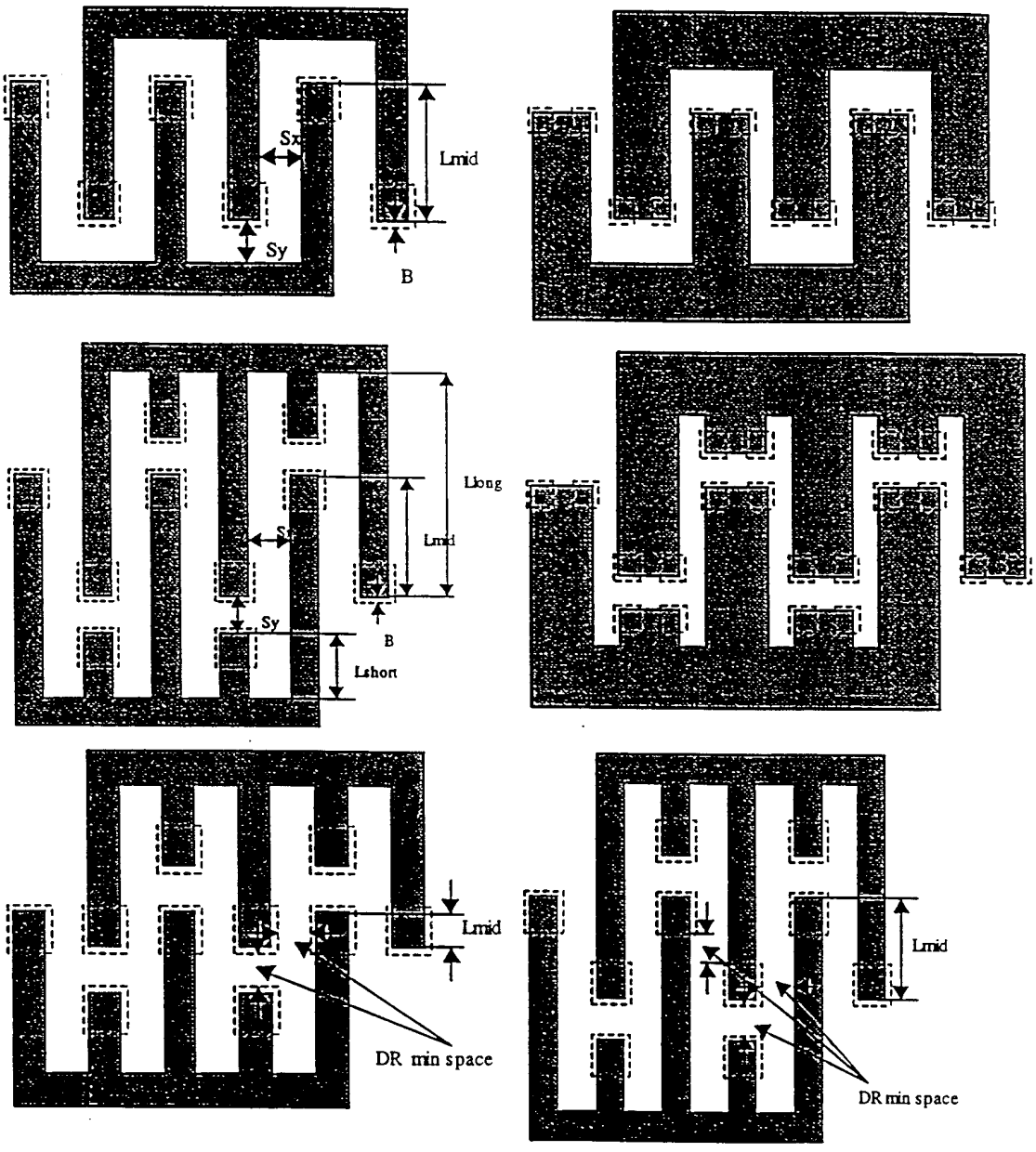

Sx
Lmid
Sy
B
Llong
Lmid
Sy
B
Lshort
Lmid
DR min space
Lmid
DR min space

FIGURE 15

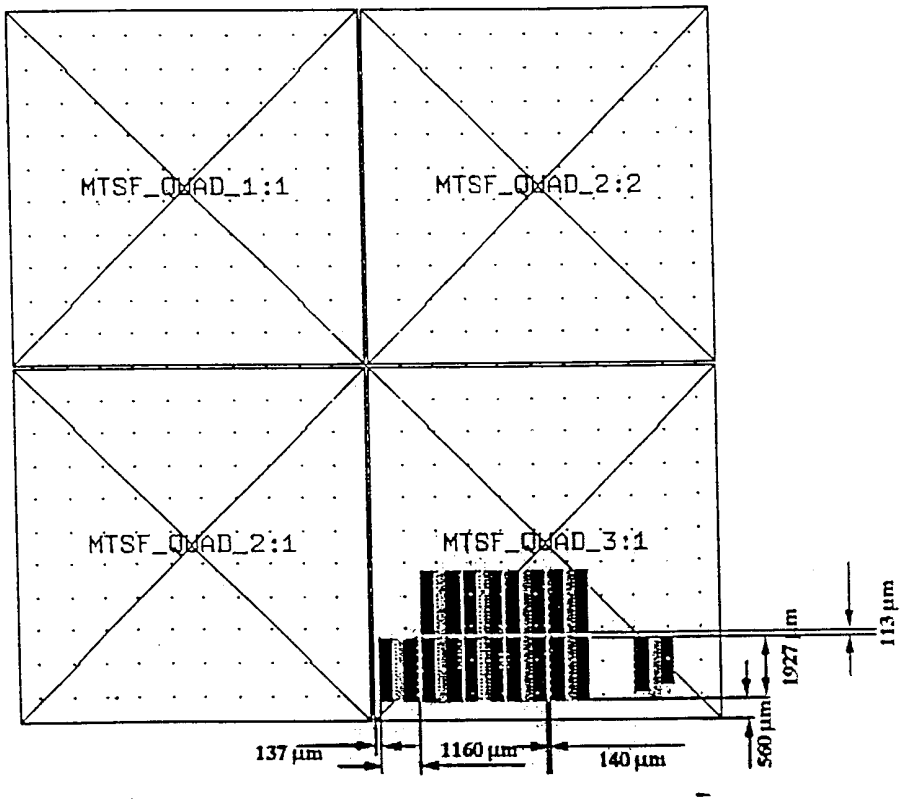

MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
137 µm
1160 µm
140 µm
560 µm
1927 µm
113 µm

FIGURE 16

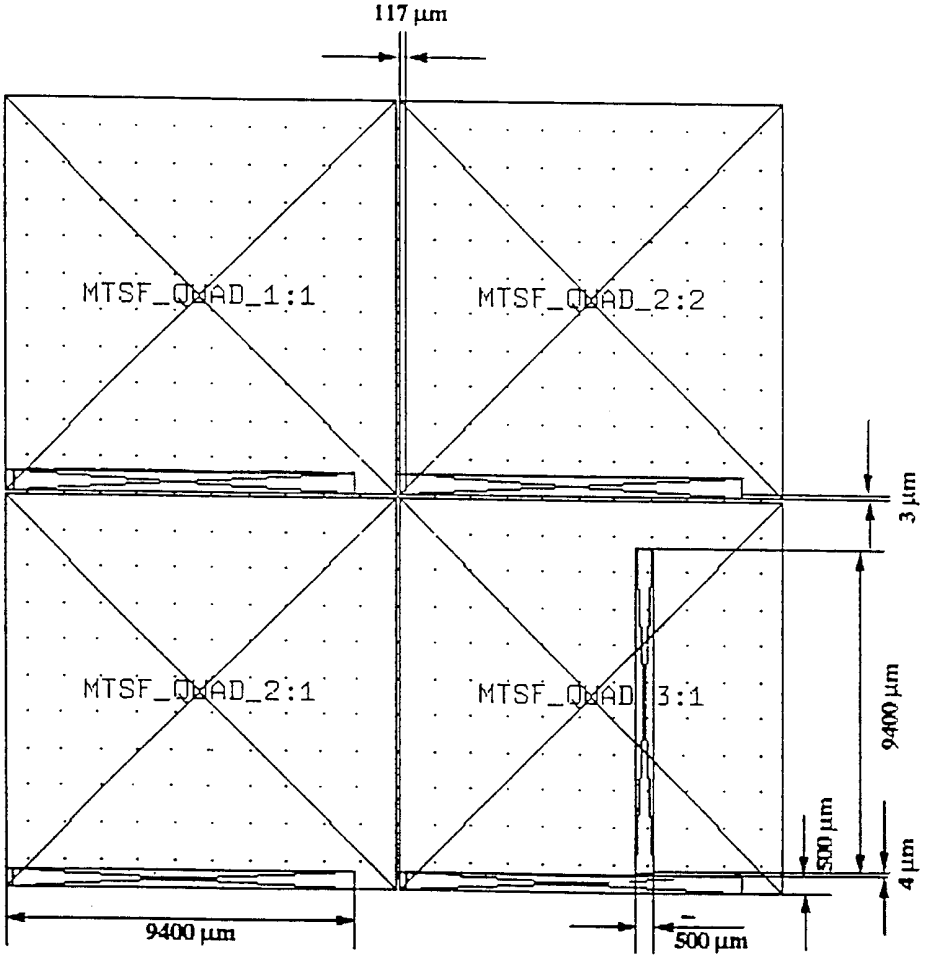

117 µm
MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
3 µm
9400 µm
500 µm
4 µm
9400 µm
500 µm

FIGURE 17

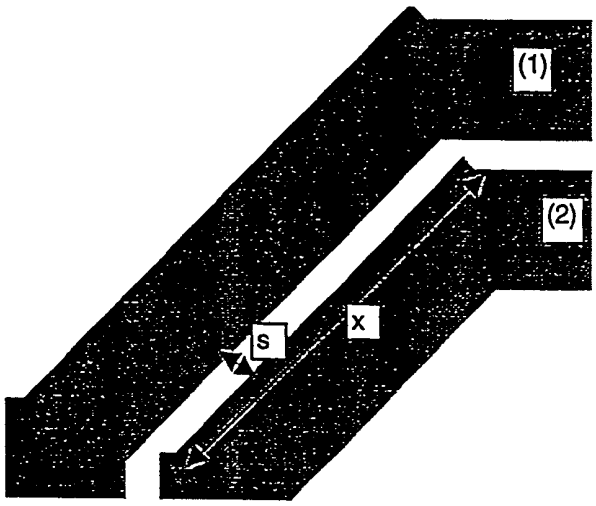


FIGURE 18

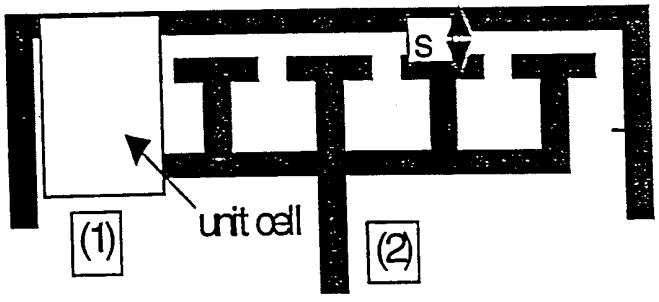


FIGURE 19

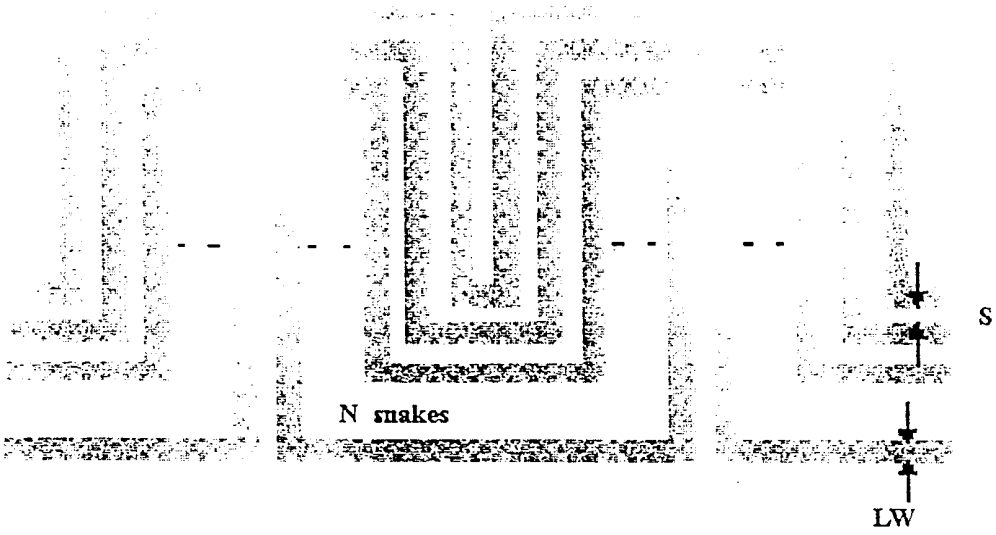


FIGURE 20

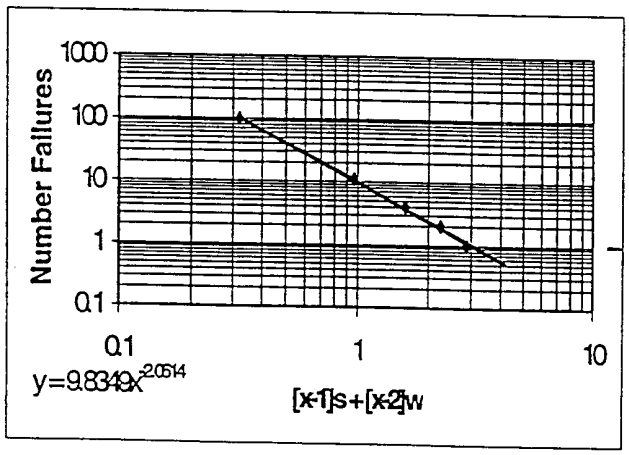


FIGURE 21

FIGURE 22(a)

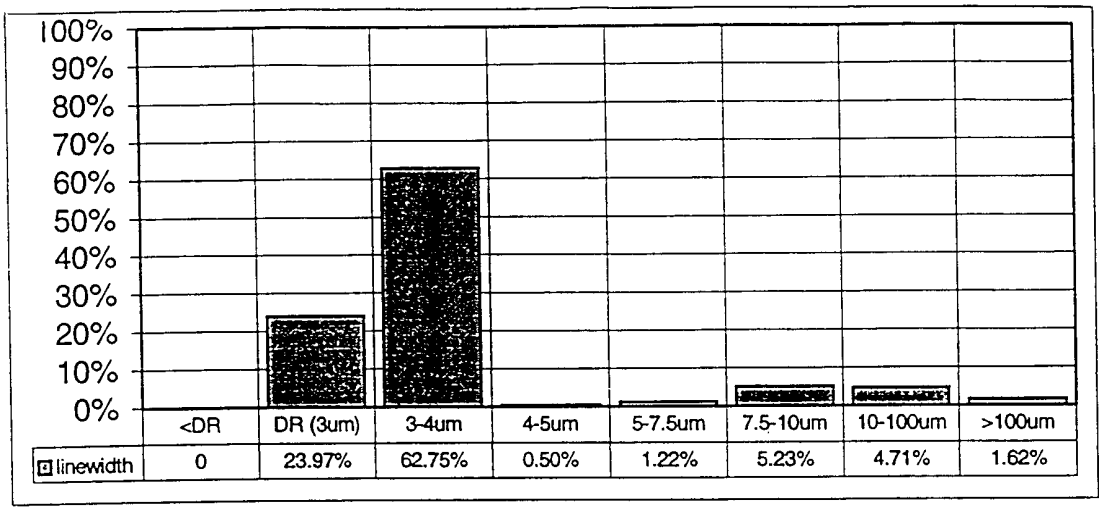


FIGURE 22(b)

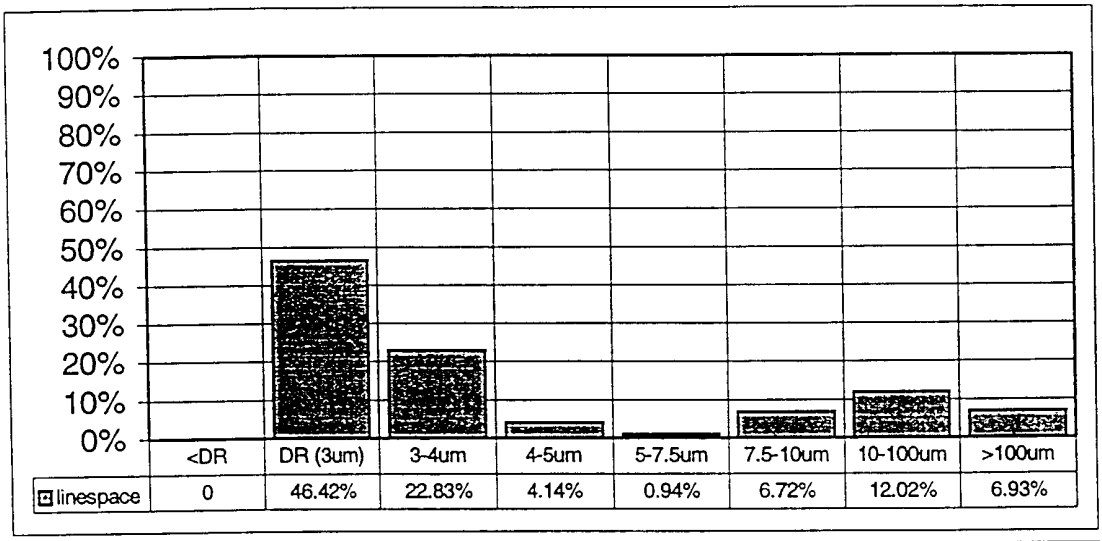


FIGURE 22(c)