United States Patent

Matsumoto et al.

[15] **3,660,643**

[45] **May 2, 1972**

[54] SHIFT REGISTER CIRCUIT

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Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 769,320, Oct. 21, 1968.

[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.**.....**235/92 J,** 235/92 R, 235/92 SH, 340/168, 317/140

[51] **Int. Cl.**.....**H03k 23/25**

[58] **Field of Search**.....235/92 SH, 92 J; 340/168; 317/140

[56] **References Cited**

UNITED STATES PATENTS

2,914,749 11/1959 Sande.....340/168 S

3,042,900 7/1962 Werts.....340/168 S

3,379,863 4/1968 Werts.....235/92 R

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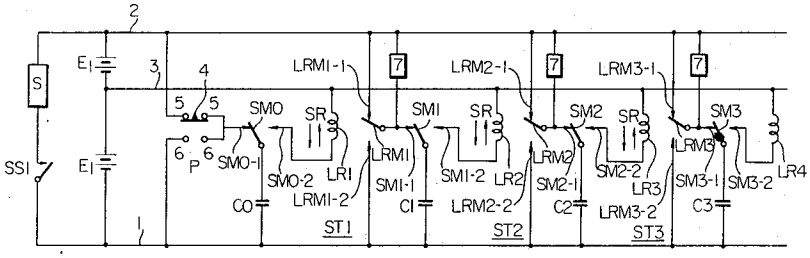
[57] **ABSTRACT**

Shift register circuits in which each register stage comprises a magnetic lutch relay and a capacitor adapted to be coupled to a movable contact of said relay through a double-throw transfer switch, two stationary contacts of said relay being connected respectively to a reference potential and a first power source of a first potential, coil of said relay having one end connected to a second power source of a second potential lower than said first potential and the other end adapted to be coupled to the capacitor in the immediately preceding stage through the double-throw transfer switch in the immediately preceding stage.

4 Claims, 7 Drawing Figures



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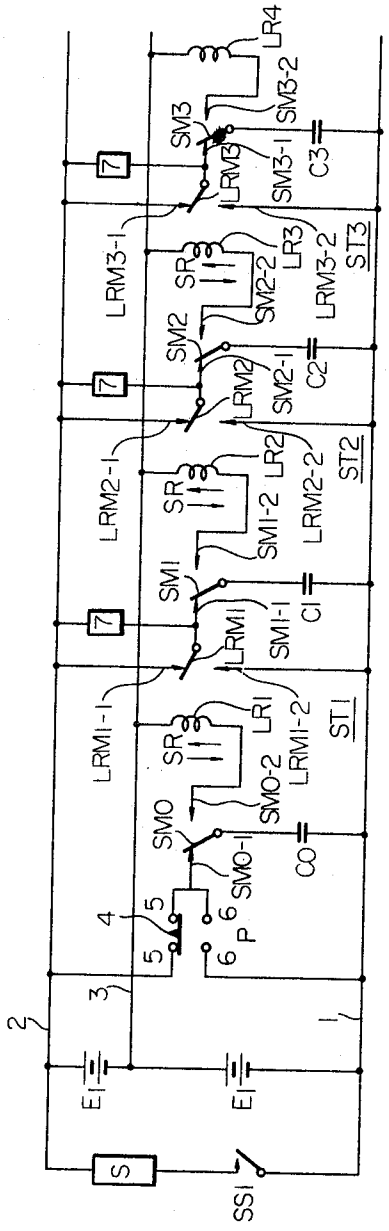
SHEET 1 OF 7

Fig. 1



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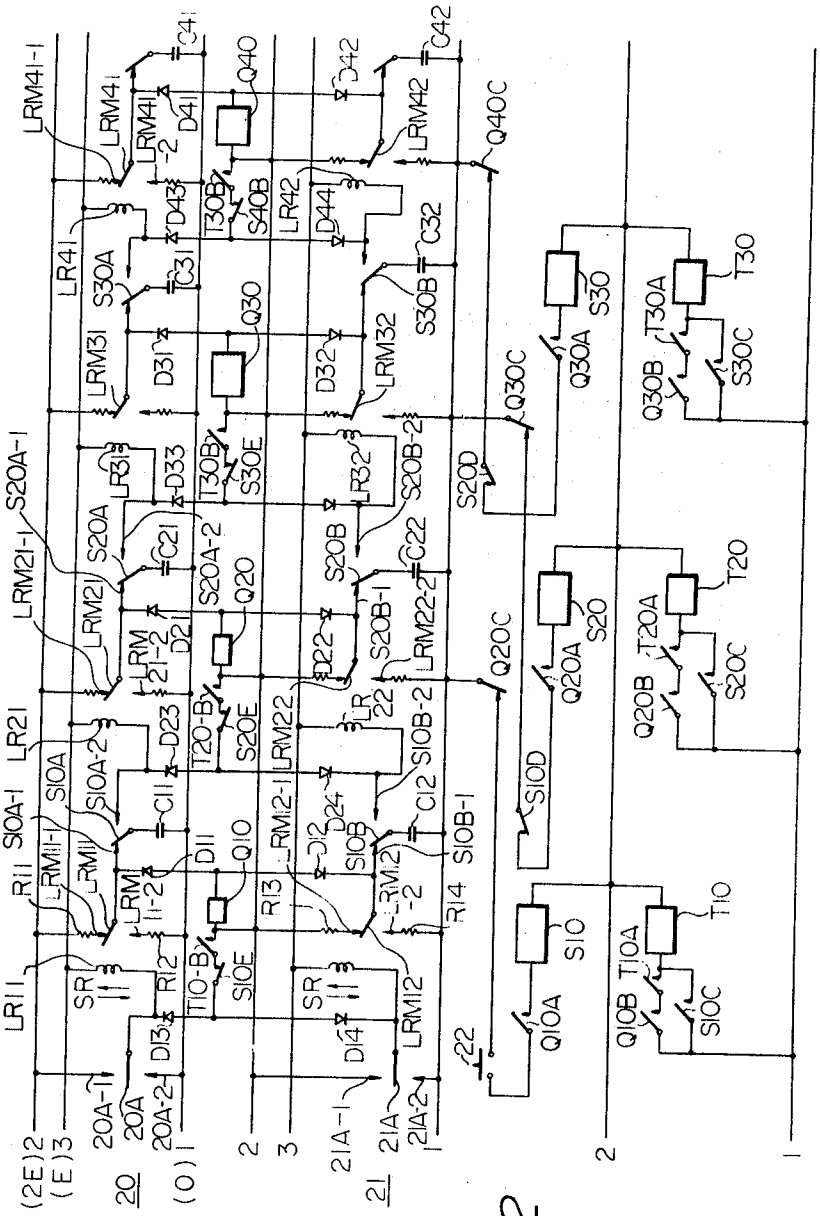

Fig. 2

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Fig. 3

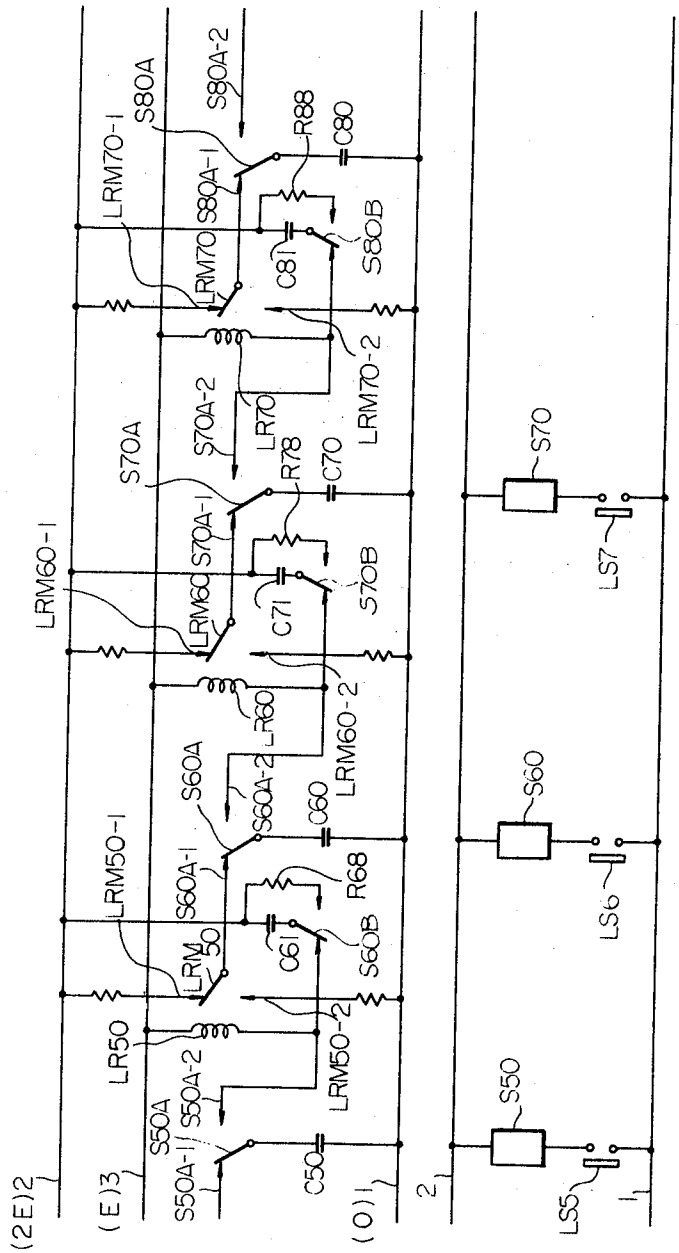

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Fig. 4

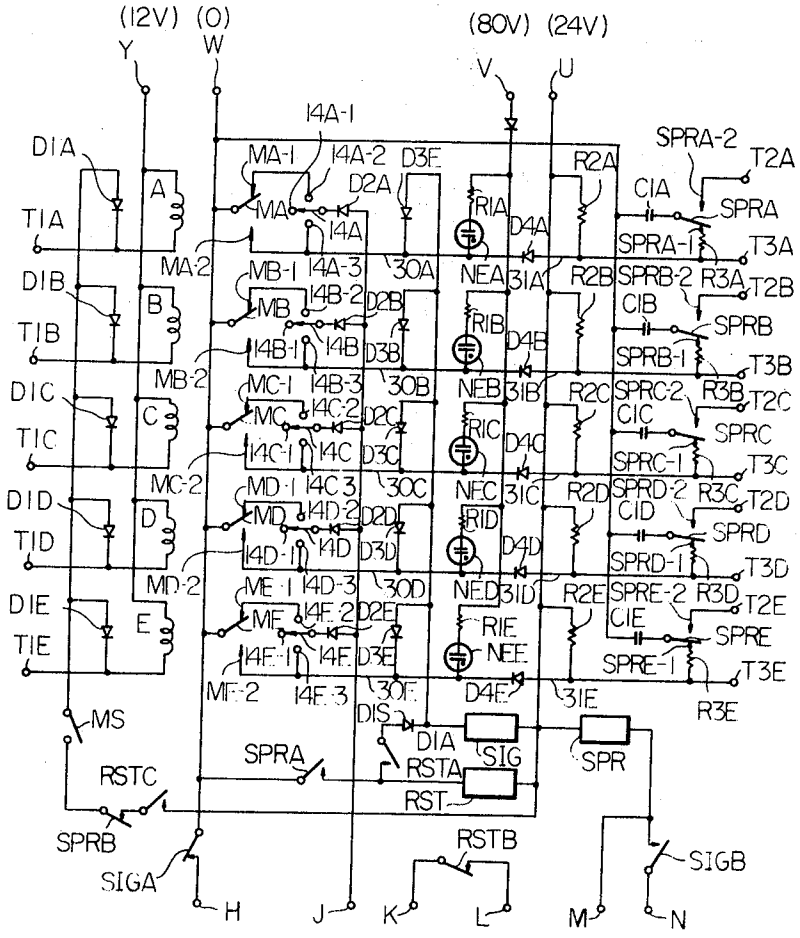

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Fig. 5

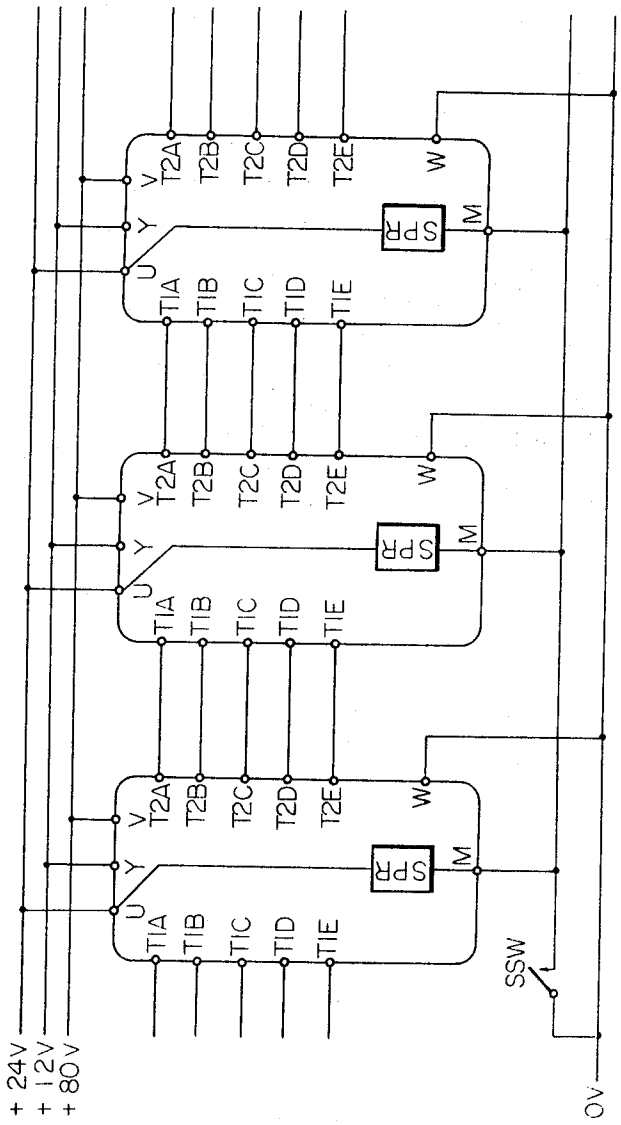

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Fig. 6

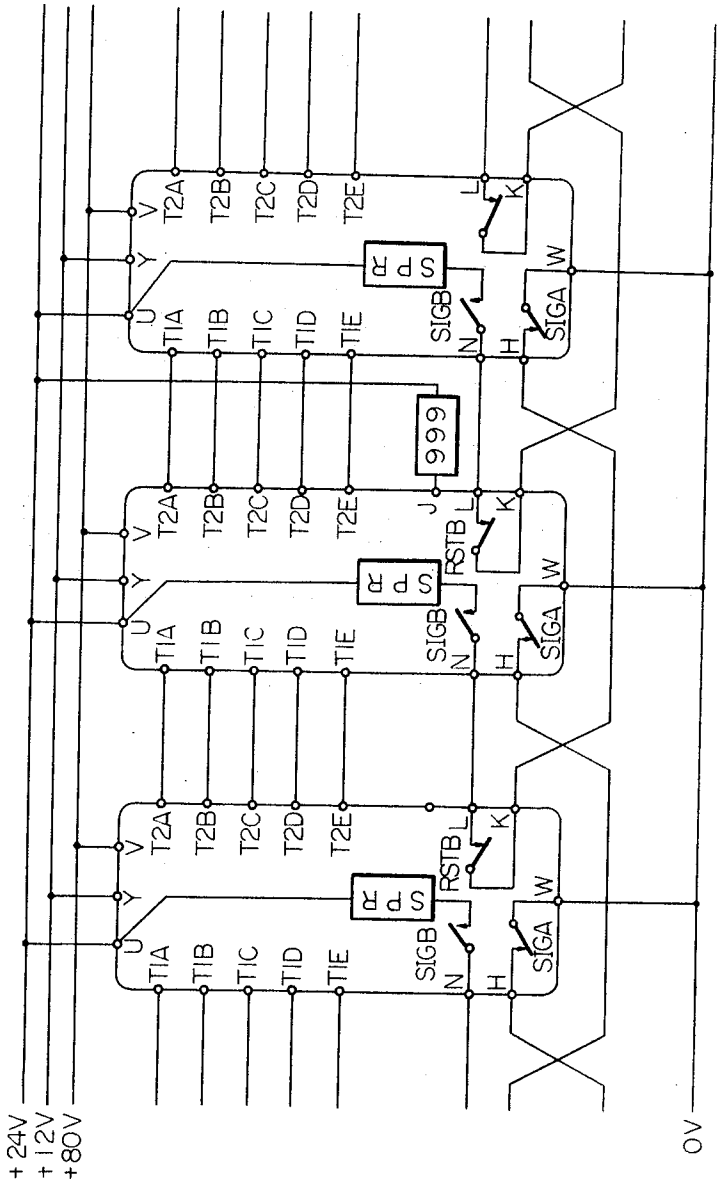

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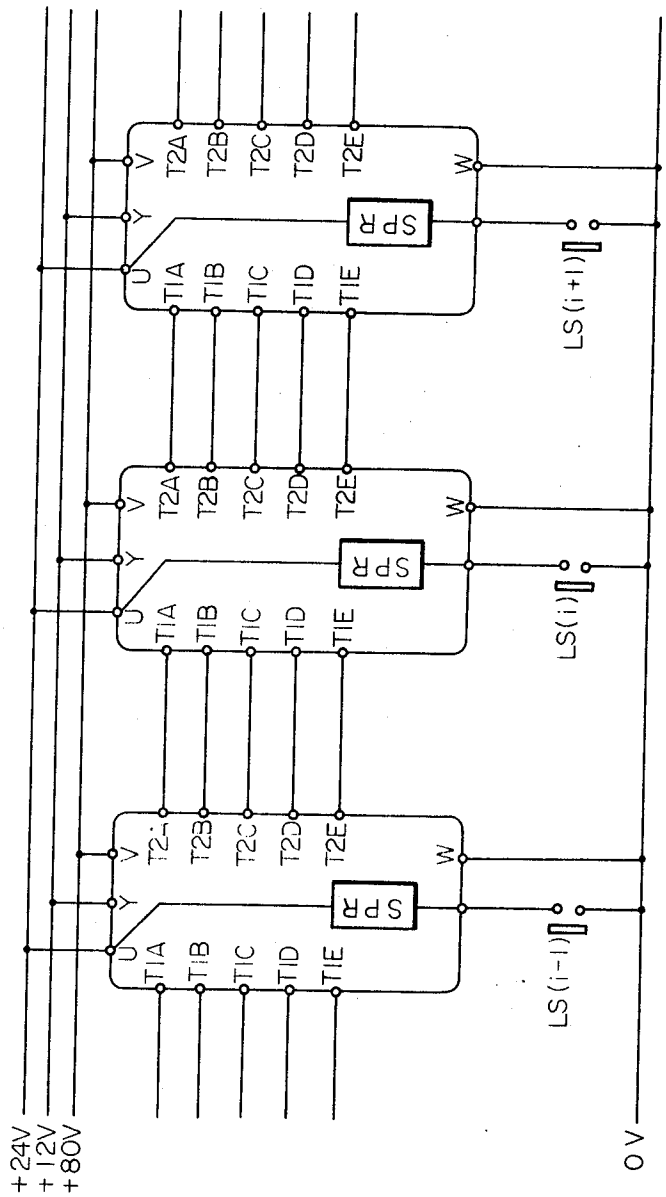
Fig. 7



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SHIFT REGISTER CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION:

This application is a continuation-in-part of our application Ser. No. 769,320, filed Oct. 21, 1968, entitled "Automatic Carrying System".

FIELD OF THE INVENTION

This invention relates to a shift register circuit, and more particularly to a shift register circuit utilizing magnetic lutch relays.

DESCRIPTION OF THE PRIOR ART

A shift register circuit has been known which utilizes magnetic lutch relays. In one type of known shift register circuit of this kind, such as those shown in the U.S. Pat. No. 3,379,863, two magnetic lutch relays are required for each bit, so that the shift register circuit is expensive. Another type of shift register circuit has been known in which only one magnetic lutch relay is required for each bit, as shown, for example, in the U.S. Pat. No. 3,042,900. However, in the shift register circuit shown in this United States Patent, it is necessary to utilize magnetic lutch relays of the type having a plurality of control windings, and because of high cost of this type of magnetic lutch relay, the shift register circuit of this type is also expensive. Accordingly, it is highly desirable to obtain a shift register circuit which requires only one magnetic lutch relay for each bit and which can be constituted by readily available magnetic lutch relays of the type having a single control winding.

SUMMARY OF THE INVENTION

The present invention provides a shift register circuit which requires for each bit only one magnetic lutch relay of the type having a single control winding.

In accordance with the invention, a shift register circuit is provided in which there are provided a first bus of a reference potential, e.g. ground level, a second bus of a first potential, e.g. a level of 2E volt, and a third bus of a second potential lower than said first potential, e.g. a level of E volt, and in which each register stage comprises a magnetic lutch relay having its movable contact normally coupled to said second bus through one of two stationary contacts of the relay, a capacitor, and a double-throw transfer switch arranged so as to normally couple said capacitor to the movable contact of said relay, said magnetic lutch relay including two stationary contacts connected respectively to said first and second buses and a single coil having one end connected to said third bus and the other end adapted to be coupled to the capacitor in the immediately preceding stage through the transfer switch in said immediately preceding stage upon actuation of the transfer switch in said immediately preceding stage, said magnetic lutch relay having such characteristic that its movable contact is switched between said two stationary contacts thereof in accordance with the direction of current caused to flow through said relay coil, whereby upon actuation of said transfer switch in one stage, the movable contact of the magnetic lutch relay in the next succeeding stage is switched so as to be electrically connected to said first bus, if and only when the movable contact of the relay in said one stage has been electrically connected to said first bus.

Further, the present invention can be incorporated in any of the following registers because of the provision of a unique transfer circuit: (1) a simultaneous shift register circuit in which bits are shifted simultaneously in response to each shifting pulse, (2) a storage type shift register circuit in which bits once entered into the first stage are shifted automatically so that they fill the register stages, beginning with the last stage, and (3) a shift register circuit in which each stage can be operated individually so that transfer switches only in selected stages are actuated at a given time (hereinafter referred to as ""individually operable shift register").

One advantage of the invention is that the shift register circuit can be produced by the utilization of magnetic lutch relays of the type having a single control winding which are readily available in the market, thus making it possible to constitute it at low cost. Also, since the shift register circuit according to the invention can be produced from minimum number of components and parts, it is highly reliable in operation.

Another advantage of the invention is that since a unique transfer circuit including independently operable transfer contacts, signal detecting relays and reset timing relays is provided, any of a simultaneous shift register, a storage type shift register and an individually operable shift register can be manufactured without requiring any special pulse generating circuit.

Still another advantage of the invention is that since a transfer contact is provided for each magnetic relay, the amount of current caused to flow through each contact is so small that its life can be lengthened without any special care in maintenance.

These and other features and advantages of the present invention will be better understood by reference to the following description made in conjunction with the accompanying drawings:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic circuit of a simultaneous shift register explaining the principle of operation of the shift register according to the invention.

FIG. 2 shows a storage type shift register circuit having four stages each adapted to register two bits which comprises a plurality of basic circuits shown in FIG. 1 and the associated relays for detection of signals having a binary value "1".

FIG. 3 is a circuit diagram of an individually operable shift register which is particularly applicable to register or store instruction signals related to an article carrier adapted to be moved along a track for the purpose of conveying articles from one to other stations.

FIG. 4 shows a basic circuit unit of a shift register capable of registering five bits in each stage which is constructed in accordance with the invention and which can be assembled to form any of said simultaneous shift register, storage type shift register and individually operable shift register.

FIG. 5 shows a wiring diagram illustrating how the basic circuit units of FIG. 4 can be connected to each other in order to constitute a simultaneous shift register.

FIG. 6 shows a wiring diagram illustrating how the basic circuit units of FIG. 4 can be connected to each other in order to constitute a storage type shift register.

And,

FIG. 7 shows a wiring diagram illustrating how the basic circuit units of FIG. 4 can be connected to each other in order to constitute an individually operable shift register.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic view showing a simultaneous shift register having a plurality of consecutively arranged stages ST1, ST2, ST3 — each adapted to register one bit which is taken by way of an example for purpose of illustrating the principle of operation in accordance with the invention. A coil S of a conventional electromagnetic relay having movable contacts SMO, SM1, SM2 — , and a normally open contact SS1 connected in series with the relay coil S are connected across a first and a second power supplies E1 and E2 which are in turn connected in series to one another. The contact SS1 is associated with coil means (not shown) which is adapted to be energized when it is required to energize the coil S. All of the contacts illustrated in the drawing are shown in their normal state. A first bus 1 at a reference potential level, for example, ground level, extends from the negative terminal of the first power supply E1, a second bus 2 extends from the positive terminal of the second power supply E2, and a third bus 3 ex-

tends from the junction between the positive terminal of the first power supply E1 and the negative terminal of the second power supply E2. The first register stage ST1 includes a magnetic lutch relay LR1 having one end connected to the third bus 3 and the other end adapted to be connected to a capacitor CO through a double-throw transfer switch comprising the movable contact SMO and stationary contacts SMO-1 and SMO-2 when the relay coil S is energized. One stationary contact LRM1-1 of the magnetic lutch relay LR1 is connected to the second bus 2, while the other stationary contact LRM1-2 is connected to the first bus 1. The movable contact LRM1 is adapted to be switched to engage the stationary contact LRM1-2 in response to current flowing through the magnetic lutch relay coil LR1 in the direction indicated by an arrow S and held thereat until the coil LR1 is energized in the direction of R, and also adapted to be switched to engage the stationary contact LRM1-1 in response to current flowing through the coil LR1 in the direction indicated by another arrow R and held thereat until the coil LR1 is energized in the direction of S. The first stage further comprises a capacitor C1, and a double-throw transfer switch comprising the movable contact SM1 and stationary contacts SM1-1 and SM1-2. The movable contact SM1 of the transfer switch in the first stage ST1 is normally coupled electrically to the movable contact LRM1 of the magnetic lutch relay LR1 in the first stage. Each of the remaining stages has similar construction to that of the first stage. In the input circuit of the first stage ST1, there is provided a two position push-down switch P having a movable contact 4 and pair of stationary contacts 5,5 and 6,6 which are connected at their one sides to the second and first buses 2 and 1, respectively, the other sides of said stationary contact pair being jointly connected to the stationary contact SMO-1 which normally engages the capacitor CO through the movable contact SMO of the relay S. The push-down switch P, in cooperation with the capacitor CO, serves to set a signal to be entered into the first stage ST1.

In the shift register circuit according to the invention, it is prescribed that the potential level 2E on the second bus 2 corresponds to a binary signal value "0", and the reference potential level on the first bus 1 corresponds to another binary signal value "1". Thus, when a "1" signal is registered in a stage, the movable contact of the magnetic lutch relay in that stage is connected electrically to the first bus 1, so that the capacitor in that stage is at the level of the reference potential, on the other hand, when a "0" signal is registered in that stage, the movable contact of the magnetic lutch relay in that stage is connected electrically to the second bus, so that the capacitor in that stage is charged up to the potential level of 2E. Further, in the following description, the normal state of each magnetic lutch relay shown in the drawing will be referred to as "reset state", while the state of the magnetic lutch relay having its movable contact connected electrically to the first bus 1 will be referred to as "set state".

The operation of the shift register circuit of FIG. 1 is as follows:

When the movable contact 4 of the input entry switch 4 is in the position shown in FIG. 1, i.e. when a "0" is set up in the switch P, the capacitor CO is charged up to the potential level of 2E. Similarly, the capacitors C1, C2, — are charged up to the potential level of 2E. Thereafter, when the contact SS1 is closed by application of a shift pulse to the coil means (not shown) associated with the contact SS1, the movable contact SMO will be switched to engage the stationary contact SMO-2, thus permitting the capacitor CO, which has been charged up to the potential level of 2E, to be discharged so that current flows to the third bus 3 having the potential level E through the magnetic lutch relay LR1 in the direction indicated by the arrow S. However, since the magnetic lutch relay has been reset, the current has no effect on the status of the movable contact LRM1. This signifies that a "0" signal is registered in the relay LR1 in the first stage. When, the coil S is energized, other movable contacts SM1, SM2, — of the relay S will be also switched toward their righthand positions respectively, but their movable contacts will not be switched, since in each of the magnetic lutch relays LR2, LR3, — , current will flow in the direction of R. Thus, each of the relays LR2, LR3, — indicates that a "0" signal is registered therein. After the storage capacitor CO has been discharged, the movable contact SMO may be returned to its original position by deenergizing the coil S.

Now, let us suppose that a "1" signal is set on the input entry switch P by pushing down the movable contact 4. When the movable contact 4 is pushed down to engage the stationary contacts 6,6, the capacitor CO, which has been charged up to the potential level of 2E, will be discharged, so that its potential will become zero. Thereafter, when the relay S is energized to cause the movable contact SMO to engage the stationary contact SMO-2, current will flow from the third bus 3 through the magnetic lutch relay coil LR1 in the direction of S until the capacitor CO is charged up to the potential level of E, which will set the magnetic lutch relay LR1, that is, the movable contact LRM1 will be switched to engage the stationary contact LRM1-2. This signifies that a "1" signal is registered in the relay LR1 in the first stage ST1. When the relay S is energized, other movable contact SM1, SM2, — will be also driven to their righthand positions, but the magnetic lutch relays LR2, LR3, — will not be set since the capacitors C1, C2, — have been charged up to the potential level of 2E before the actuation of the movable contacts SM1, SM2, — so that when these movable contacts are actuated, current will flow in the direction of R in each of the relays LR2, LR3, — . After the capacitor CO has been charged up to the potential level of E, the coil S can be deenergized so that the movable contact SMO, SM1, SM2, — are returned. Thus, the time period during which the shift coil S is to be energized, and hence the pulse width of shift pulse required for actuating the switch SS1 can be as small as possible, so long as it is large enough to permit current to flow for a sufficient time period to actuate the relay LR1 and to permit the capacitor CO to be charged up through the relay coil LR1.

Then, the movable contact 4 of the switch P is returned to its original position. In this state, the capacitors CO, C1, C2, C3 have the potential levels of 2E, 0, 2E, 2E, respectively. When the shift coil S is reenergized, each of the magnetic lutch relays LR1, LR3, LR4 allows current to flow therethrough in the direction of R, while the relay LR2 allows current to flow therethrough in the direction of S, as a result of which only the relay LR2 is set, indicating that a "1" signal is registered only in the second stage ST2. Thus, the "1"signal, which has been shifted into the first stage by the first shift pulse applied to the coil associated with the shift switch SS1, will be shifted into the second stage ST2 by the second shift pulse. In this way, a signal initially entered into the first stage ST1 is shifted sequentially to the succeeding stages upon each energization of the shift relay S by successive shift pulses.

Output from each stage can be extracted by connecting loads, such as relays 7, respectively between the second bus 2 and each of the movable contacts of the magnetic lutch relays LR1, LR2, LR3, — , as shown in FIG. 1. In this case, when a magnetic lutch relay in any of the stages has a "1" signal registered therein, the load associated with that stage will be energized. Alternatively, if each of the magnetic lutch relays is replaced by an interlocked multi-contact type relay so that one set of contacts of each multi-contact type relay is used in place of the magnetic lutch relay in each stage, then another set of contacts may be used for extract the output from that stage.

FIG. 2 shows a storage type shift register circuit having four stages each adapted to register two bits which is constructed in accordance with the invention. In this type of shift register circuit, any "1" signal entered into the first stage is automatically shifted into the succeeding stage, if the said succeeding stage is in empty state, that is, if the said succeeding stage has no "1" signal which has been registered therein. Accordingly, "1" signals are registered in the consecutively arranged stages in such a manner that they always fill the register stages,

beginning with the last stage, and if a "1" signal registered in the last stage is extracted so that it is cleared or emptied, a "1" signal which has been registered in the second stage from the last stage will be automatically shifted into the cleared last stage.

The first stage includes magnetic lutch relays LR11 and LR12 for registering two bits, and capacitors C11 and C12 connected respectively to the relays LR11 and LR12 in the similar manner as in FIG. 1, the second stage includes magnetic lutch relays LR21 and LR22, and capacitors C21 and C22 connected respectively to the relays LR21 and LR22, the third stage includes magnetic lutch relays LR31 and LR32, and capacitors C31 and C32, and the fourth stage includes magnetic lutch relays LR41 and LR42, and capacitors C41 and C42. It is to be noted that further stages can be added, if desired. The first stage is provided with a conventional magnetic relay Q10 connected to the movable contacts of the relays LR11 and LR12 through diodes D11 and D12 respectively for indicating whether there is a "1" signal registered in the first stage, and the relay Q10 is adapted to be energized when at least one of the relays LR11 and LR12 has a "1" signal registered therein. The relay Q10 has normally opened contacts Q10A and Q10B. The second stage is provided with a conventional magnetic relay Q20 having normally open contacts Q20A, Q20B and a normally closed contact Q20C. Similarly, the third stage is provided with a magnetic relay Q30 having normally open contacts Q30A, Q30B and a normally closed contact Q30C, and the fourth stage is provided with a similar relay Q40.

The first stage is further provided with a relay S10 which functions to shift a "1" signal registered in the first stage into the second stage when a "shift condition" is established, as will be described later, and also to reset the relays LR11 and LR12 upon completion of shifting operation, as will be also described later. The relay S10 has a first transfer switch comprising a movable contact S10A and stationary contacts S10A-1, S10A-2, a second transfer switch comprising contacts S10B, S10B-1 and S10B-2, a normally closed contact S10D, and normally open contacts S10C and S10E. Each of the remaining stages is provided with a similar relay S20, S30, — having contacts corresponding to those of the relay S10. The first stage is further provided with a relay T10 having normally open contacts T10A and T10B which is used to reset the magnetic lutch relays LR11 and LR12 of the first stage, and the relay T10 is adapted to be energized upon energization of the shift relay S10 and to self-hold the energized state until both the relays LR11 and LR12 have been reset. Each of the remaining stages is provided with a similar relay T20, T30, — having normally open contacts corresponding to those of the relay T10. In the circuit of FIG. 2, one ends of respective magnetic lutch relay are connected to their associated resetting coils, such as Q10, Q20, Q30, — through diodes such as D13, D14, D23, D24, D33, D34, respectively. In the input circuits of the first stage, there are provided a first three-position self-return type switch 20 having a movable contact 20A and stationary contacts 20A-1, 20A-2, and a second three-position self-return type switch 21 having a movable contact 21A and stationary contact 21A-1, 21A-2. These relays 20 and 21 are used respectively to enter a signal having a binary value "1" or "0". Reference numeral 22 designates a push-down switch which determines when "1" signal set into the magnetic lutch relays LR11 and LR12 of the first stage are to shifted into the second stage. More particularly, the switch 22 serves to align the leading edge of a "1" signal emitted from the relay LR11 with the leading edge of another "1" signal emitted from the relay LR12. Since a "1" signal, once entered into any of the stages, is automatically shifted into the next succeeding stage, so long as the said next succeeding stage is in empty state, a "1" signal entered by the switch 20 leads a "1" signal entered by the switch 21, if the switch 20 is actuated before the switch 21, and if it were not for the switch 22. If the signal setting switches 20 and 21 are of electrically operated type, then the switch 22 is preferably constituted by another electrically operated switch which is adapted to maintain the signal path between the first bus 1 and the contact Q10A in broken state until "1" signals have been registered in both of the magnetic lutch relays LR11 and LR12.

First, let us assume that a "0" signal and a "1" signal are to be registered respectively in the magnetic lutch relays LR11 and LR12 of the first stage. For this purpose, the movable contact 20A of the switch 20 is closed so as to engage the contact 20A-1, while the movable contact 21A of the switch 21 is closed so as to engage the contact 21A-2. Then, the relay LR11 will remain in its original reset state, while the relay LR12 will be set, thus indicating that a "1" signal is registered in the relay LR12 of the first stage. When the relay LR12 is set, a circuit from the second bus 2 through the relay Q10, the diode D12, the contacts LRM12, LRM12-2, and a capacitor R14 to the first bus 1 will be completed, thus energizing the relay Q10 to close the normally open contact Q10. Thereafter, the switch 22 may be closed to complete a circuit from the second bus 2 through the relay S10, the contact Q10A, the switch 22, and the normally closed contact Q20C, whereby the relay S10 is energized to cause the movable contacts S10A and S10B to be switched to engage respectively the stationary contacts S10A-2 and S10B-2, thus permitting the signals to be shifted from the magnetic lutch relays LR11 and LR12 into the magnetic lutch relays LR21 and LR22, respectively, in accordance with the principle of operation described in conjunction with FIG. 1. In consequence, the relay LR21 remains reset, while the relay LR22 is set. Simultaneously, the relay T10 will be energized since the normally open contact S10C is closed. When the relay LR22 is set, the relay Q20 of the second stage will be energized in the same manner as that in which the relay Q10 of the first stage was energized. Now, the normally closed contact Q20C is opened to deenergize the relay S10. However, despite of the fact that the relay S10 is deenergized, the relay T10 will not be deenergized since the relay T10 self-holds its energized state through the contacts T10A and Q10B which are now in closed state. Since the relay T10 is in energized state, the relay T10B is in closed state, and therefore, current will be permitted to flow through the magnetic lutch relays LR11 and LR12 in such direction as to reset these relays LR11 and LR12, from the second bus 2 via the contacts T10B, S10E, and thence through the diodes D13 and D14, respectively. When both of the relays LR11 and LR12 have been reset, the relay Q10 will be deenergized to open the contact Q10B. Then, the relay T10 may be released from its self-holding condition, and consequently the relay T10 will be deenergized. In this way, resetting current to the relays LR11 and LR12 in the first stage can be permitted to flow only after the "1" signal has been shifted from the first stage into the second stage, and the resetting current to these relays LR11 and LR12 can be terminated only when these relays LR11 and LR12 have been reset. Consequently, at this time, both of the magnetic lutch relays LR11 and LR12 have "0" signals registered therein.

Now, since a "1" signal has been shifted into the second stage, the relay Q20 is energized. When both relays Q30 and S10 are in deenergized state and the relay Q10 is in energized state, the shifting relay S20 of the second stage will be energized. Thus, the "1" entered into the second stage is shifted into the third stage because the movable contacts S20A and S20B engage the stationary contacts S20A-2 and S20B-2, respectively. In this manner, the "1" signal entered initially into the first stage will reach the last stage. Let us assume that the stage having the magnetic lutch relays LR31 and LR32 is the last stage. In this case, if a normally open contact is inserted, as a contact for timing extraction of output from the last stage, in place of the contact 40C which is connected in the signal circuit of the shifting relay S30 of the last stage, the shifting relay S30 of the last stage can be energized by closing said output extraction timing contact after a "1" signal has entered into the last stage so that the condition that shifting operation for the second stage from the last stage has been completed is established, and thereafter the shifting relay S30

can be deenergized to reset the magnetic lutch relays of the last stage, by opening said output extraction timing contact.

FIG. 3 shows an individually operable shift register circuit having a plurality of stages in which neither a simultaneous shifting operating as in FIG. 1 nor a sequential shifting operation as in FIG. 2 is executed. More particularly, in this type of shift register circuit, only selected ones of the register stages can be activated individually at a given time so that a "1" signal in each of the enabled stage is shifted into the next succeeding stage. This shift register circuit has shifting relays, such as S50, S60, S70, each associated with each register stage, whereby when the shifting relay associated a selected stage is energized, a binary signal which has been registered in the immediately preceding stage will be shifted into said selected stage.

Reference letters LS5, LS6 and LS7 designate normally open switches which are adapted to be actuated for a limited time period in order to energize the shifting relays S50, S60 and S70, respectively. The shifting relay S60 is connected in series with the switch LS6 between the first bus 1 and the second bus 2, and has a first movable contact S50A adapted to be switched between stationary contacts S50A-1, S50A-2, and a second movable contact S50B adapted to be switched between stationary contacts S50B-1, S50B-2. Each of the remaining shifting relay is connected similarly between the first and second bus, and contacts corresponding to those of the shifting relay S60.

The operation of the shift register circuit of FIG. 3 is as follows:

In the state shown in FIG. 3, all of magnetic lutch relays LR50, LR60 and LR70 are reset, all of storage capacitors C50, C60 and C70 have been charged up to the potential level of 2E, and all of capacitors C61, C71 and C81 have been charged up to the potential level of E. If the switch LS6 is actuated, the shift relay S60 is energized to cause the movable contacts S60A and S60B to engage the stationary contacts S60A-2 and S60B-2, respectively. Thus, a binary signal which has been registered in the magnetic lutch relay LR50 will be shifted into the magnetic lutch relay LR60, and simultaneously the electrical charge on the capacitor C61 will be discharged through a resistor R68 via the contacts S60B, S60B-2. It will be apparent that if the magnetic lutch relay LR50 has been set, the magnetic lutch relay LR60 will be set in response to the energization of the shifting relay S60. When the limited time period of operation of the switch LS6 is over, the relay 60 will be deenergized to return the movable contacts S60A and S60B to their original positions. At the time of engagement of the movable contact S60B with the stationary contact S60B-1, current of small magnitude but large enough to reset the magnetic lutch relay LR50 will flow through the relay LR50. Thus, after each actuation of the switch LS6, the signal stored in the relay LR50 has been shifted in the relay LR60 in the next succeeding stage, and in addition the relay LR50 is assuredly reset so as to have a "0" signal registered therein.

The shift register circuit of FIG. 3 may be used to constitute route instruction means for a load or article carrier adapted to run on multi-sectioned track means in an automatic load carrying system. For example, if said switches LS5, LS6, LS7, —— are positioned respectively at entry ends of respective track sections so that when the load carrier enters from one track section to the next adjacent track section the switch associated with said next adjacent track section is actuated, and if the route instruction signal for the load carrier is constituted by binary signals which are transmitted over the consecutively arranged register stages, then the route instruction may be shifted stage by stage as the load carrier proceeds along the multi-sectioned track means.

FIG. 4 shows an example of a unit circuit of a shift register comprising one stage adapted to register five bits which is constructed in accordance with the concept described hereinbefore. The entire circuit components shown in FIG. 4 can be mounted on a printed circuit board so as to form a circuit module. By using a plurality of unit circuits of this circuit configuration, and by connecting properly the circuit terminals of these units circuits to each other, it is possible to constitute any of a simultaneous shift register, a storage type shift register, and an individually operable shift register. The unit circuit is provided with circuit terminals W, Y, U and V for connection to power supplies, circuit terminals T1A, T1B, T1C, T1D and T1E used as signal input terminals, circuit terminals T2A, T2B, T2C, T2D and T2E adapted to be connected to the signal input terminals of the next succeeding stage, circuit terminals T3A, T3B, T3C, T3D and T3E used for reading bits currently registered, circuit terminals M and N used as input terminals for shift pulses, and additional circuits terminals H, J, K and L. The terminal W may be connected to the ground. The terminal Y may be connected to a first voltage source of potential E, for example, DC 12 volts. The terminal U may be connected to a second voltage source of potential 2E, for example, DC 24 volts. The terminal V may be connected to a third voltage source of, for example, DC 80 volts, and used to supply electric power for energizing neon lamps NEA through NEE for visible indication of the contents of the unit circuit. Reference letters A, B, C, D and E designate magnetic lutch relays for registering five bits. The magnetic lutch relay A has a movable contact MA and stationary contacts MA-1 and MA-2. Each of the remaining lutch relays B through E has contacts corresponding to those of the relay A. Reference letters D1A through D1E designate diodes used for resetting the magnetic lutch relays A through E. A movable contact 14A and three stationary contacts 14A-1, 14A-2, 14A-3 constitute a first manual snap switch, a movable contact 14B and three stationary contacts 14B-1, 14B-2, 14C-3 constitute a second manual snap switch, and in this manner a total of five manual switches are provided which are used to decode a code comprising five bits. It is prescribed that when the movable contact MA of the magnetic lutch relay A engages the stationary contact MA-2, the relay A has a binary "1" signal registered therein, and that when the movable contact MA engages the stationary contact MA-1, the relay A has a binary "0" signal registered therein. Thus, it is possible to know whether the relay A has stored therein a "1" signal or a "0" signal by setting the movable contact MA on either of the stationary contact MA-1 or MA-2 in order to detect in which of the two positions of the movable contact MA the terminal J can be grounded.

In decoding the code comprising five bits registered in the five magnetic lutch relays A through E, it is possible to utilize a relationship $\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} = \overline{A \cdot B \cdot C \cdot D \cdot E}$ which is an equation valid for binary bits. In order to utilize this relationship, it is possible to set the movable contact of each of the manual snap switches so as to engage the upper side stationary contacts, such as 14A-2, 14B-2, when the associated magnetic lutch relay has a "0" signal registered therein and so as to engage the lower side stationary contacts, such as 14A-3, 14B-3, when the associated magnetic lutch relay has a "1" signal registered therein. In this case, a ground level signal will appear at the terminal J only when the combination of set conditions of the movable contacts 14A through 14E of the snap switches (this corresponds to a reading code) is in concordance with the code comprising five bits registered in the relays *A* through *E*. The diodes D2A through 2E serve as OR gates providing a logical sum function $\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$. Reference letters D3A through D3E designate diodes which can serve as OR gates permitting a relay S1G to be energized when at least one of the magnetic lutch relays A through E has a "1" signal registered therein. The neon lamp NEA is connected in series with a resistor R1A between a signal line 30A and the terminal V, and adapted to be turned on when the magnetic lutch relay A has a "1" signal registered therein so that the signal line 30A is grounded. Each of the remaining lamps NEB through NEE is connected between the terminal V and one of the signal lines 30B through 30E in the similar manner. A diode 4A is connected between the signal line 30A and a signal line 31A connected to the terminal T3A, and it serves to prevent

the neon lamp A from being turned on through the terminal T3A or through a resistor R2A when the magnetic lutch relay A has a "0" signal registered therein. The unit circuit of FIG. 4 includes a shifting relay SPR connected between lead wires from the terminals U and M and having movable contacts SPRA through SPRE and stationary contacts SPRA-1, SPRA-2, SPRB-1, SPRB-2, SPRC-1, SPRC-2, SPRD-1, SPRD-2, SPRE-1 and SPRE-2. The relay SPR further has a normally closed contact SPRB. The movable contact SPRA is normally engaged with the contact SPRA-1. Capacitors C1A through C1E are connected between a lead wire from the terminal W and respective one of the movable contacts SPRA through SPRE. A resistor R2A is connected between the signal line 31A and a lead wire from the terminal U, and it is used to charge the capacitor C1A from the terminal U through the resister R2A and a limiting resistor R3A up to the potential level of 24 volts, when the magnetic lutch relay A has a "0" signal registered therein so that the signal line 30A is disconnected from the ground terminal W.

Thus, in the circuit of FIG. 4, when a selected magnetic lutch relay has a "0" signal registered therein, the associated signal line will be disconnected from the ground so that the associated capacitor is charged up to a predetermined positive potential level, while, when a "1" signal is registered, the associated signal line will be connected to the ground so that the said associated capacitor is at zero potential. Also, it may be understood that if a load is connected between the terminal U and respective one of the terminals T3A through T3E, it will be energized when a "1" signal is registered. The relay SIG has a normally closed contact SIGA and a normally open contact SIGB. The contact SIGB permits shifting pulses applied to the terminal N to energize the shifting relay SPR only when at least one "1" signal is registered in the unit circuit.

The unit circuit of FIG. 4 further includes a relay RST having normally open contacts RSTA, RSTC and a normally closed contact RSTB. The relay RST can be used to reset the magnetic lutch relays A through E when the unit circuit is used to constitute a storage type shift register. The relay RST will be energized when the relay SPR is energized to close its normally open contact SPRA, and it will self-hold its energized state through its contact RSTA, a diode D1S, at least one of the diodes D3A–D3E, and the contacts of at least one of the magnetic lutch relays *A–E* which has been set, until all of the magnetic lutch relays *A* through *E* have been reset so that all of them have "0" signals registered therein. The unit circuit further includes a manually operable normally open switch MS. When the relays *A* through *E* are to be reset upon each shifting operation, for example, when the unit circuit is used to constitute a storage type shift register, the manual switch MS may be maintained in closed state to cause resetting current to flow during the time period between the deenergization of the relay SIG and the deenergization of the relay RST, whereby the relay *A* through *E* are assuredly reset.

FIG. 5 shows a wiring diagram illustrating how a plurality of unit circuits of FIG. 4 can be interconnected to form a simultaneous shift register circuit. The signal output terminals T2A through T2E of one unit circuit are connected to the signal input terminals T1A through T1E of the adjacent unit circuit, respectively. The terminal W is connected to the ground, and the terminal Y, U, V are connected power sources of 12 volts, 24 volts and 80 volts, respectively. It will be noted that the terminals M of respective unit circuits are connected in common to a switch SSW so that they may be energized simultaneously.

FIG. 6 shows a wiring diagram illustrating how a plurality of unit circuits of FIG. 4 can be interconnected to form a storage type shift register circuit. In FIG. 6, it can be understood that the shifting relay SPR in the stage under consideration (that is, the relay SPR located in the center stage in FIG. 6) will be energized to allow the content thereof to be shifted into the next succeeding stage, when the following three conditions are satisfied, likely in the storage type shift register circuit of FIG. 2:

1. There is no "1" signal registered in the next succeeding stage, so that the relay SIG in the said next succeeding stage is not in energized state.
2. Shifting operation for the next preceding stage has been completed, so that the relay RST in the said next preceding stage is not in energized state.
3. There is at least one "1" signal registered in the stage under consideration, so that the relay SIG in the stage under consideration is in energized state.

After the signals have been shifted from the stage under consideration into the next succeeding stage, the shifting relay SPR in the stage under consideration is reset since the condition 3 with respect to the stage under consideration is dissatisfied. When the relay SPR in the stage under consideration is reset, the relay SPR in the next succeeding stage will be energized since all of the three conditions 1, 2 and 3 with respect to the next succeeding stage are satisfied. In this way, the signals will be shifted successively over the consecutively arranged stages.

In order to decode the content of each register stage or unit circuit, a relay 999 having a normally closed contact (not shown) may be connected between the terminal J of the unit circuit under consideration and the power supply of 24 volts. As described in conjunction with FIG. 4, when the combination of settings of the manually settable switches 14A through 14E is in concordance with the code comprising five bits registered in the unit circuit under consideration, the terminal J is disconnected from the ground. Therefore, said normally closed contact of the relay 999 may be used to extract the decoded output. Also, as previously noted, ground level signals appear respectively at the terminals T3A, T3B, T3C, T3D and T3E shown in FIG. 4, when the related magnetic lutch relays have "1" signals registered therein respectively. Therefore, if a full decoder is required, a relay of the full decoder may be connected to these terminals.

FIG. 7 shows a wiring diagram illustrating how a plurality of unit circuits of FIG. 4 can be interconnected to form a individually operable shift register circuit. In FIG. 7, it will be understood that the shifting relays SPR in respective stage can be energized individually by means of switches LS(i-1), LS(i), LS(i+1) to shift the content of a stage under consideration into the next succeeding stage. In the circuit of FIG. 7, the content of each register stage can be decoded in the manner as in the circuit of FIG. 6.

Although the invention has been described with respect to certain specific embodiments, it will be appreciated that modifications and changes may be made by those skilled in the art without departing from the teaching of the invention.

We claim:

1. A shift register circuit comprising a first bus of a reference potential, a second bus of a first potential relative to said reference potential, a third bus of a second potential lower than said first potential, and a row of a plurality of consecutively arranged register stages, each of said stage including a magnetic lutch relay having its movable contact normally coupled to said second bus through one of its two stationary contacts, a capacitor having one end connected to said first bus, and a double-throw transfer switch arranged so as to normally couple the other end of said capacitor to said movable contact of said magnetic lutch relay, said two stationary contacts of said relay being connected respectively to said first and second buses, the coil of said magnetic lutch relay having one end connected to said third bus and the other end adapted to be coupled to the capacitor in the immediately preceding stage through the transfer switch in said immediately preceding stage when said transfer switch in said immediately preceding stage is actuated, said magnetic lutch relay having such characteristic that its movable contact is switched between said two stationary contacts thereof in accordance with the direction of current caused to flow through the coil thereof, whereby upon actuation of the transfer switch in one stage, the binary signal is shifted from said one stage into the next succeeding stage.

2. A shift register circuit according to claim 1 wherein said transfer switch is associated with a relay coil for controlling the operation of the transfer switch.

3. A shift register circuit according to claim 1 wherein there are provided a plurality of rows of consecutively arranged register stages which are disposed to form an upper row and a lower row so that each stage includes an upper stage section and a lower stage section, each stage of the shift register circuit further comprising a signal detecting relay coupled to the movable contacts of the magnetic lutch relays of the same stage and having a normally closed contact and two normally open contacts, a relay adapted to actuate said transfer switch and further having a normally open contact and two normally closed contacts, and a reset indicating relay adapted to indicate when all of the magnetic lutch relays in the associated stage have been reset and having two normally open contacts, said transfer switch actuating relay in one stage being connected between said first and second buses through said normally closed contact of said signal detecting relay of the next succeeding stage, said normally closed contact of said transfer switch actuating relay of the immediately preceding stage and one of said normally open contacts of said signal detecting relay of said one stage, said reset indicating relay of said one stage being connected between said first and second buses

through a series circuit of the other of said normally open contact of said signal detecting relay of said one stage and one of said two normally open contacts of said reset indicating relay of said one stage across which one of said normally open contact of said transfer switch actuating relay of said one stage is connected, each of the coils of the magnetic lutch relays of said one stage being coupled to said second bus through the other of said normally open contacts of said reset indicating relay of said one stage and the other of said normally closed contacts of said transfer switch actuating relay of said one stage.

4. A shift register circuit according to claim 1 wherein a gang switch having two sets of double-throw switch contacts are provided, one of said two set being used as said transfer switch for shifting the signal from the magnetic lutch relay in one stage to the magnetic lutch relay in the next succeeding stage, the other of said two set of the gang switch being connected between the second bus and said other end of the coil of the magnetic lutch relay in said one stage through a second capacitor, and wherein a resistor is connected between the normally open contact of said other set of double-throw switch and said second bus, and means is provided for actuating said gang switch.

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