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(71) Applicants *(for all designated States except US)*: **PHILIPS LUMILEDS LIGHTING COMPANY, LLC** [US/US]; 370 West Trimble Road MS 91/MG, San Jose, California 95131 (US). **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: **EPLER, John E.**; c/o 370 West Trimble Road MS 91/MG, San Jose, California 95131 (US). **NEFF, James G.**; c/o 370 West Trimble Road MS 91/MG, San Jose, California 95131 (US). **SHCHEKIN, Oleg B.**; c/o 370 West Trimble Road MS 91/MG, San Jose, California 95131 (US).

(74) Agents: **BEKKERS, Joost, J.J.** et al.; High Tech Campus Building 44, NL-5656 AE Eindhoven (NL).

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[Continued on next page]

(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE INCLUDING A WINDOW LAYER AND A LIGHT-DIRECTING STRUCTURE

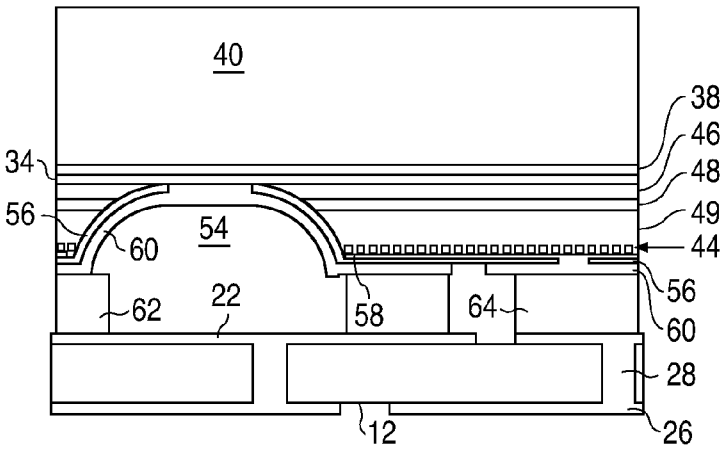

FIG. 6

(57) Abstract: A device includes a semiconductor structure comprising a light emitting layer (48) disposed between an n-type region (44, 49) and a p-type region (46). The semiconductor structure is disposed between a window layer (40) and a light-directing structure (44). The light-directing structure is configured to direct light toward the window layer; examples of suitable light- directing structures include a porous semiconductor layer and a photonic crystal. An n-contact (58, 64) is electrically connected to the n-type region and a p-contact (60, 62) is electrically connected to the p- type region. The p-contact is disposed in an opening (54) formed in the semiconductor structure.

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Published:

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SEMICONDUCTOR LIGHT EMITTING DEVICE INCLUDING A WINDOW LAYER AND A LIGHT-DIRECTING STRUCTURE

BACKGROUND

DESCRIPTION OF RELATED ART

[0001] Fig. 1 illustrates a thin-film flip-chip semiconductor light-emitting device described in more detail in US Patent No. 7,256,483, which is incorporated herein by reference. As used herein, the term "GaN" may represent any III-N material.

[0002] The LED of Fig. 1 is grown on a growth substrate. Typically, a relatively thick (approx. 1-2 micron) undoped or n-type GaN layer is grown on a sapphire growth substrate using conventional techniques. Other substrates may also be used, such as SiC, Si, SiCOI, and ZnO. In the case of gallium-phosphide (III-P) LEDs, the growth substrate is typically GaAs or Ge. The relatively thick GaN layer typically includes a low temperature nucleation layer and one or more additional layers so as to provide a low-defect lattice structure for the n-type cladding layer and active layer. One or more n-type cladding layers 16 are then formed over the thick n-type layer, followed by an active layer 18, one or more p-type layers 20, including one or more cladding layers and a p-type contact layer.

[0003] Various techniques are used to gain electrical access to the n-layers. In a flip-chip example, such as the device shown in Fig. 1, portions of the p-layers and active layer are etched away to expose an n-layer for metallization. In this way the p contact and n contact are on the same side of the chip and can be directly electrically attached to the package substrate contact pads. Current from the n-metal contact initially flows laterally through the n-layer. In contrast, in a vertical injection (non-flip-chip) LED, an n-contact is formed on one side of the chip, and a p-contact is formed on the other side of the chip. An electrically insulating substrate is removed to expose the conductivity type layer that is buried, often an n-type layer. Electrical contact to one of the p or n-contacts is typically made with a wire bond or a metal bridge, and the other contact is directly bonded to a package substrate contact pad.

[0004] In the flip chip illustrated in Fig. 1, after etching to expose an n-type layer, the n- and p-contact metals 50 and 24 are formed. The n- and p-contacts 50 and 24 may include

bonding metals, diffusion barriers, or other layers to protect the optical properties of the contact. The p-metallization 24 may be highly reflective to light emitted by the active layer. After the contacts are formed, a wafer of devices may be diced into individual devices.

[0005] The metallization layers are then bonded to metal contact pads 22 on the package substrate 12. The bond technology may be solder, thermocompression, interdiffusion, or a Au stud bump array bonded by an ultrasonic weld.

[0006] The package substrate 12 may be formed of the electrically insulating material AlN, with gold contact pads 22 connected to solderable electrodes 26 using vias 28 and/or metal traces. Alternatively, the package substrate 12 may be formed of a conducting material if passivated to prevent shorting, such as anodized AlSiC. The package substrate 12 may be thermally conductive to act as a heat sink or to conduct heat to a larger heat sink. Ultimately the LED may have a lens cap attached, or be coated with a phosphor (for converting blue or UV light to create a white light), or be further processed, and the package may be soldered to a printed circuit board, if appropriate for the particular application.

[0007] An underfill material 52 may be deposited in the voids beneath the LED to reduce thermal gradients across the LED, add mechanical strength to the attachment, and prevent contaminants from contacting the LED material.

[0008] After bonding the device to the package substrate, the growth substrate is removed by a technique appropriate to the substrate material; for example by laser lift-off, etching, or lapping. The semiconductor structure exposed by removing the substrate may be thinned, then optionally roughened or patterned. A phosphor material may be deposited over the LED die. For example, a ceramic phosphor slab may be attached to the LED die by an organic adhesive.

[0009] In the device illustrated in Fig. 1, many fabrication steps are performed after a wafer is diced into individual devices. Organic materials may be included in the device, for example as underfill or to attach the ceramic phosphor.

SUMMARY

[0010] Devices according to embodiments of the invention are fabricated by a process where most steps occur at a wafer level, before the wafer is diced into individual devices.

The fabrication process may eliminate the need for organic materials.

[0011] In accordance with embodiments of the invention, a device includes a semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region. The semiconductor structure is disposed between a window layer and a light-directing structure. The light-directing structure is configured to direct light toward the window layer; examples of suitable light-directing structures include a porous semiconductor layer and a photonic crystal. An n-contact is electrically connected to the n-type region and a p-contact is electrically connected to the p-type region. The p-contact is disposed in an opening formed in the semiconductor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 is a cross sectional view of a thin film flip chip semiconductor light emitting device.

[0013] Fig. 2 is a cross sectional view of a portion of a device, including a semiconductor structure grown on a growth substrate.

[0014] Fig. 3 is a cross sectional view of the structure of Fig. 2 after etching trenches through the bonding layer and semiconductor structure.

[0015] Fig. 4 illustrates bonding a semiconductor light emitting device to a window layer.

[0016] Fig. 5 illustrates the bonded structure resulting from Fig. 4, after removing the growth substrate and forming a porous region.

[0017] Fig. 6 illustrates a semiconductor light emitting device connected to a mount.

[0018] Fig. 7 illustrates a semiconductor light emitting device with large area contacts formed on a stack of metal and dielectric layers.

DETAILED DESCRIPTION

[0019] In some embodiments of the invention, a thin-film flip-chip semiconductor light-emitting device is fabricated in a series of wafer-level, rather than die-level, steps. Wafer-level fabrication may be more reliable and less time consuming than die-level fabrication. Also, embodiments of the invention also do not require organic materials. Eliminating

organic materials eliminates problems associated with organic materials such as yellowing, and may increase the temperature at which the device may be fabricated or operated.

[0020] Figs. 2-5 show fabrication of a device according to embodiments of the invention. In Fig. 2, a semiconductor structure 32 is grown over a suitable growth substrate 30, often GaN, Al_2O_3 or SiC. Semiconductor structure 32 includes a light emitting or active region sandwiched between an n-type region and a p-type region. The n-type region is typically grown over the substrate before the p-type region.

[0021] The n-type region may include multiple layers of different compositions and dopant concentration including, for example, preparation layers such as buffer layers or nucleation layers which may be n-type or not intentionally doped, release layers designed to facilitate later release of the growth substrate or thinning of the semiconductor structure after substrate removal, and n- or even p-type device layers designed for particular optical or electrical properties desirable for the light emitting region to efficiently emit light.

[0022] The light emitting region is grown over the n-type region. Examples of suitable light emitting regions include a single thick or thin light emitting layer and a multiple quantum well light emitting region including multiple thin or thick quantum well light emitting layers separated by barrier layers. For example, a multiple quantum well light emitting region may include multiple InGaN light emitting layers separated by GaN or InGaN barriers. One or more light emitting layers in the device may be doped, for example with Si, or the light emitting layer or layers may be not intentionally doped.

[0023] The p-type region is grown over the light emitting region. Like the n-type region, the p-type region may include multiple layers of different composition, thickness, and dopant concentration, including layers that are not intentionally doped, or n-type layers.

[0024] An electrically conductive bonding layer 34 is formed over the top layer of semiconductor structure 32, generally the p-type region, using a conventional thin-film deposition technique such as vacuum evaporation, sputtering, and electron beam deposition, which may be followed by annealing in air. Suitable materials for conductive bonding layer 34 are minimally optically absorbing at the wavelength emitted by the light emitting layers of the semiconductor structure, are conductive enough to not significantly add to the series resistance of the device, and form an ohmic contact with the top layer of semiconductor

structure 32. Suitable materials include, for example, transparent conductive oxides such as indium tin oxide (ITO), zinc oxide, and ruthenium oxide. Bonding layer 34 may be, for example, between 200 nm and 1 μm thick in some embodiments, and about 500 nm thick in some embodiments. In some embodiments, bonding layer 34 is a thick, transparent, conductive layer, such as a spin-on or sol-gel material. In some embodiments, bonding layer 34 has an index of refraction that is close to the index of semiconductor structure 32 or window layer 40. In embodiments where the index of refraction of any bonding layer is low, the power transmission may be improved by random or patterned structuring of the interface between the high index and low index materials.

[0025] One or more trenches 36 are etched through bonding layer 34 and semiconductor structure 32, fully or partially down to growth substrate 30, as illustrated in Fig. 3. Trenches 36 may define the boundaries of individual devices. Trenches 34 are formed by conventional patterning and etching steps.

[0026] In Fig. 4, the structure illustrated in Fig. 3 is bonded to a window layer. Window layer 40 may be, for example, a wavelength converting structure such as a ceramic phosphor, a suitable transparent substrate or carrier such as a sapphire or glass layer, or a filter such as a distributed Bragg reflector, for modifying the spectrum to provide a desired color such as amber for signal lights. Ceramic phosphors are described in more detail in US Patent No. 7,361,938, which is incorporated herein by reference. Window layer 40 is preferably thick enough to permit wafer level handling of the window layer/semiconductor structure combination after the growth substrate is removed. Window layer 40 may be between 80 μm and 1 mm thick in some embodiments, between 100 μm and 500 μm thick in some embodiments, and between 100 μm and 200 μm thick in some embodiments.

[0027] If conductive bonding layer 34 and window layer 40 are not suitable for bonding, prior to bonding a transparent bonding layer 38 is formed on window layer 40 or on conductive bonding layer 34. Bonding layer 38 may be the same material as bonding layer 34, though it need not be. Bonding layer 38 may be a transparent conductive oxide, a non-conducting glass material, or other dielectric material such as silicon nitride. For example, bonding layer 38 may be an ITO layer, soda-lime glass, borosilicate, or other glass-like layer with a thickness between 200 nm and 1 μm thick, often with a thickness of about 500 nm. Alternatively, bonding layer 38 may be a transparent organic material such as

benzocyclobutene (BCB), spin-on glass, or silicone. A wavelength converting material such as a phosphor may be disposed in bonding layer 38. For example, a red-emitting phosphor may be disposed in bonding layer 38, and a yellow- or green-emitting phosphor such as cerium-doped yttrium aluminum garnet may be disposed in or on window layer 40, such that the composite light emitted from the device appears warm white. Alternatively, a mixture of phosphors may be disposed in a silicone bonding layer 38, to provide the desired spectrum. In such devices, window layer 40 may be transparent. In some embodiments, bonding layer 38 is patterned or roughened, which may increase light extraction from the device. Other suitable bonding materials are described in Published US Patent Application No. 2006-0105478, titled "Bonding an Optical Element to a Light Emitting Device," and incorporated herein by reference. In some embodiments, bonding layer 38 is quite thin, for example on the order of tens of angstroms thick. Such a bonding layer 38 may serve as a surface modifier for either the conductive bonding layer 34 or the window layer 40, or both. This bonding layer may be transparent as-deposited or may be a non-transparent layer that is chemically reacted to both bond the layers together and become transparent. Examples of suitable thin bonding layers include thin metal layers that may be diffused thermally to bond to an ITO bonding layer 34 and thin silicon oxide bonding layer 38, or that may be bonded using oxide-to-oxide bonding techniques.

[0028] Bonding layers 34 and 38 are bonded, as shown by arrow 42 in Fig. 4, for example by anodic bonding, direct bonding via plasma preparation of hydrophilic surfaces, or bonding via use of an intermediate bonding layer.

[0029] Growth substrate 30 is removed by a process appropriate to the substrate material, as illustrated in Fig. 5. A sapphire substrate can be removed by laser lift off. Substrates may be removed by etching, grinding, or lift off by etching away a sacrificial layer. The bottom surface of the n-type region is exposed by removing the substrate. The n-type region may be thinned, for example by photoelectrochemical etching, to remove unwanted material or material damaged by substrate removal.

[0030] The rays of light generated by the light emitting layer are approximately isotropically distributed and many rays will not escape from the semiconductor into the bonding layer(s). These rays are redirected by making a part of the remaining thickness of the n-type region of semiconductor structure 32 porous, as illustrated in Fig. 5. Porous region 44

is generally electrically and thermally conducting, and designed to scatter light toward window layer 40, and away from a later-formed n-contact. The amount of scattering is determined by the thickness and porosity of the porous layer. The porous layer generally has a thickness between 0.5 and 40 microns. The porous layer may have a porosity between 5% and 80% and often has a porosity between 20% and 40%. The porosity is limited on the lower end by the ability of the porous layer to scatter light and on the upper end by the resistivity and mechanical stability of the porous layer. Suitable porosity may be related to the thickness of the porous region. In order to provide the same amount of scattering, a thicker porous region may be less porous than a thinner porous region. The light rays reflected and scattered by a porous layer will have a Lambertian radiation pattern with maximum intensity directed perpendicular to surface.

[0031] Porous layer 44 may be formed by a two step process. In the first step, the pores are created by an electrochemical anodic etch. In this step, the depth of the porous region is determined. In the second step, the pores are enlarged by a photochemical anodic etch until the desired porosity is reached. A porous layer may be formed as follows: the wafer is connected to a copper plate by, for example, silver paste. A material such as Teflon isolates the portion of the wafer that is to be made porous. The wafer is exposed to a suitable electrolyte such as 0.5 M H_2SO_4 as the working electrode in a standard electrochemical cell, with a Saturated Calomel Electrode (SCE) as reference and a platinum counter electrode. The cell is controlled by a potentiostat. Application of a strong positive potential (15 V SCE) causes etching of submicron pits at surface defects, on the order of microns apart. These pits serve as the starting points for the etching of the sub-surface network of tunnel-like structures. The etching primarily occurs at the end of the tunnels such that the network grows deeper but the tunnels do not enlarge and merge. The amount of material removed is primarily a function of the time-integrated current density, although the etchant solution, bias voltage, and substrate doping influence the pore density and size. The resulting depth of the porous structure is a function of all these variables.

[0032] In one example of a photochemical anodic etching second step, the electrochemically etched wafer is exposed to an H_2O:H_2SO_4:H_2O_2 electrolyte using 50 mW/cm^2 of sub-bandgap light from a Xe lamp, under an applied positive potential of 2 V SCE. The applied potential is too low for the above-described anodic etching process to take place and the sub-bandgap light is only absorbed at the electrolyte-semiconductor interface,

so the primary effect is to increase the porosity of the layer defined in step one. The degree of porosity is determined by the time-integrated current density which is a function of light intensity, etchant concentrations and substrate parameters. Any suitable semiconductor material may be made porous by the process described above, such as Si, GaN, SiC, and GaP. Binary materials such as GaP and GaN are attractive candidates for porous regions, though ternary and quaternary III-phosphide and III-nitride materials may also be made porous. The conductivity type and dopant concentration in the semiconductor material may influence the characteristics of the porous layer, for example by influencing the size and spacing of the pores formed. In some embodiments, the porous region is formed from an n-type GaN layer that is doped with a dopant concentration between zero (not intentionally doped) and 10^{19} cm^{-3}.

[0033] Any structure that redirects light toward window layer 40 may be substituted for porous region 44. For example, rather than being made porous, the surface of the n-type region exposed by removing the substrate may be roughened, or textured with, for example, a photonic crystal structure. Alternatively, porous region 44 may be replaced by a reflective material, such as a reflective metal or coating.

[0034] One or more openings which expose bonding layer 34 are etched through the semiconductor structure, then contacts are formed, and the wafer is singulated into individual devices. A finished device, attached to a mount, is illustrated in Fig. 6. An opening 54 is etched through porous region 44, non-porous n-type region 49, light emitting region 48, and p-type region 46 to expose conductive bonding layer 34. Conductive bonding layer 34 serves as the electrical contact to the p-type region. N-contact metal 58 is formed on the remaining part of porous region 44, and p-contact metal 60 is formed on the exposed portion of conductive bonding layer 34. N- and p-contact metals 58 and 60 may be electrically isolated by dielectric layer 56.

[0035] The device may be attached to any suitable surface. The device illustrated in Fig. 6 is mounted on a mount 12, which may be similar to the package substrate described above in the background section text accompanying Fig. 1. N- and p-interconnects 64 and 62 connect the n- and p- contacts 58 and 60 on the device to contacts 22 on mount 12. Top-side contacts 22 on mount 12 are connected to bottom-side contacts 26 by, for example, conductive pillars 28. Interconnects may be, for example, elemental metals, solder, metal

alloys, semiconductor-metal alloys, thermally and electrically conductive pastes or compounds such as epoxy, eutectic joints between dissimilar metals such as Pd-In-Pd, or Au stud bumps.

[0036] Devices according to embodiments of the invention may have several advantages. In the device described in the background section and Fig. 1, many fabrication steps are die-level steps; that is, they are performed after dicing a wafer into individual devices. For example, attaching the device to a package substrate, underfilling the device, removing the growth substrate, thinning or texturing the exposed semiconductor surface, and placing a phosphor material over the device are die-level steps. Die-level steps can be time consuming and difficult to control, such as, for example, placing each die correctly on the package substrate and dispensing the correct amount of underfill in the proper place. In some embodiments of the invention, nearly all fabrication steps are wafer-level steps, not die-level steps. Wafer-level steps may be less time consuming and easier to control than die-level steps.

[0037] The device described in the background section may include organic materials, for example as an underfill to support the LED die during substrate removal, or as an adhesive to attach a ceramic phosphor layer to the device. Organic materials are problematic because they can degrade when exposed to heat and light, which can limit the temperature at which the device can be operated, or undesirably change the color point of light emitted from the device. Devices according to embodiments of the invention do not require organic underfill materials or adhesives.

[0038] In addition, an organic adhesive layer that attaches a ceramic phosphor to the LED die in the device described in the background section may be as thick as 10-15 μm. The thick adhesive can direct a significant amount of light out the side of the device, rather than the top of the device, the preferred surface for light to exit the device. Excessive sidelight can negatively impact the color uniformity and color point of light exiting the device. In embodiments of the invention, the bond between the LED die and the window layer is as thin as 1 μm, which may significantly reduce the amount of side light emitted from the device. Also, some bond materials such as ITO may conduct heat generated in a ceramic phosphor window layer through the LED die to the mounting surface more efficiently than an organic adhesive conducts heat.

[0039] In the device described in the background section, the package substrate is necessary to prevent damage to the semiconductor device during substrate removal. Since window layer 40 provides mechanical support to the semiconductor structure during and after removal of the growth substrate, a package substrate or other mount is not required. Fig. 7 illustrates a device without a package substrate. The n- and p-contacts 58 and 60 formed on the semiconductor structure are redistributed to large area contacts 68 and 70 by one or more dielectric layers 56 and 66, bonding metal layers 63 and 65, and conductive interconnects 62 and 64. Dielectric layers 56 and 66 may be, for example, SiN_x. Interconnects 62 and 64 are described above in the text accompanying Fig. 6. Bonding metal layers 63 and 65 may be, for example, an Al/Ni/Au alloy. Large area contacts 68 and 70 may be, for example, gold.

[0040] In the device illustrated in Fig. 1, p-type region 20, which is disposed between the active region 18 and reflective p-contact 24, is thin, which may reduce the efficiency of the device by introducing undesirable cavity resonances. In embodiments of the invention, the non-porous n-type region 49 is thicker than p-type region 20, thus no cavity resonances are created. Elimination or reduction of cavity resonances may relax limitations on the thickness of the semiconductor between the active region and the reflective contact, and may permit the active region to be grown thicker, have thicker layers, or have more layers.

[0041] In some embodiments, a ceramic phosphor window layer 40 is color matched to a semiconductor wafer prior to bonding. The color point of light emitted by a particular ceramic phosphor window layer/semiconductor wafer combination may be adjusted by laser trimming of the ceramic phosphor before or after bonding the window layer to the semiconductor wafer.

[0042] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

CLAIMS

What is being claimed is:

1. A device comprising:

a semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region;

a window layer;

a light-directing structure, the light-directing structure being configured to direct light toward the window layer; and

an n-contact electrically connected to the n-type region and a p-contact electrically connected to the p-type region;

wherein:

the semiconductor structure is disposed between the window layer and the light-directing structure; and

the light-directing structure is disposed on a surface of the n-type region; and

the p-contact is disposed in an opening formed in the semiconductor structure.

2. The device of claim 1 further comprising at least one transparent bonding layer disposed between the p-type region and the window layer.

3. The device of claim 2 wherein the bonding layer is conductive, is directly connected to the p-type region, and is one of a transparent conductive oxide, indium tin oxide, zinc oxide, and ruthenium oxide.

4. The device of claim 2 wherein a combined thickness of all layers disposed between the p-type region and the window layer is less than 2 μm.

5. The device of claim 2 wherein the p-contact is disposed on the bonding layer in an opening etched through the semiconductor structure to expose the bonding layer.

6. The device of claim 2 wherein the at least one transparent bonding layer is a transparent conductive oxide directly connected to the p-type region, the device further comprising an additional transparent bonding layer disposed between the at least one transparent bonding layer and the window layer.

7. The device of claim 6 further comprising a wavelength converting material disposed in the additional transparent bonding layer.

8. The device of claim 6 wherein an interface between the additional transparent bonding layer and the at least one transparent bonding layer is adapted to scatter light.

9. The device of claim 6 wherein the additional transparent bonding layer is one of a transparent conductive oxide, a non-conducting glass material, a dielectric material, silicon nitride, ITO, soda-lime glass, borosilicate glass, an organic material, benzocyclobutene, spin-on glass, and silicone.

10. The device of claim 1 wherein a bond between the window layer and the p-type region is substantially free of organic material.

11. The device of claim 1 wherein the window layer is one of an optical filter, sapphire, and glass.

12. The device of claim 1 wherein the window layer comprises a wavelength converting material configured to absorb light emitted by the light emitting layer and emit light of a different wavelength.

13. The device of claim 12 wherein the wavelength converting material is disposed in a ceramic layer.

14. The device of claim 1 wherein the light-directing structure comprises one of a porous semiconductor layer and a photonic crystal formed in a surface of the n-type region.

15. The device of claim 1 wherein the light emitting layer is a III-nitride layer.

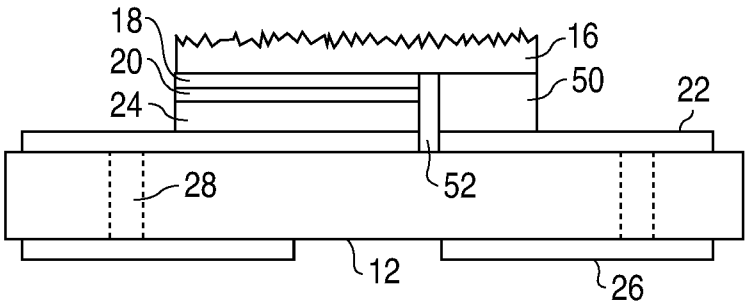

FIG. 1
(PRIOR ART)

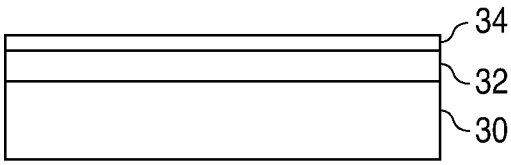

FIG. 2

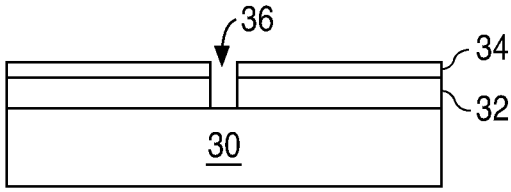

FIG. 3

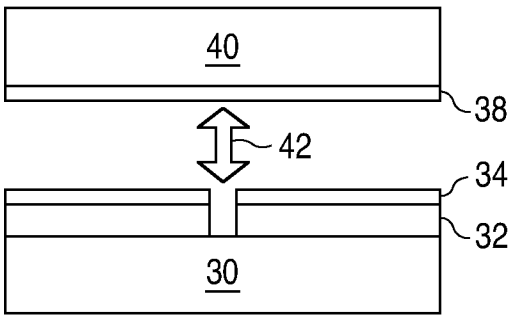

FIG. 4

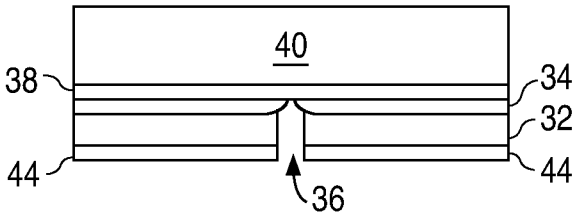

FIG. 5

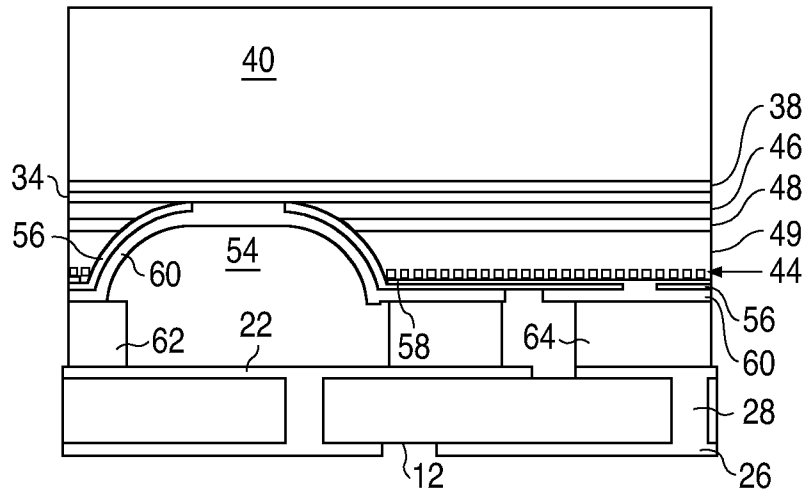
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FIG. 6

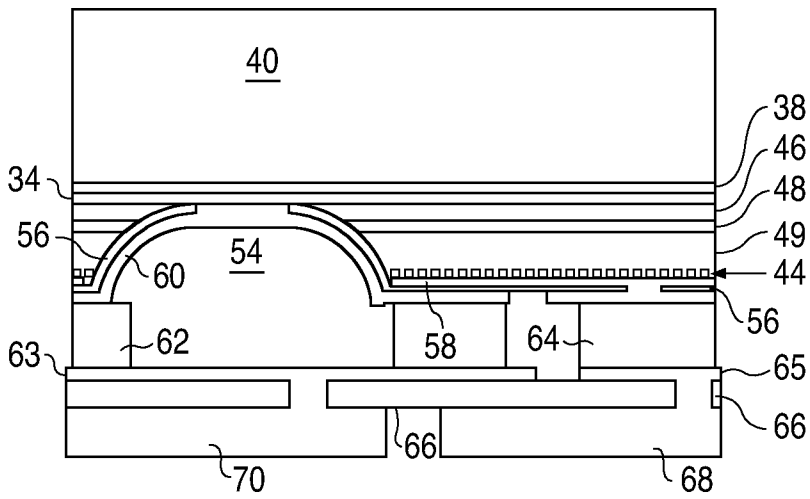
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FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/053065

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/091704 A1 (SHOWA DENKO KK [JP]; ARIMITSU MASAO [JP]) 16 August 2007 (2007-08-16)	1-2,4, 10,15
Y	abstract; figures 2,3,4,8,10 page 17	3,5-9,14
X	US 2005/189558 A1 (LIU WEN-HUANG [TW]) 1 September 2005 (2005-09-01)	1-3,5-6, 9,11-13, 15
Y	abstract; figure 4 paragraph [0017] paragraph [0016]	14
X	EP 1 705 764 A1 (HAMAMATSU PHOTONICS KK [JP]) 27 September 2006 (2006-09-27)	1-2,4, 10-11,14
Y	abstract; figures 2-11 paragraphs [0028], [0041], [0071]	3,5-9,14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2009	29/10/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Heising, Stephan

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/053065

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/063460 A1 (PHILIPS INTELLECTUAL PROPERTY [DE]; KONINKL PHILIPS ELECTRONICS NV [NL) 7 June 2007 (2007-06-07)	1-2, 10-13,15
Y	abstract; figures 10,11	14
A	paragraph [0034] paragraph [0050] paragraph [0037] paragraph [0036]	7
Y	US 2007/284607 A1 (EPLER JOHN E [US] ET AL) 13 December 2007 (2007-12-13) abstract; figures 2-12	14
A	US 2004/211972 A1 (DU SHAWN X [US] ET AL) 28 October 2004 (2004-10-28)	8
A	WO 2005/093863 A1 (SHOWA DENKO KK [JP]; TAKEUCHI RYOUICHI [JP]; NABEKURA WATARU [JP]; UDA) 6 October 2005 (2005-10-06)	2-3
A	US 2006/011935 A1 (KRAMES MICHAEL R [US] ET AL KRAMES MICHAEL R [US] ET AL) 19 January 2006 (2006-01-19) paragraph [0058] paragraph [0086]	1-15
A	US 2004/041157 A1 (WATANABE YUKIO [JP]) 4 March 2004 (2004-03-04)	1-15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2009/053065

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers allsearchable claims.

2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search reportcovers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-15

TCO based bonding layer
window layer material
light direction structure material
light emission material

1.1. claims: 11-13

window layer material

1.2. claim: 14

light direction structure material

1.3. claim: 15

light emission material

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/053065

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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