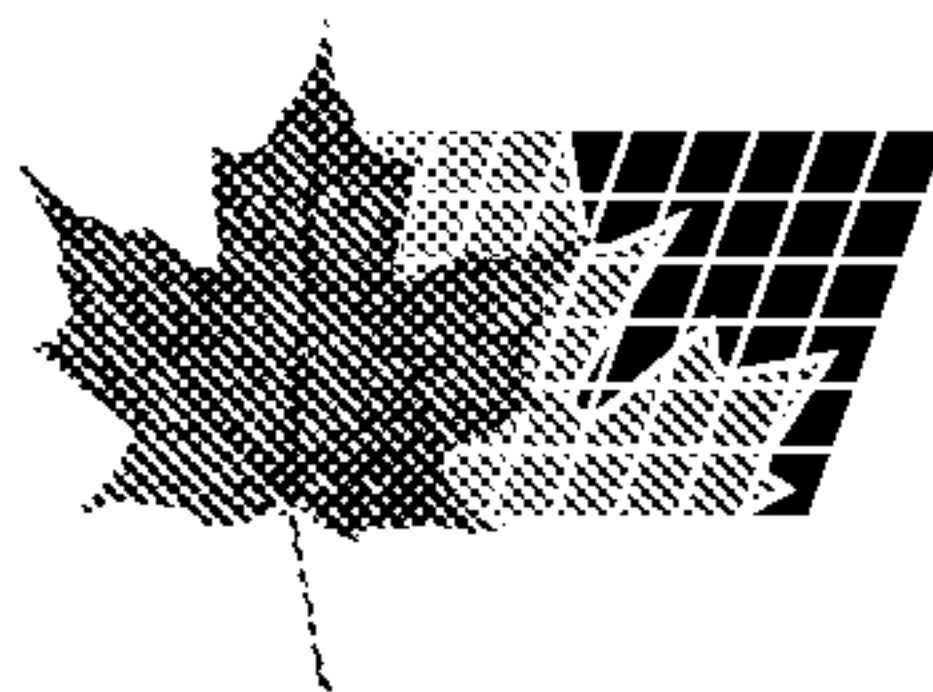




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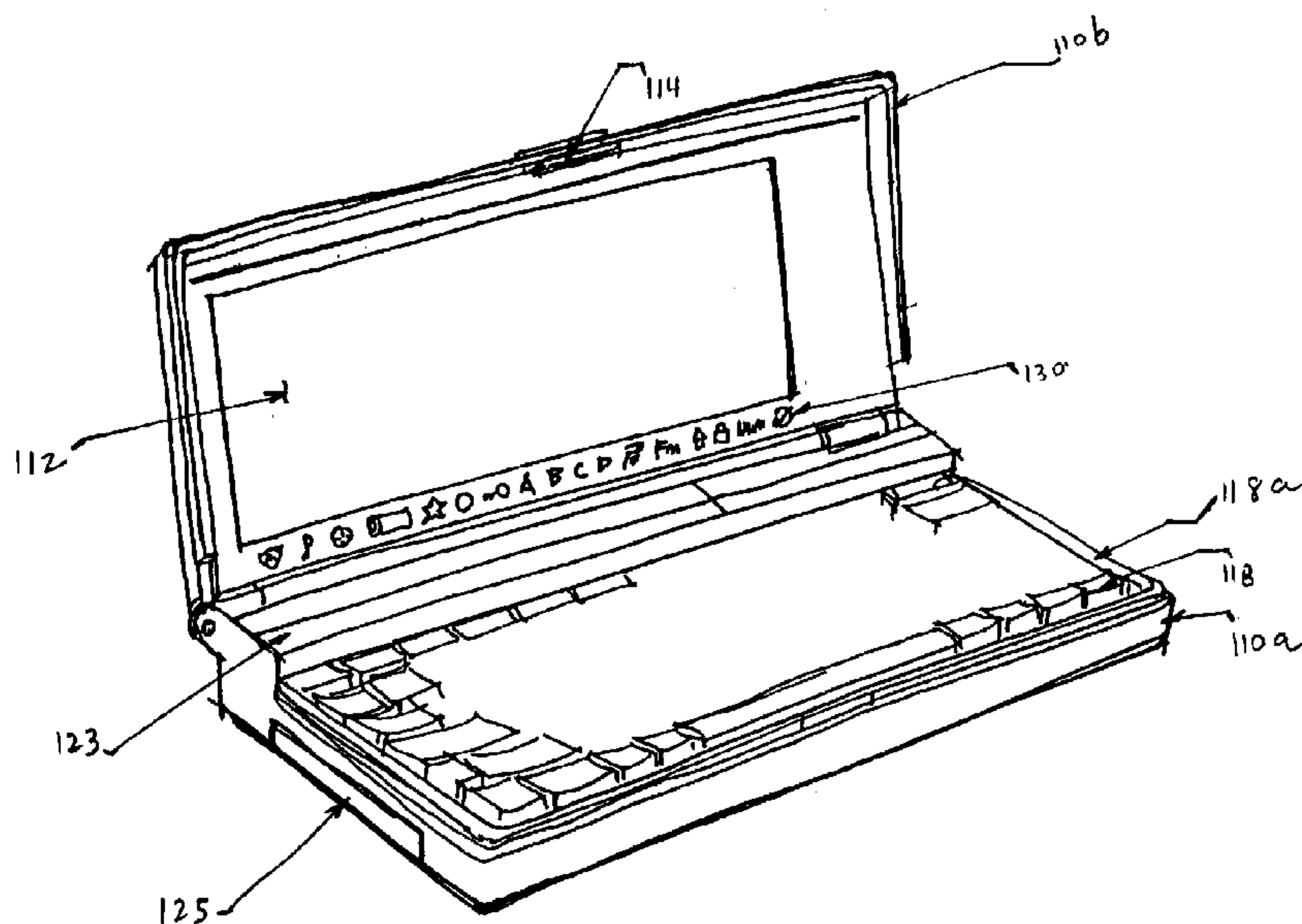
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(54) **ORDINATEUR PORTATIF CONSOMMANT PEU D'ENERGIE**

(54) **PORTABLE LOW POWER COMPUTER**



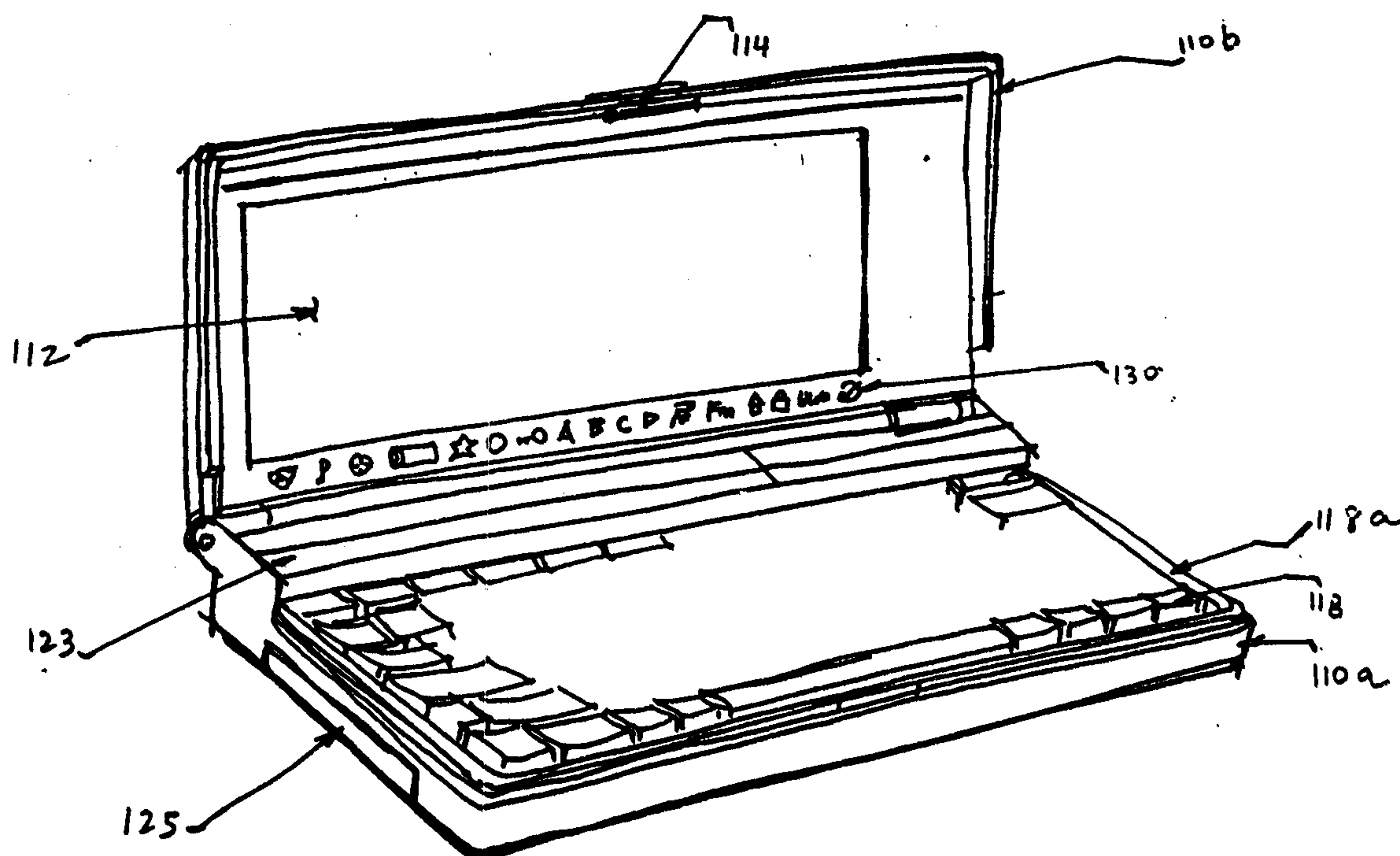
(57) L'invention se rapporte à un ordinateur (110a et 110b) portatif alimenté par batterie, qui comporte plusieurs caractéristiques permettant de concevoir l'ordinateur avec une petite taille et une faible consommation de courant, tout en lui conférant la fonctionnalité d'un ordinateur de taille normale.

(57) A portable battery powered computer (110a and 110b) includes several features to make the computer small in size and low in power consumption, while providing the functionality of a full sized computer.



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(21) International Application Number: PCT/US90/03639 (22) International Filing Date: 28 June 1990 (28.06.90) (30) Priority data: 375,721 30 June 1989 (30.06.89) US (71) Applicant: POQET COMPUTER CORPORATION [US/US]; 650 North Mary Avenue, P.O. Box 62199, Sunnyvale, CA 94086-2994 (US). (72) Inventors: FAIRBANKS, John, P. ; 862 Radcliff Court, Sunnyvale, CA 94087 (US). HARPER, Leroy, D. ; 19990B Olivewood, Cupertino, CA 95014 (US). PRODMOU, Stavro, E. ; 14975 Page Mill Road, Los Altos, CA 94022 (US). CULLIMORE, Ian, H., S. ; 690 Matadero Avenue, Palo Alto, CA 94306 (US). ANGLIN, Noah, L. ; 11100 Enchanto Vista, San Jose, CA 95127 (US). ICHIKAWA, Shinpei ; 4094 Gladhill Street, Newbury Park, CA 91320 (US). MACHAMER, Roy, J. ; 2810 Franklin Street, No. 34, San Francisco, CA 94123 (US). MIRACLE, Gary, R. ; 151 Summerhill Drive, Scotts Valley, CA 95066 (US).		(74) Agents: KLIVANS, Norman, R. et al.; Skjerven, Morrill, MacPherson, Franklin & Friel, 25 Metro Drive, San Jose, CA 95110 (US). (81) Designated States: AT, AT (European patent), AU, BB, BE (European patent), BF (OAPI patent), BG, BJ (OAPI patent), BR, CA, CF (OAPI patent), CG (OAPI patent), CH, CH (European patent), CM (OAPI patent), DE*, DE (European patent)*, DK, DK (European patent), ES, ES (European patent), FI, FR (European patent), GA (OAPI patent), GB, GB (European patent), HU, IT (European patent), JP, KP, KR, LK, LU, LU (European patent), MC, MG, ML (OAPI patent), MR (OAPI patent), MW, NL, NL (European patent), NO, RO, SD, SE, SE (European patent), SN (OAPI patent), SU, TD (OAPI patent), TG (OAPI patent). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: PORTABLE LOW POWER COMPUTER**(57) Abstract**

A portable battery powered computer (110a and 110b) includes several features to make the computer small in size and low in power consumption, while providing the functionality of a full sized computer.

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PORTABLE LOW POWER COMPUTER

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10 FIELD OF THE INVENTION

This invention relates to small low power computers, in particular battery operated computers using liquid crystal displays.

BACKGROUND OF THE INVENTION

15 Personal computers have become faster and smaller in recent years. Desk top computers typically use household power and run commercially available software written for execution through an operating system such as MS-DOS® (MS-DOS® is a registered trademark of Microsoft Corporation) or Unix® (Unix® is a registered trademark of
20 American Telephone & Telegraph). In addition to the computing unit, these computers include a monitor for displaying information to the user and a keyboard for receiving information from the user. They may include
25 disk drives, a printer, a communications modem, and may include even more peripheral devices. Since the computer must be compatible with commercially available software, a basic input/output system (BIOS) which is unique for each computer converts commands generated by the operating
30 system or application program to specific machine commands implemented by the hardware of the machine. These computers include an internal clock which operates continuously when the machine is turned on and controls the central processor to access memory, load registers,

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read and write to disk, detect keyboard use, and control a display, all operations synchronized with cycles of the internal clock. In addition, if the computer accesses an external port, the external communications may be
5 controlled by an asynchronous clock through a UART (universal asynchronous receiver/transmitter). The power used by these desk-top wall-plug computers has not been of particular concern because it is small when compared with power used by other appliances which also use the same
10 power source.

Methods for reducing power used by a computer have included using CMOS circuitry, and using liquid crystal display monitors rather than cathode ray tube monitors or plasma display technology.

15 There exists a class of small, lightweight computers which have been designed for low power and may use batteries. These computers do not have the computing capability of a desk top machine nor the ability to run the full range a commercial software and operating systems
20 available for desk top machines. They typically have reduced display resolution and inconvenient keyboards.

Another class of computers generally described as lap top computers are battery operated, portable, and may run a broad range of commercial software. However, these lap
25 top computers are powered by bulky rechargeable batteries and can only operate for a few hours before requiring the batteries to be recharged.

SUMMARY OF THE INVENTION

The present invention provides a computer combining
30 many features which allow the computer to occupy a small space and allow for operation of the computer using considerably lower power than that of the lap top computers presently available, and yet which has the computing power of a desk-top IBM XT or AT and a display
35 monitor which can display 80 characters by 25 lines. A test of one XT compatible computer shows a battery life of

about 100 hours of operation with two AA alkaline batteries. A preferred embodiment uses standard batteries widely available, so that this computer can continuously serve a user travelling to remote parts of the world. that is, spare batteries can be
5 easily carried (a single AA size battery, for example, is less than two inches long and one inch thick) and may be purchased widely just as are batteries used in most flashlights and portable radios. The preferred embodiment could use any battery which met the form factor of the compartment and had the same
10 approximate electrical specifications. Another embodiment could use a battery other than AA size batteries.

Thus, the computer operates effectively on inexpensive batteries that, as in the example of AA batteries, initially provide about 1.6 volts, and as they are drained later provide
15 only about .8 volts. Prior art computers require batteries that provide a level amount of voltage during their useful lives.

In a preferred embodiment the computer is housed in a two-part low profile rectangular case hinged along one long edge and latched at an opposite edge. The hinge extends along a back
20 edge of the case and rotatably joins upper and lower portions of the case. The case is preferably of a plastic such as polycarbonate and/or ABS plastic or both. The case is of molded constructions.

A lower portion of the case includes a keyboard, one or
25 two memory cards, batteries, and most of the integrated circuit components of the computer. The integrated circuit components in this lower portion are attached to the lower side of a printed circuit board which occupies most of the rectangular area encompassed by the case. Included in these integrated circuit
30 components are two

ASIC (application specific integrated circuit) chips. In order to conserve space, particularly vertical space, these ASIC chips are put on the board without the usual packaging. Such packaging (which is omitted) would include a plastic or ceramic protective
5 cover surrounding a lead frame which connects interior pin-outs to exterior pins. The unpackaged chip is bonded directly to the lower printed circuit board, thereby saving both horizontal and vertical space in the present very compact structure. The microprocessor chip is also attached directly to the printed
10 circuit board without intervening packaging, which reduces connection points and cost.

Also attached to the lower side of this printed circuit board are connectors for receiving removable memory cards, preferably at least two connectors for two cards. These
15 connectors are the same thickness as the card itself. No circuit components are located on that part of the printed circuit board adjacent to where the memory cards are placed, so that the memory cards fit within the existing envelope of the computer housing.

At one or several edges of the printed circuit board
20 are pads to which traces extend from pins of the integrated circuit chips to which test signals are applied during manufacturing. These pads are accessed with edge connectors which are designed to slip over an edge of the board and make electrical contact with the pads. This avoids the need for
25 applying test probes to the interior of the circuit board and thereby saves time and avoids testing mistakes.

The upper side of the same printed circuit board in the lower portion of the case serves as a back plate for the keyboard. Traces for electrically detecting each key

state are applied directly to the upper side of this printed circuit board. The keyboard includes a keyplate through which extend a plurality of keys. The keys press corresponding cones in an insulating flexible membrane, 5 each cone including a conductive flexible pad which in a compressed position spans conductive traces on the printed circuit board and in a non-compressed position leaves these conductive traces unconnected.

The keyboard occupies most of the inner surface of 10 the lower case, occupying more than half, and preferably 70% or more of the surface area of the inner surface of the lower case.

The upper side of this printed circuit board also includes traces for detecting a machine reset. As a novel 15 feature of the present invention, reset is activated by inserting a pointed object such as a pencil point through an opening in the keyboard and pressing an electrically conductive pad rather than by pressing a key or combination of keys.

20 As another novel feature of the present invention, one of the keyboard keys is an on/off toggle key. The computer never turns completely off, but in the off state operates only a low frequency clock which keeps time-of-day.

25 After testing of the lower printed circuit board and installation of the membrane during assembly of the computer, the keyplate which holds the keys in position is welded to the lower portion of the case in order to achieve accurate registration of the keys, the membrane, 30 and the traces.

Located between the hinge and the keyboard area is a compartment including batteries and a capacitor. This capacitor is sufficient to maintain volatile memory with the computer in the off state while batteries are being 35 changed. The batteries are covered by a plate which is imprinted with descriptions of a top row of keyboard function keys, these function keys being located just

adjacent to the battery cover plate. In one embodiment, four notations in four different colors are imprinted on the cover plate adjacent each function key. Keys for "shift", "alt", "ctrl", and a special logo key are correspondingly colored to
5 indicate to a user that combining the "shift", "alt", "ctrl", or the logo key with the adjacent function key produces the function noted in color adjacent the function key. Alternate cover plates, tapes for attaching to the cover plate, or cards for placing adjacent this cover plate may be provided for use with
10 different software packages.

An upper portion of the case houses a liquid crystal display plus a separate power supply for the liquid crystal display. In one embodiment a space is provided between the display and the outside of the upper case for insertion of a
15 display back light powered by separate batteries or other power source. The liquid crystal display occupies most of the entire area enclosed by the upper portion of the case, with a narrow frame surrounding the liquid crystal display and its cover.

The display when displaying characters shows 25 lines
20 of 80 characters per line. A line of characters is typically 8 pixels tall so that the standard 25 lines of text are displayed using 200 rows of pixels. Additionally, a status line using one or more rows of pixels at the top, bottom or both, of the display are provided for showing status of various software programs and
25 hardware conditions. Coordinating with these displayed status lines are imprinted legends along the top, bottom, or both margins of the display frame for indicating to the user the meanings represented by these status lines. As with the keyboard, different legends can be provided for different
30 software packages.

Since separate power supplies are located in the two portions of the computer case, the number of current carrying lines which must extend between the upper and lower housing is minimized. A cable including these lines extends from the lower
5 to the upper portion of the case and is located toward the interior of the computer from the hinge axis. The cable has sufficient length to span from its lower point of connection to its upper point of connection when the computer case is fully open. The spiral design of the cable acts as a spring so that
10 when the computer is closed, the excess cable slack is taken up in a cable cover located in the upper or lower portion of the case, preferably lower. This cable cover protects the cable from excess flexure, assuring long life.

This arrangement of the components allows for the
15 computer to fold to a very compact size for being carried and to open to a convenient size in which the two components which interface with the user, namely the keyboard and the display, are large enough to be convenient. To further reduce thickness, the keys are made so that some keys are pressed by the display upon
20 closing the computer case. Preferably, these are the front (lower) row of keys.

In one embodiment, the keyboard is controlled such that a multiplicity of key presses does not cause an executing program to cease operation. The on/off key is a key not depressed when
25 the case is closed. When the

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on/off key is pressed to toggle the computer to its off state, other keys are deactivated such that pressing the other keys upon closing the case is not detected by the computer. When the computer is in this off state, the processor does not lose its place in the program which was running. All memory remains static but execution is halted until the machine is moved out of the off state. While in this off state, timer interrupts are processed allowing time of day updating, and allowing software which uses the time of day interrupt to process the interrupt.

The computer of the present invention includes a power management system which maintains as many components of the computer in an off state for as much time as possible even when the computer is on. Individual components can be turned off while other components remain on. Components of the machine which can be turned off while the machine appears to a user to be on include the oscillator and clock which cycle the central processor, another oscillator and clock which control the display, a direct memory access (DMA) clock tied to the central processor oscillator which controls direct memory access circuits, and an oscillator and clock for communication to an external port. While the machine is turned on, that is, while the display is on and the machine is responding to user input, the hardware detects activities for which some parts of the machine can be turned off. These clocks can actually be turned off while the user is in the midst of executing a program. For example, when a user is executing a word processing program, the clock which controls the central processor is turned off for most of the time between one keystroke and the next.

In a preferred embodiment, four activities are monitored for determining when parts of the machine can be turned off: the state of the on/off switch, keyboard presses, software activity and clock ticks generated by a low frequency clock and a divider circuit. When these activities are not occurring, certain clocks and devices

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driven by the clocks are turned off. Because in a preferred embodiment CMOS circuitry is used, which uses most of its power when switching, turning off oscillators and their associated clocks greatly reduces power consumption of the system.

5 Turning off devices themselves also reduces power.

The invention may be summarized as a compact portable computer including a keyboard, the keyboard comprising: a keyplate having a plurality of keys and a printed circuit board underlying and held in a spaced relation to said keyplate, said
10 printed circuit board having two surfaces, a first surface bearing conductive traces for detecting key presses of the keys of the keyplate, and an opposing second surface having most of the integrated circuit components of the computer mounted thereon, thereby providing a compact portable computer
15 keyboard.

According to another aspect the invention provides a computer system comprising; a main processor integrated circuit of the computer system; a full function alphanumeric keyboard for inputting data into said main processor; a display device
20 for outputting data from said main processor; and a printed circuit board, one side of said printed circuit board having said main processor integrated circuit mounted thereon and the other side of said printed circuit board bearing conductive traces for detecting key presses of said keyboard.

25 BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1. Perspective view of the computer.

Figure 2. Exploded view of keyboard.

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Figure 3. System diagram showing interconnections of the integrated circuit chips.

Figure 4. A circuit board, front side.

Figure 5. Circuit board of Figure 4, rear side.

5 Figures 6A, 6B. Attachment of IC's to a circuit board.

Figure 7. A test structure.

Figures 8A, 8B. A computer reset structure.

Figure 9. A border plate, display and keyboard.

10 Figures 10A to 10Ce. Schematics of a peripheral ASIC.

Figures 11A to 11Ad. Schematics of a system ASIC.

Appendix A is an I/O map.

Identical reference numbers in various figures refer
15 to identical or similar structures.

DETAILED DESCRIPTION OF SOME PREFERRED EMBODIMENTS

Overview of System Components

Fig. 1 shows a perspective view of the computer showing upper case 110a, lower case 110b, display 112, display
20 frame 113, keyboard 118, key plate 118a, battery

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cover 123, hinge 111, latch 114, memory card tray 125, and display indicator graphics 130.

Fig. 2 shows an exploded view of the computer keyboard 118 showing keyplate 118a with keys such as 181, 5 182, and 183, membrane 128 with cones such as 281, 282, and 283 each holding a conductive pad (not shown), and printed circuit board 138.

Membrane 138 is elastomeric, and protrudes upward in a plurality of locations to form a plurality of 10 elastomeric cones, one beneath each key, for example cones 281, 282, and 283 beneath keys 181, 182, and 183 respectively. Each cone is truncated at a flat (or relatively flat) upper surface which is contacted by an underside of its corresponding key. Extending downward 15 from the flat upper surface of each of the elastomeric cones into the interior of the respective cone is an elastomeric conductive pill. When a key is pressed, its corresponding cone is compressed, moving its corresponding pill into position to span conductive traces (not shown) 20 on the printed circuit board 138.

Figure 4 shows a first side of the printed circuit board 138 including IC chip mounting areas 302, 304, 306.

Figure 5 shows the rear (i.e., second) side of the printed circuit board 138 including key contacts such as 25 310, 312, etc. to which conductive traces such as 318, 320, etc. are connected.

Figure 6A shows in a side view how one IC chip 340 is electrically connected to printed circuit board 138 by bond wires 342, 344, etc. from pins 346, 348, etc. on chip 30 340 to bonding pads 350, 352 on printed circuit board 138. IC chips such as 340 thus preferably do not have the usual lead frame packaging. Figure 6B shows a top view of Figure 6A.

Figure 7 shows a test structure as provided on 35 printed circuit board 138. As shown, five separate test interconnect areas are provided, 360, 362, 364, 366, 368, each consisting of several pads such as 370, 372 to which

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test signals are provided by test cables such as 380. Test cable 380 is connected to printed circuit board 138 only when testing is to be performed. Card edge test connector 382 connects test cable 380 to the pads 370, 372, etc. As shown, indicating locator such as 390, 392 are provided as cut outs in the edge of printed circuit board 138 to locate the card edge test connectors such as 382. Note that as shown in Figures 4 and 5, such a test structure is provided on both sides of printed circuit board 138.

Figure 8A shows a top view including dimensions of a portion of the keyboard 118 of the computer showing key 181 in keyplate 118a. Key 181 is partly cut away to expose cone 281.

Figure 8B shows a cross-sectional view along line B-B in Figure 8A. As shown in Figure 8B (key 181 not shown) a corresponding gap 400 has been left in keyplate 118a exposing cone 281. Thus it is possible to press down on cone 281 with an object (such as a pencil point) through gap 400. Preferably this is done to reset the computer, by compressing conductive pill 402 against traces 404, 406 on printed circuit board 138.

Fig. 3 shows a chip architecture computer system diagram showing interconnections of the integrated circuit chips physically shown in Fig. 2b plus the LCD driver chips located in the upper case and not shown in Fig. 2b.

The system of Fig. 3 includes an 80C88 microprocessor 16, a Peripheral ASIC chip 17, a System ASIC chip 18, and an LCD RAM 15, all physically located on a PCB board. This small combination of integrated circuit chips models in one embodiment an IBM XT computer. It may model other computers in other embodiments. They are physically located in the lower portion of the computer casing beneath the keyboard. Also physically located in the lower portion of the case is 512K of system RAM 19, a BIOS ROM chip 20, an application ROM chip 21, one or two memory cards 22a and 22b, and expansion port 23, and UART driver

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chip 24. VCO and other oscillators 11, and system power supply 13 (which in a preferred embodiment includes two AA batteries) are also located in the lower portion of the case in addition to keyboard 12.

5 Located in the upper portion of the case is the LCD display, an optional audio transducer, and a separate power supply.

Display driver 14 includes row and column drivers and the analog power supply plus a unique display scan
10 technique which lowers power. The entire system was designed to lower power. In particular, oscillators 11 require low power because they can be turned off when not actively used, a unique feature. The majority of the digital logic is CMOS, including memory 19, BIOS 20,
15 application ROM 21. These draw microamps in the standby state and up to 100 milliamps in operation.

On the reverse side of the PC board is the lower level of the keyboard unit. The contact lines of the keyboard are applied directly to the reverse side of the
20 PC board.

Following is a list of the blocks and lines shown in Fig. 3.

BLOCK 11

VCO/OSCILLATORS. This block contains all of the
25 frequency oscillators used in the system. They include a display clock oscillator running at about 800 KHz, a communications clock oscillator running at 1.8432 MHz, a low frequency oscillator running at 32,768 Hz, and a voltage controlled oscillator (VCO) which operates between
30 1 and 8 MHz.

There are four oscillators. The oscillator which drives the Processor 16 is voltage controlled, so if there is a sag in the supplied voltage, the frequency will drop to compensate for the lower performance of the CMOS
35 circuits. This also allows the processor speed to be automatically adjusted when the system power supply changes output voltages. At 5 volts all components will

run at 8 mHz. At 3 volts they would not run at 8 mHz but at 2 mHz the system will run. There is a power advantage to running at 3 volts because

$$P = C * V^2 * F$$

5 in a CMOS system where P is power, C is a constant, V is voltage, and F is frequency. So changing voltage from 5 volts to 3 volts gives almost a 3:1 power savings. Also, reducing the frequency from 8 mHz to 2mHz also conserves power.

10 In a preferred embodiment there are actually two modes, 5 volts and automatic. In automatic mode, the system moves after a delay from 3 volts to 5 volts when power demand is heavier. When current exceeds a certain level, preferably between 1 and 10 milliamps, the system moves to 5 volts.

OSC IN

15 These four lines provide the oscillator outputs from block 11 to the Peripheral ASIC 17 for distribution to other parts of the system.

OSC GATE

20 These three lines provide control signals from Peripheral ASIC 17 to block 11 to enable the respective oscillators. These signals are used to enable or disable the oscillators in block 11. There are only three enable signals because the low frequency oscillator is always running.

BLOCK 12

25 **KEYBOARD.** This is a standard matrix keyboard arranged in a 6x11 matrix of columns and rows. When a key is pressed, it completes the circuit between a selected row and column. The rows and columns are scanned by the keyboard control circuits within the Peripheral ASIC 17.

The novel feature of Keyboard 12 is that fewer lines are needed between keyboard 12 and ASIC 17. Controller 17 uses only 7 return lines and 11 scan lines for a total of 18 lines to keyboard 12. Conventional keyboards use about 26 lines. Also unlike typical personal computers of today, no chip is dedicated as a keyboard controller. All keyboard control occurs in ASIC 17. Saving a chip saves power and board space.

KBSCAN[0..10]

10 These are the keyboard matrix 12 scan lines. The keyboard control circuits within the Peripheral ASIC 17 send out a scan signal on each of these lines individually and monitor the KBCOL[0..5] lines for a signal return.

KBCOL[0..5]

15 These are the keyboard matrix 12 column lines. These lines are monitored during keyboard scanning for a signal which would indicate that a key is pressed providing a path from one of the KBSCAN[0..10] lines to one of the KBCOL[0..5] lines.

20 POKEYN

 This is a line from the keyboard 12 which is associated with specially labeled key. When this key is pressed, it provides a path to ground causing a low signal on this line. When said key is not pressed there is no path to ground. The line is pulled up to VDD to assure that its default state is high. This signal is monitored by the Peripheral ASIC 17 and may interact with software running on the processor 16.

ONOFFN

30 This is a line from keyboard 12 which is associated with a special key used to turn the computer on and off. When this key is pressed, it provides a path to ground causing a low signal on this line. Otherwise the line is pulled up to VDD to assure that its default state is high. This signal is monitored by the Peripheral ASIC 17 and may interact with software running on the processor 16.

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MRESETN

This is a line from the keyboard 12 which is associated with the reset opening in the keyboard. When this contact is connected by inserting a pointed object 5 into the opening, it provides a path to ground causing a low signal on the line. This signal is monitored by the Peripheral ASIC 17 which resets the computer when a low transition is detected.

BLOCK 13

10 SYSTEM POWER SUPPLY. This is the power supply for the majority of the circuits within the computer. One notable exception is the display which has its own power supply located within block 14 as described above. This power supply includes the power source, namely two AA-size 15 batteries, and necessary circuits to provide needed voltages and current for the computer.

SELVDD

This signal into block 13 is used to select from two possible supply modes: high voltage output (SELVDD= Low), 20 and automatic mode (SELVDD=Tristate). In another embodiment a low level output on this line forces the power supply into a low voltage mode. In the current invention, low voltage is three volts, and high voltage is five volts. In automatic mode, current demand is sensed, 25 and when it passes a predetermined threshold, approximately 20 milliamperes in the current invention, it moves the voltage output from low to high voltage after a programmed delay. This signal is controlled by a bit within the Peripheral ASIC 17 allowing software to select 30 between the high voltage and automatic modes of power supply operation.

LOWBAT

This signal from block 13 to the Peripheral ASIC is used to monitor the voltage of the system batteries. It 35 is low to indicate that batteries are above a predetermined threshold (see discussion of BATMON), and goes high when these batteries fall below the threshold.

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This signal is monitored by the Peripheral ASIC 17 and may interact with software running on the processor 16. Since software running on the processor is able to monitor the real time condition of the batteries and determine when the batteries are about to expire, the BIOS will refuse to move from the off state when it is determined that doing so would jeopardize the integrity of the system memory and processor states.

BATMON

10 This signal is used by the battery voltage monitor circuits in 13. The signal can be manipulated by the processor 16 to set the threshold at which LOWBAT will change states. When BATMON is high, the threshold is 1.8 volts. When it is low, the threshold is 1.6 volts. This is used to sense low and dead battery conditions.

VBAT

This is the battery voltage from the computer batteries which is used by the circuits and power supply within block 14 and ranges between 1.6 and 1.3 volts.

20 SPKD

This is the signal from Peripheral ASIC 17 to the drive circuits of the audio transducer within 14. This signal is controlled by a bit within the Peripheral ASIC 17 which can be manipulated by the processor.

25 LCDPWRN

This signal controls the LCD power supply within 14. When it is low, the power supply is enabled and running. When it is high, the power supply is disabled and producing no output. This signal is controlled by a bit within the Peripheral ASIC 17 which can be manipulated by the processor.

LCD_CLOCKS

These five signals are used to clock the LCD driver chips within 14. They are generated by the display drive refresh circuits within the Peripheral ASIC 17.

BLOCK 14

VIDEO DISPLAY. This block contains the LCD display

driver circuits, the display power supply, the LCD screen, an audio transducer, and drive circuits for the audio transducer.

LCD driver 14 and LCD RAM 15 control a liquid crystal display screen which is used in the present invention. LCD RAM 15 receives information about characters or graphic images to be displayed on the LCD screen. LCD RAM 15 includes a character memory which stores an ASCII representation and display attribute for each display character position, bit map images of each character in the character set currently in use, and a bit map memory where each display pixel on the LCD display is represented. A look-up table is also stored which is used by the display controller located within the Peripheral ASIC 17. Additional memory is provided which can be used as nonvolatile data storage. LCD RAM 15 includes two 32K x 8 static RAM chips. These chips store character and attribute data, LCD bit map data, character bit map data, and character translation data.

LCDDATA[0..7]

These are the data lines between the display controller within the peripheral ASIC 17 and both the LCD RAM 15 and the LCD driver chips located within display driver 14. Data is sent from Peripheral ASIC 17 to display driver 14 during display refresh cycles in order

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to update data in the driver chips which is ultimately displayed on the LCD display. A two way path exists between Peripheral ASIC 17 and LCD RAM 15 and is used when the display driver circuits in Peripheral ASIC 17 read and write data in the two RAM chips 15.

LCDADDR[0..14]

These are the address lines used to access the two RAM chips in LCD RAM 15. The addresses are generated by display control circuits within Peripheral ASIC 17.

10 VRAMCSN

This signal line from the display control circuits within Peripheral ASIC 17 is used to chip select one of the two RAM chips within LCD RAM 15. Specifically, this line selects the RAM used to store character, attribute, and LCD bit map data. This line is connected to the chip select pin on the RAM chips in LCD RAM 15.

VRAMOEN

This signal line from the display control circuits within Peripheral ASIC 17 is used to enable the currently selected RAM chip within LCD RAM 15 (see discussion of VRAMCSN and VROMCSN) to drive data from the memory location specified by LCDADDR[0..14] onto the data bus LCDDATA[0..7].

VMEMWN

25 This signal line from the display control circuits within Peripheral ASIC 17 causes the currently selected RAM chip within LCD RAM 15 (see discussion of VRAMCSN and VROMCSN) to latch the data on LCDDATA[0..7] into the address specified by LCDADDR[0..14].

30 VROMCSN

This signal line from the display control circuits within Peripheral ASIC 17 is used to chip select one of the two RAM chips within LCD RAM 15. Specifically, this line selects the RAM used to store character bit maps and translation address data. It is connected to the chip select pin on the RAM chips within LCD RAM 15.

BLOCK 16

80C88 CPU. This is the processor on which the architecture of the computer is based. It may be purchased from Intel Corporation, Harris Semiconductor, or
5 OKI Semiconductor.

S[0..2]

These are processor status pins of microprocessor 16 and are connected to the 8288 compatible Bus Controller cell located with the System ASIC 18. Their function is
10 detailed in the data sheet of both the 80C88 and 8288 components available from Intel Corporation.

LOCKN

This is the processor pin LOCK from processor 16 and is connected to the System ASIC 18.

15 INTR

This is the processor pin INTR which is used to generate interrupts. It is connected to the 8259 compatible Programmable Interrupt Controller cell located within the System ASIC 18. The function of this signal is
20 detailed in the data sheet of both the 80C88 and 8259 components available from Intel Corporation.

SNMI

This signal line is connected to the NMI (non maskable interrupt) pin of the processor 16. A signal on
25 this line is generated by the System ASIC 18 and is the processor 16 non-maskable interrupt. The term nonmaskable interrupt indicates the interrupt cannot be masked by the microprocessor 16. This interrupt can be masked by circuits external to microprocessor 16.

30 AAD[0..7]

Processor 16 address data bus lines. These lines are the multiplexed address and data bus of the processor and connect to the peripheral ASIC 17 and the 8288 compatible Bus Controller cell located with the System ASIC 18.
35 Their function is detailed in the data sheet of both the 80C88 and 8288 components available from Intel Corporation.

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AA[8..19]

These are the high order processor 16 address lines. They are connected to both the circuits within the Peripheral ASIC 17, and the 8288 compatible Bus Controller cell located within the System ASIC 18. Their function is detailed in the data sheet of both the 80C88 and 8288 components available from Intel Corporation.

SYSCLK

This is the system clock signal line used to clock both the processor 16 and circuits within the System ASIC 18. The system clock signal is generated within the Peripheral ASIC 17 (where it is also used) and is derived either from the VCO oscillator located in block 11 or from an external source provided on line EXTSYSCLK.

15 CPURDY

This is the READY signal line on the processor 16 and is used to extend processor 16 read and write operations to allow slower devices to interface with the processor 16. The signal on this line comes from the Peripheral ASIC 17. Circuits within the Peripheral ASIC 17, the System ASIC 18 (see SREADY), or external devices connected through the Expansion Port 23 (see IOCHRDY) may use this line to synchronize data transfer with the processor 16.

BLOCK 1725 PERIPHERAL ASIC

This is one of two ASIC chips preferably used in the present invention. PERIPHERAL ASIC 17 is the interface between the processor and peripheral devices, including keyboard 12, system power supply 13, LCD display driver 14, and LCD RAM 15. It also interfaces to oscillators 11 and turns them on and off under software control. A schematic of Block 17 is shown in Figures 10A to 10Ce.

Numbering in the lower right corner of the schematics of Figures 10 and 11 is hierarchical. Each figure includes, in addition to the blocks, a list of signals entering and exiting the block, each signal name surrounded by an arrow. Signals on buses more than one

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bit wide have names specifying the number of lines in the bus.

Figures 10 and 11 show in detail a presently preferred embodiment of the invention. The circuits of
5 Figures 10 and 11 are each respectively an application specific integrated circuit chip as implemented by LSI Logic Corporation. Names of lines, buses, and gates meet the specifications of LSI Logic Corporation and can be used to generate a net list of gates to be connected in an
10 ASIC chip.

The PERIPHERAL ASIC 17 (application specific integrated circuit) is one chip of a two chip implementation of an IBM PC/XT compatible computer. A
complete PC/XT compatible system may be implemented with
15 this chip, a SYSTEM ASIC 18 (described below), an Intel 8088 compatible CPU, and memory devices. The PERIPHERAL ASIC 17 supports a 640 x 200 pixel LCD display, a 11 x 7 key keyboard matrix, RS-232 communications, time keeping, and power management functions.

20 The PERIPHERAL ASIC chip performs peripheral functions including RS-232 serial communications, LCD display control, keyboard control, time keeping, and power management. The PERIPHERAL ASIC contains a National Semiconductor 16C450 compatible circuit for serial
25 communications, as well as display controller, keyboard controller, timer, and power management circuits unique to the PQ-XT.

The PERIPHERAL ASIC chip supports serial communication through the use of a National Semiconductor
30 16C450 compatible UART. The 16C450 compatible registers are located at ports 03F8 - 03FFh, compatible with the COM1 definition for the IBM PC/XT, along with the use of interrupt request IRQ4. The PERIPHERAL ASIC supports enabling/disabling the UART by writing a zero/one to bit 4
35 of port F6E1h. Disabling the UART causes its registers to disappear from the port map. The UART is enabled upon reset of the PERIPHERAL ASIC.

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The PERIPHERAL ASIC supports the time keeping functions used in an IBM PC/XT compatible machine. The circuit utilizes a 32.768 KHz clock reference and divides this to the normal 18.2 Hz (54.9 ms) interrupt request IRQ0 used by the BIOS to keep time.

The PERIPHERAL ASIC can also generate interrupts at a much lower frequency, specifically, once every 56.2 seconds. This interrupt frequency is to be used when the machine is idle in order to allow the machine to wake up to update time less frequently and therefore burn less power. A set of registers, port F6E5h (LSB) and port F6E6h (MSB), hold the number of 54.9 ms increments. This provides the BIOS a way to insure that no time is lost if the computer wakes up and returns to the 54.9 ms timer interrupt frequency somewhere in the middle of the 56.2 second cycle. Since the value in ports F6E5 - F6E6h is free-running, it should be cleared before initiating a 56.2 second cycle. This may be accomplished by writing a one to bit 6 of port F6E4h. Returning bit 6 of port F6E4h to zero will allow incrementing to occur.

The PERIPHERAL ASIC is designed to interface to a 11 row by 7 column matrix keyboard. The keyboard controller scans the keys by driving a single row low (to 0) and sampling the column inputs. If a key is down, the controller determines whether it is a new push or the key is just being held down. If it is a new push, the controller will generate the appropriate scan code and interrupt the processor via interrupt request, IRQ1. The controller will then suspend sampling until the interrupt is cleared by writing a one followed by a zero to bit 7 of port 0061h. Scan codes are read from port 0060h. Table 1 lists the scan code returned for each key in the 11 x 7 matrix. If no key is pushed the controller will continuously scan the keyboard until a key is detected. If the last key pushed is held for a sufficient amount of time, the controller will repeatedly interrupt the processor. Keyboard repeat times are broken into two

classifications, the time before the first repeat interrupt, and the time for subsequent repeat interrupts. Repeat times may be programmed by writing to bits 4 - 7 of port F6E0h. Table 2 shows the corresponding repeat times 5 for values written to port F6E0h.

The keyboard controller runs off a 32.768 Khz clock, with each row being scanned approximately 256 times a second. Keyboard scanning may be halted by writing a one to bit 6 of port 0061h. Writing a zero back to bit 6 of 10 port 0061h will resume scanning where the controller left off.

The keyboard controller modifies the scan codes of certain keys depending upon the level of the PQKEYN input. This input, which is grounded when its 15 corresponding key is pushed, will cause certain keys to return an alternate scan code. Table 1 lists the scan codes of those keys affected by the PQKEYN input. Table 2 lists keyboard repeat speeds.

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TABLE 1
KEYBOARD SCAN CODES (HEX)

ROW #	COL 0	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6
ROW 0							
5 KEY	UP-ARW	R-SH	J	ALT	F	:	NULL
NM CODE	48	36	24	38	21	27	00
PQ CODE	49	36	24	38	21	4E	00
ROW 1							
10 KEY	RTN	SP	DN-ARW	L	Z	H	INS
NM CODE	1C	39	50	26	2C	23	52
PQ CODE	4C	39	51	26	2C	23	52
ROW 2							
15 KEY	D	K	G	'	R-ARW	DEL	L-ARW
NM CODE	20	25	22	28	4D	53	4B
PQ CODE	20	25	22	28	4F	53	47
ROW 3							
20 KEY	CTL	U	P	X	B	,	NULL
NM CODE	1D	16	19	2D	30	33	00
PQ CODE	1D	16	4A	2D	30	33	00
ROW 4							
25 KEY	O	]	C	N	.	CAP	A
NM CODE	18	1B	2E	31	34	3A	1E
PQ CODE	18	1B	2E	31	34	3A	1E
ROW 5							
30 KEY	[	S	L-SH	V	M	I	/
NM CODE	1A	1F	2A	2F	32	17	35
PQ CODE	1A	1F	2A	2F	32	17	35
ROW 6							
35 KEY	F2	F5	F8	\	E	TAB	Y
NM CODE	3C	3F	42	2B	12	0F	15
PQ CODE	3C	3F	42	2B	12	0F	15
ROW 7							
40 KEY	F10	F1	SCR	F4	Q	F7	R
NM CODE	44	3B	46	3E	10	41	13
PQ CODE	45	3B	46	3E	10	41	13
ROW 8							
45 KEY	1	3	7	9	-	5	=
NM CODE	02	04	08	0A	0C	06	0D
PQ CODE	02	04	08	0A	0C	06	0D
ROW 9							
50 KEY	4	'	2	6	8	BK-SP	0
NM CODE	05	29	03	07	09	0E	0B
PQ CODE	05	29	03	07	09	0E	0B
ROW 10							
55 KEY	ESC	T	F3	W	F6	PSCR	F9
NM CODE	01	14	3D	11	40	37	43
PQ CODE	01	14	3D	11	40	37	43

TABLE 2
KEYBOARD REPEAT SPEEDS

	PORT BITS	VALUE	DESCRIPTION
	F6E0 4-5	0	Initial repeat time of 625 ms.
5	4-5	1	Initial repeat time of 375 ms.
	4-5	2	Initial repeat time of 281 ms.
	4-5	3	Initial repeat time of 187 ms.
	6-7	0	Subsequent repeat interval of 281 ms.
	6-7	1	Subsequent repeat interval of 187 ms.
10	6-7	2	Subsequent repeat interval of 94 ms.
	6-7	3	Subsequent repeat interval of 47 ms.

The PERIPHERAL ASIC includes a MDA and CGA compatible display controller. It generates all needed signals, as well as refresh data to drive a 640 x 200 pixel LCD (liquid crystal display). The display controller in the PERIPHERAL ASIC may be disabled, allowing for an external controller by writing a one to bit 1 of port F6E1h. The PERIPHERAL ASIC's display controller is enabled upon reset.

20 The PERIPHERAL ASIC's display controller may respond as either an MDA or a CGA video adapter. Writing a 0/1 to port F6E1 will select MDA/CGA compatibility. The display controller is in MDA mode upon reset. Table 3 defines all the display modes supported by the display controller, including exceptions in compatibility, but functionally the controller has two primary modes of operation, graphics mode and text mode.

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TABLE 3
SUPPORTED VIDEO MODES

<u>VID MODE</u>	<u>DISPLAY CHARACTERISTICS</u>	<u>EXCEPTIONS</u>
00	40 x 25 b/w text	
5 01	40 x 25 16-color text	Attributes have fixed color mapping.
02	80 x 25 b/2 text	
10 03	80 x 25 16-color text	Attributes have fixed color mapping.
04	320 x 200 4-color graphics	Treated as mode 06.
05	320 x 200 b/w graphics	
06	640 x 200 b/2 graphics	

15 In CGA graphics mode the screen is mapped into the processor memory space at addresses B8000 - BBFFFh in an interlaced fashion. Each bit in the CGA memory space that is written high (i.e., 1) will appear black in its corresponding location on the screen, while each bit written
20 low (i.e., 0) will appear white. The CGA graphics mode standard calls for interlacing scan rows. Thus, the first row of the screen resides at addresses B8000 - B804Fh, the second row at BA000 - BA04Fh, the third row at B8050 - B809F, and so on.

25 In text mode the screen is broken into character locations, with a two byte address for each location. The CPU writes ASCII codes for the character (even byte) and its corresponding attributes (odd byte), and requires the controller to manage putting the character bit-map on the
30 screen. The display controller in the PERIPHERAL ASIC does this by mapping the screen into unused CPU memory space, BC000 - BFFFF, in a similar non-interlaced fashion to the graphics mode, and then copying each character's bit-map to the appropriate position in this "Bit-map"
35 memory. This approach allows the controller to refresh the screen using 1/4 the memory cycles needed by generating the characters "on the fly". This approach

requires an extra 16 Kbytes of additional memory for display purposes. The process of writing the character bit-maps to bit-map memory may be disabled by a write of a one to bit 3 of port F6E1h. The PERIPHERAL ASIC enables
5 automatic updating of bit-map memory upon reset.

Character bit maps are stored in ROM, along with a translation address, address of the character position in bit-map memory. The memory map of video memory as well as the character ROM is included in Appendix A.

10 Character attributes with bit 7 high (1) indicate that the character should be blinking. The controller recognizes when a blinking attribute is written to normal video memory and initiates a scan, or search, for
characters with blinking attributes. When a character is
15 found, its corresponding location is written in bit-map memory with either the character bit map, if an internal 2 Hz signal is high, or with a blank box if the internal 2 Hz signal is low. This causes a blinking effect to the screen. This scanning is done twice a second for as long
20 as blinking characters remain on the screen. If the controller scans the video memory and does not find a character with a blinking attribute, the controller ceases memory scanning until a new blinking attribute is written. Blinking characters may be disabled by a write
25 to a CGA or MDA compatible register, or by writing a one to bit 2 of port F6E1h. The blinking circuit is enabled at port F6E1h upon reset.

The CGA standard defines four 4 Kbyte pages of video memory in 80 x 25 text mode, and eight 2 Kbyte pages
30 in 40 x 25 text mode. Only one page may be displayed on the screen at a time, however, the displayed page may be changed by a write to a CGA compatible I/O register. The display controller on the PERIPHERAL ASIC preferably does not handle automatic page changes. Instead it
35 accomplishes page changes by generating a nonmaskable interrupt (NMI). The CPU must then rewrite the newly selected memory page causing the bit-map memory to be

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updated. Three bits indicating the current page may be read from port F6E7 bits 2-4. These bits denote the starting address in 2 Kbyte increments from the beginning of video memory.

5 The PERIPHERAL ASIC drives the display with the normal column, row, and frame clock signals. The column clocks are signals used to shift data into the column drivers on the LCD. The column clock outputs are at the same frequency as the display input clock, approximately
10 700 - 900 KHz and alternate activity every 40 clocks. The row clock output is active once every 80 column clocks indicating a change in the row to be refreshed. The frame clock is active once every 201 row clocks indicating the beginning of a new frame. The frame clock is every 201
15 rows, because the controller can support refreshing an extra row of pixels, which may be used a status line, or not used at all. The phase output signals (both polarities) toggle a programmable multiple of row clocks. This is to control problematic parasitic bleeding
20 phenomena on the LCD display. The number of row clocks per phase clock change is changed by writing bits 0-1 of port F6EDh. A contrast signal is also generated by the PERIPHERAL ASIC for use in the LCD. This output is a variable duty-cycle 1 KHz signal. By writing to bits 0-3
25 of port F6E0h, the duty-cycle may be changed from 1/16, corresponding to 0h, up to 15/16, corresponding to both Eh and Fh.

 The PERIPHERAL ASIC includes many features for managing power consumption including the ability to power
30 down and disable parts of the machine and stop clocks. Included is the ability to determine when to disable features. To do this, four special NMI's are generated. The first NMI interrupts the processor when timer
interrupt requests, IRQ0, have occurred. This give the
35 BIOS the capability of timing events even when the normal timer interrupt vector has been stolen. The second NMI is generated on keyboard interrupt requests, IRQ1. These are

used to monitor keyboard input and to allow support for special function keys not supported in the hardware. The third NMI is an interrupt when memory address 00058h has been read. This is an indication that the INT16h software interrupt has been called.

- 5 This is used to determine if the system is idle. Once the software has determined that the machine is idle, it may disable certain computer functions using special I/O ports, thus lowering power consumption. The final and most powerful NMI is the on/off key input. This comes from a key on the keyboard that notifies
- 10 the BIOS that the user wishes to turn the system off.

The processor clock may be disabled with a write to port F6ECh bit 6 with a zero followed by a one. The clock will stop low in the middle of the last I/O write cycle and remain low until an interrupt wakes it. An IRQ0, IRQ1, IRQ4, or NMI may

15 wake the system, if enabled. Each NMI has a mask bit in a special register and the IRQ's have a separate clock mask bit that will mask it from waking the processor, but not mask the interrupt request line from becoming active. The UART clock may be stopped by writing a one to bit 7 of port F6ECh. The charge

20 pump on the RS-232 compatible drivers may be disabled by writing a one to bit 5 of port F6ECh. The LCD display can be turned off by writing a one to bit 3 of port F6ECh. This also stops the display clock, refreshing, contrast and all associated signals. Finally, the power supply voltage may be set to 5 volts with a

25 write of a zero to bit 2 of port F6ECh. This output will go to high impedance with a write of a one to bit 4 of port F6ECh forcing the power supply into automatic mode. In this mode, the power supply voltage will be set based on current consumption.

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The PERIPHERAL ASIC performs various support functions that contribute to the functioning of the system, such as battery alarm, memory card detection, setting configuration dip switches, and the protection of
5 a 32 Kbyte memory space as an internal disk drive.

A NMI is generated when a LOWBAT signal is active. This signal indicates that the system battery is either low or very low depending upon the value in bit 5 of port F6E4h. This NMI is used to notify the user via
10 the status line in the display and shuts the system down.

The PERIPHERAL ASIC supports two memory cards to be used as either disk drives or executable memory. This support includes NMI's that notify software when they are being removed or inserted, or if the internal RAM card
15 battery is low.

The prior art IBM PC/XT contained dip switches that were read to determine the system's configuration. These switches are implemented in the present invention as latches that may be set by software to return the required
20 value. This switch register is located at port F6E2h.

The PERIPHERAL ASIC includes the ability to replace the video character ROM with a 32 K x 8 SRAM. This enables the RAM to contain the bit-maps and translation addresses and still have 24 Kbytes free for an
25 internal disk drive. This memory is not normally present in the CPU memory space, but may be enabled by writing a one to bit 4 of port F6E4h. The memory will appear from A8000 - AFFFFh.

The PERIPHERAL ASIC can multiplex an external
30 clocking source onto ZSYSCLK, the system clock output, and by-pass the VCOI input. This is accomplished by driving the PERCLKN signal low. This capability was implemented to insert an alternate clock source from a peripheral. If a peripheral is supplying power and there is no worry of
35 depleting the internal batteries or of supply voltages sagging, there is no reason not to allow the system to run at a higher speed, e.g., 8 MHz.

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TABLE 4
PIN DESCRIPTION - PERIPHERAL ASIC

<u>SIGNAL</u>	<u>I/O</u>	<u>ACTIVE</u>	<u>DIE PAD</u>	<u>DESCRIPTION</u>
SRESET	I	HIGH	7	System Reset.
5 SYSCLK	I	HIGH	49	System Clock.
STEST	I	HIGH	5	Input to force the chip into test mode.
BUSDRV	I	HIGH	50	Input to enable the bus hold circuitry.
10 AAD[0..7]		B HIGH	20-27	8088 CPU multiplexed Address/Data bus.
AA[8..19]		I HIGH	129-138	8088 CPU High order address bits.
15 S[0..2]	I	HIGH	1,2 28,29,31	8088 CPU status signals.
SREADY	O	HIGH	120	Output indicating the current CPU cycle controlled by the SYSTEM ASIC may conclude.
20 INTR	O	HIGH	117	Output indicating a pending system interrupt.
25 SNMI	O	HIGH	124	Output indicating a pending non-maskable interrupt.
30 LOCKN	I	LOW	6	Input indicating the CPU is executing an uninterruptable machine cycle.
SA[0..19]		O HIGH	91,92,32 93-99,66 100,67,68 101,102 106-109	Latched system address bus.
35 SX[20..22]		O HIGH	110,111	Latched high order address bits for 90 expansion memory devices.
40 RB1P[0..7]		B HIGH	54-57,59	Data bus for memory residing at 60-62 addresses from 00000 - 7FFFFh.
45 EXPP[0..7]		B HIGH	38-45	Data bus for memory residing at addresses from 80000 - FFFFFh and all I/O.
50 RS[0..15]		O LOW	71,72,37	Chip select signals for memory 73-85 residing at

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5	SMEMRN	0	LOW	125	addresses from 00000h(RS0) - 7FFFFh(RS15). Signal that enables memory devices to drive data onto their corresponding data bus.
10	SMEMWN	0	LOW	126	Signal that indicates to memory devices that data is available on their corresponding data bus.
15	SIORN	0	LOW	127	Signal that enables I/O devices to drive data onto the data bus.
20	SIOWN	0	LOW	128	Signal that indicates to I/O devices that data is available on the data bus.
25	SALE	0	HIGH	119	Signal used to latch the CPU address prior to data being placed onto the bus.
30	AEN	0	HIGH	118	Signal indicating that the DMA controller is the current bus master.
35	EMCS[0..3]	0	LOW	63-65	Chip selects for the expansion 30 memory devices that are accessed through the memory mapping circuitry.
40	IRQ[0..7]	I	HIGH	8-10,12	Asynchronous interrupt request 13-15,34 signals to the interrupt controller. They should be held high until acknowledged.
45	DREQ[1..3]	I	LOW	46-48	Asynchronous DMA request signals to the DMA controller. DREQ's should be held until they are acknowledged by the corresponding DACK.
50	DACK[1..3]	0	LOW	113-115	Acknowledge signal from the DMA controller in response to a DMA request and a
55					

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5	TC	O	HIGH	116	successful bus arbitration. Output from the DMA controller indicating the completion of a DMA transfer.
10	PERINTR	I	HIGH	4	An input from the PERIPHERAL ASIC indicating a NMI service request.
15	IOCHRDY	I	HIGH	3	Input from the I/O channel indicating that the I/O or memory device is ready to complete the data transfer.
20	DISEXPP	O	HIGH	112	Output to the I/O channel indicating that the current cycle is for expansion memory devices only.
25	VDD		PWR	16,35,53 89,121	+5 Volts
30	VSS		PWR	17-19,36 51,52,69 70,86-88 103-105 122,123	Ground

BLOCK 18

SYSTEM ASIC chip 18 is the system manager. It comprises four major units, a bus controller, an interrupt controller, a memory manager and a direct memory access (DMA) controller. The bus controller generates input/output and memory control signals. The interrupt controller of SYSTEM ASIC 18 responds to interrupts from the PERIPHERAL ASIC 17, and interrupts from expansion port 23. The direct memory access (DMA) controller in SYSTEM ASIC chip 18 controls access between memory 19 and input/output devices. A schematic of block 18 is shown in Figures 11A to 11Ad.

The SYSTEM ASIC (application specific integrated circuit) is the second chip of a two chip implementation of an IBM PC/XT compatible. A complete PC/XT compatible system may be implemented with this chip, a PERIPHERAL

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ASIC 17 as described above, an Intel 8088 compatible CPU, and memory devices. The SYSTEM ASIC supports 512 Kbytes of static RAM, and up to 8 Mbytes of memory in each of four additional devices.

5 The SYSTEM ASIC chip performs CPU and peripheral support functions including DMA control, interrupt control, bus control, and memory mapping. The SYSTEM ASIC contains Intel 8237, 8259, and 8288, compatible circuits for support of DMA, interrupts, and bus control,
10 respectively, as well as memory mapping circuitry unique to the PQ-XT.

 The SYSTEM ASIC chip supports DMA through the use of an Intel 8237 compatible DMA controller and additional support circuitry. The 8237 supports 4 independent DMA
15 channels, three of which are available on the SYSTEM ASIC. Channel 0, normally used for DRAM refresh in the IBM PC/XT, is preferably not supported. The 8237 registers are redundantly located at ports 0000 - 000Fh and 0010 - 001F, consistent with the IBM PC/XT
20 implementation.

 Four bit page registers provide the upper four bits for each channel to make a 20 bit address for memory accesses. This limits DMA transfers to within a 64 Kbyte page. DMA operations preferably can not occur across page
25 boundaries. The DMA page registers are located at ports 0080 - 0083h, and are redundant in the I/O map up to port 009Fh to be consistent with the IBM PC/XT.

 The SYSTEM ASIC chip supports two types of interrupts, normal system interrupts and NMI's
30 (nonmaskable interrupts). Normal system interrupts are supported by an Intel 8259 compatible circuit. These system interrupts are supported in a hardware compatible manner to the IBM PC/XT, with the 8259 residing at ports 0020 - 0021h and redundantly up to port 003Fh.

35 NMI's may be generated by the assertion of the PERINTR pin coming from the PERIPHERAL ASIC, or from mapping two different physical pages into the same logical

page with the memory mapping circuitry. All NMI's may be disabled using the IBM PC/XT compatible mask register at port 00A0h and redundantly to 00BFh. The memory mapping NMI may be enabled/disabled by writing a one/zero to bit 0 of port F6C4h.

- 5 The NMI's generated by the PERINTR input are meant to be enabled/disabled within the PERIPHERAL ASIC. The memory mapping NMI is disabled upon a hardware reset.

The SYSTEM ASIC generates the memory and I/O control signals with the use of an Intel 8288 compatible circuit. This
10 circuit decodes the processor status lines and generates the bus control signals ALE, MEMWRN, MEMRDN, IOWRN, and IORDN.

Also included in the SYSTEM ASIC is a 2-bit register that controls the automatic insertion of wait states. The binary value of bits 0-1 written to port F6C3h causes the insertion of
15 the corresponding number of wait states. Upon reset, no extra wait states are inserted. However, a single wait state is inserted on all I/O operations to remain consistent with the IBM PC/XT.

The SYSTEM ASIC interfaces to two external data buses,
20 the EXPP[0..7] which is intended for use as an external I/O and expanded memory bus, and the RB1P[0..7], which is intended to interface to main memory. There are times when either or both of these data buses will not be actively driven. Because the computer is preferably wholly a CMOS system, excessive power may
25 be consumed by allowing inputs to float. Therefore, logic is included to drive these buses to a low when ordinarily they would float. The signal BUSDRV when high (1) enables this circuitry.

The SYSTEM ASIC supports up to 512 Kbytes of 32K x 8 SRAM's at addresses 00000 - 7FFFFh, and 8 Mbytes of memory in
30 each of four additional devices. The SYSTEM

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ASIC supplies 16 chip select signals, RS0 - RS15, for use with 32K x 8 SRAM's. RS0 selects the lowest 32 Kbytes, followed by RS1 and the other chip select signals.

The SYSTEM ASIC also supports mapping 64 Kbyte pages from any of four devices into the any of the four 64 Kbyte pages at addresses C0000 - CFFFFh, D0000 - DFFFFh, E0000 - EFFFFh, F0000 - FFFFFh. The paging for each memory segment is accomplished with the use of two registers. The first is a four bit register used to select which of the four possible devices is to be mapped into the corresponding segment. Table 1 defines the function of each bit in the device mapping registers. The second is a seven bit register used to select which 64 Kbyte page within the selected device is to be mapped into the corresponding segment. This second register contains the top seven bits of a 23 bit address used when accessing the selected device. Thus each device may contain up to 8 Mbytes of memory. Table 2 defines the function and port address of the device page registers.

The memory mapping circuit also generates a signal, DISEXPP, that is asserted on any bus cycle where memory mapping occurs. This signal is to be used to disable peripherals that respond to memory in the C0000 - FFFFFh memory space when a mapping operation is occurring. This signal is also asserted when bit 4 is set in the register at port F6E4h and an access to a memory location from A8000 - AFFFFh is in process. This is to disable peripherals that respond to A8000 - AFFFFh when accessing the protected memory supported by the PERIPHERAL ASIC.

TABLE 5

<u>Port Address</u>	<u>Bit</u>	<u>Value</u>	<u>Description</u>
F6C0	0	1	Map device connected to EMCS0 to C0000
5	1	1	Map device connected to EMCS1 to C0000
00h at Reset	2	1	Map device connected to EMCS2 to C0000
10	3	1	Map device connected to EMCS3 to C0000
	4	1	Map device connected to EMCS0 to D0000
	5	1	Map device connected to EMCS1 to D0000
15	6	1	Map device connected to EMCS2 to D0000
	7	1	Map device connected to EMCS3 to D0000
F6C5	0	1	Map device connected to EMCS0 to E0000
20	1	1	Map device connected to EMCS1 to E0000
80h at Reset	2	1	Map device connected to EMCS2 to E0000
25	3	1	Map device connected to EMCS3 to E0000
	4	1	Map device connected to EMCS0 to F0000
	5	1	Map device connected to EMCS1 to F0000
30	6	1	Map device connected to EMCS2 to F0000
	7	1	Map device connected to EMCS3 to F0000

TABLE 6

<u>Port Address</u>	<u>Bit</u>	<u>Value</u>	<u>Description</u>
F6C1	0-6	0-7Fh	Device page to be mapped to C000000h at Reset
40 F6C2	0-6	0-7Fh	Device page to be mapped to D000000h at Reset
F6C6	0-6	0-7Fh	Device page to be mapped to E000000h at Reset
F6C7	0-6	0-7Fh	Device page to be mapped to 0000FFh at Reset

45 SRESET

The signal line is used to reset circuits within the System ASIC 18, and the processor 16. A signal on

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this line is generated within the Peripheral ASIC 17 (where it is also used) and is a logical inversion of the signal on line MRESETN.

PERINTR

5 Generated from the Peripheral Interrupt Control circuits within the Peripheral ASIC 17, the signal on this line is used to alert programs running on the processor 16 of various hardware and software conditions. The signal connects to the System ASIC 18 where, if enabled within
10 system ASIC 18, it can reach the processor 16 on the SNMI signal.

EXPP[0..7]

This is the bidirectional data bus line between the Peripheral ASIC 17, the expansion port 23 and the
15 System ASIC 18. The System ASIC 18 is the gateway for all data to and from the processor 16.

IRQ[0..1,4]

Interrupt request signals on line IRQ0, IRQ1, and IRQ4 are all generated within the Peripheral ASIC 17 and
20 corresponding to timer tick interrupt, keyboard interrupt, and UART interrupt, respectively. The signals on these lines are connected to the pins IR0, IR1, and IR4 respectively of the 8259 compatible Programmable Interrupt Controller cell located within the System ASIC 18.

25 SREADY

This line is used by the System ASIC 18 to synchronize slow data transfer with the processor 16. This line may reflect the condition of circuits within the System ASIC 18 itself, or the condition of the signal
30 IOCHRDY from the Expansion Port 23. The signal on this line is routed through the Peripheral ASIC 17 before reaching the processor 16 on signal line CPURDY.

SALE

This is the address latch enable signal line from
35 the 8288 Bus Controller compatible cell within the System ASIC 18. The signal on this line is used internally by circuits within the System ASIC 18, those located within

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the Peripheral ASIC 17, and peripherals connected to the Expansion Port 23. This signal is used to strobe the address into the address latches and indicates that AAD[0..7] and AA[8..19] contain a valid address.

5 AEN

The Address Enable signal line from the 8237 compatible Programmable DMA controller cell within the System ASIC 18. When the signal on this line is high, it indicates that a DMA cycle is taking place. It is used internally by circuits within the System ASIC 18, those located within the Peripheral ASIC 17, and peripherals connected to the Expansion Port 23.

SIORN

An I/O read strobe signal is generated on this line by the 8288 Bus Controller compatible cell within the System ASIC 18. It is used internally by circuits within the System ASIC 18, those located with the Peripheral ASIC 17, and peripherals connected to the Expansion Port 23. When this line is low, it indicates that the processor 16 is requesting data from an I/O device.

SIOWN

An I/O write strobe signal on this line generated by the 8288 Bus Controller compatible cell within the System ASIC 18. It is used internally by circuits within the System ASIC 18, those located with the Peripheral ASIC 17, and peripherals connected to the Expansion Port 23. When this line is low, it indicates that the processor 16 is writing data to an I/O device.

SMEMRN

30 A memory read strobe signal on this line is generated by both the 8237 Programmable DMA Controller and the 8288 Bus Controller compatible cells within the System ASIC 18. When this line is low, it indicates a data Read Request from a memory device. It is used by circuits within the Peripheral ASIC 17, 512k System RAM 19, Memory Cards 22a and 22b, BIOS ROM 20, APPS ROM 21, and peripherals connected to the Expansion Port 23.

SMEMWN

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A memory write strobe signal is generated on this line by both the 8237 Programmable DMA Controller and the 8288 Bus Controller compatible cells within the System ASIC 18. It is used by circuits within the Peripheral ASIC 17, 512k System RAM 19, Memory Cards 22a and 22b, and peripherals connected to the Expansion Port 23. When this line is low, it indicates that data is to be written to a memory device.

10 RSPWRN

This line carries a signal from the Peripheral ASIC 17 used to enable the power supply within the RS232/TTL Level Shifter 24. This signal is controlled by a bit within the Peripheral ASIC 17 which can be manipulated by the processor 16. When it is high, the power supply circuits are enabled.

TTL OUT

These signal lines are SOUT, RTSN, and DTRN. The signals on these lines are generated by the 16450 compatible UART within the Peripheral ASIC 17 and connect to TTL level inputs on the level shifter circuits in 24. The function of these signals is discussed in the data sheet for the 16450 UART available from National Semiconductor.

25 TTL IN

These signal lines are SIN, CTSN, DSRN, and DCDN. The signals on these lines are translated from RS232 levels to TTL by the level shifter in 24 and presented to input pins of the 16450 compatible UART within the Peripheral ASIC 17. The function of these signals is discussed in the data sheet for the 16450 UART available from National Semiconductor.

IOCHKN

The I/O channel line checks the signal from the Expansion Port 23 which is used to indicate a problem with a peripheral. This signal is monitored by the Peripheral ASIC 17 and may interact with software running on the

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processor 16.

PERCLKN

This line indicates to the Peripheral ASIC 17 which source is to be used as the system clock, SYSCLK.

5 When low, the VCO oscillator is used. When high, EXTSYSCLK is used. This signal is provided by the Expansion Port 23.

EXTSYSCLK

This line carries the external input clock signal
10 which may be used to derive the system clock SYSCLK if selected using signal PERCLKN from the Expansion Port 23. This signal is an input to the Peripheral ASIC 17.

CARD DETECTS

These lines carry four card detect signals from
15 the Memory Cards 22a and 22b which are provided to the Peripheral ASIC 17. For each of the two cards, a signal is provided to detect the card outside the card connector, and another signal to indicate if the card is fully inserted into the connector.

20 CARD ALARMS

These lines carry two card battery alarms provided from the Memory Cards 22a and 22b to the Peripheral ASIC 17. The alarms indicate if the internal battery used in RAM memory cards needs replacing.

25 BLOCK 24

RS232/TTL LEVEL SHIFTER. Digital circuits used in the present invention operate at switching voltage thresholds conventionally known as TTL. The RS232 standard which is used in serial communications includes
30 switching voltages incompatible with the digital circuits used elsewhere in the invention. To convert between the TTL signals of the UART located within the Peripheral ASIC 17 (see TTL OUT, TTL IN) to RS232 signals made available on the Expansion Port 23, a level shifter is used. In
35 the present invention, this is accomplished by a MAX241 device available from MAXIM.

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BLOCK 19512k SYSTEM RAM.

The main processor system RAM arranged as 512k x 8 bits using sixteen conventional 32k x 8 chips.

5 BLOCK 20

BIOS ROM. A ROM (read only memory) used to hold software which is nonvolatile and shipped with the computer. This ROM may contain BIOS control code, application programs, operating system files, and miscellaneous other data.

BLOCK 21

APPS ROM. A ROM is used to hold software which is nonvolatile and shipped with the computer. This ROM may contain BIOS control code, application programs, operating system files, and miscellaneous other data.

BLOCK 22

This block includes blocks 22a and 22b, which are two identical removable memory cards which are accessible to the processor 16 when inserted into the computer.

20 SYSTEM SERIAL NUMBER

A space is provided within BIOS ROM 20 (or alternatively in other ROM in the computer) for a system serial number unique to each individual computer. This serial number is programmed into the read only memory at the time of manufacture and cannot be changed by the user. Access to the serial number is provided by means which are known to the user only by means of information provided by the manufacturer as described below.

This serial number is useful for data entry and tracking at a repair center, for providing an additional level of security for the computer user for entry into an external secure local or remote network, for deterring theft and for allowing software vendors to serialize applications programs for individual computers. The serial number is used by matching it with an external list of serial numbers.

Preferably the serial number is 32 bytes and

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includes an eight byte serial ID number, and attributes such as a two byte country of manufacture, a two byte native country code, a one byte ROM size (expressed in megabits), and a four byte configuration code for ROM contents, plus 14 reserved bytes and a one byte checksum. In one embodiment, the serial number is encrypted.

Software access to the serial number is provided by SAI function 30h, Service 1, accessed by means of software interrupt 66. This returns:

10 DX:AX pointing to ASCIIIZ
 (zero terminated) unencrypted string.
 Thus, for example, access by software is attained
 by:
 Setting up the processor register for the SAI
15 call involving software interrupt 66h.
 Looking at the ASCIIIZ string returned, pointed to
 by address DX:AX.

Alternatively, access to the serial number is attained by examining the contents of physical address
20 such as E0040h on the 128 Kbyte system ROM. This page is not mapped into the address space at start-up, and so must be explicitly mapped in to gain access. Thus physical access in this example is attained by:

 Setting up the processor registers.
25 Writing to the ASIC I/O port to map in the
 E segment of system ROM.
 Looking at address E0040h, (i.e., E004:0000).

BLOCK 23

EXPANSION PORT. This circuitry is used to
30 interface between the computer and external peripheral devices. This port preferably contains all signal lines necessary to be compatible with the IBM PC XT expansion bus. Beyond the standard definition of what is included in such a compatible bus, this bus allows a peripheral to
35 provide both the system power and system clock. Included in this connector are also the RS232 signals which usually require a separate connector.

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INDICATOR GRAPHICS

As shown in Figure 9, indicator graphics 130 include legends 500, 502, etc. imprinted along the margin of the display 112. These legends such as 500, 502, are used in conjunction with an adjacent status line (not shown) located on the display 112 for indicating to the user the status of software programs and hardware conditions such as a low battery, caps lock, scroll lock, shift lock, or similar data. Preferably an audio sound, such as from a piezoelectric transducer (not shown), is also used to direct the user's attention to the display indicators.

KEYBOARD GRAPHICS

The computer also includes a second set of symbols such as 516, 518, 520, 524 as shown in Figure 9 imprinted on a margin of the keyboard 118a. These symbols such as 516, 518, 520, 524 describe the functions of an adjacent row of keyboard function keys (not shown). In one embodiment, four symbols in four different colors are provided adjacent each function key. Keys for "shift", "alt", "ctrl", and a special logo key (not shown) are correspondingly colored to indicate that simultaneously pressing the "shift", "alt", "ctrl", or the special logo key with the adjacent function key produces the functions noted in color by the symbol 502, 504, etc., adjacent to the function key.

The above description of the invention is illustrative and not limiting; further embodiments will be apparent in light of the invention.

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APPENDIX A

The following is a definition of the I/O map L. Table 1 show the ports included that are compatible with the IBM PC/XT, while Tables 2 and 3 show the . specific I/O for the *SYSTEM* ASIC and *PERIPHERAL* ASIC respectively.

TABLE 1
IBM PC/XT COMPATIBLE I/O

<u>I/O Address</u>	<u>Usage</u>
0000-001F	DMA Controller internal registers
0020-003F	Interrupt Controller internal registers
0060-0063	PPI Internal I/O
0080-009F	DMA Page Registers
00A0-00BF	NMI Mask Register
03B0-03BB	Monochrome Display Adapter registers
03D0-03DF	Color Graphics Adapter registers
03F8-03FF	Primary Asynchronous Adapter registers

TABLE 2
SYSTEM ASIC . . . SPECIFIC I/O

<u>Port Address</u>	<u>Bit</u>	<u>Value</u>	<u>Description</u>
F6C0	0	1	Map device connected to EMCS0 to C0000 – CFFFFh
00h at Reset	1	1	Map device connected to EMCS1 to C0000 – CFFFFh
	2	1	Map device connected to EMCS2 to C0000 – CFFFFh
	3	1	Map device connected to EMCS3 to C0000 – CFFFFh
	4	1	Map device connected to EMCS0 to D0000 – DFFFFh
	5	1	Map device connected to EMCS1 to D0000 – DFFFFh
	6	1	Map device connected to EMCS2 to D0000 – DFFFFh
	7	1	Map device connected to EMCS3 to D0000 – DFFFFh
F6C1	0-6	0-7Fh	Device page to be mapped to C0000 – CFFFFh
00h at Reset			
F6C2	0-6	0-7Fh	Device page to be mapped to D0000 – DFFFFh
00h at Reset			
F6C3	0-1	0h	Select 0 wait states for memory cycles
00h at Reset		1h	Select 1 wait state for memory cycles
		2h	Select 2 wait state for memory cycles
		3h	Select 3 wait state for memory cycles

F6C4	0	1	- 46 -
00h at Reset	1-7		Enable Error NMI Reserved
F6C5	0	1	Map device connected to EMCS0 to E0000 - EFFFFh
80h at Reset	1	1	Map device connected to EMCS1 to E0000 - EFFFFh
	2	1	Map device connected to EMCS2 to E0000 - EFFFFh
	3	1	Map device connected to EMCS3 to E0000 - EFFFFh
	4	1	Map device connected to EMCS0 to E0000 - FFFFFh
	5	1	Map device connected to EMCS1 to E0000 - FFFFFh
	6	1	Map device connected to EMCS2 to E0000 - FFFFFh
	7	1	Map device connected to EMCS3 to E0000 - FFFFFh
F6C6	0-6	0-7Fh	Device page to be mapped to E0000 - EFFFFh
00h at Reset			
F6C7	0-6	0-7Fh	Device page to be mapped to F0000 - FFFFFh
FFh at Reset			
F6E4	0-3		Reserved for <i>PERIPHERAL</i> ASIC
00h at Reset	4	1	Assert DISEXPP on accesses to A8000 -
AFFFFh	5-7		Reserved for <i>PERIPHERAL</i> ASIC

PERIPHERAL ASIC TABLE 3 . . . SPECIFIC I/O

<u>Port Address</u>	<u>Bit</u>	<u>Value</u>	<u>Description</u>
F6E0	0-3	0-Fh	Duty cycle of the contrast signal. 0h corresponds to 1/16 duty cycle, 1h corresponds to 2/16 duty cycle,... Eh corresponds to 15/16 duty cycle, Fh corresponds to 15/16 duty cycle.
R/W	4-5	0-3h	Initial keyboard repeat delay
00h at Reset	6-7	0-3h	Subsequent keyboard repeat delay
F6E1	0	0	MDA compatible display
R/W		1	CGA compatible display
00h at Reset	1	1	Disable the internal display
	2	1	Disable the character blinking feature
	3	1	Disable the automatic updating of bit-map memory by the display controller
	4	1	Disable the UART from the I/O bus
	5	1	Masks IRQ0's from waking the system clock
	6	1	Masks IRQ1's from waking the system clock
	7	1	Masks IRQ4's from waking the system clock

F6E2
V only
00h at Reset

0-3 0-Fh
4-7 0-Fh

PC/XT compatible dip switches 5-8.
PC/XT compatible dip switches 1-4.

F6E3
R only

0 1
1 1
2 0
3 0
4 0

5 0
6 0
7 1

EXTRA input signal is active (high).
LOWBAT input signal is active (high).
PQKEYN input signal is active (low).
ONOFFN input signal is active (low).
PERCLKN input signal is active (low).
EXTSYSCLK is in use.
CALMAN input is active (low).
CALMBN input is active (low).
Display controller is in a state to which
the system clock may be stopped.

F6E4
R/W
0Xh at Reset

0 0
1 0
2 0
3 0
4 1

5 0
6 1
7 1

CDET1AN input is active (low).
CDET2AN input is active (low).
CDET1BN input is active (low).
CDET2BN input is active (low).
Enable access to font ROM/RAM
at A8000 - AFFFFh.
LOWBAT signal indicates a dead battery
LOWBAT signal indicates a low battery
Clear 54.9 ms increment counter.
INT16h has been called since the last time
NMI's were cleared.

F6E5
R only

0-7 0-FFh

Least significant byte of the 54.9 ms
increment counter.

F6E6
R only

0-1 0-3h
2-7

Most significant bits of the 54.9 ms
increment counter
Reserved

F6E7
R only

0-1 0h
1h
2-3h
2 1

3-5 0h
1h
2h
3h
4h
5h
6h
7h

6 1

Select 40 x 25 text mode (CGA only)
Select 80 x 25 text mode
Select graphics mode (CGA only)
Enable the display controller to refresh
the LCD.
Display B8000-B8FFFh (CGA 80 x 25 text only).
Display B8000-B87FFh (CGA 40 x 25 text only).
Display B8000-B8FFFh (CGA 80 x 25 text only).
Display B87FF-B8FFFh (CGA 40 x 25 text only).
Display B9000-B9FFFh (CGA 80 x 25 text only).
Display B97FF-B9FFFh (CGA 40 x 25 text only).
Display B9000-B9FFFh (CGA 80 x 25 text only).
Display B97FF-B9FFFh (CGA 40 x 25 text only).
Display BA000-BAFFFh (CGA 80 x 25 text only).
Display BA7FF-BAFFFh (CGA 40 x 25 text only).
Display BA000-BAFFFh (CGA 80 x 25 text only).
Display BA7FF-BAFFFh (CGA 40 x 25 text only).
Display BB000-BBFFFh (CGA 80 x 25 text only).
Display BB7FF-BBFFFh (CGA 40 x 25 text only).
Display BB000-BBFFFh (CGA 80 x 25 text only).
Display BB7FF-BBFFFh (CGA 40 x 25 text only).

IRQ0 timer interrupt has occurred since the

	7	1	last time NMI's were cleared. IRQ1 keyboard interrupt has occurred since the last time NMI's were cleared.
F6E8	0	1	Enable the EXTRA signal to generate an NMI.
R/W	1	1	Enable the LOWBAT signal to generate an NMI.
00h at Reset	2	1	Enable any of the card detect signals to generate an NMI if they are individually enabled.
	3	1	Enable the video controller to generate an NMI when video display pages are changed.
	4	1	Enable the PQKEYN signal to generate an NMI.
	5	1	Enable the ONOFFN signal to generate an NMI.
	6	1	Enable the IOCHKN signal to generate an NMI.
	7	1	Enable both CALMAN and CALMBN to generate an NMI.
F6E9	0	1	Enable the CDET1AN signal to generate an NMI.
R/W	1	1	Enable the CDET2AN signal to generate an NMI.
00h at Reset	2	1	Enable the CDET1BN signal to generate an NMI.
	3	1	Enable the CDET2BN signal to generate an NMI.
	4	1	Enable an IRQ0 request to generate an NMI.
	5	1	Enable an IRQ1 request to generate an NMI.
	6	1	Enable NMI's for reading 00058h (INT16h).
	7	0	Clear all NMI's and indicator latches.
F6EA	0	1	Signal ONOFFN has been active since the last time NMI's were cleared.
R only	1	1	Signal PQKEYN has been active since the last time NMI's were cleared.
	2	1	The display page register has been written since the last time NMI's were cleared.
	3	1	The PERIPHERAL ASIC generated an NMI.
	4	1	One of either CALMAN or CALMBN signal has been active since the last time NMI's were cleared.
	5	1	Signal LOWBAT has been active since the last time NMI's were cleared.
	6	1	Signal EXTRA has been active since the last time NMI's were cleared.
	7	1	Signal IOCHKN has been active since the last time NMI's were cleared.
F6EB	0	1	Signal CDET1AN has made a 0-1 transition since the last time NMI's were cleared.
R only	1	1	Card a extended pin out-going NMI. Signal CDET1AN has made a 1-0 transition since the last time NMI's were cleared.
	2	1	Card a extended pin in-coming NMI. Signal CDET2AN has made a 0-1 transition since the last time NMI's were cleared.
	3	1	Card a micro switch out-going NMI. Signal CDET2AN has made a 1-0 transition since the last time NMI's were cleared.
	4	1	Card a micro switch in-coming NMI. Signal CDET1BN has made a 0-1 transition since the last time NMI's were cleared.

	5	1	Card a extended pin out-going NMI. Signal CDET1BN has made a 1-0 transition since the last time NMI's were cleared.
	6	1	Card a extended pin in-coming NMI. Signal CDET2BN has made a 0-1 transition since the last time NMI's were cleared.
	7	1	Card a micro switch out-going NMI. Signal CDET2BN has made a 1-0 transition since the last time NMI's were cleared. Card a micro switch in-coming NMI.
F6EC R/W 00h at Reset	0	0	Timer generates IRQ0's every 54.9 ms.
		1	Timer generates IRQ0's every 56.2 s.
	1	0	Reserved always 0.
	2	0	SELVDD output low (5 Volts) if F6ECh bit 4 is low.
		1	SELVDD output high (3 Volts) if F6ECh bit 4 is low.
	3	0	LCDPWRN signal low (display power and clocks active).
		1	LCDPWRN signal high (display power and clocks disabled).
	4	0	SELVDD signal follows the polarity of F6ECh bit 2.
		1	SELVDD signal is disabled to high impedance.
	5	0	RWPWRN signal is low (RS-232 driver's charge pump is enabled).
		1	RSPWRN signal is high (RS-232 driver's charge pump is disabled).
	6	1	Stop the processor clock. Must have previously been low.
	7	1	Sets BAUDCLKG signal low (disables the 1.8432 MHz crystal circuit).
F6ED	0-1	0h	PHCLK/PHCLKN will change every 1 ROWCLK's.
		1h	PHCLK/PHCLKN will change every 2 ROWCLK's.
		2h	PHCLK/PHCLKN will change every 4 ROWCLK's.
		3h	PHCLK/PHCLKN will change every 8 ROWCLK's.
	2	1	Value will be read from 0062h bit 4.
	3	1	Value will be read from 0062h bit 6.
	4	1	Value will be read from 0062h bit 7.
	5-7		Reserved.

CLAIMS:

1. A compact portable computer including a keyboard, the keyboard comprising:

5 a keyplate having a plurality of keys and a printed circuit board underlying and held in a spaced relation to said keyplate, said printed circuit board having two surfaces, a first surface bearing conductive traces for detecting key presses of the keys of the keyplate, and an opposing second surface having most of
10 the integrated circuit components of the computer mounted thereon, thereby providing a compact portable computer keyboard.

2. A compact portable computer according to claim 1, wherein the keyboard further comprises:

15 a membrane underlying and held in fixed relation to the keyplate and having formed on one surface thereof a plurality of cones, one beneath each key, each cone having a flat upper surface for contact by the overlying key, and each cone including an elastomeric conductive body inside the cone, the printed
20 circuit board underlying the membrane, and at least one pair of conductive traces underlying each conductive body.

3. A compact portable computer according to claim 1, wherein the integrated circuit components are wire bonded to the
25 printed circuit board.

4. A compact portable computer according to claim 1, wherein an additional pair of conductive traces are provided for resetting the computer, said additional pair of conductive traces
30 being shorted together by a conductor which is moveable into place against the pair of conductive traces by an object inserted

through an opening in the keyplate, the opening exposing the conductor.

5. A compact portable computer according to claim 1,
5 wherein said keyboard has at least seventy-seven keys.

6. A compact portable computer according to claim 1,
further comprising a case for holding the keyboard, said printed
circuit board being held between said case and said keyboard and
10 the keyboard being joined to the case by a weld.

7. A compact portable computer according to claim 1,
wherein the integrated circuit components are unpackaged.

15 8. A compact portable computer according to claim 1,
wherein the computer comprises a processor for executing an
operating system and associated application programs in
accordance with a clock signal; and

wherein said conductive traces include a pair of on/off
20 traces for causing said computer to toggle between an on state
and an off state, said pair of on/off traces being connected upon
pressing of an on/off key which moves a conductor against said
pair of on/off traces;

said off state being a state in which said processor
25 retains its place in a currently executing applications program
and said clock signal is supplied to said processor at a low
frequency.

9. A compact portable computer according to any one of
30 claims 1 to 7, further comprising a display of a size
substantially similar to the size of the keyboard.

10. A compact portable computer according to claim 9, further comprising a hinged lid for the keyboard, the display being provided on an inside surface of the lid.

- 5 11. A computer system comprising;
a main processor integrated circuit of the computer system;
a full function alphanumeric keyboard for inputting data into said main processor;
10 a display device for outputting data from said main processor; and
a printed circuit board, one side of said printed circuit board having said main processor integrated circuit mounted thereon and the other side of said printed circuit board
15 bearing conductive traces for detecting key presses of said keyboard.

12. A computer system according to claim 11, wherein the display device is of a size substantially similar to the size of
20 the keyboard.

13. A computer system according to claim 11 or 12, further comprising a hinged lid for the keyboard, the display device being provided on an inside surface of the lid.

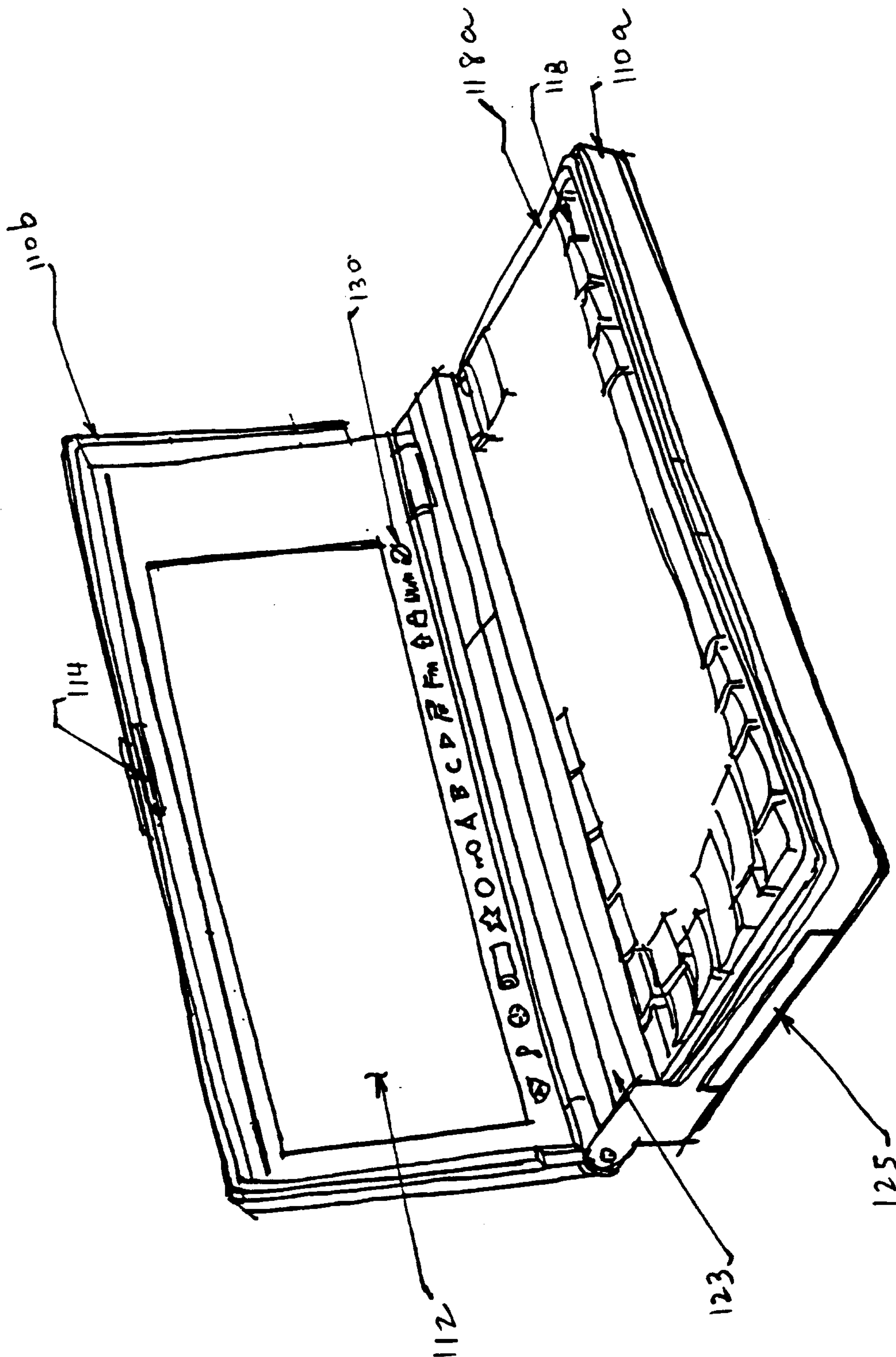


Figure 7

2

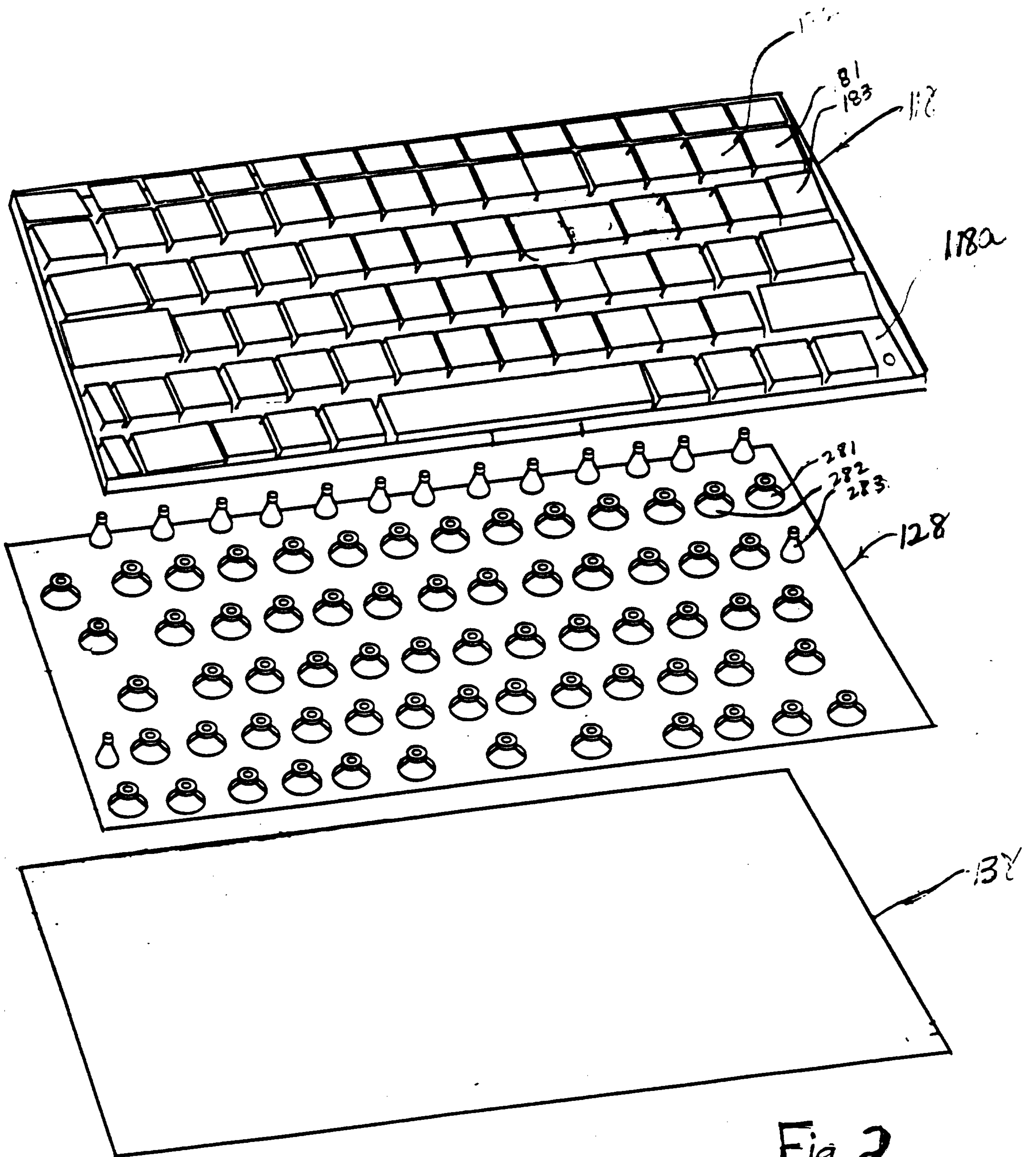
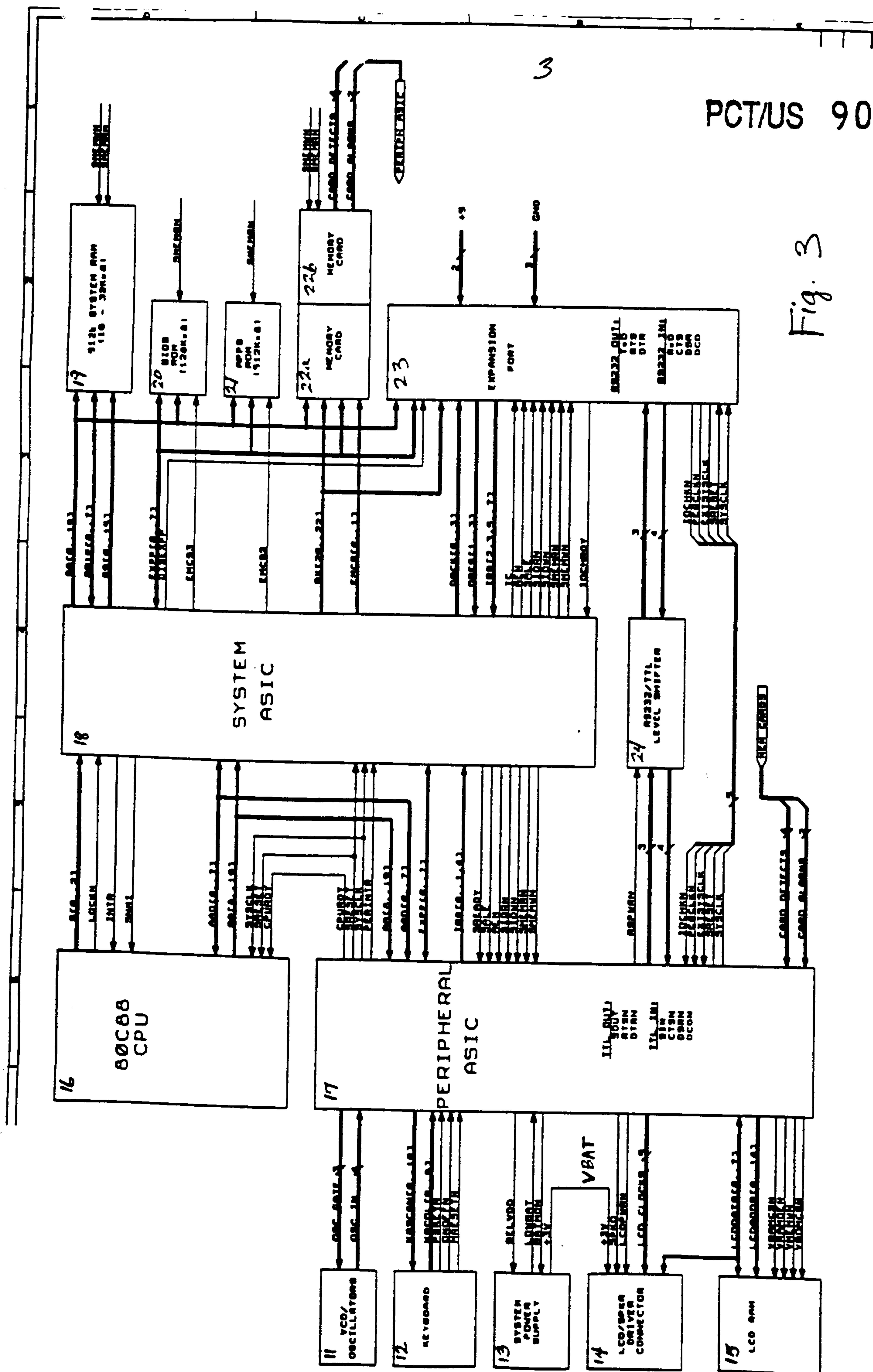


Fig. 2

PCT/US 90/03639

Fig. 3



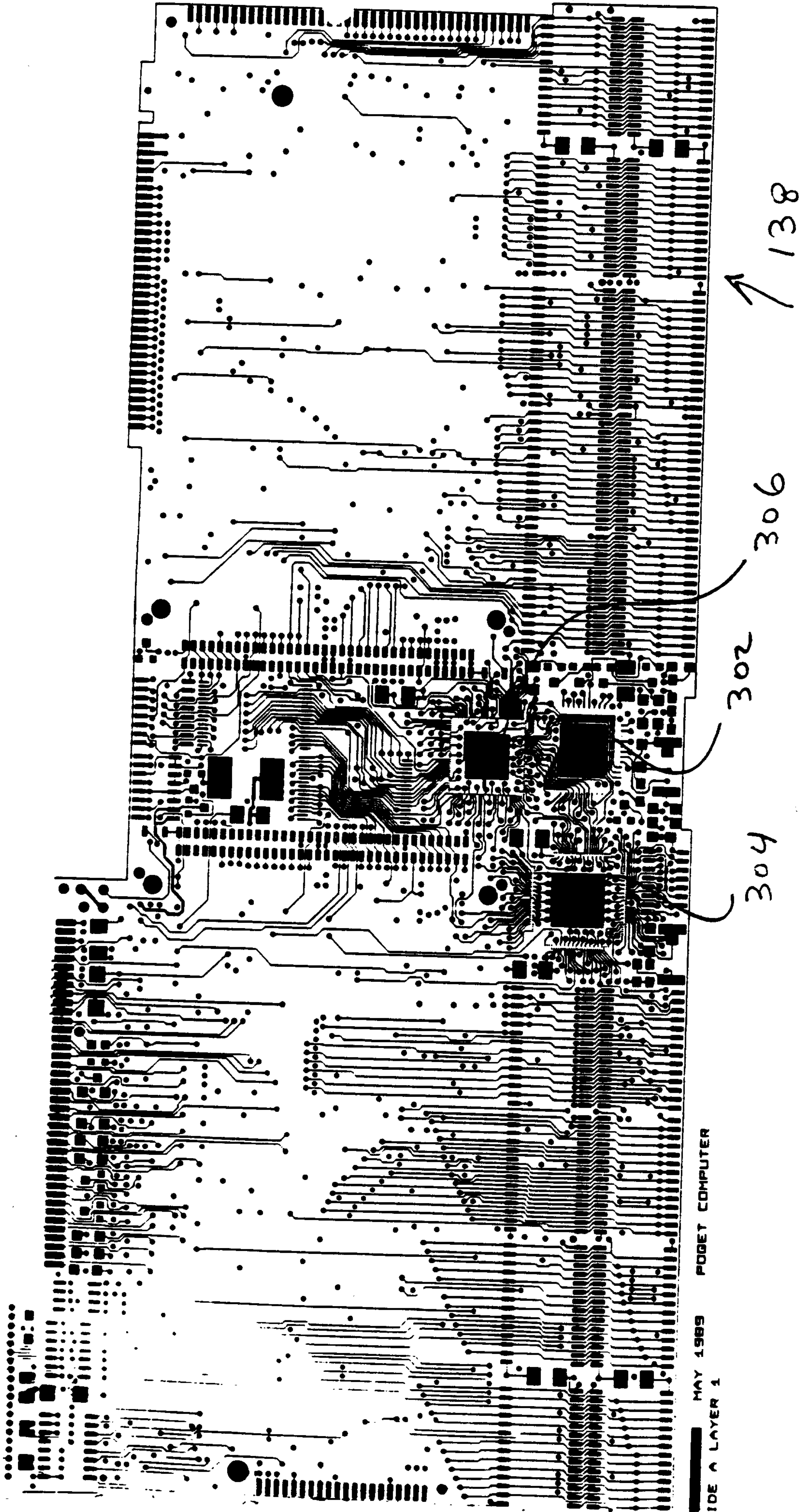


Figure 4

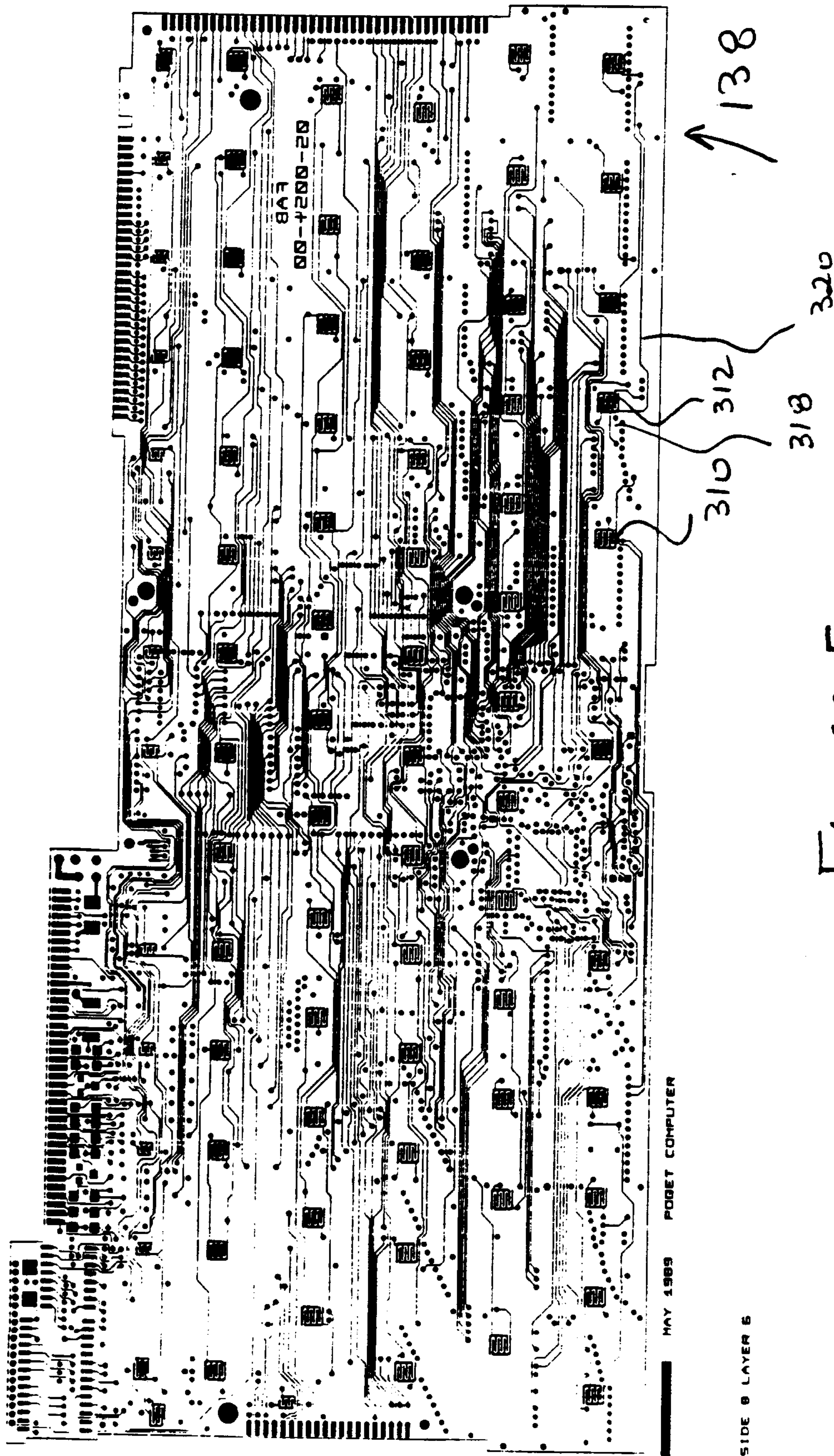
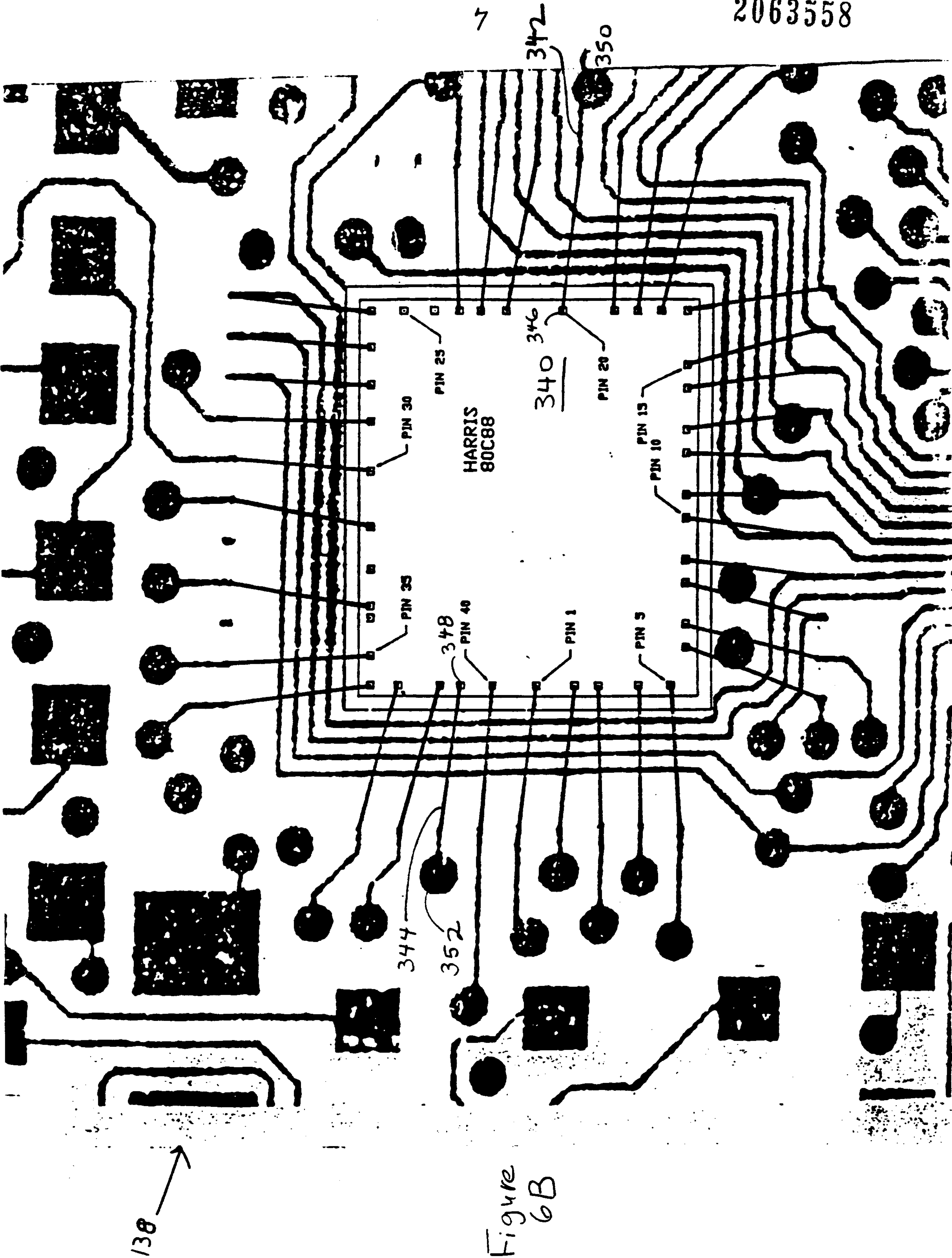
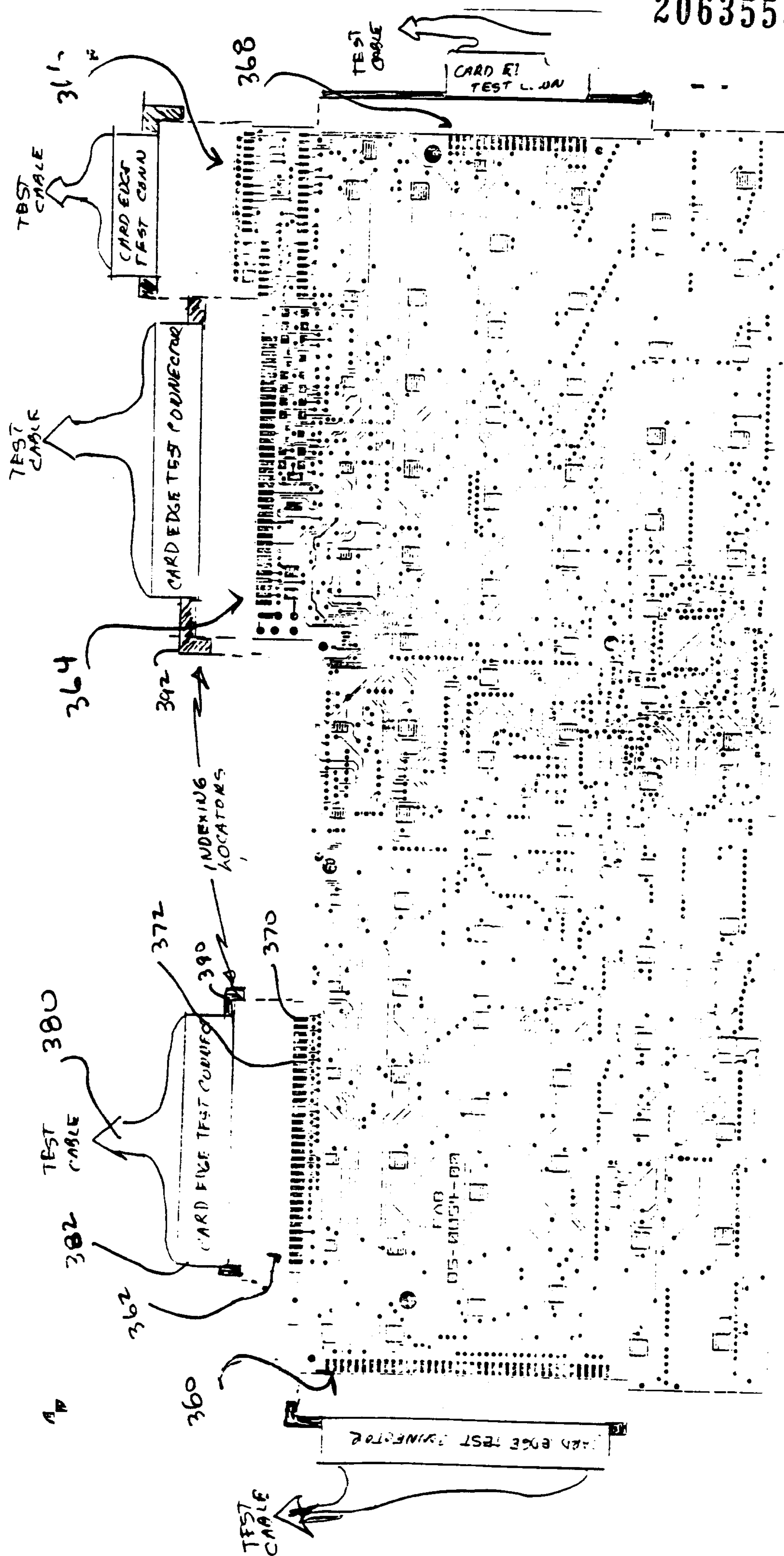


Figure 5



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8



8

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Figure 7

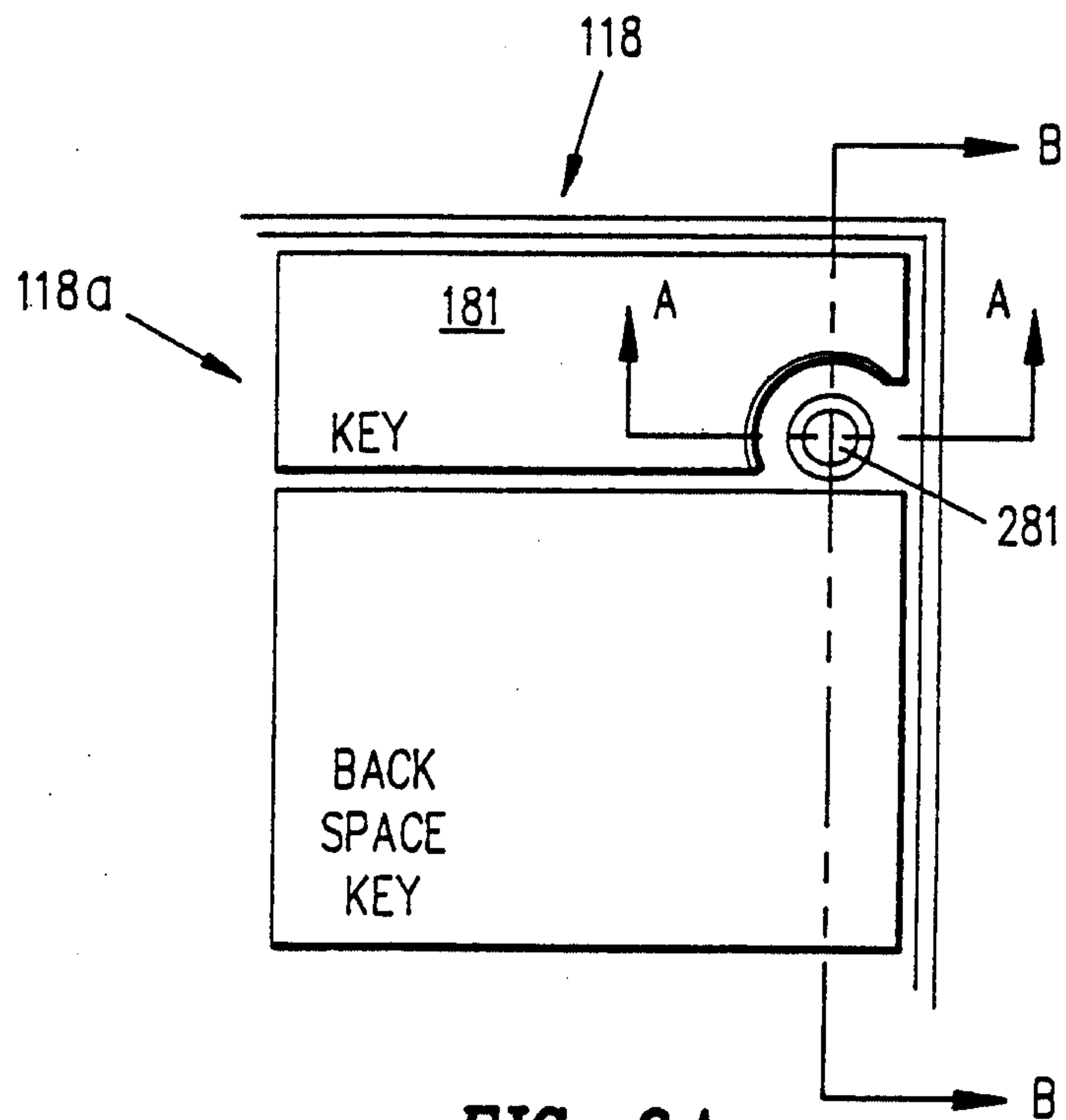


FIG. 8A

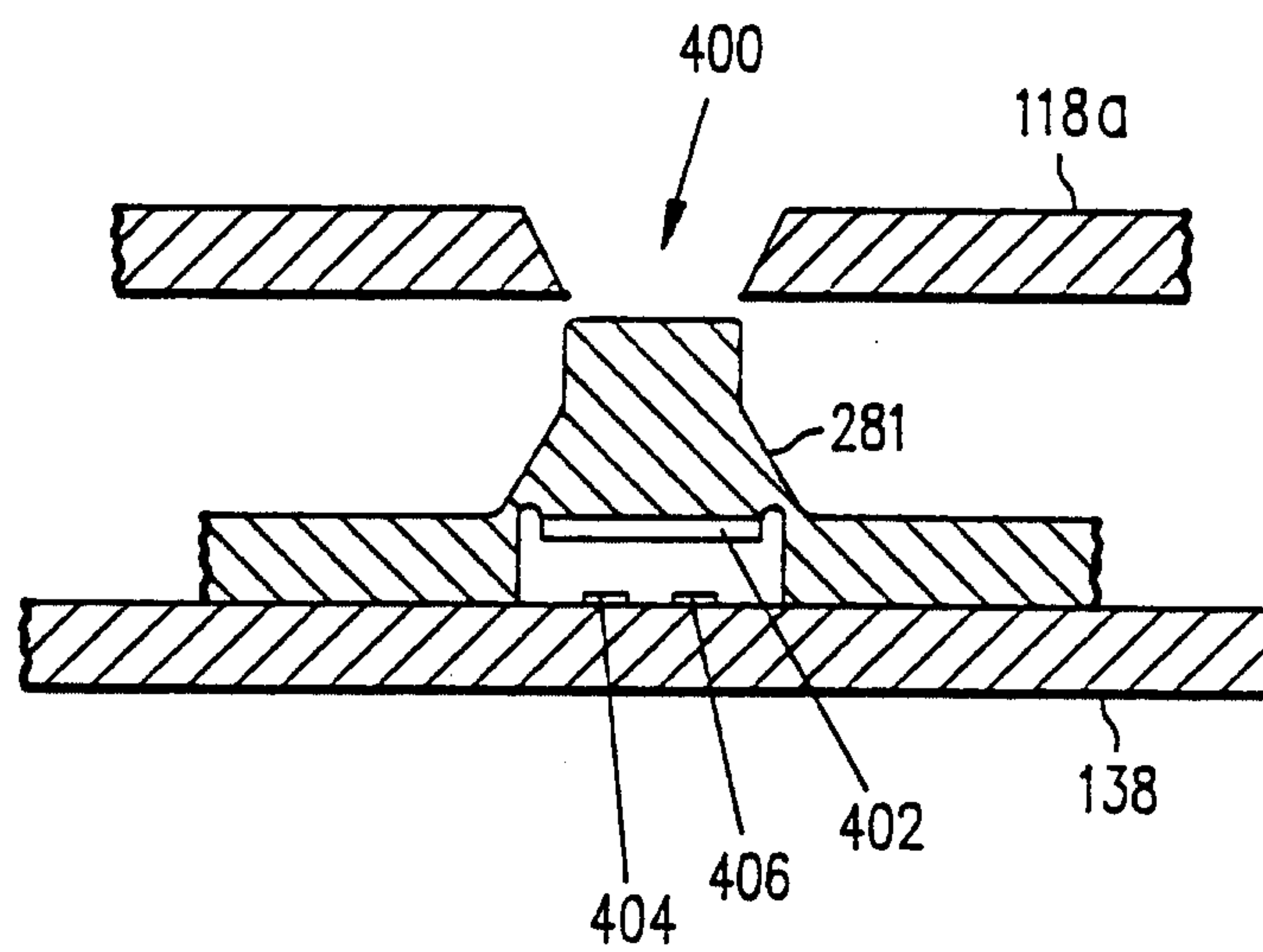
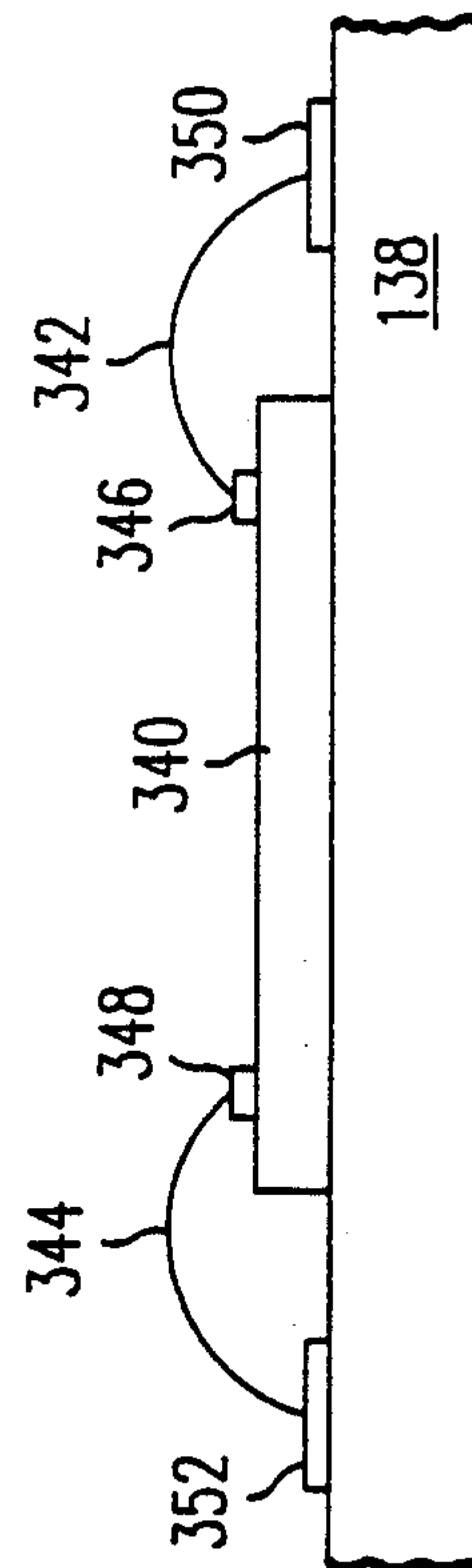
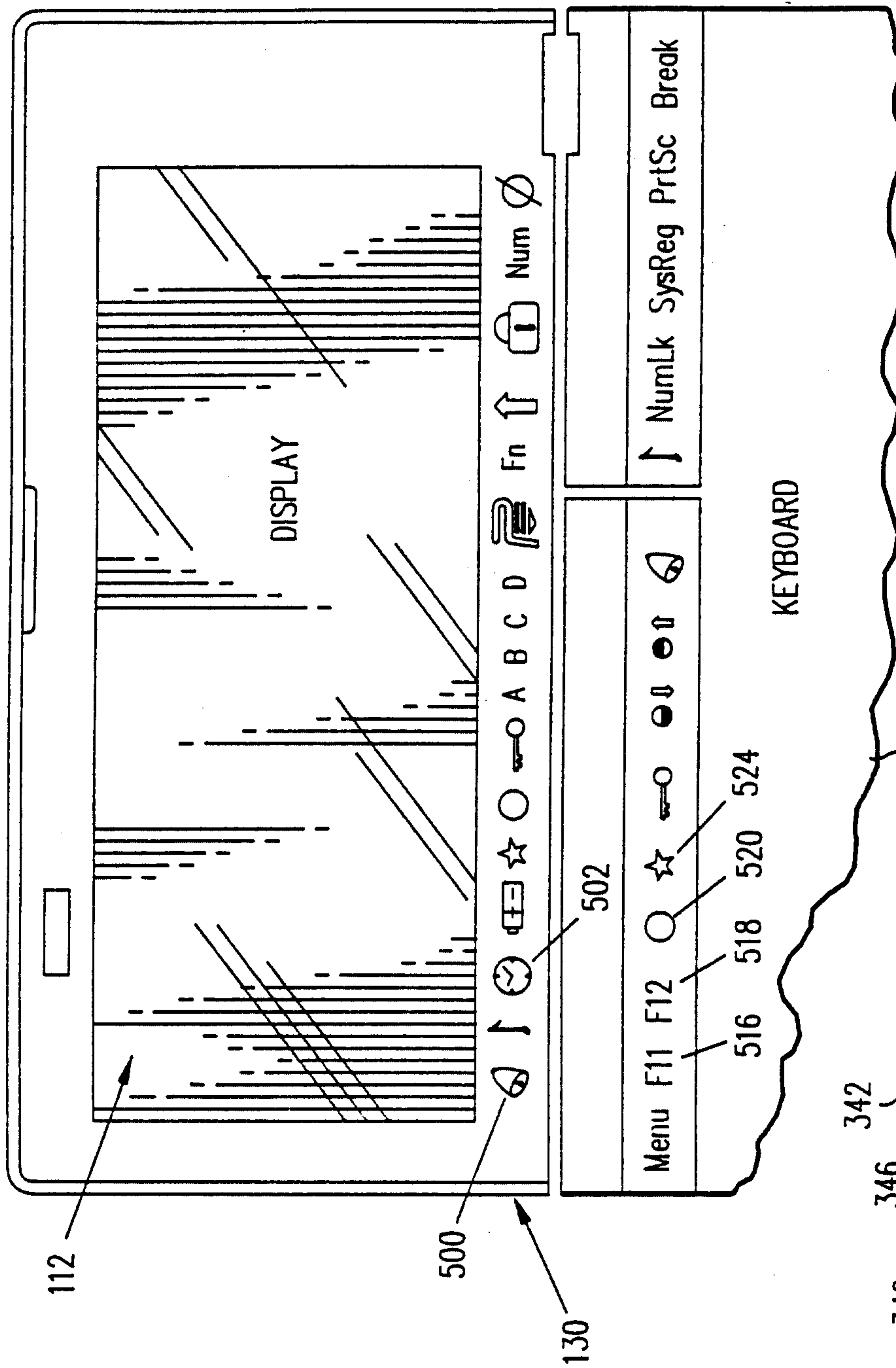


FIG. 8B



PERIPHERAL ASIC C-BUS CROSS REFERENCE

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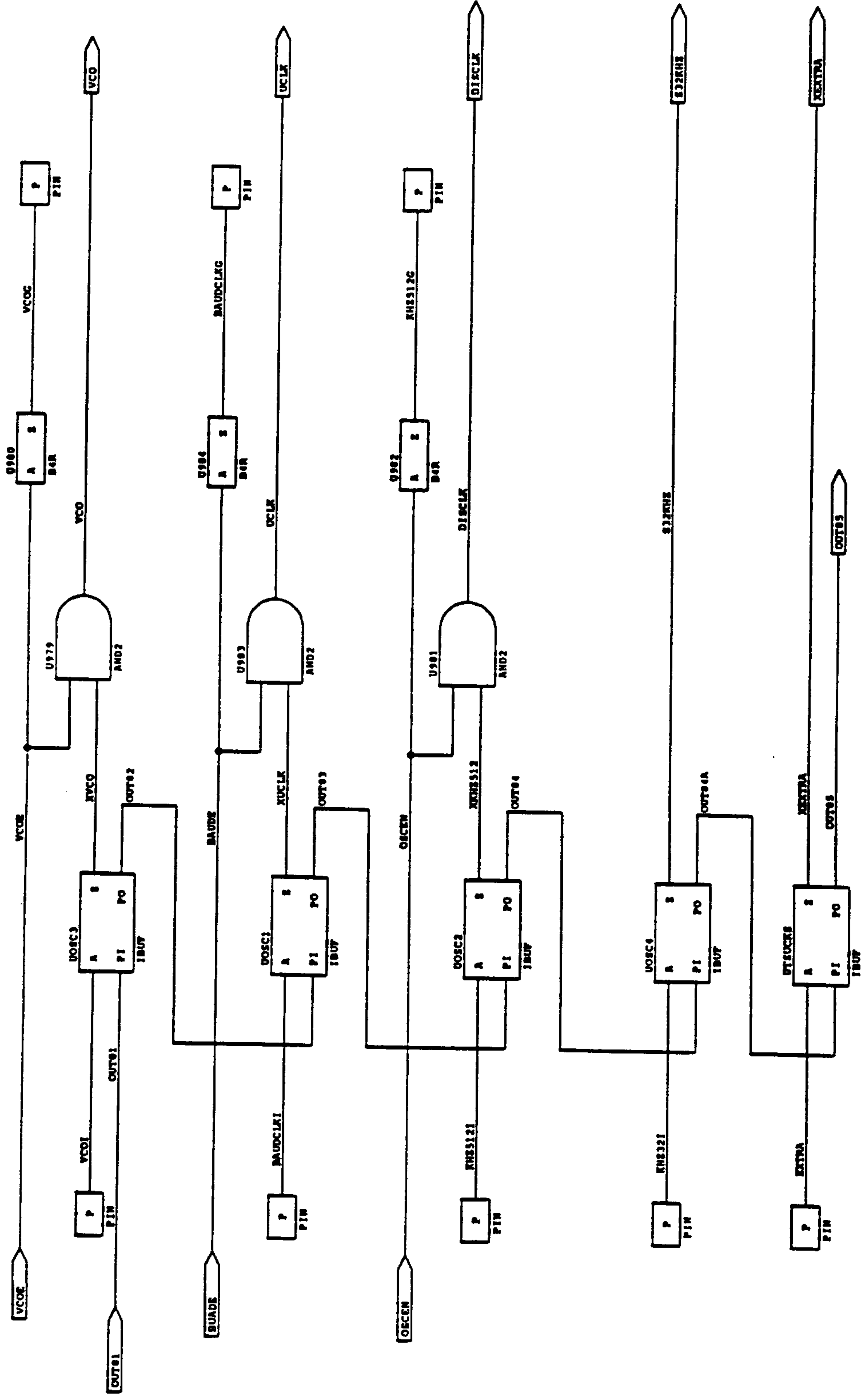
June 27, 1989

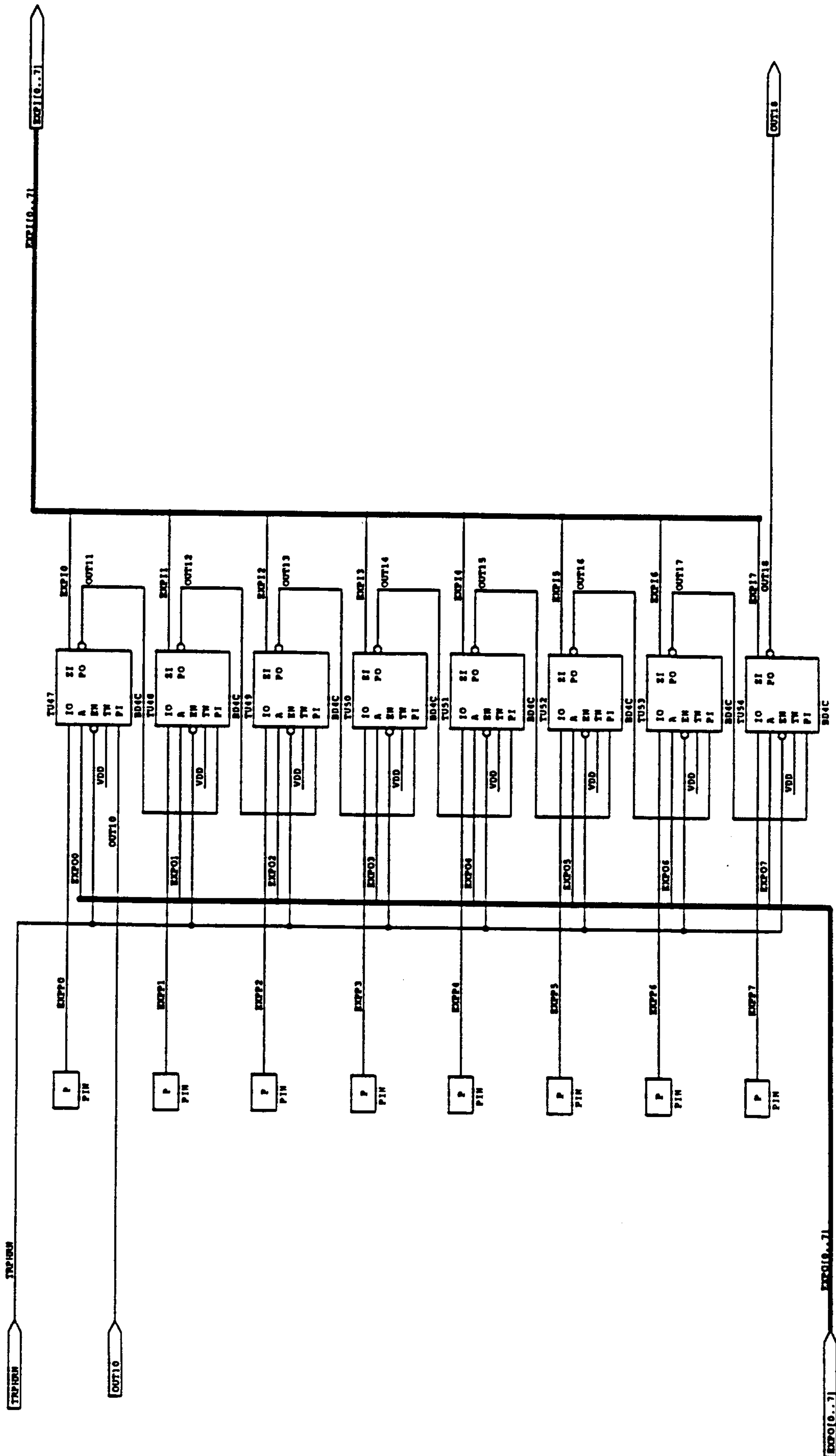
C0	XAENN	C39	XPQKEYN
C1	XDEADBATT	C40	S4HZ
C2	XLOWBAT	C41	SPKDRV
C3	CLRKBIRQ	C42	S16KHZ
C6	IOCHK	C43	XTEST2
C7	IORDN	C45	XONOFFN
C8	IOWRN	C48	ZRSPWRN
C9	RESET	C49	XCDDET1N
C10	RPTSEL0	C50	XCDDET2N
C11	RPTSEL1	C51	XCALM1N
C12	RPTSEL2	C52	XCALM2N
C13	RPTSEL3	C53	XPERCLKN
C14	TEST	C57	HLDKBCCLK
C15	TMRSEL0	C61	BAUDE
C16	TMRSEL1	C62	VCOE
C17	ZSELVDD	C63	DSPLYOFF
C18	ZPERINTR	C64	RDYN
C22	OSCEN	C65	XIOCHKN
C24	TMRINTR	C66	XSIN
C25	ZIRQ1	C67	XCTSN
C26	ZIRQ4	C68	XDSRN
C27	UCLKE	C70	XKBCOL0
C28	YOUSTOP	C71	XKBCOL1
C31	PRPHRN	C73	XEXTSYSCLK
C32	VTRAP	C74	XKBCOL2
C35	CONTVAL0	C75	XKBCOL3
C36	CONTVAL1	C76	XKBCOL4
C37	CONTVAL2	C77	XKBCOL5
C38	CONTVAL3	C78	XKBCOL6
C89	CGA	C69	XDCCDN
C90	MDA		

12

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Doc. No. 10 B





14

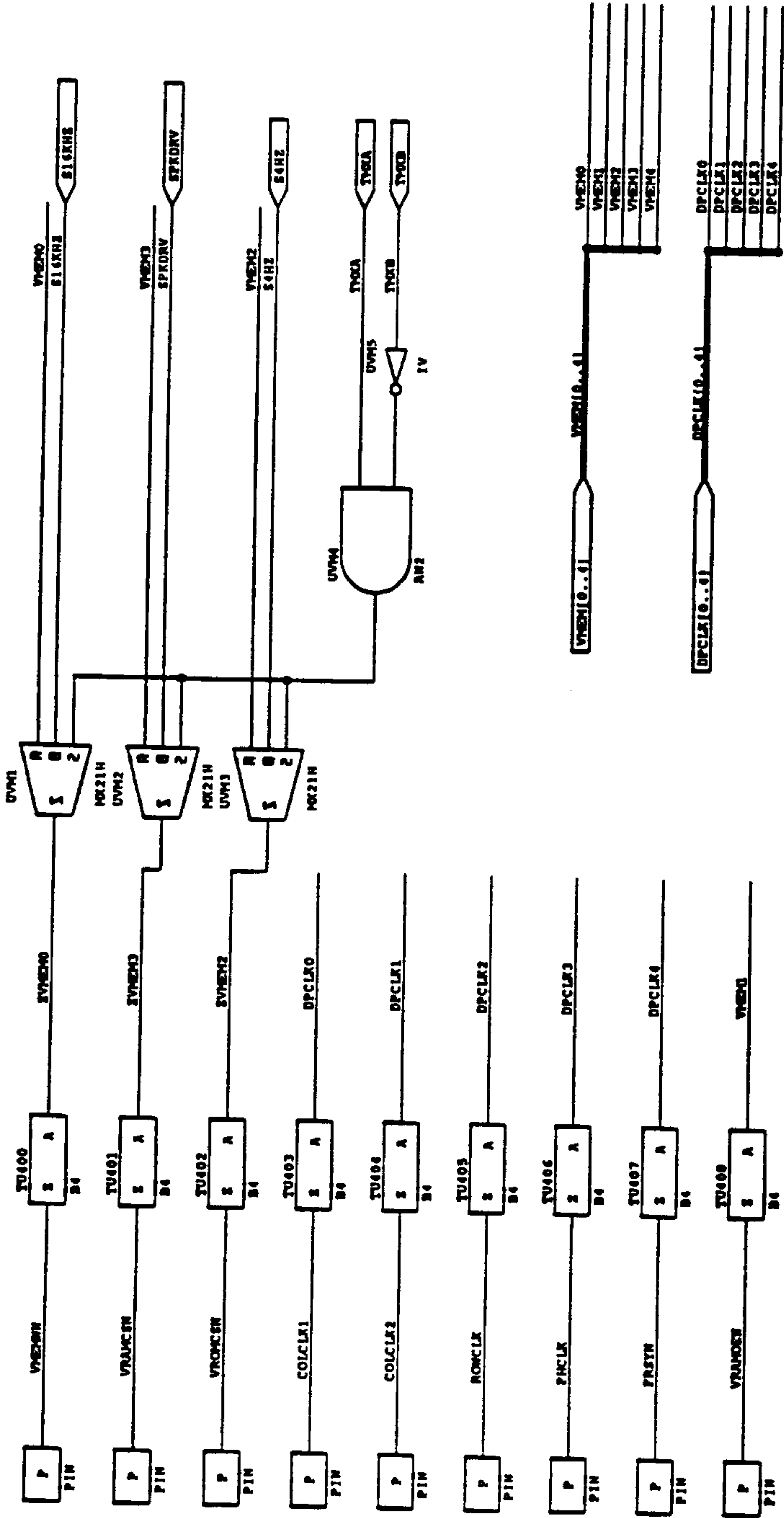


FIG. 10D

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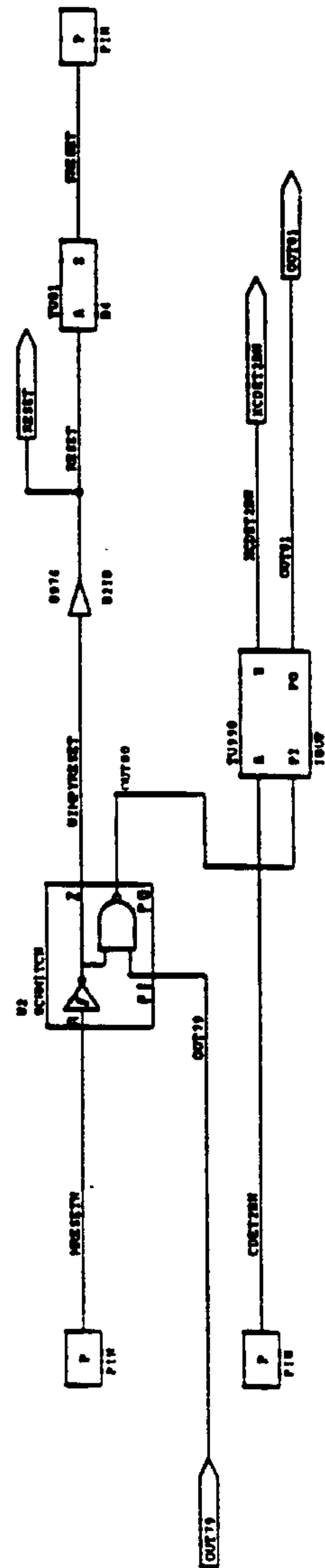
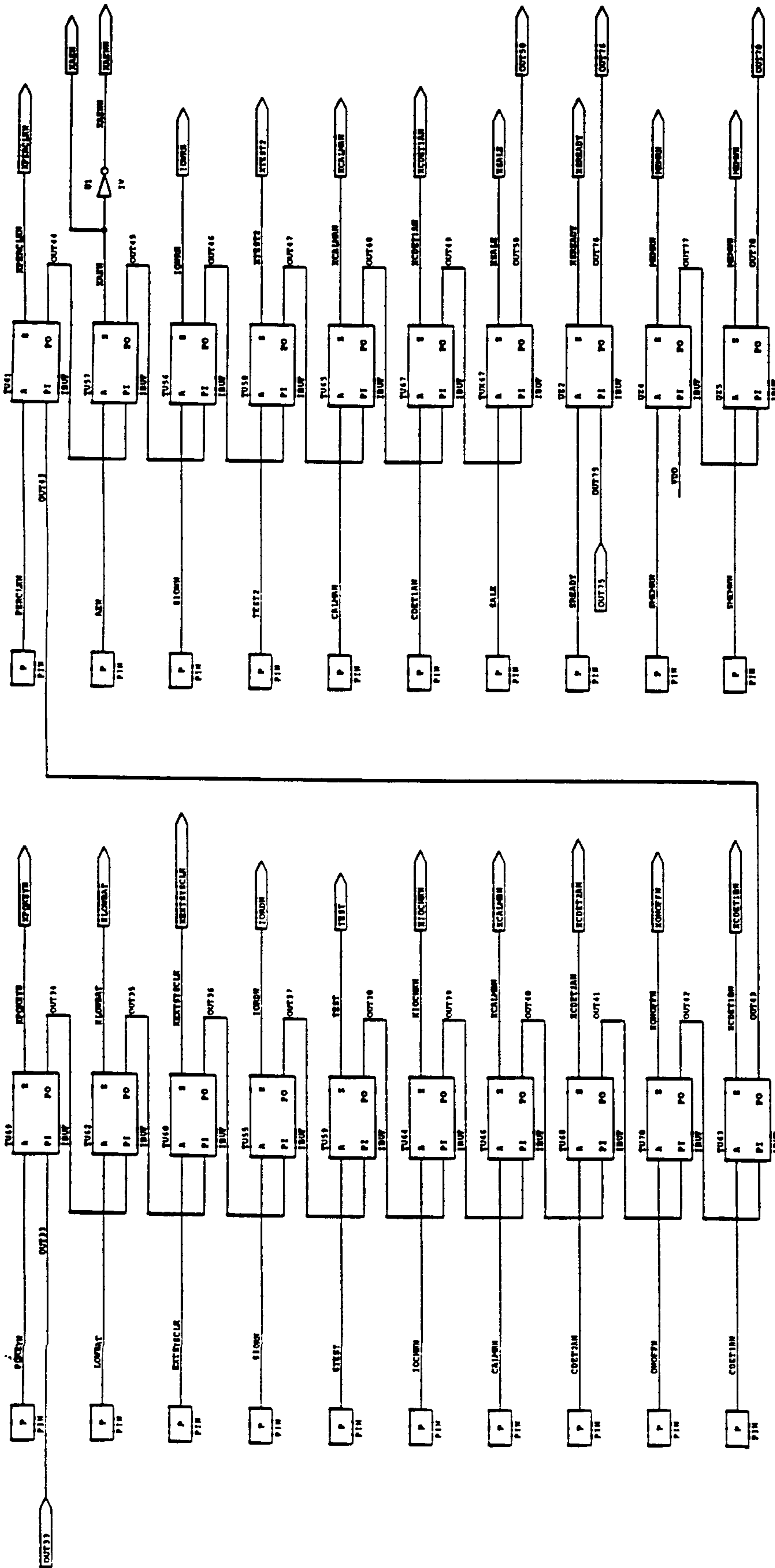
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Fig. 10E



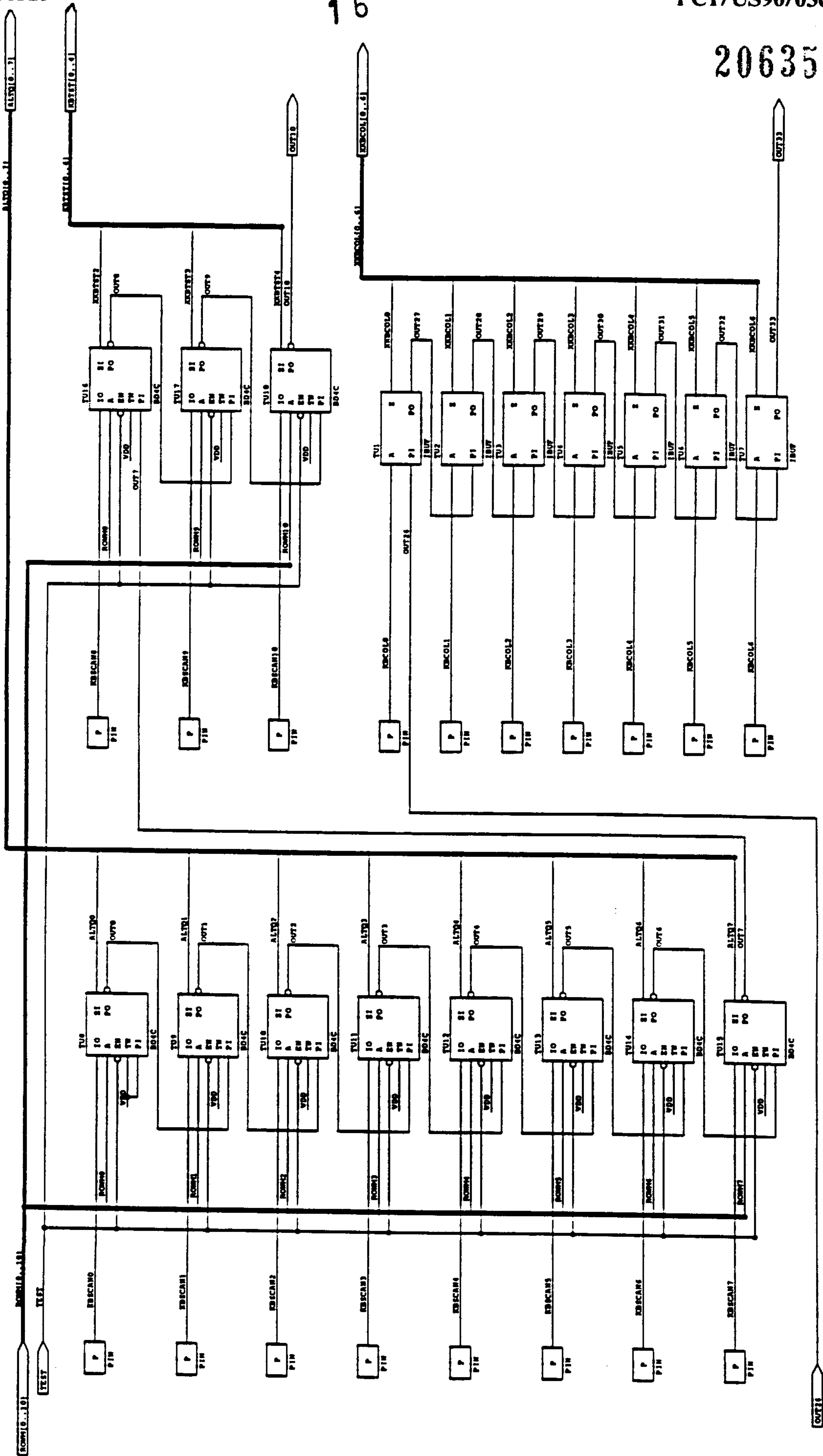


Fig. 10 G

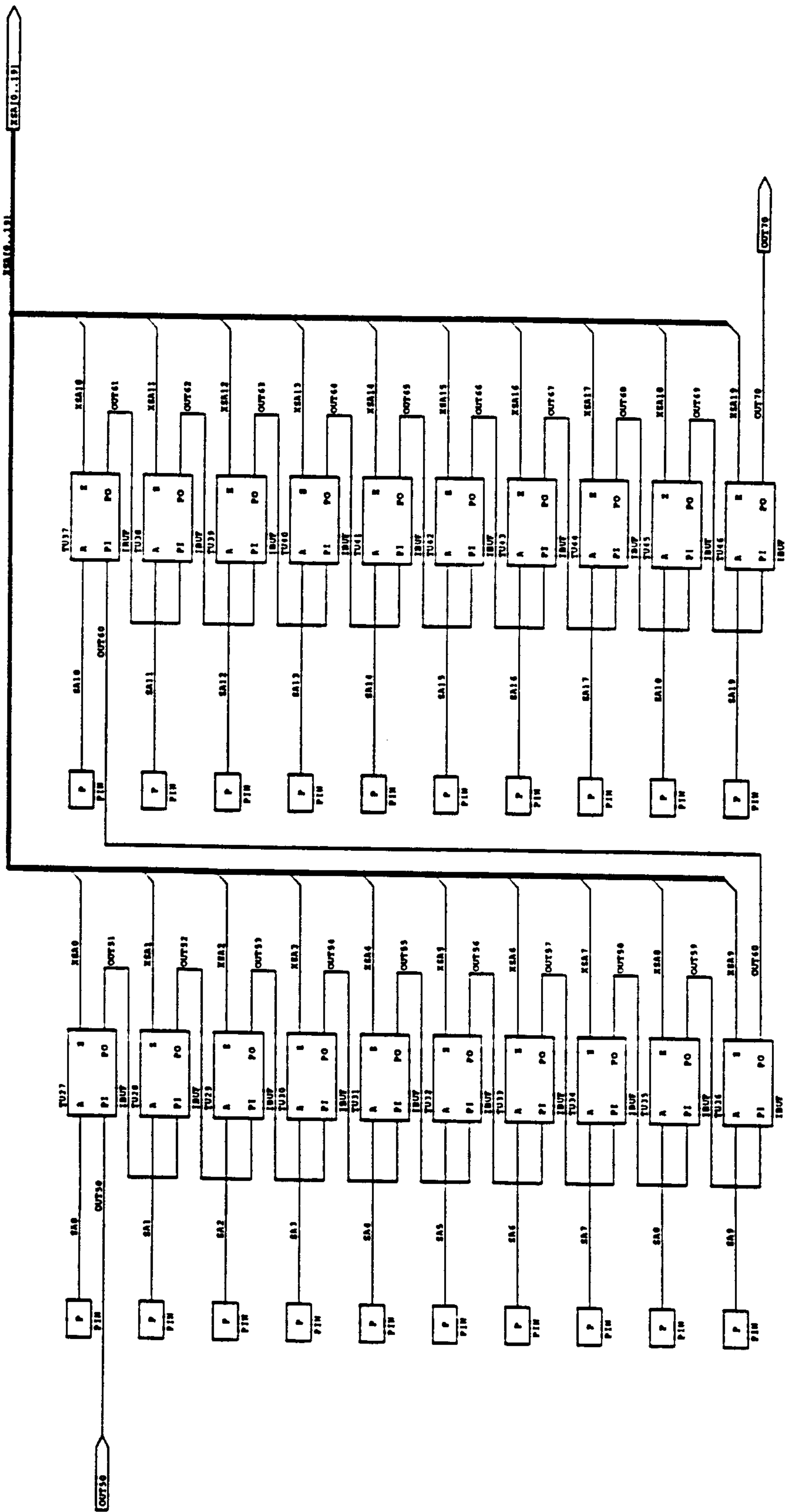
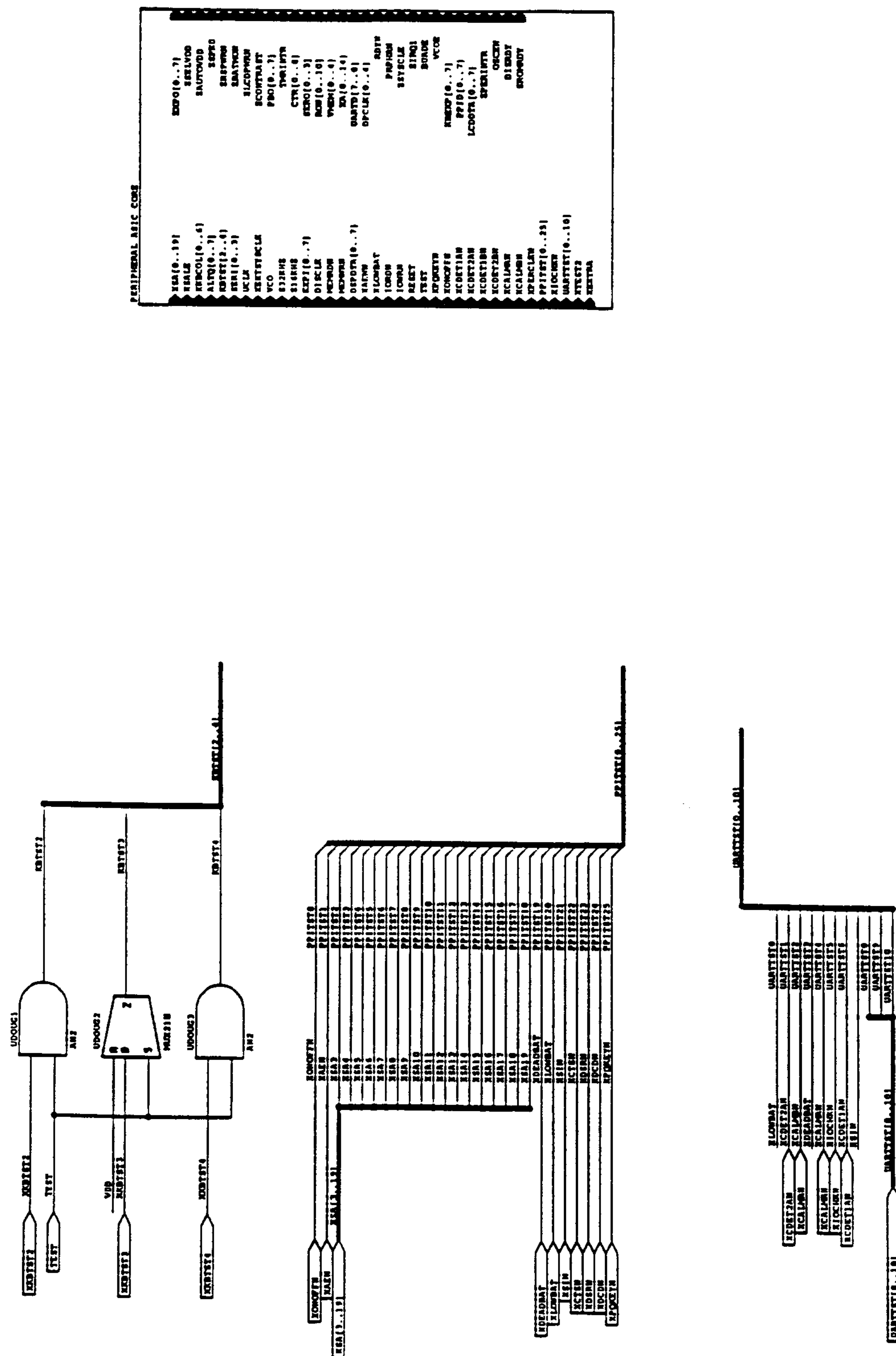




Fig. 10 H



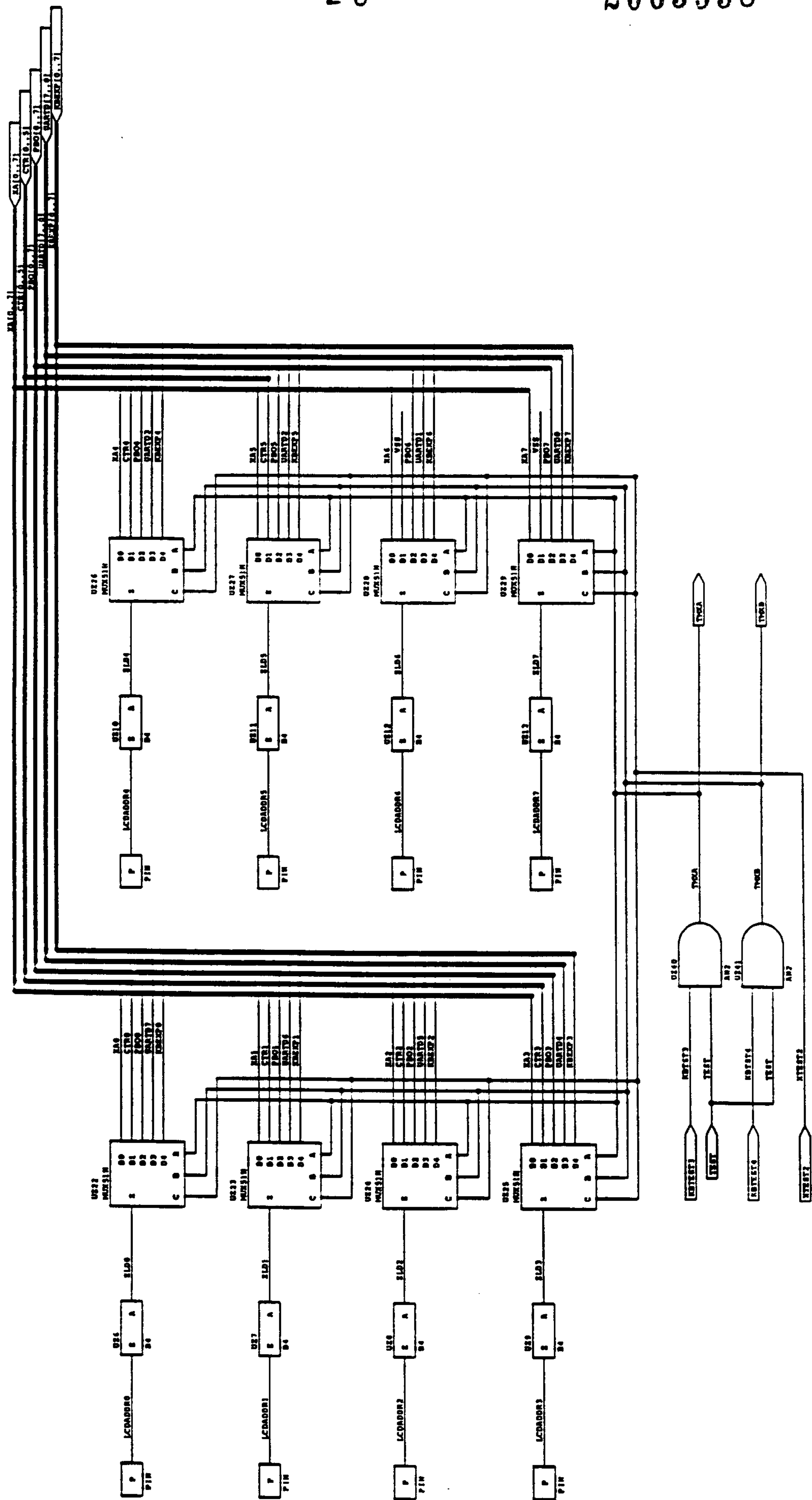


Fig. 10 J $\varphi 0.000.8$

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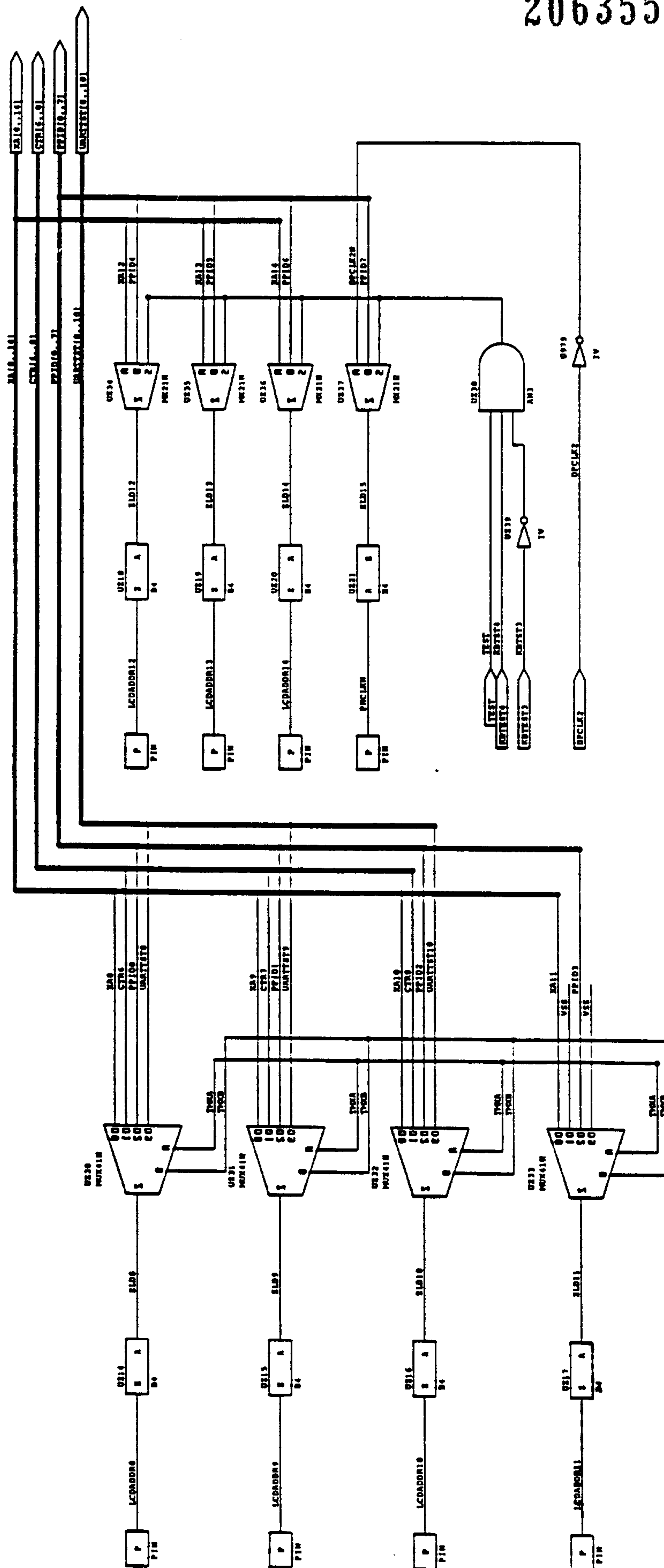
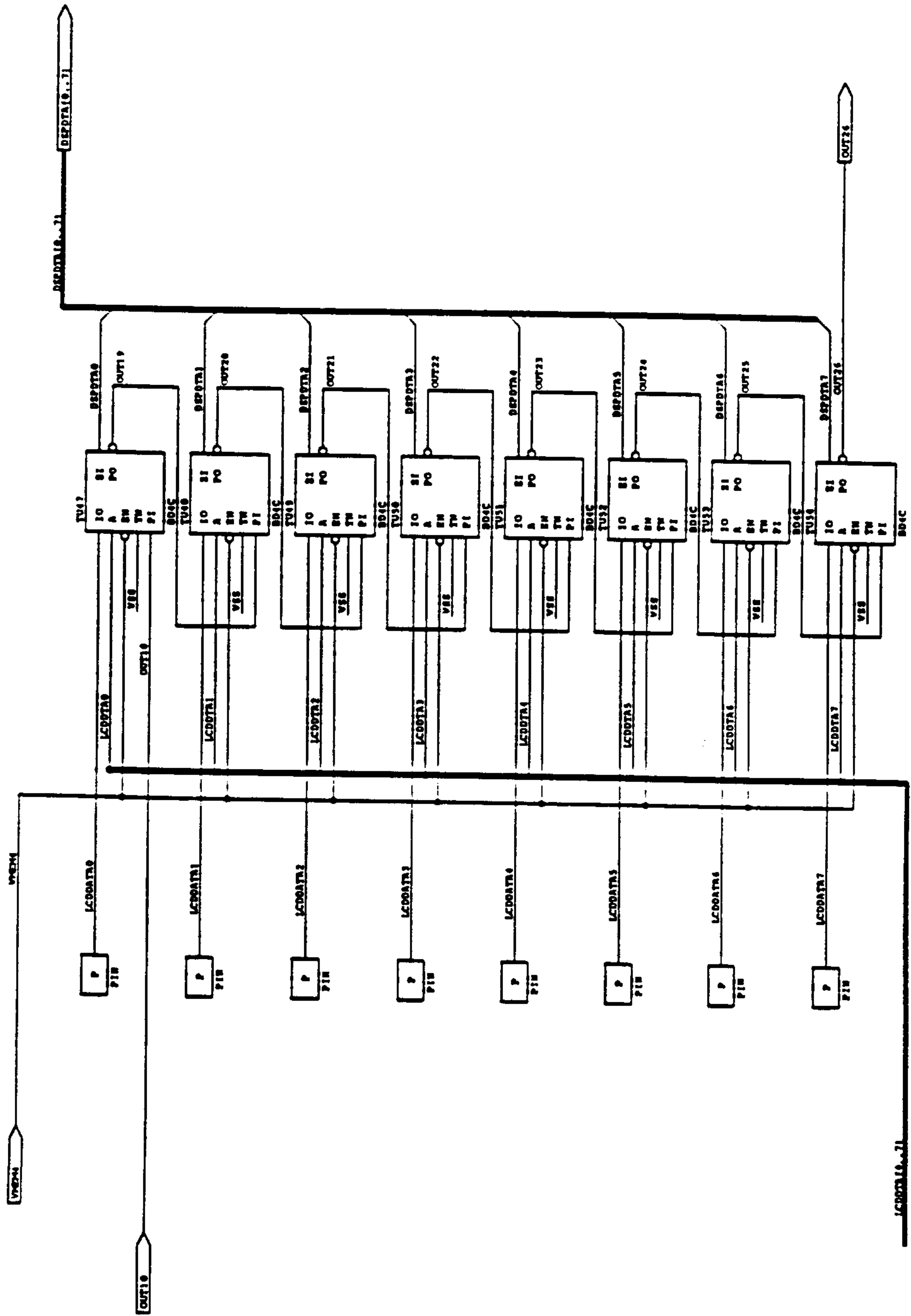


Fig. 10K

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22

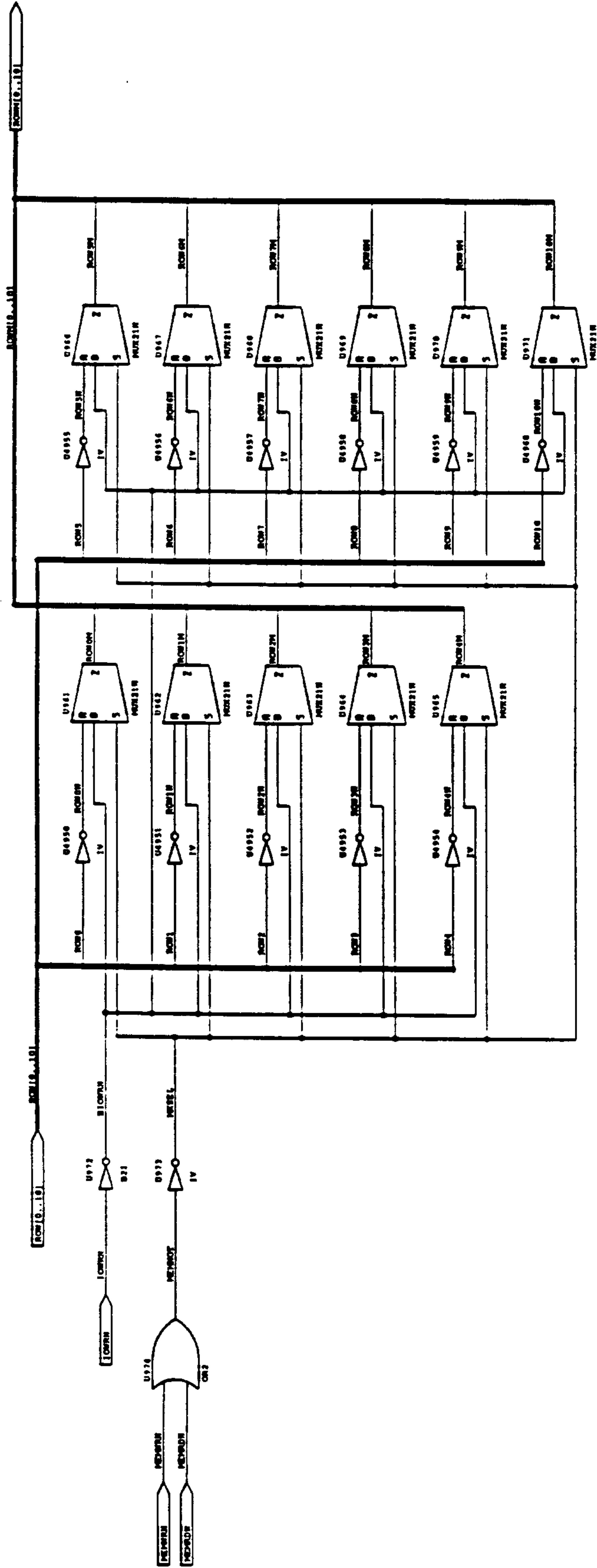
Fig. 10L



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00.00008

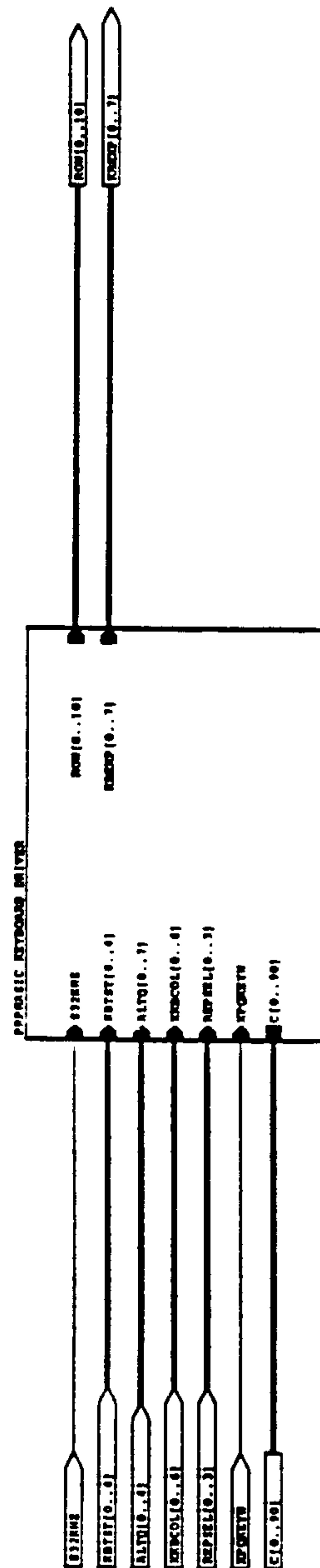
Fig 10M



24

$\phi\phi.\phi1\phi$

Fig. 10N



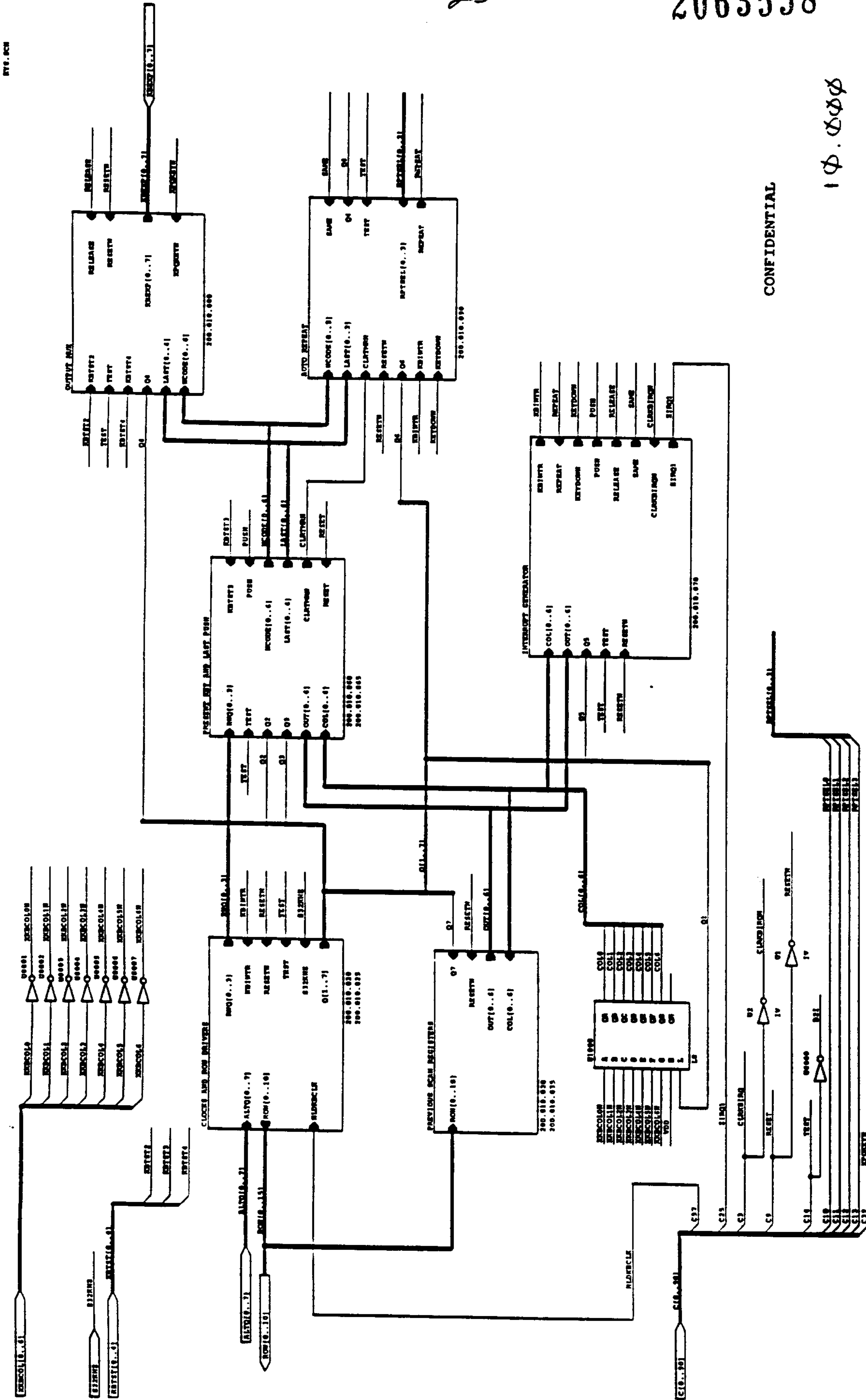
25

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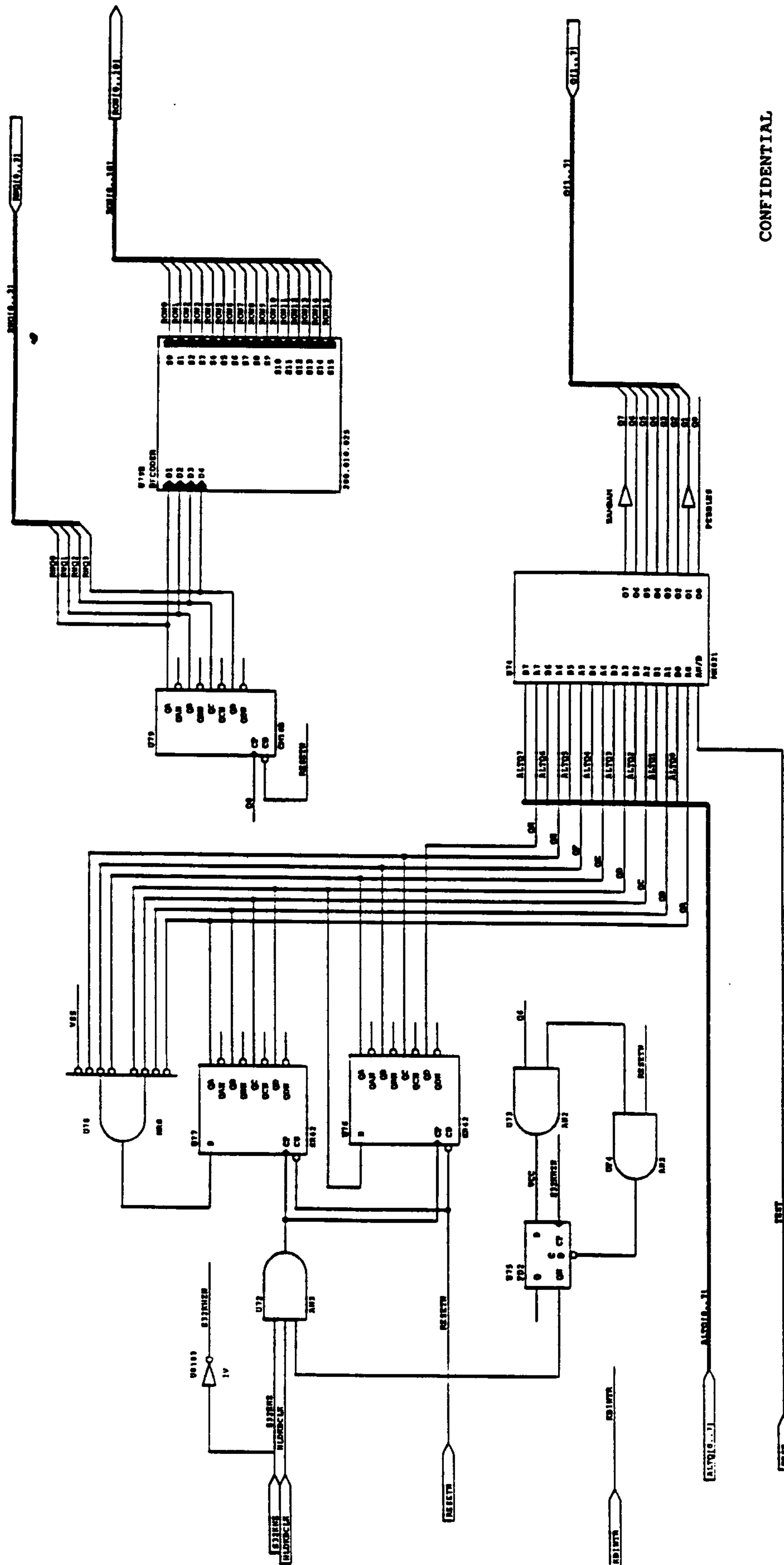
14.888

Fig. 10 D



26

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 $1\phi.\phi.1\phi$

Fig. 10 P

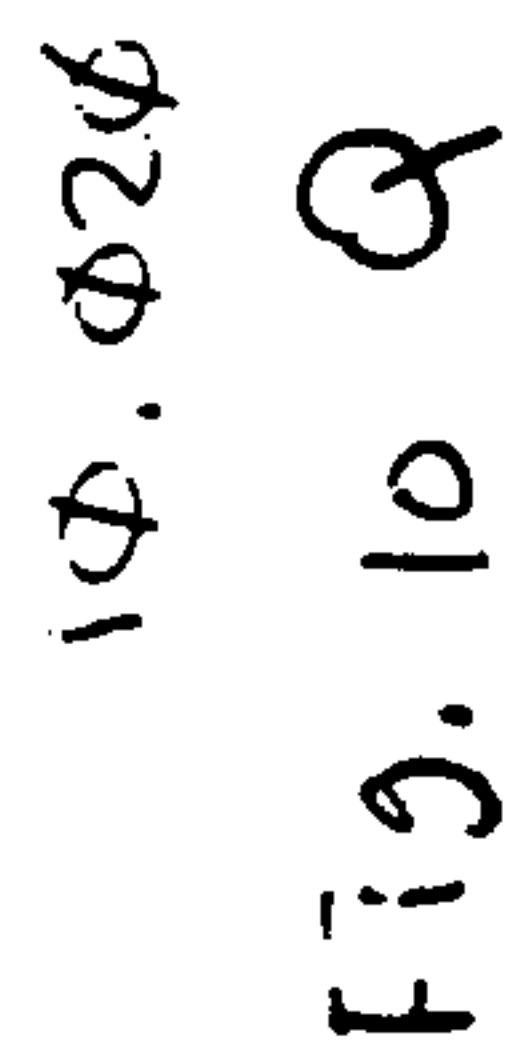
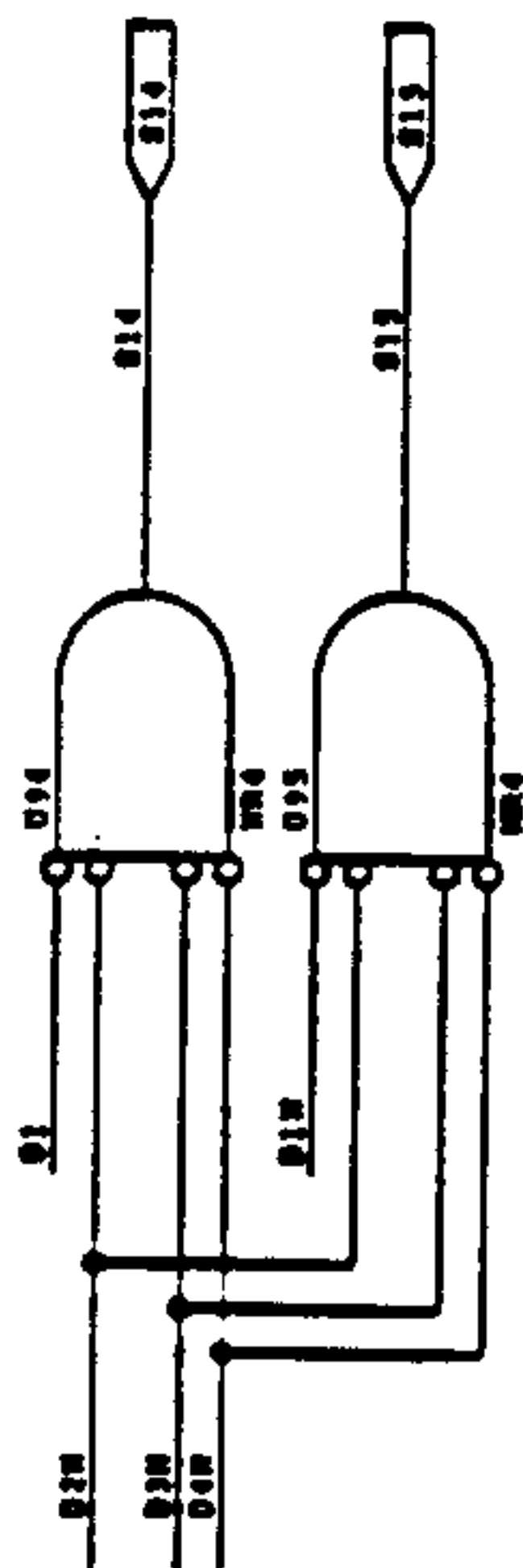
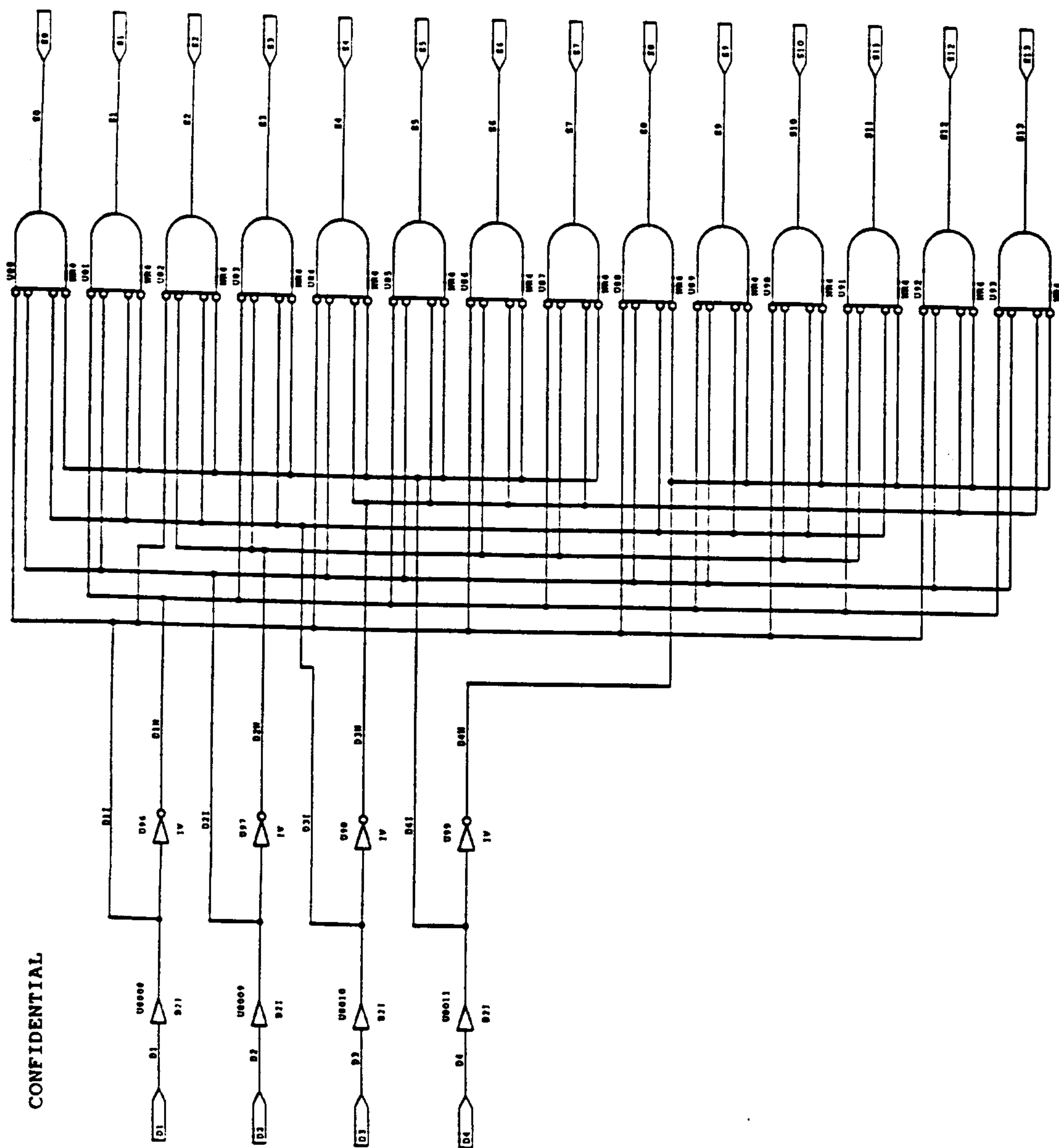


Fig. 10

14.030
Fig. 10 R

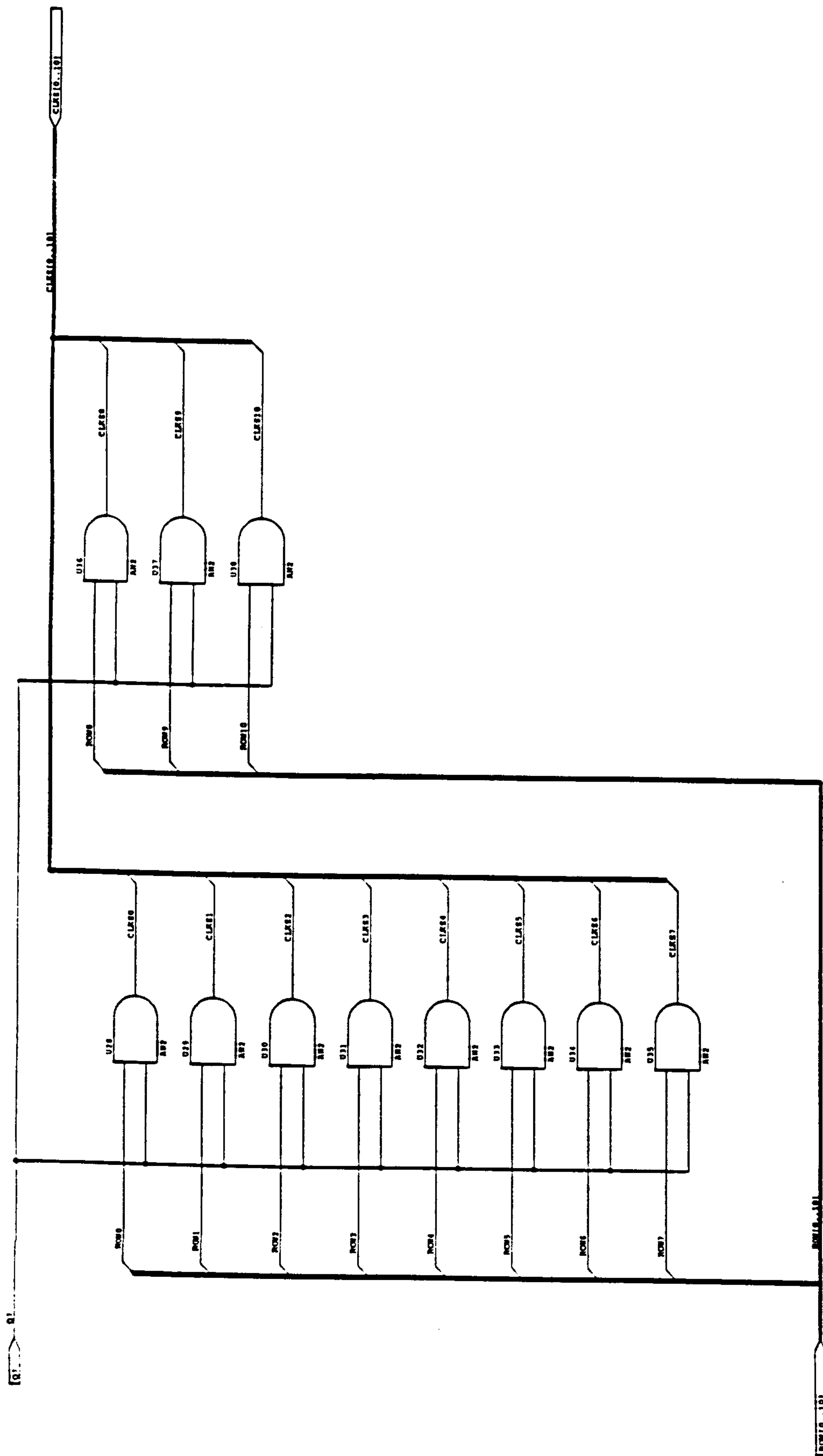


29

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$1D, 4\phi$

Fig. 10 S

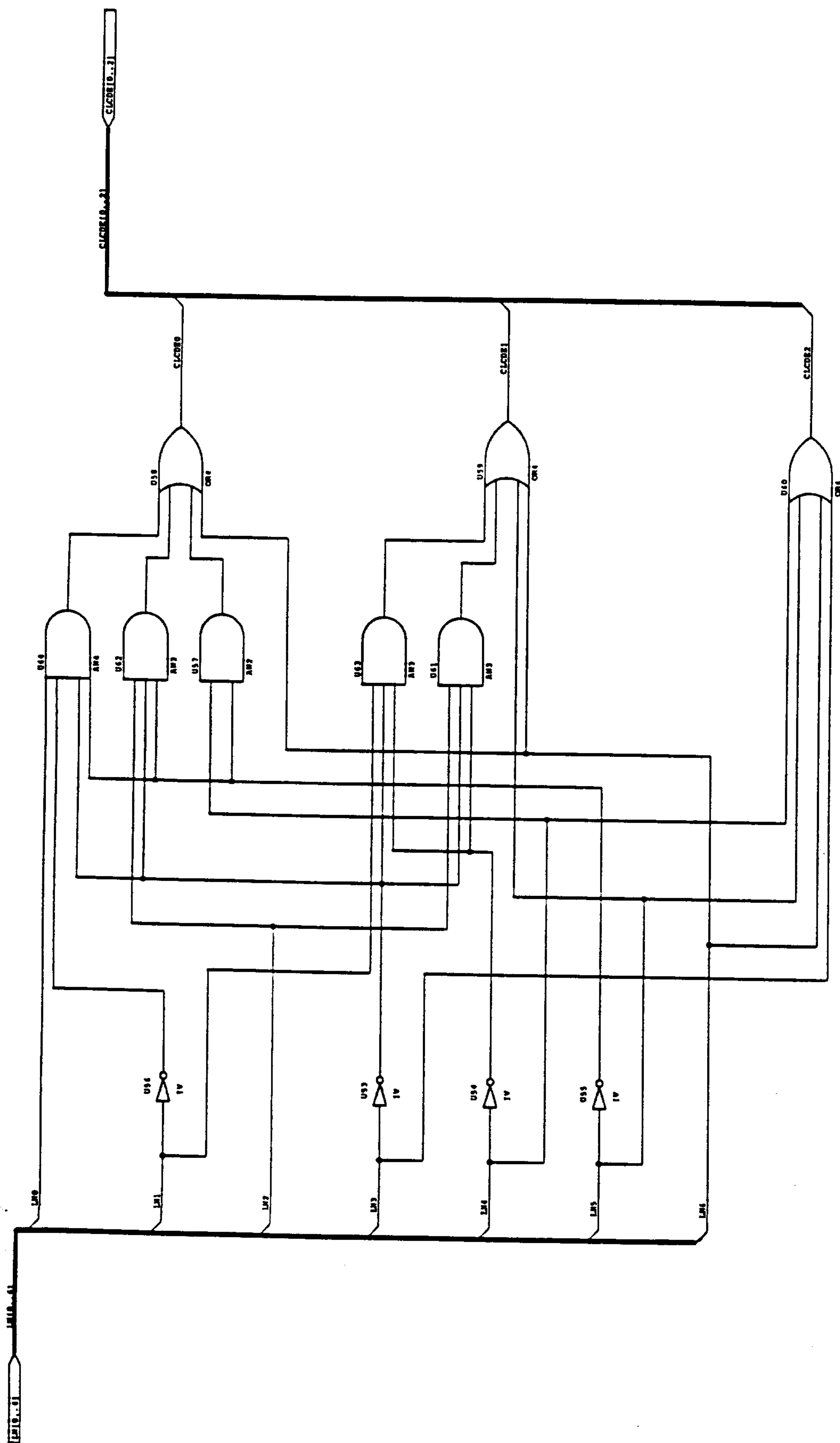


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31

Fig. 10 U

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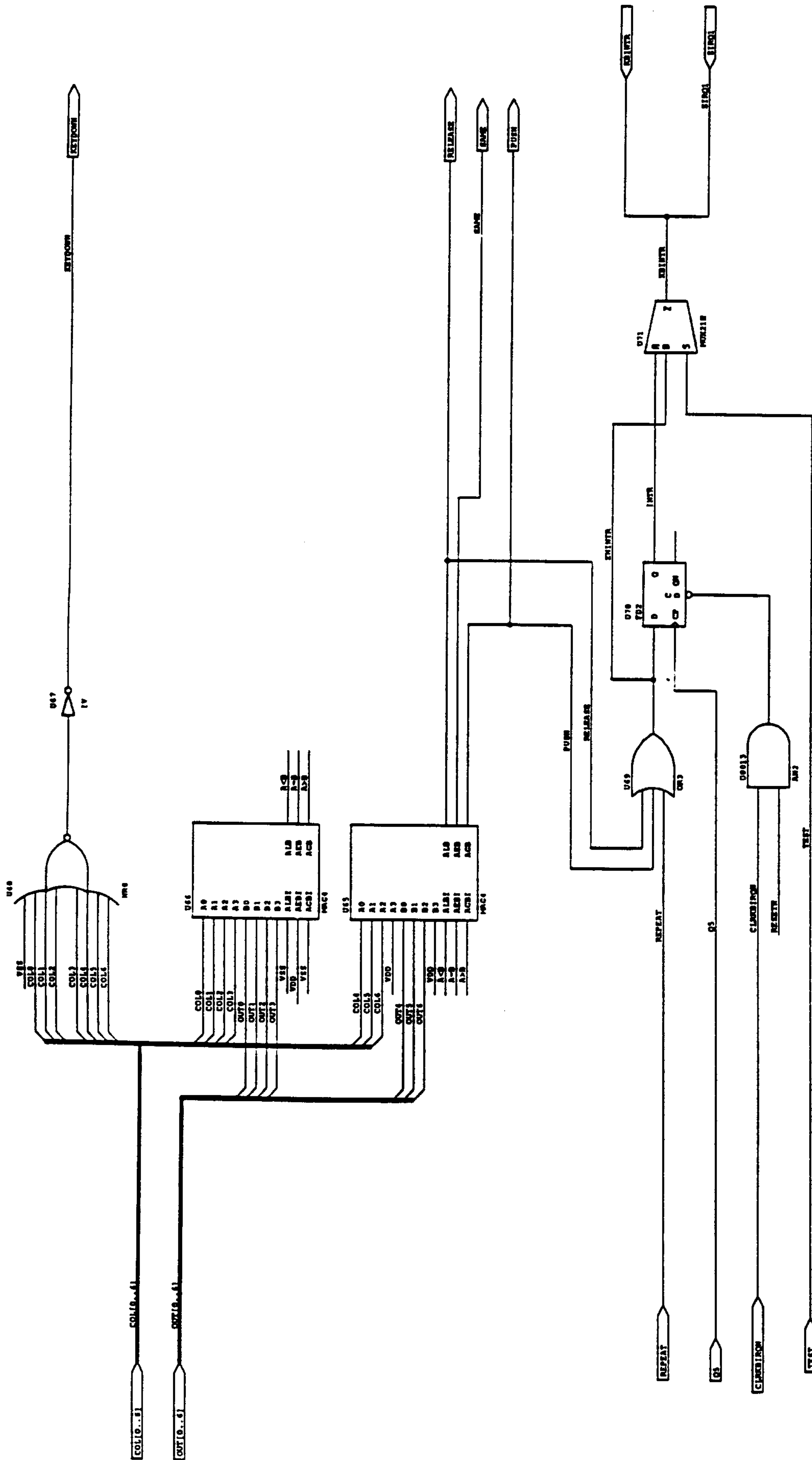


32

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14.0770
Fig. 10V

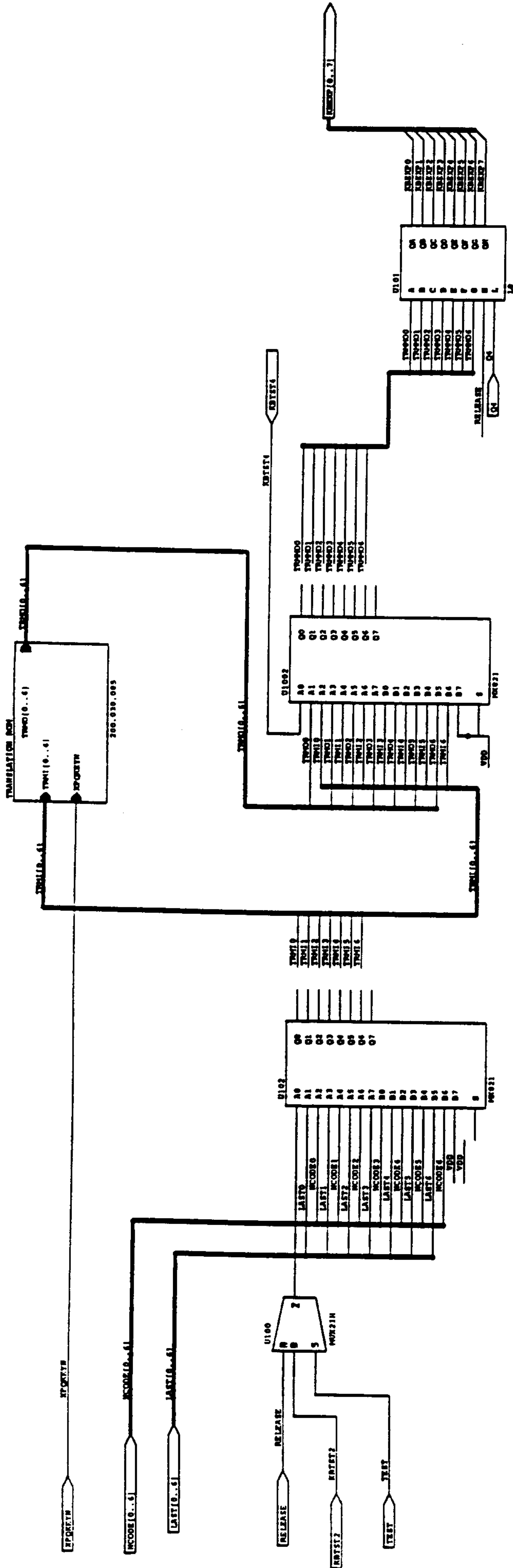


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10.080

Fig. 10W

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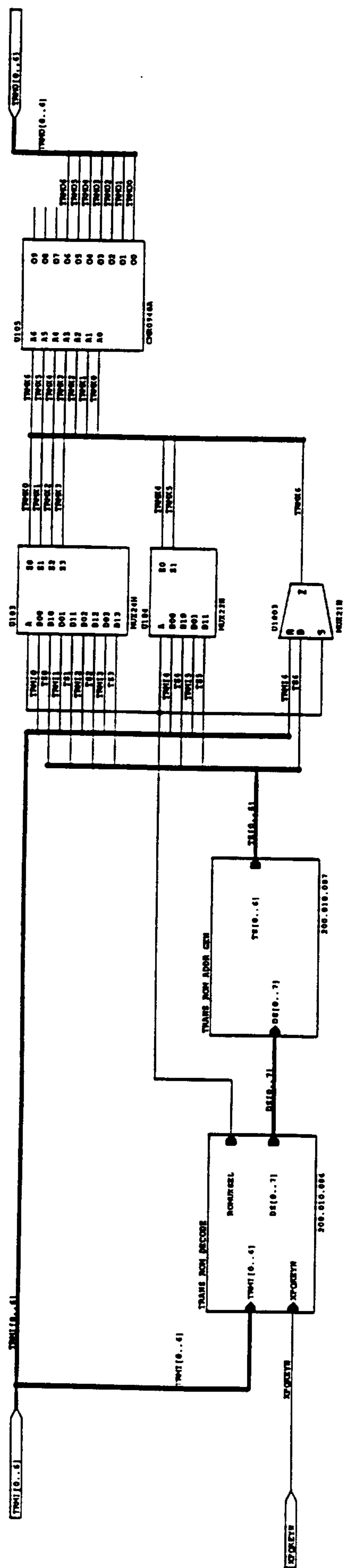
33

34

10. 1992

Fig. 10X

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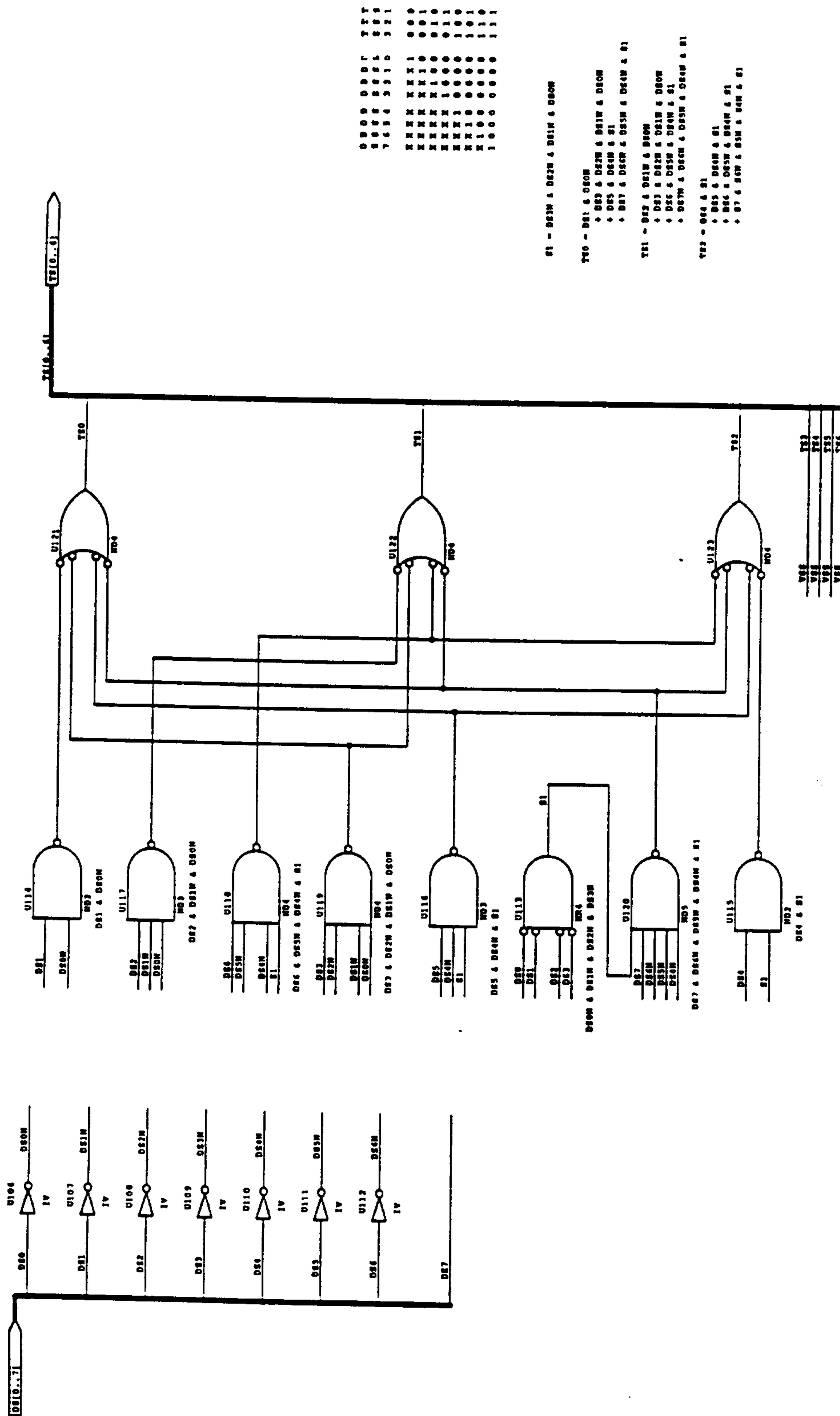


35

15. 150

Fig. 10Y

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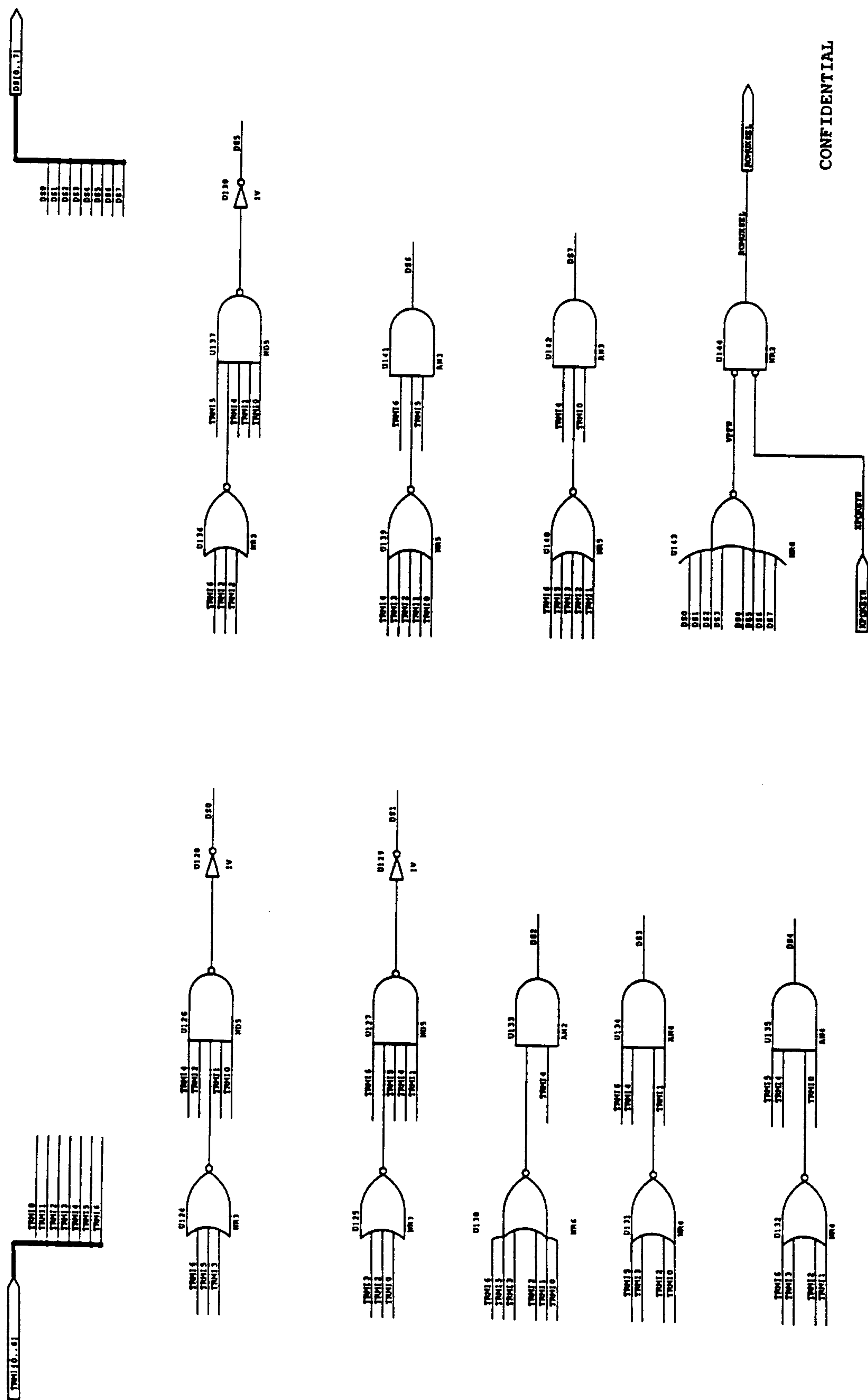
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36

1711

Fig. 102

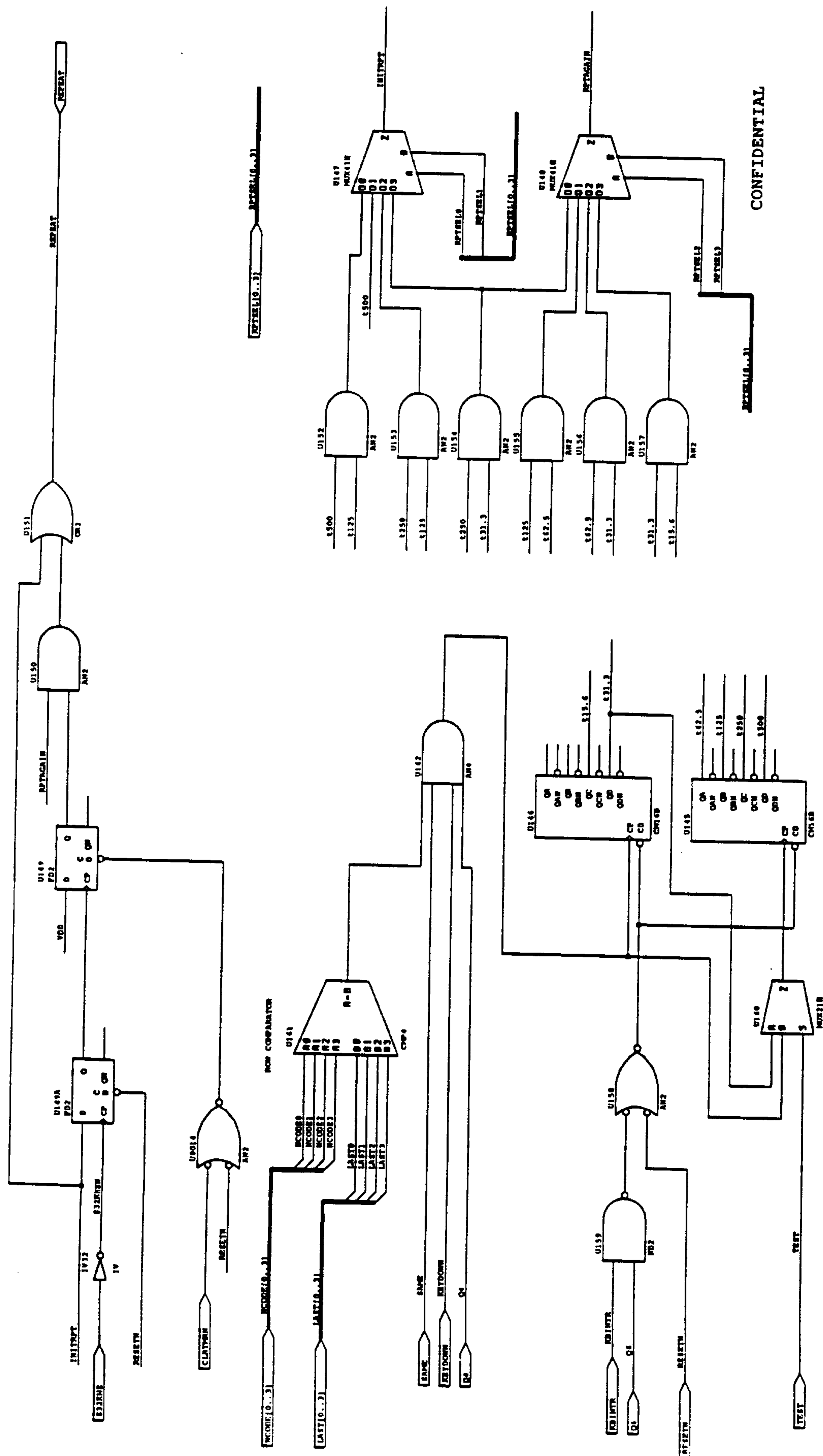
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37

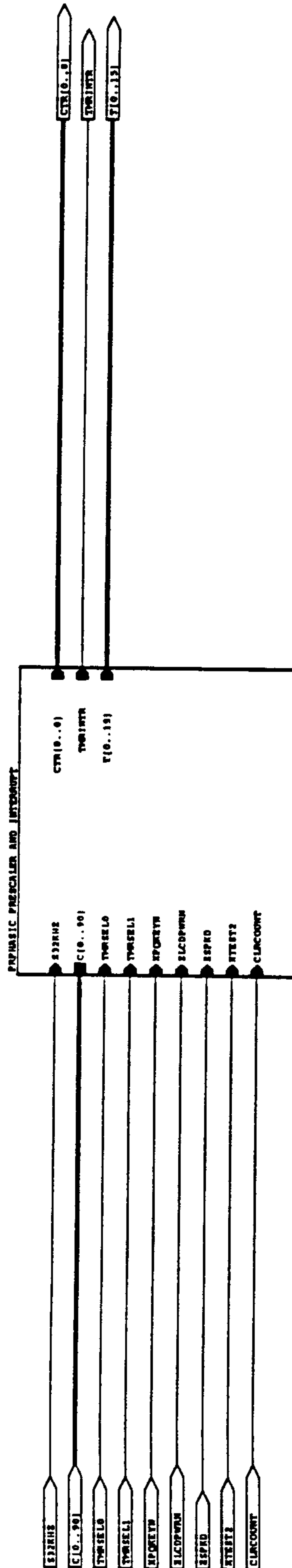


14.124
Fig. 10Aa

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38

00.020
Fig. 10 Ab

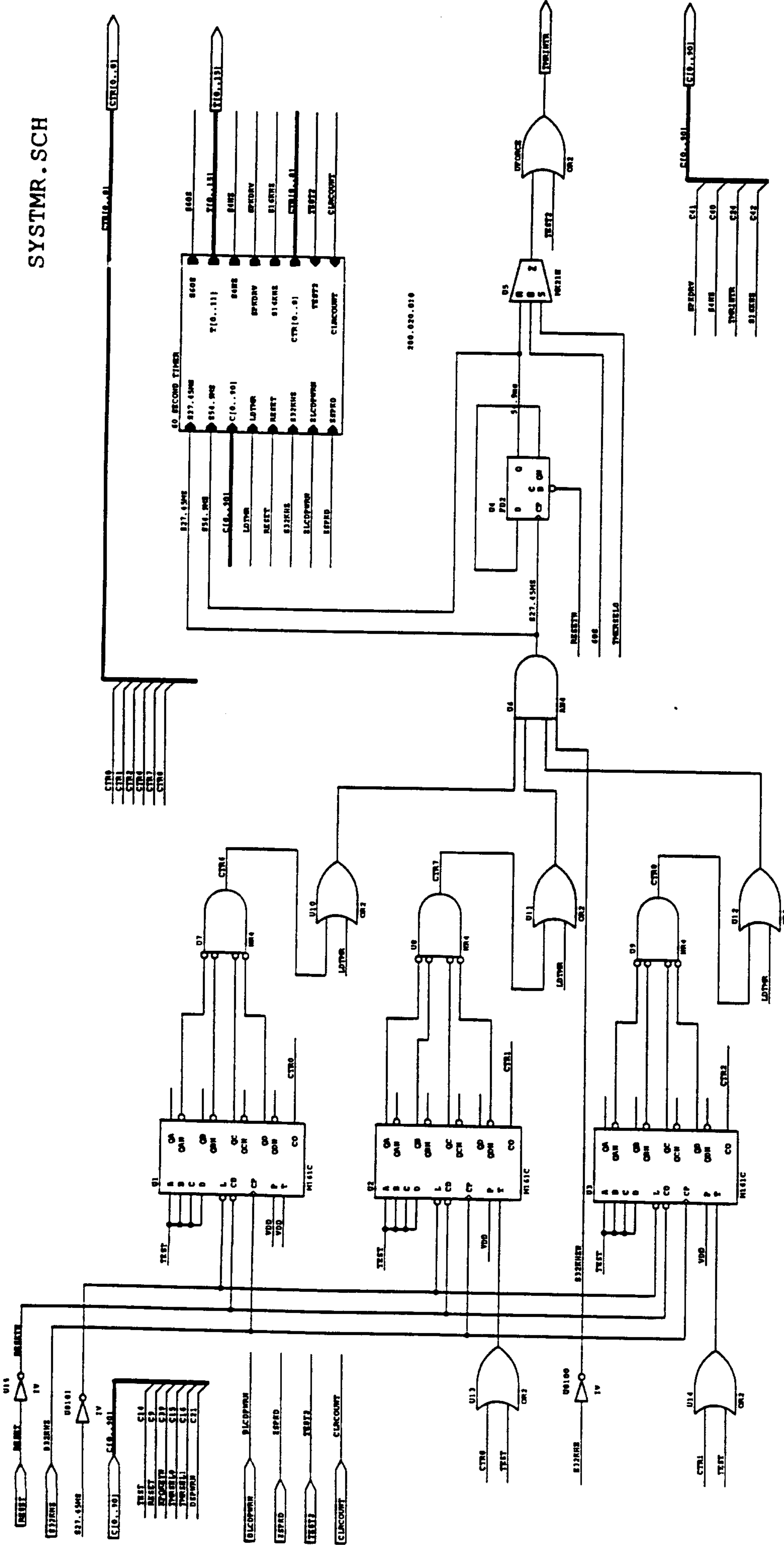


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2.6.016
Fig. 10A c

SYSTMTR.SCH



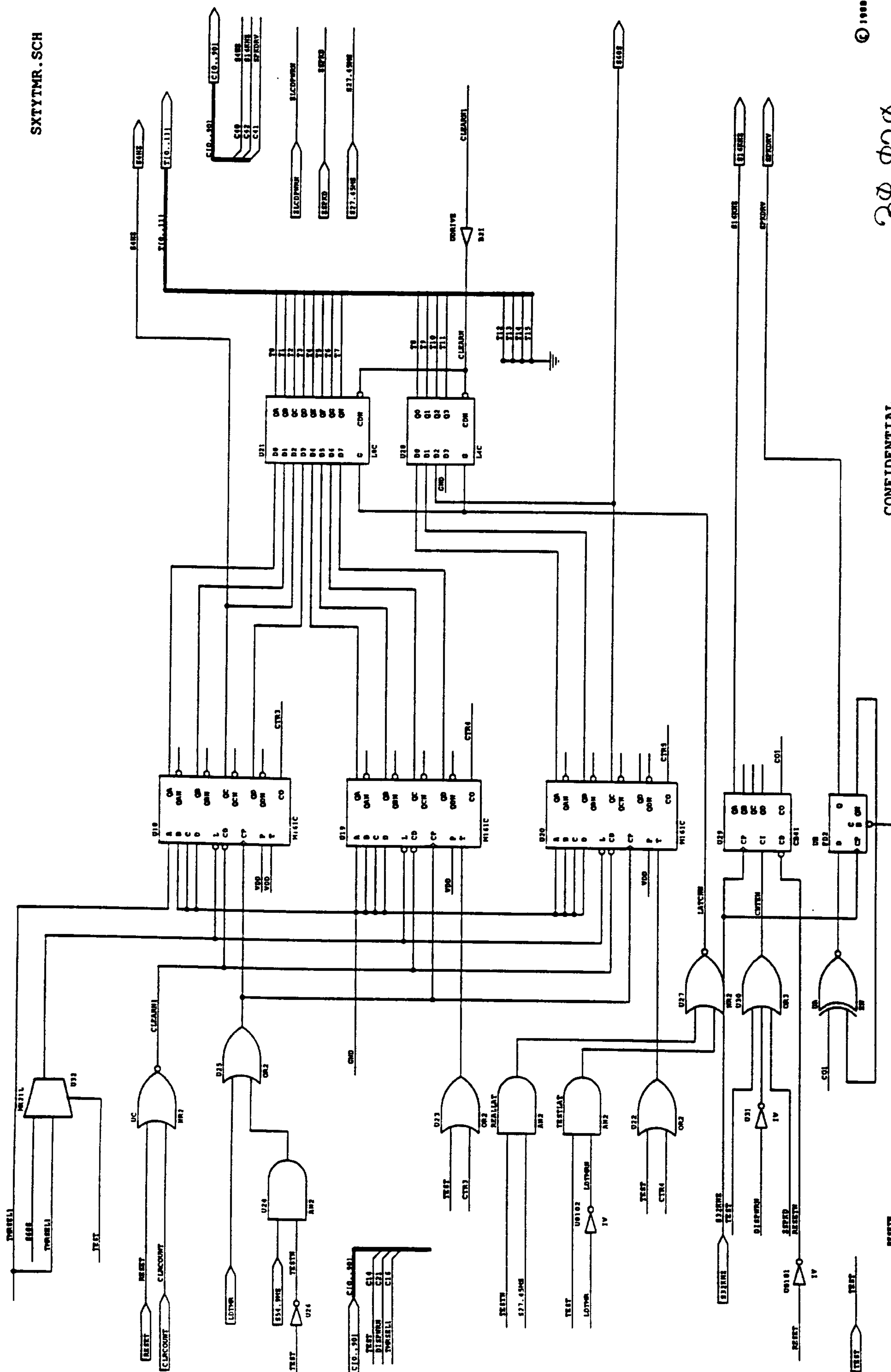
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20. 020
Fig. 10 Ad.

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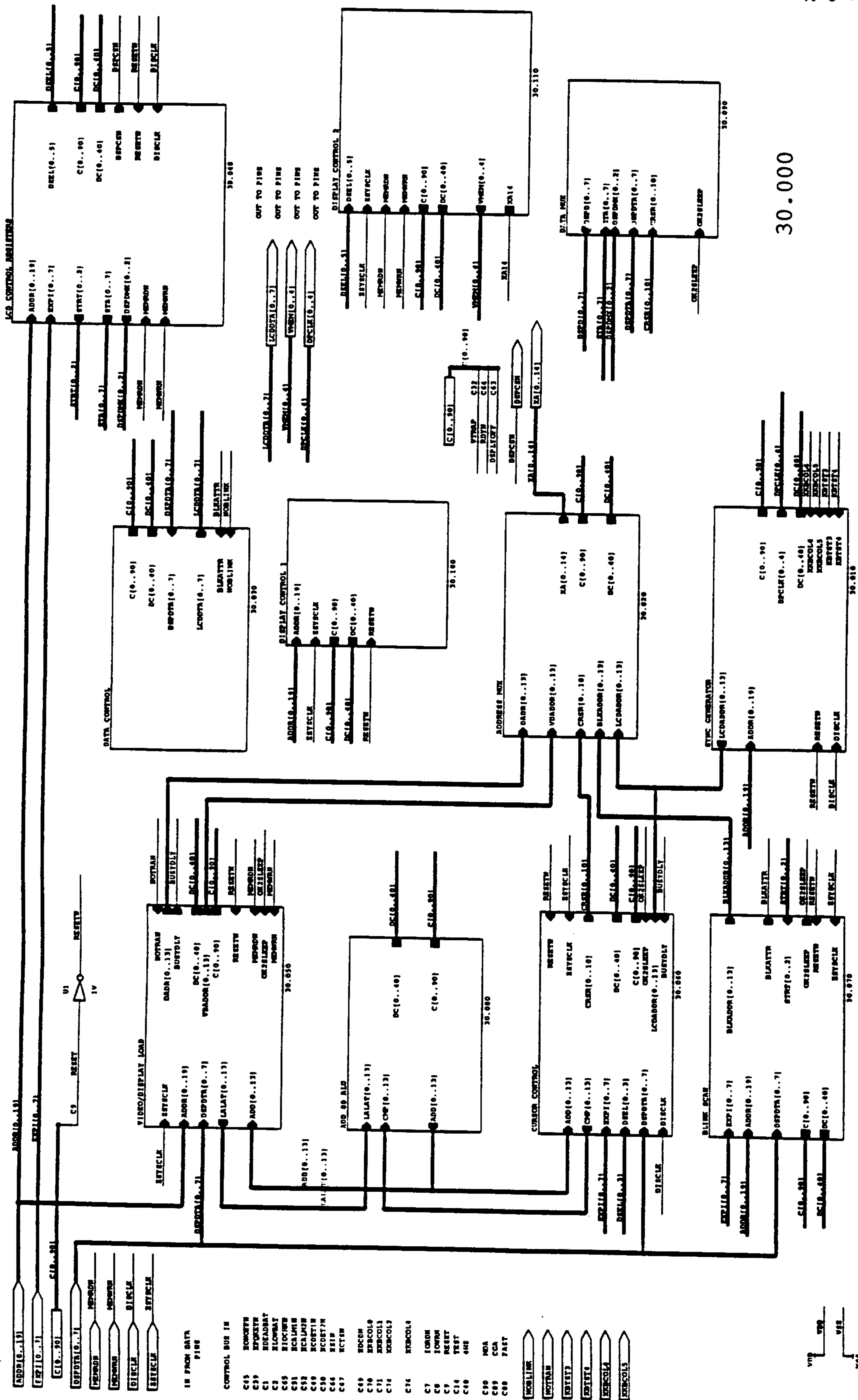
SXTYTMR.SCH

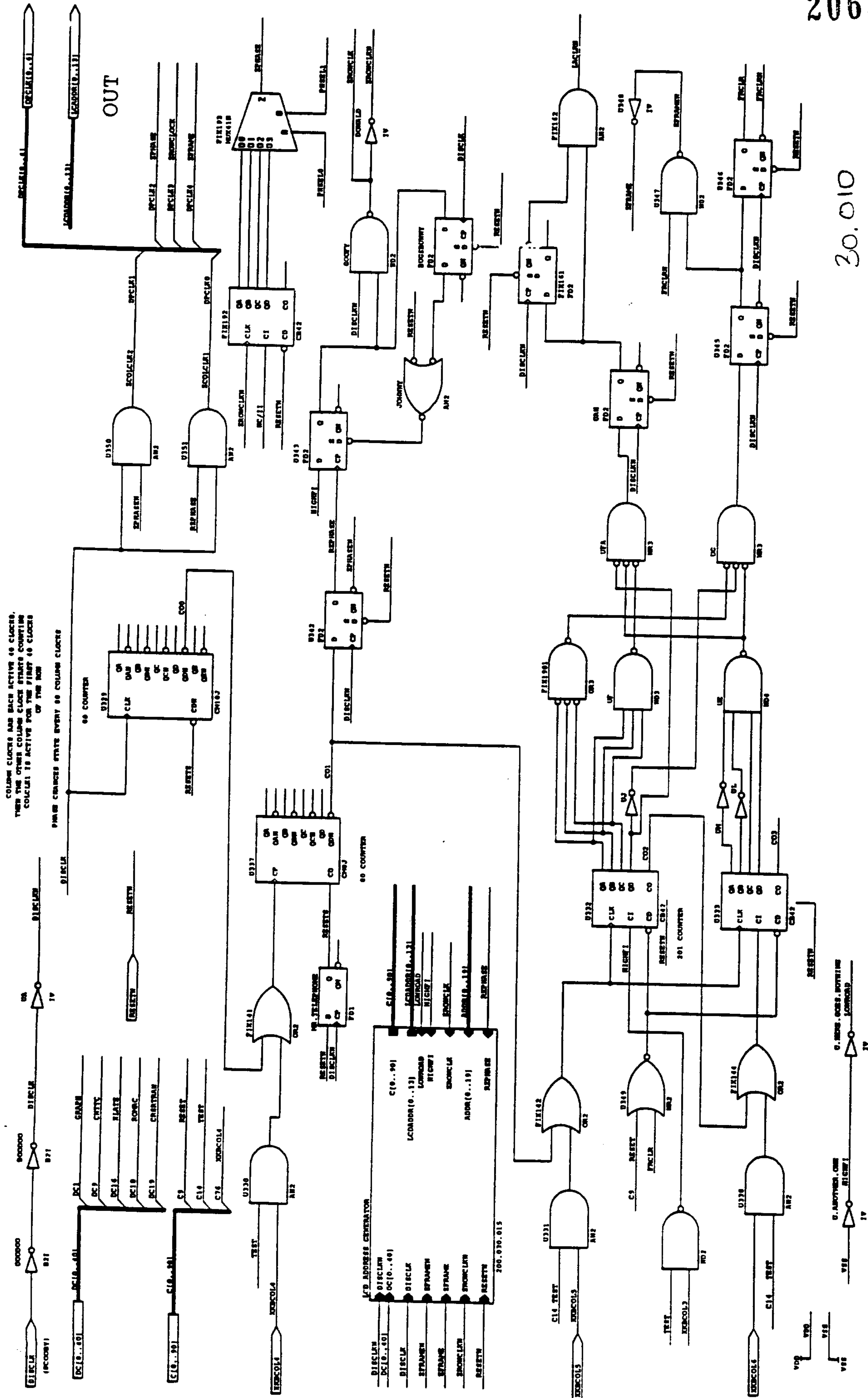


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42

Fig. 10 Af





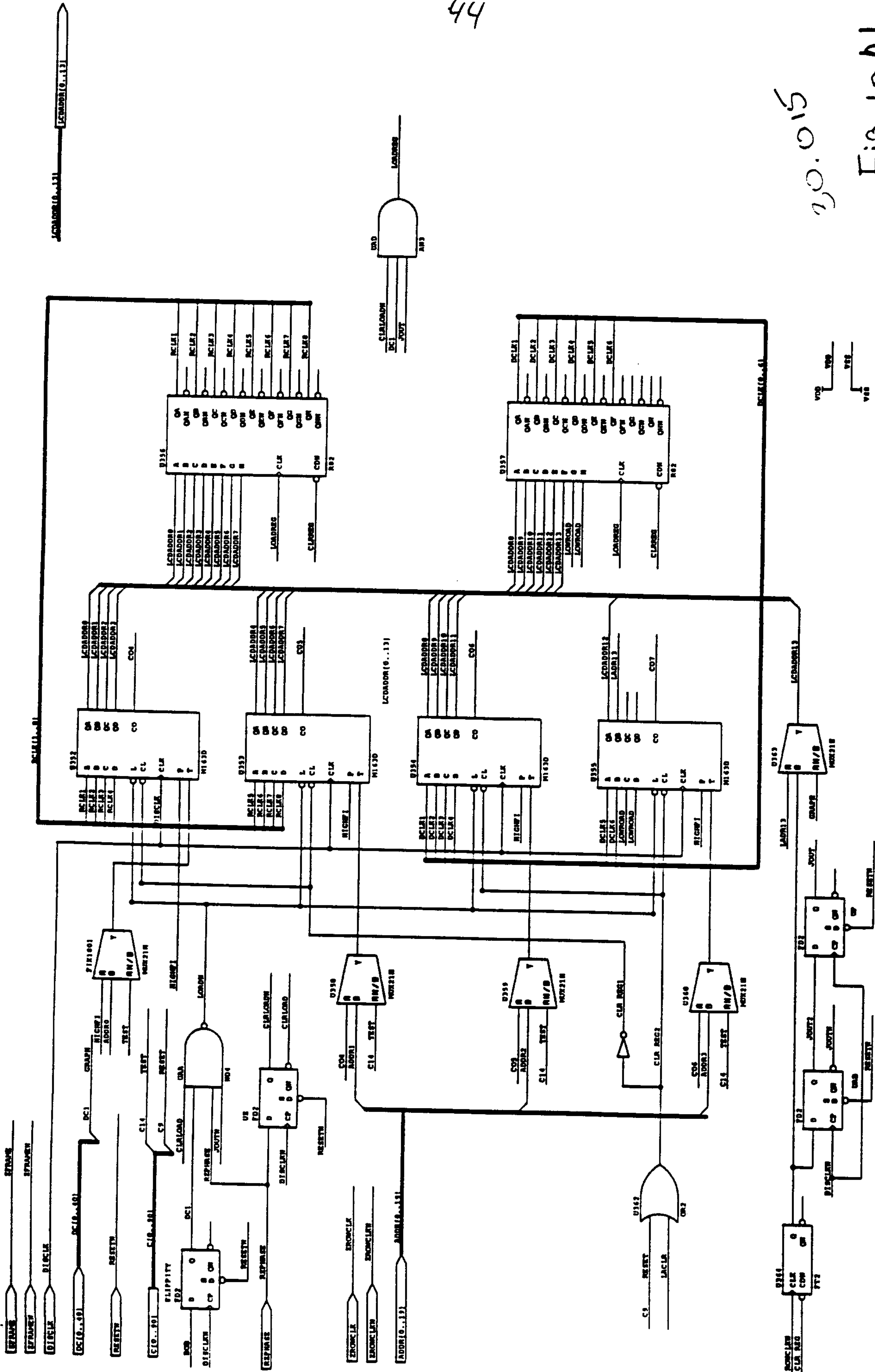
30.010
Fig. 10A9

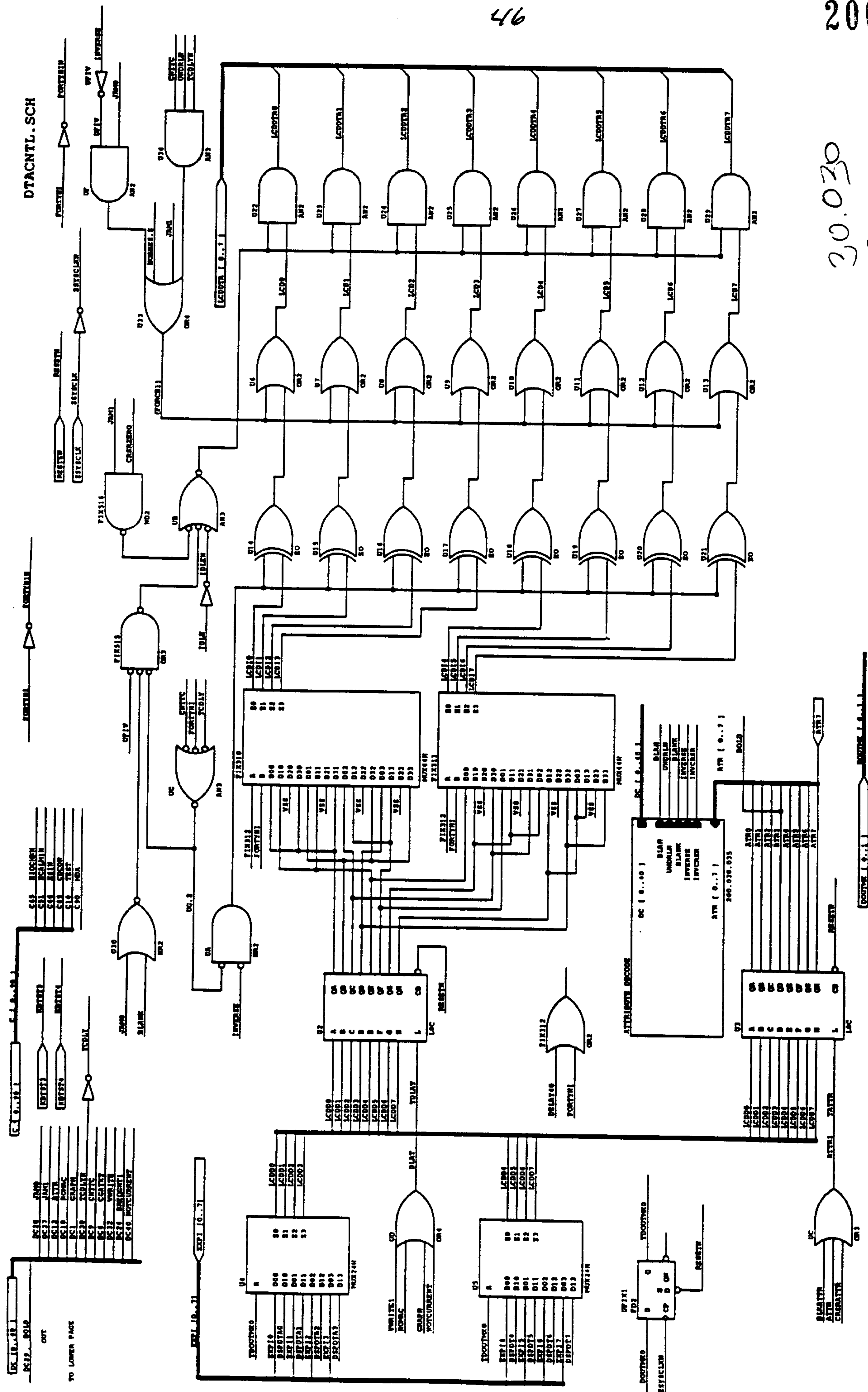
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44

20.015

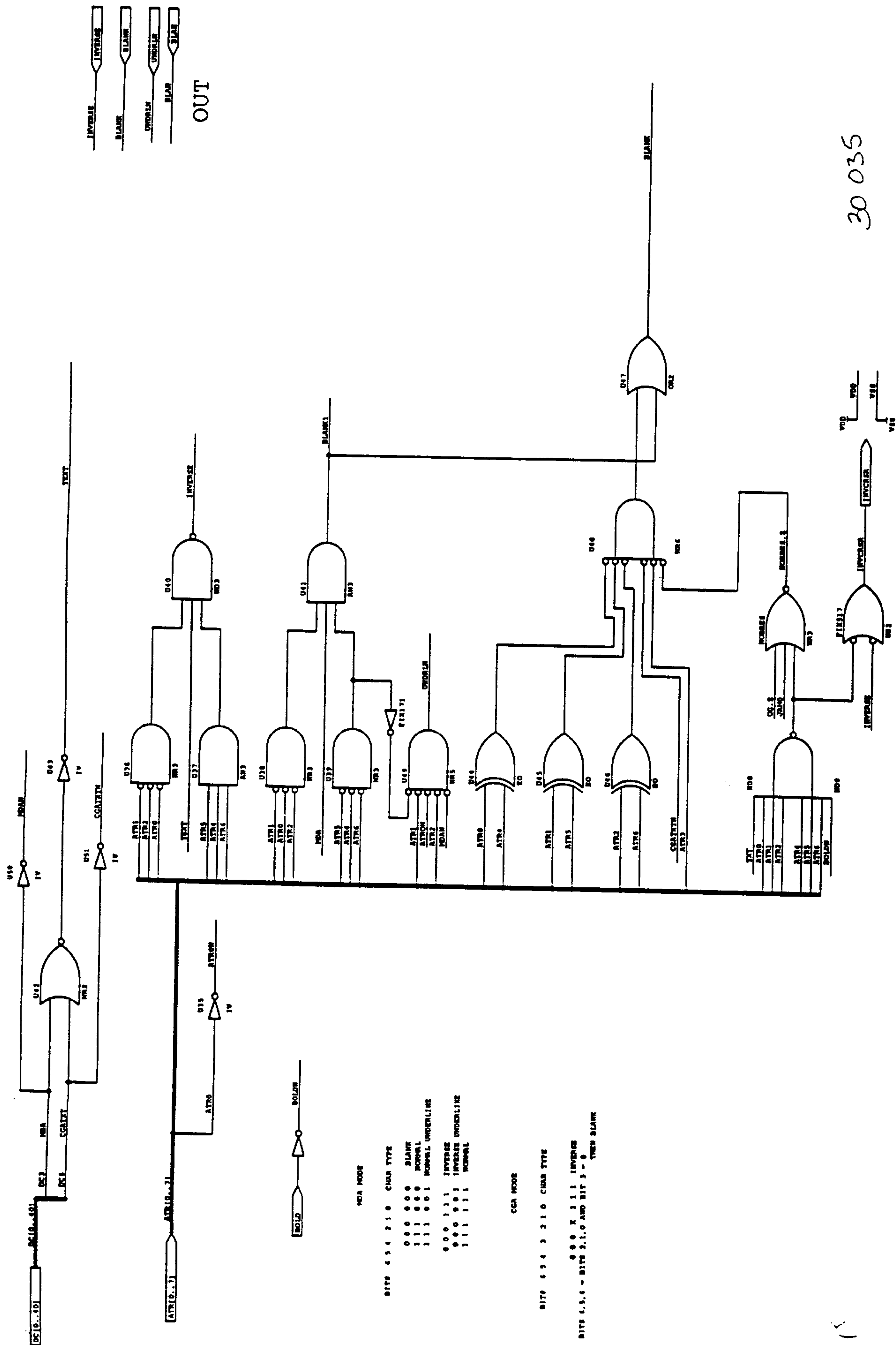
Fig. 10A

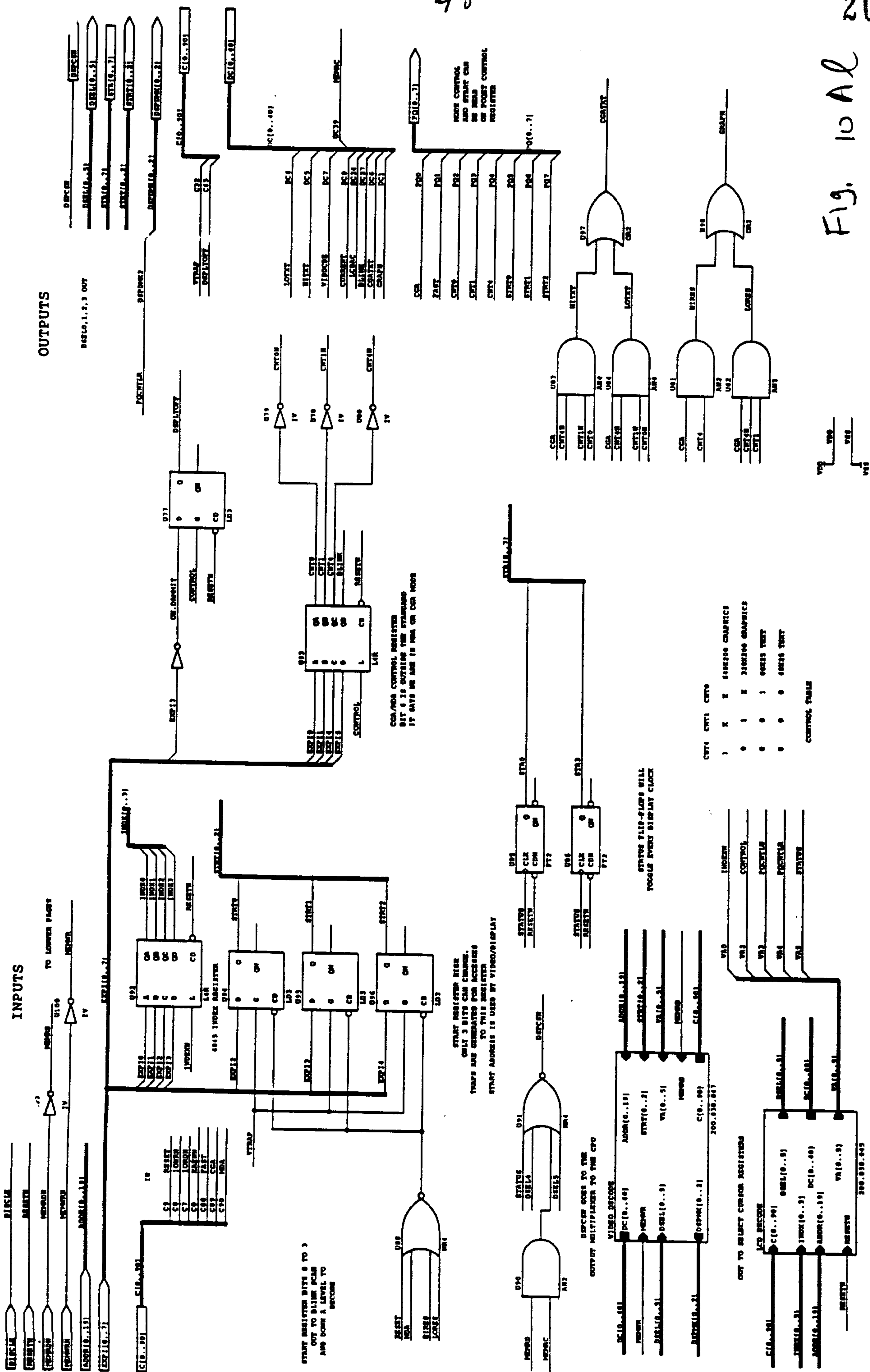




47

30 035
-19.10 AK

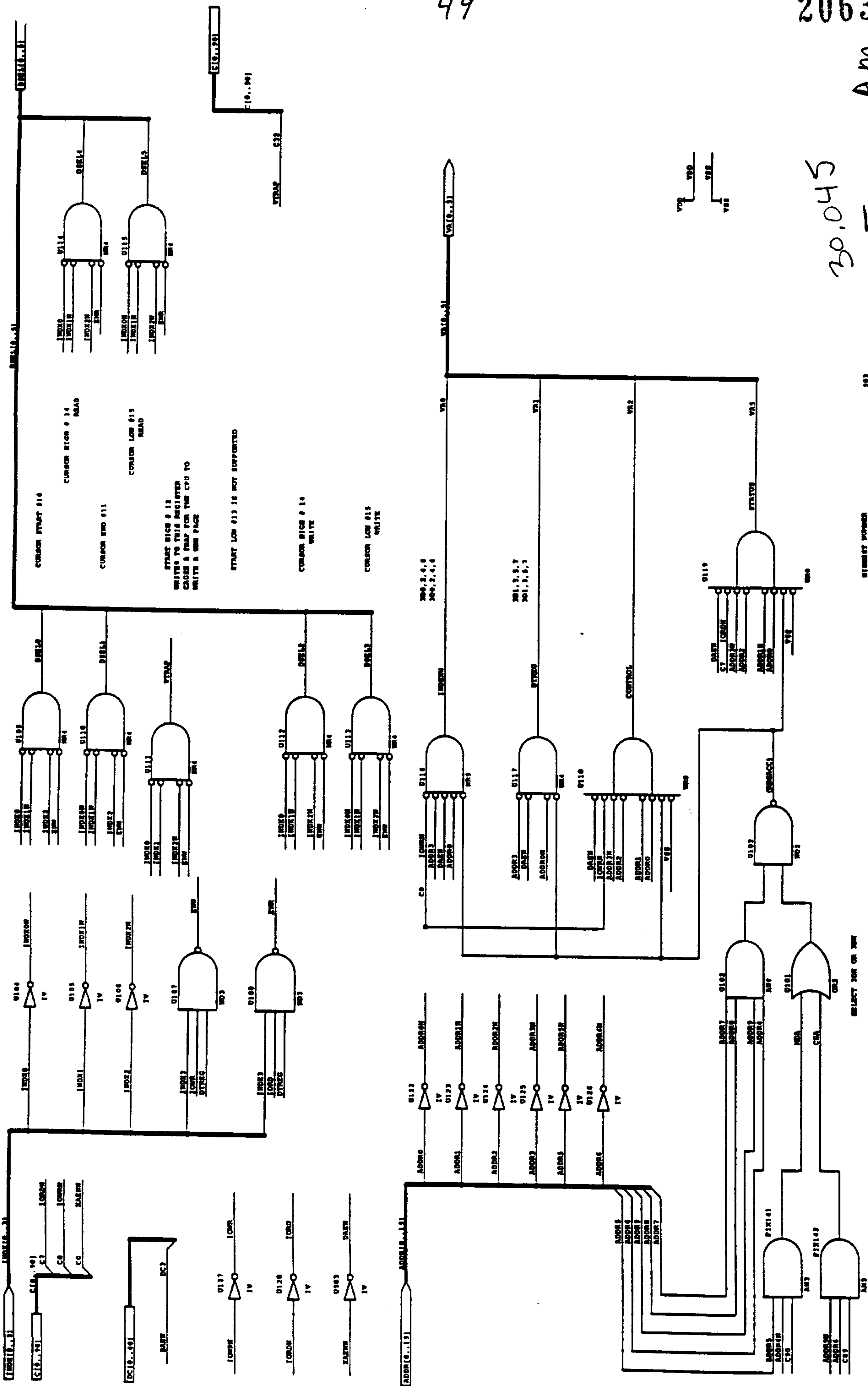




49

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30.045
Fig. 10 Am

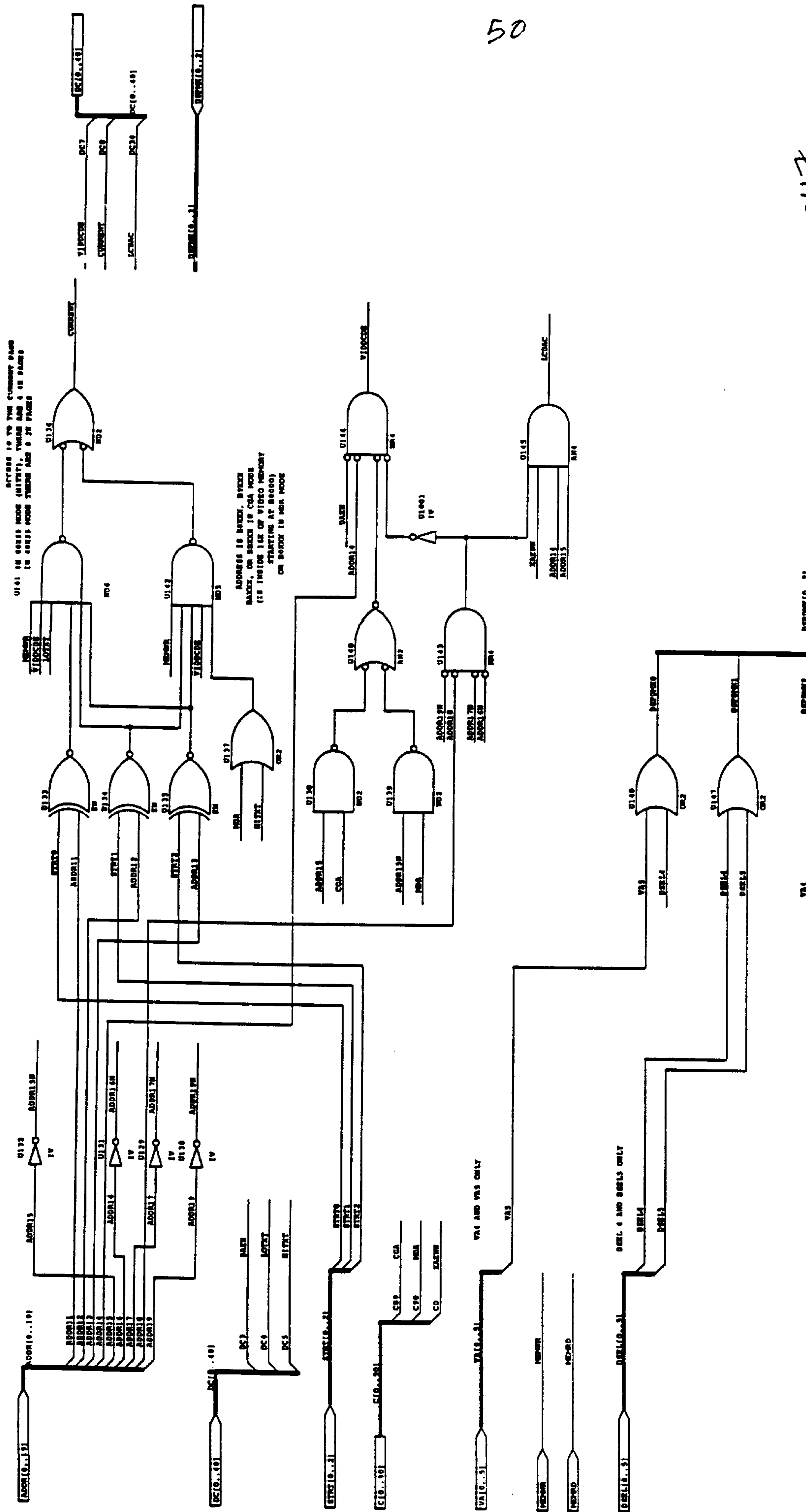


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50

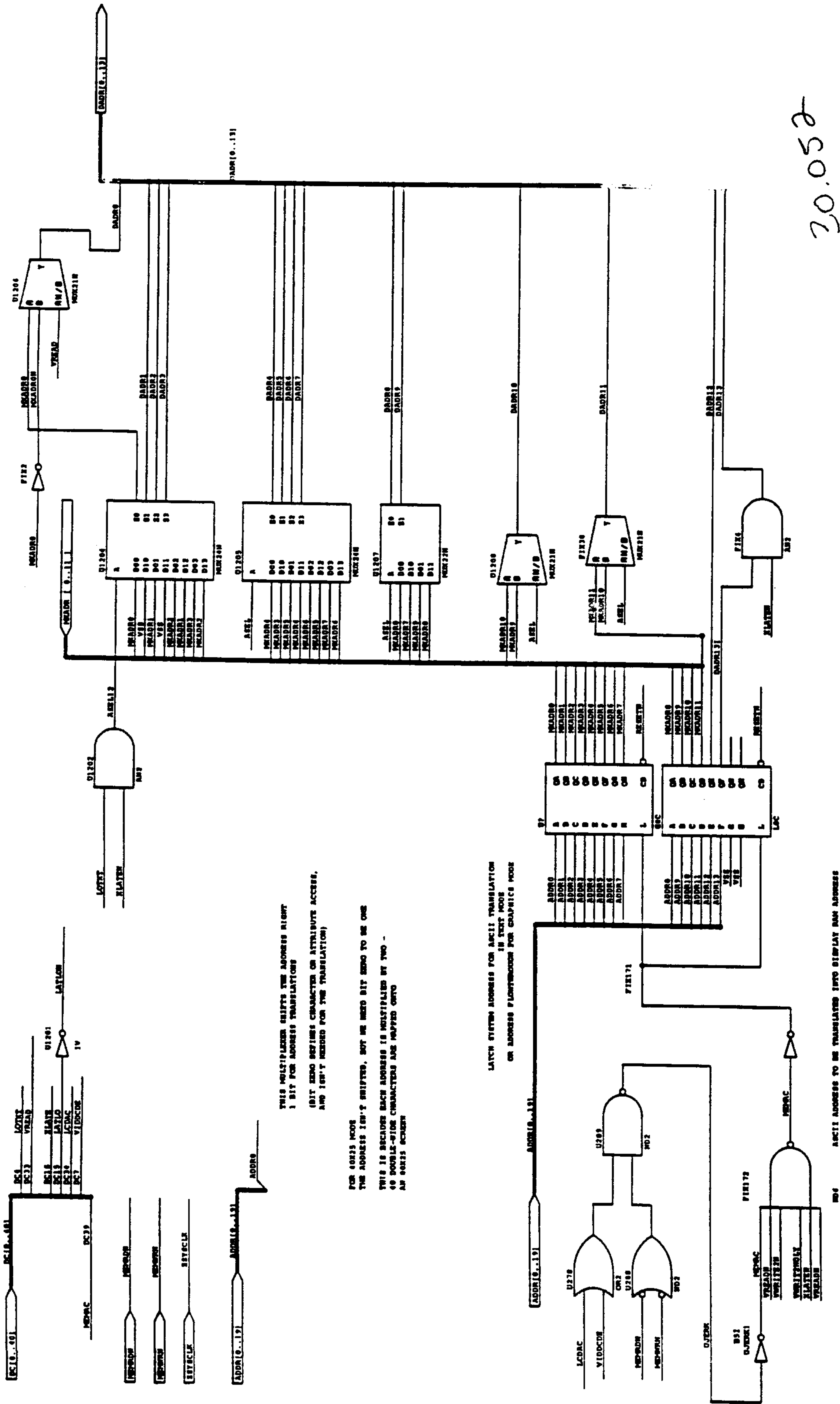
30,047

Fig. 10 Ah



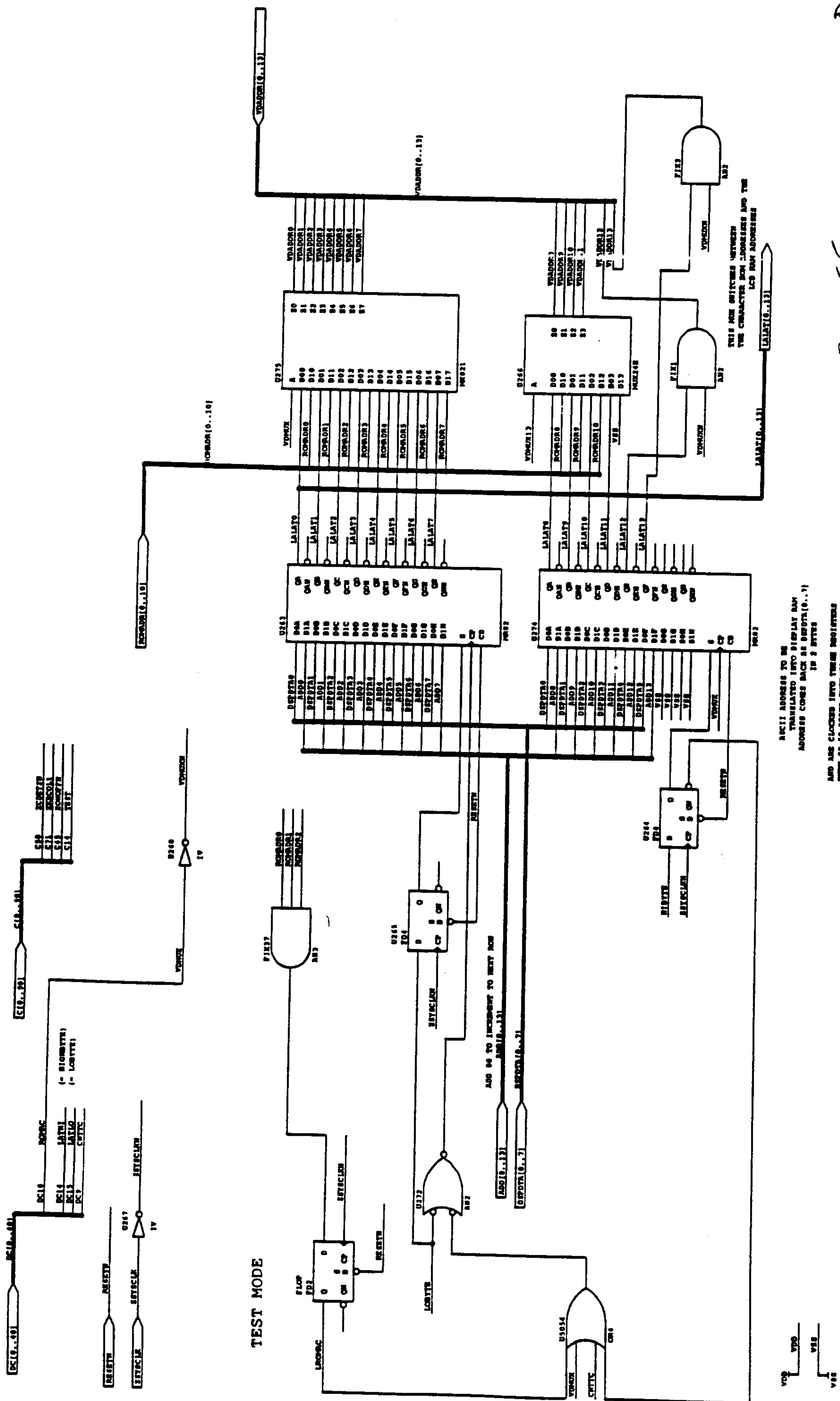
STONEST WORKS 1001

30.052
Fig. 10 AP



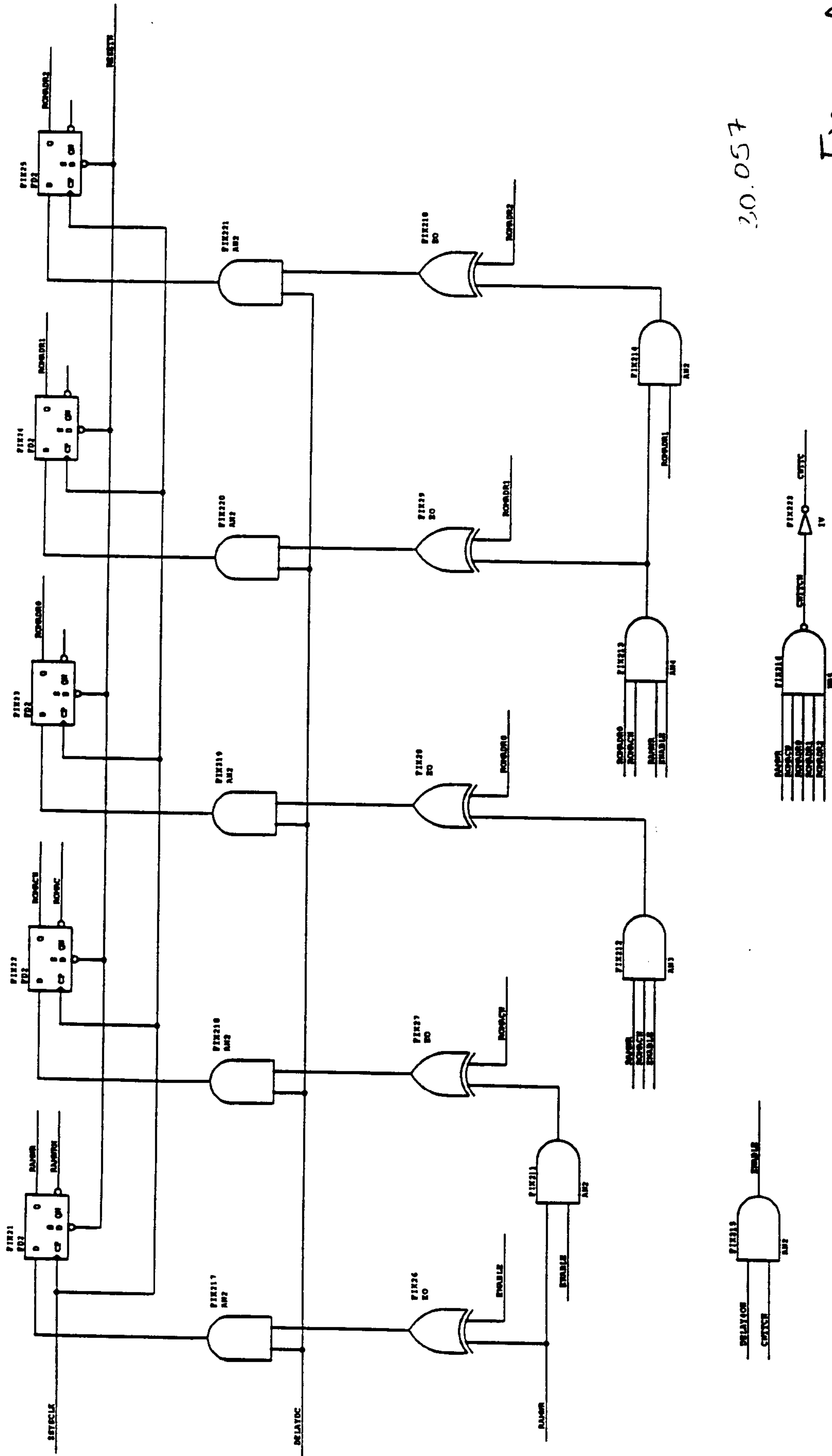
30.055

Fig. 10 AgB



30.057

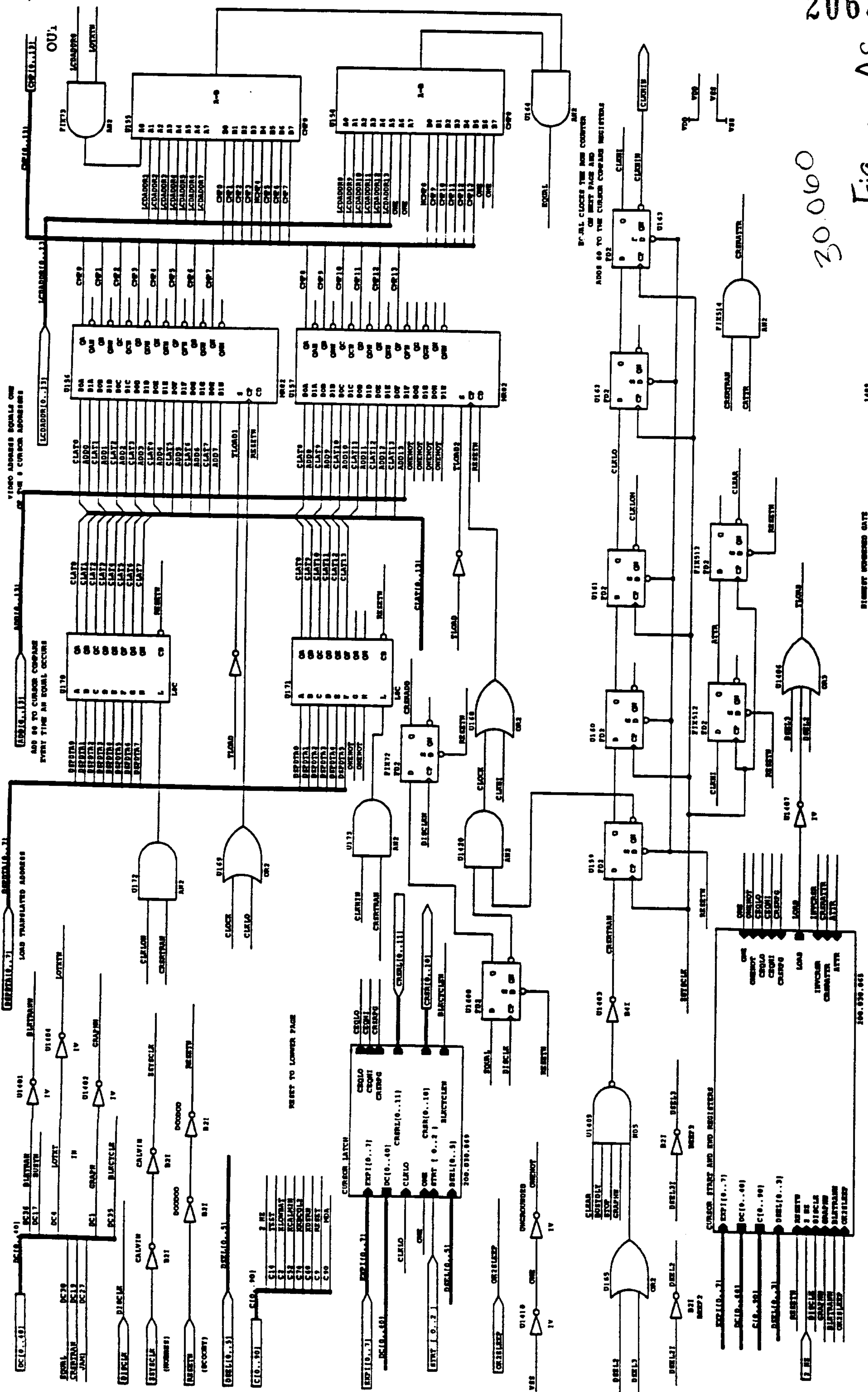
Fig. 10 Ar



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Fig. 10 AS

300600



SHOWN IN FIG. 10 AS

200,000,000

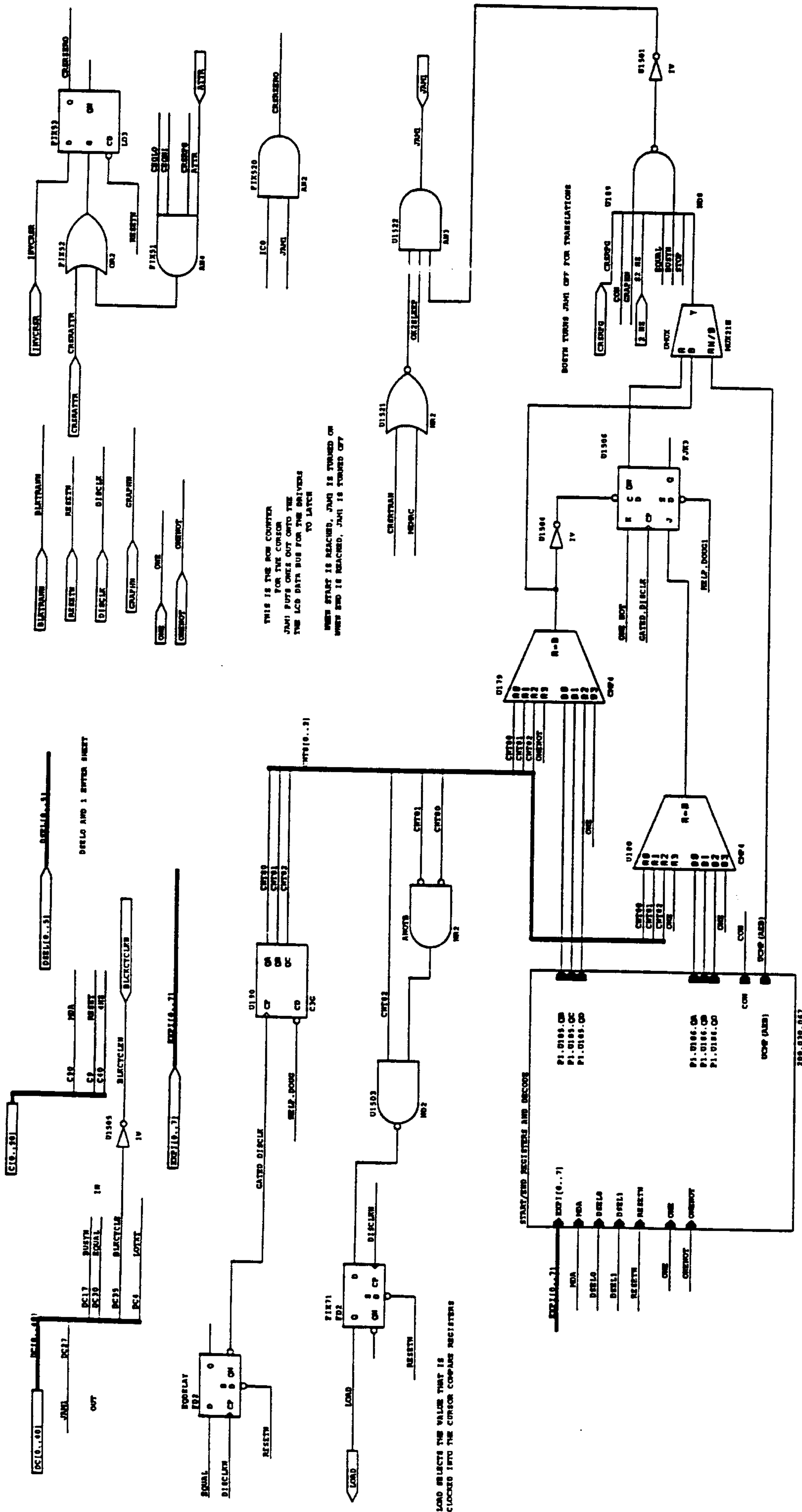
30.005

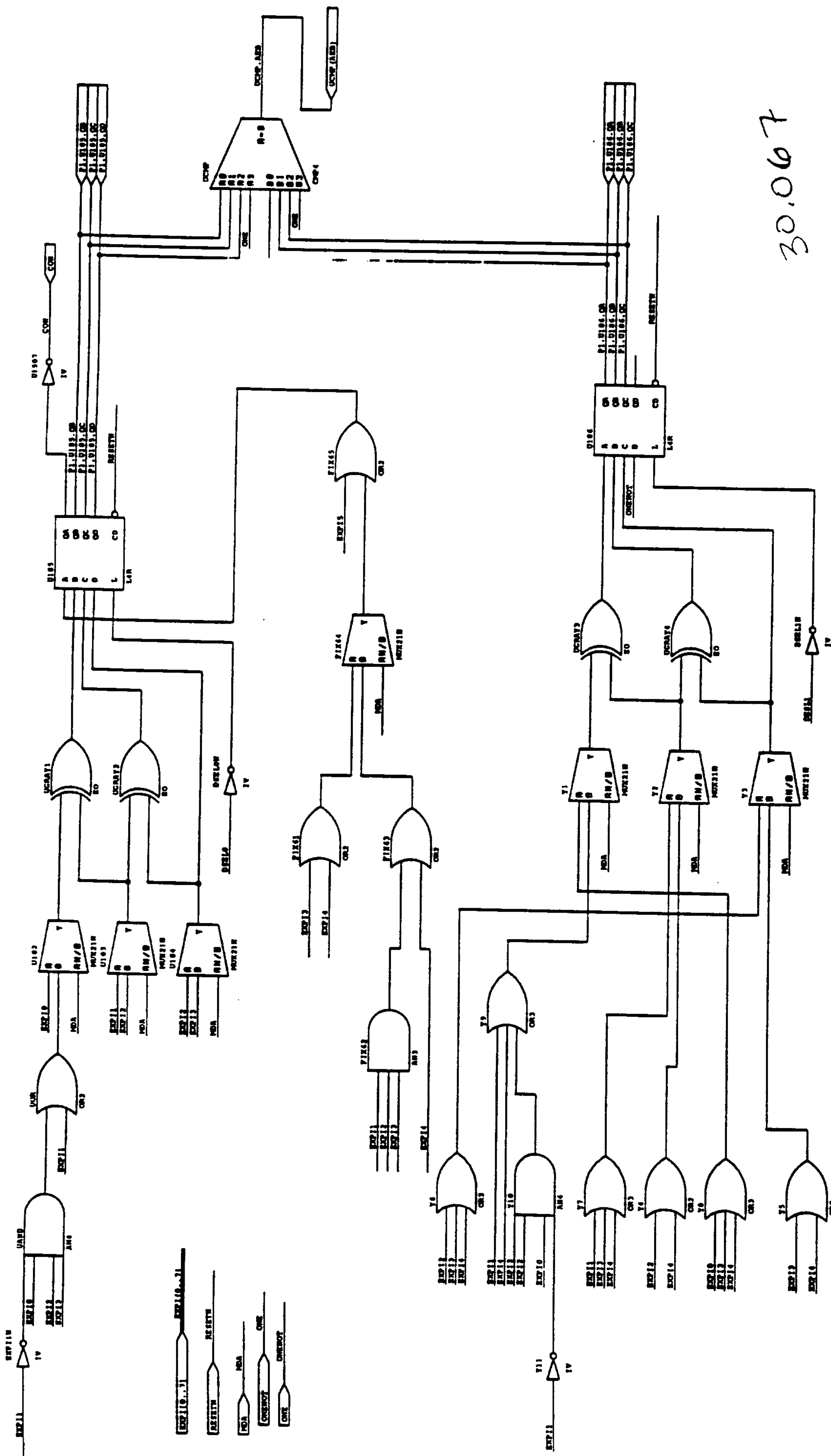
Fig. 10 At

1507

DIAGRAM NUMBER DATE

VDD
VSS





30.067

2063558

30.069

Fig. 10 AV

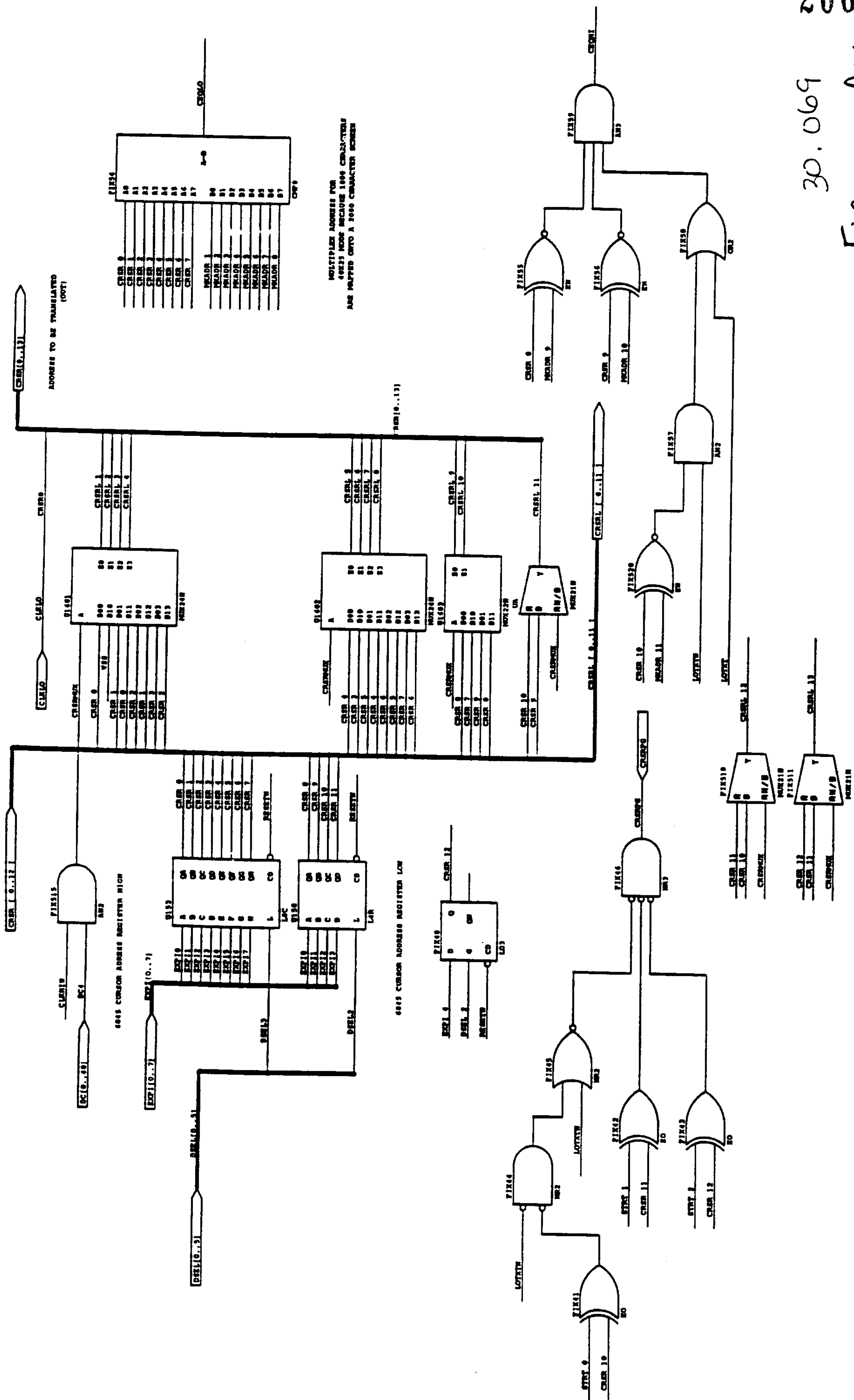
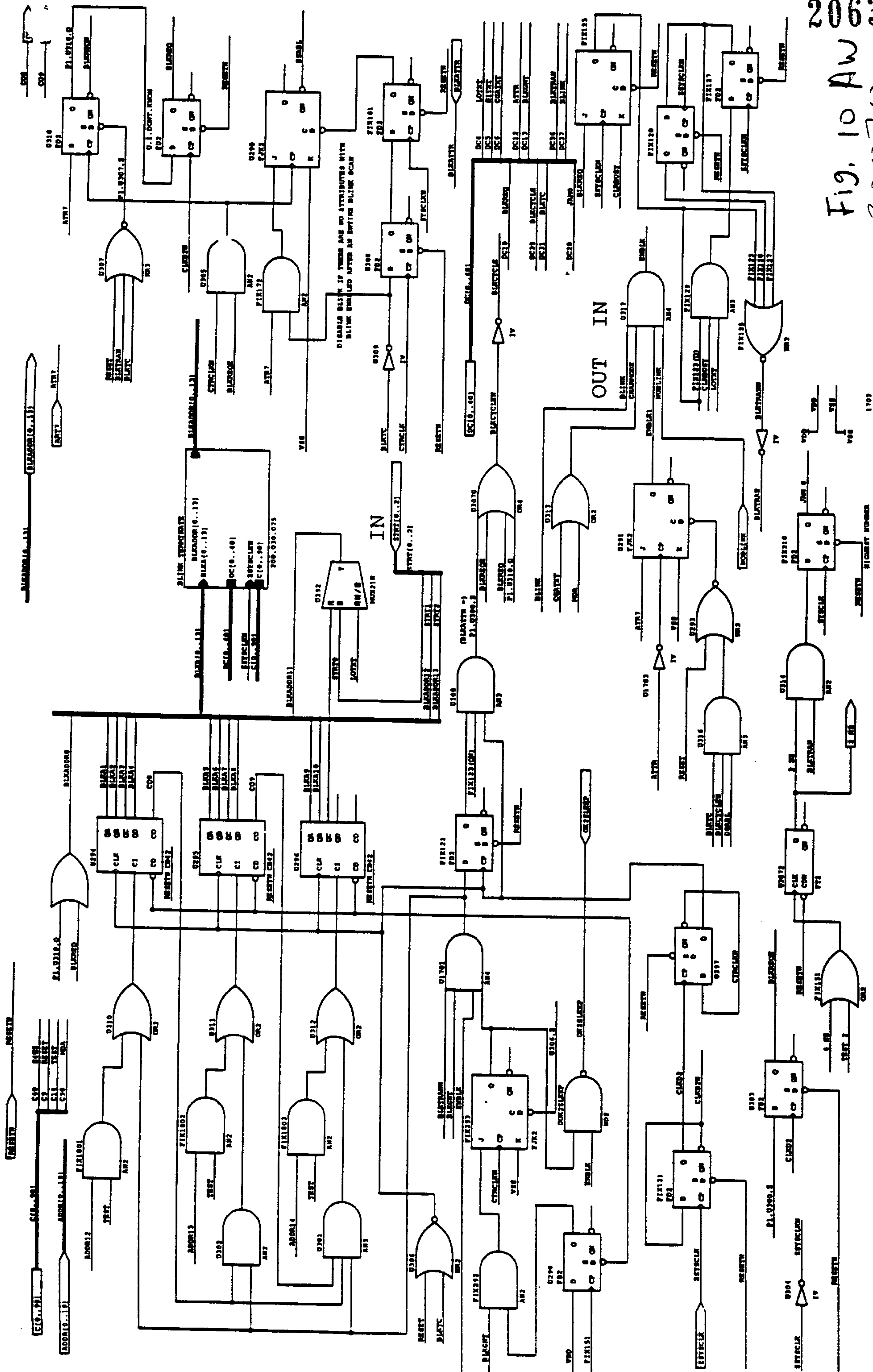
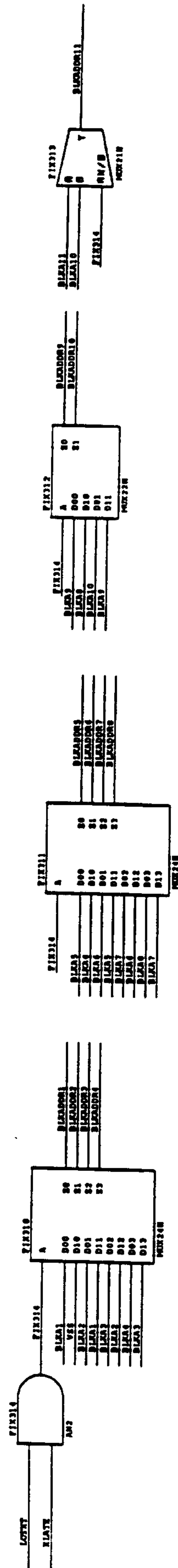


Fig. 10 Aw
20,070





SECRET FRODOEN

30.075

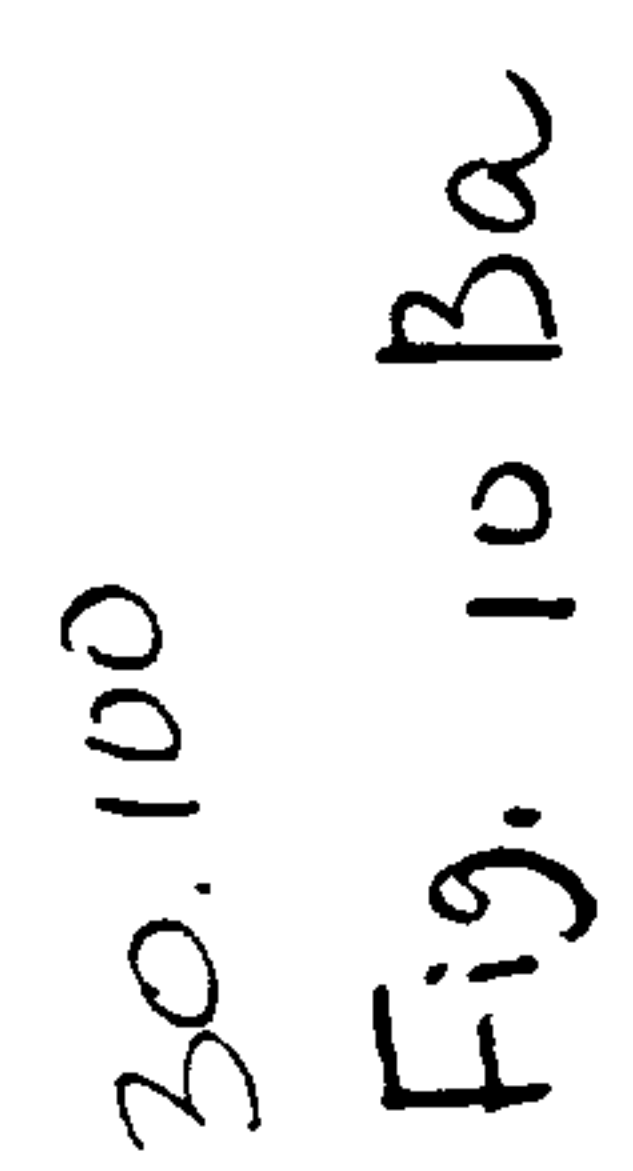


Fig. 10 Ba

30.105

Fig. 10Bb

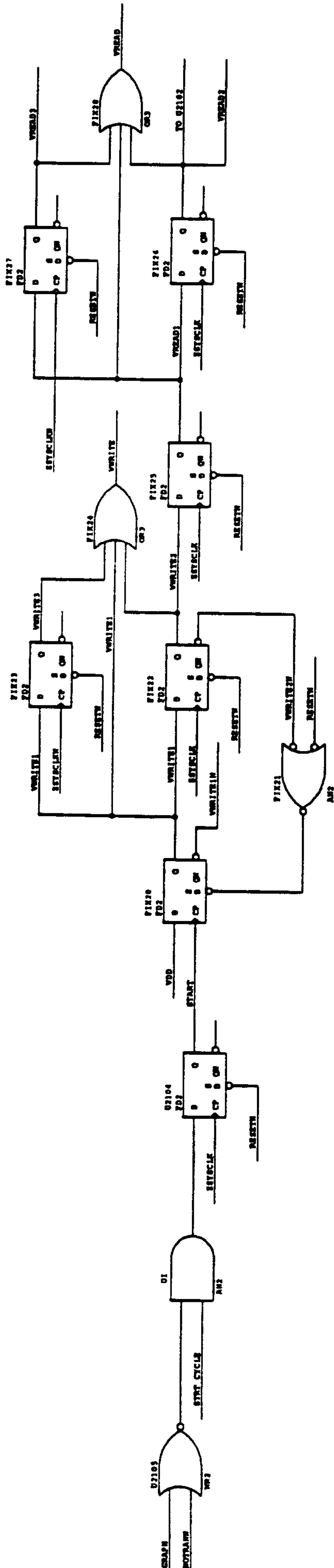
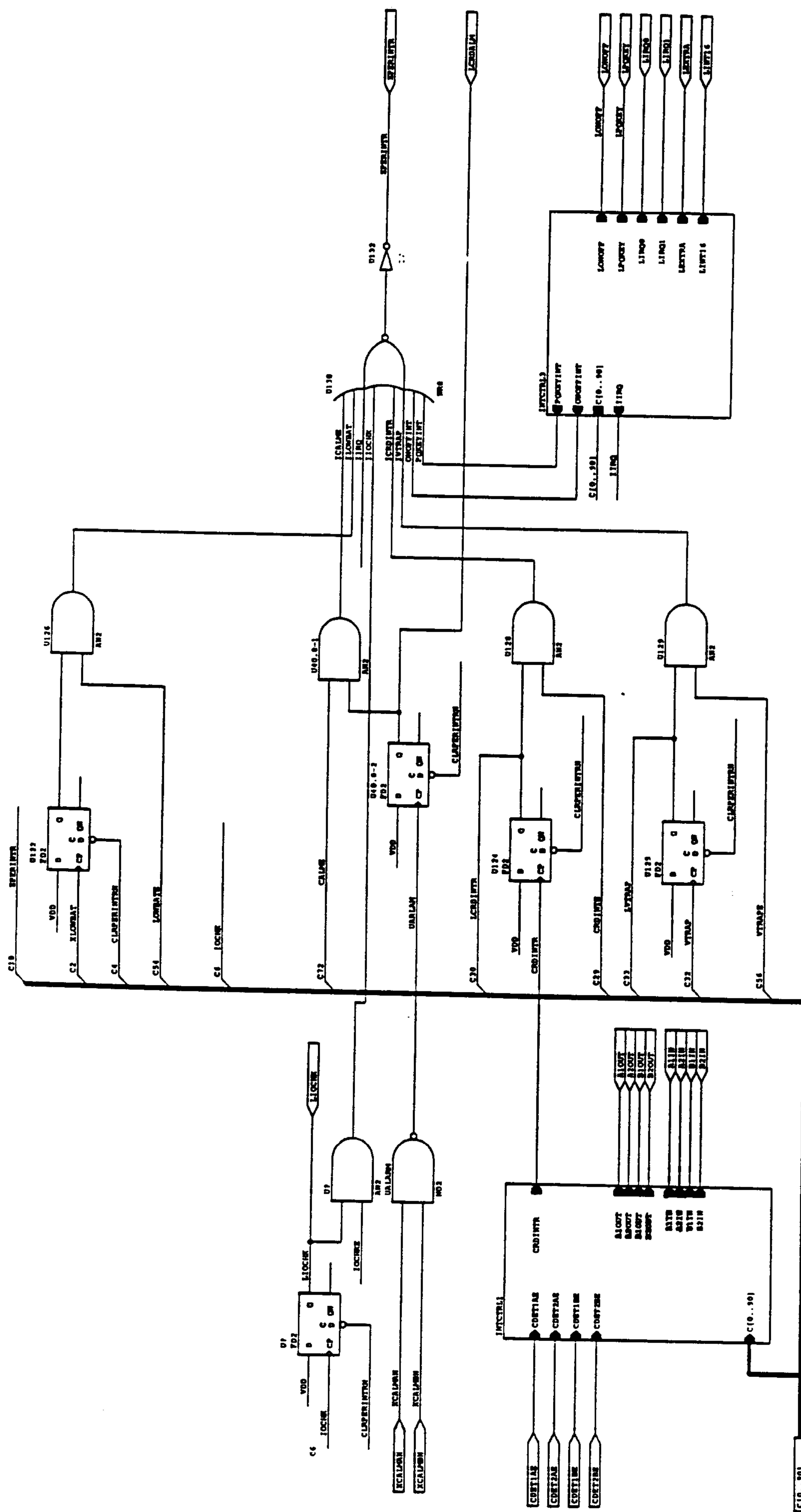




Fig. 10 BC

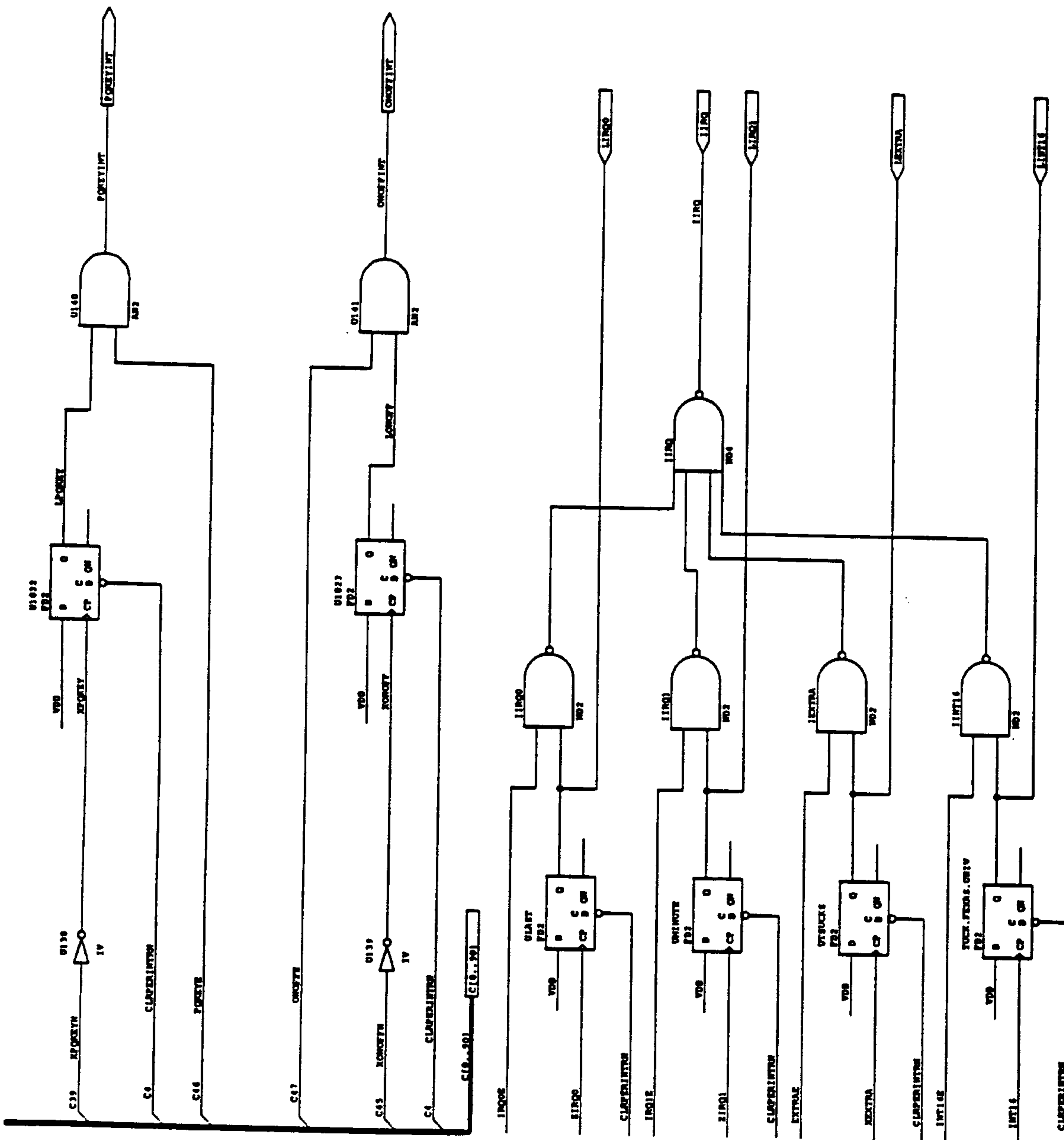
2063558

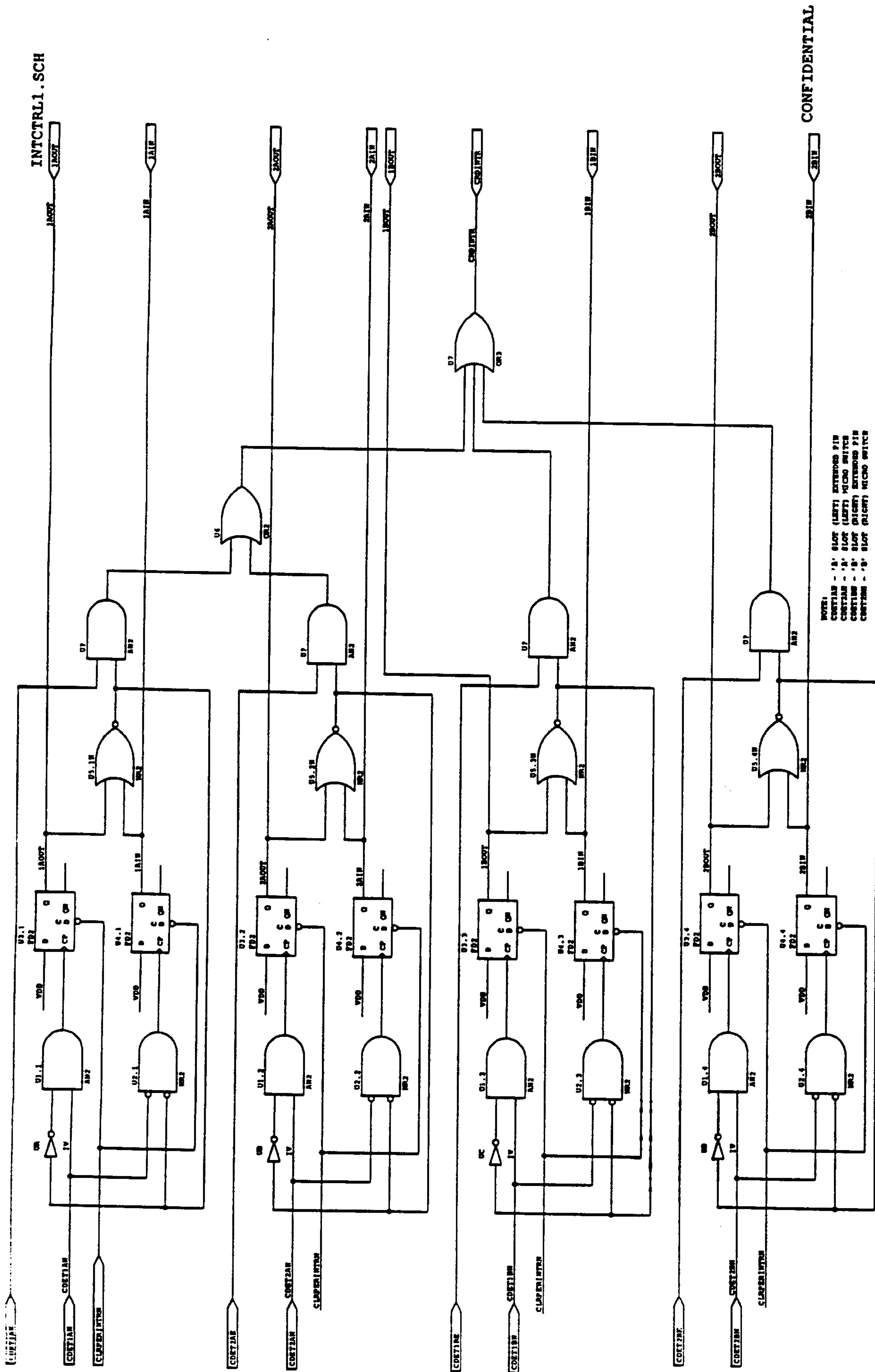
Fig. 10 Be 4ϕ . $\phi_{1\phi}$



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4φ.φ2φ
Fig. 10 Bf





NOTE:
 'A' SLOT (LEFT) EXTENDED PIN
 'B' SLOT (LEFT) MICRO SWITCH
 'C' SLOT (RIGHT) EXTENDED PIN
 'D' SLOT (RIGHT) MICRO SWITCH
 ALL SIGNALS NEGATIVE TRUE, PULSED UP

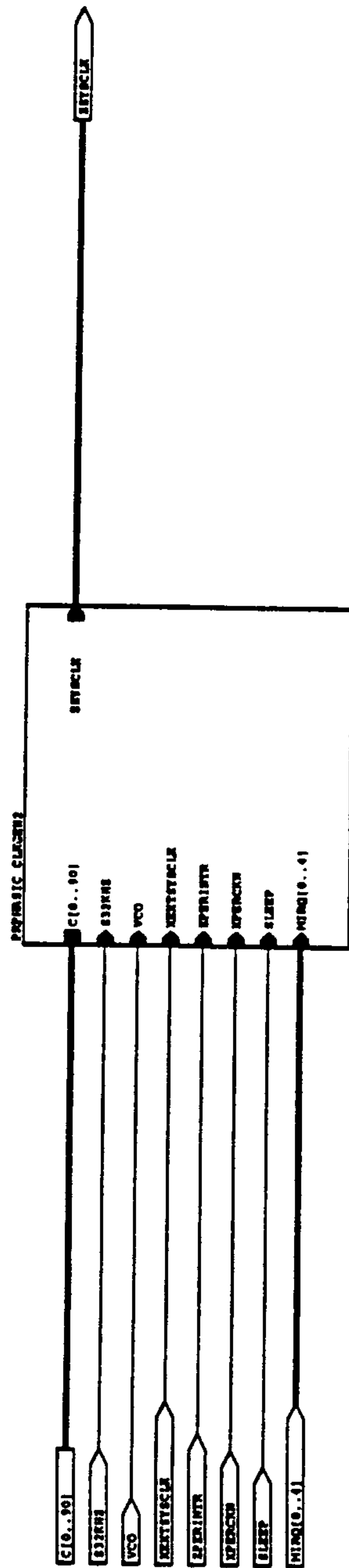
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40.0338
 Fig. 10B9

70

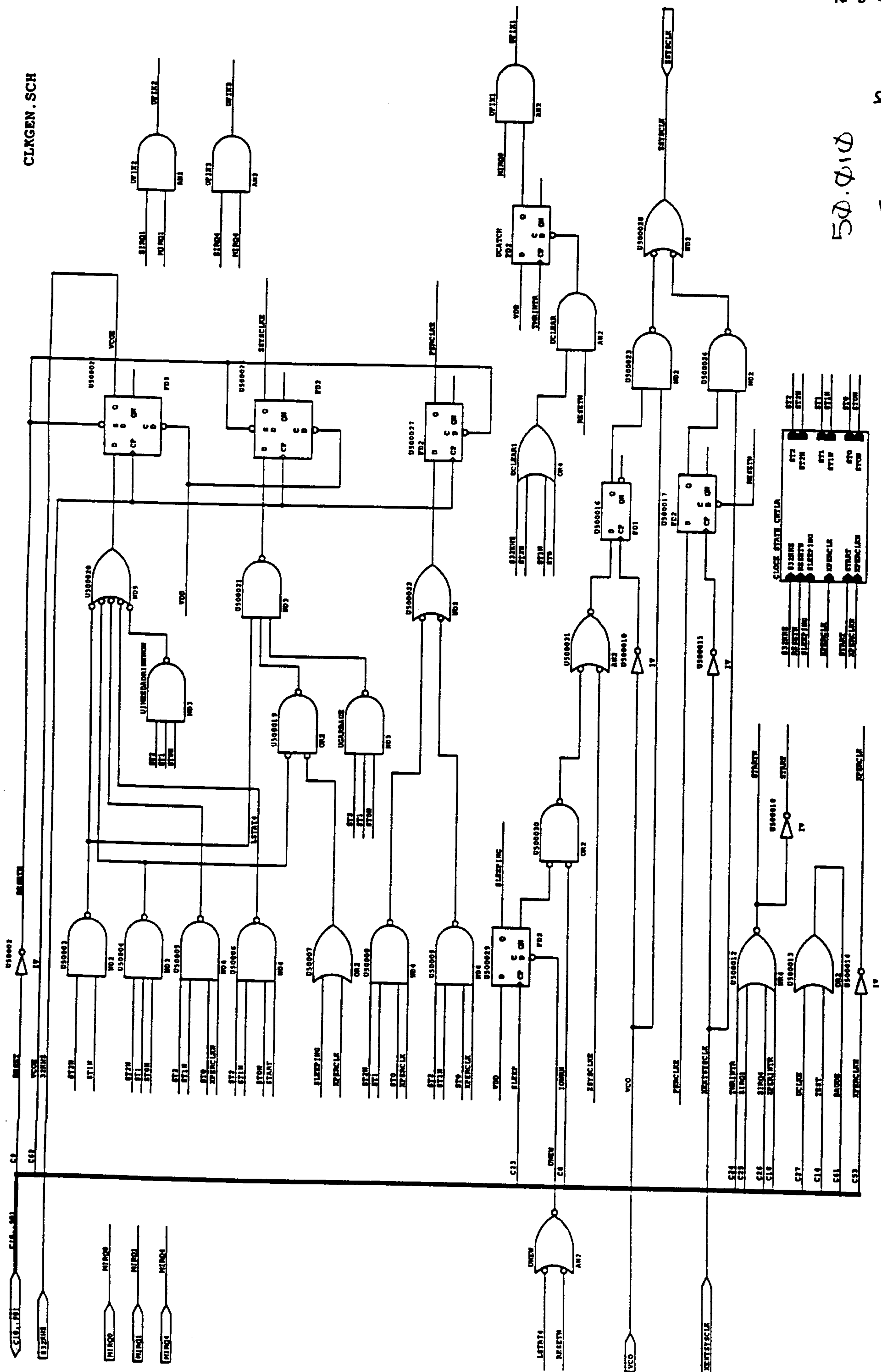
ΦΦΦ50

Fig. 10 Bh



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50.010
Fig. 10 Bi

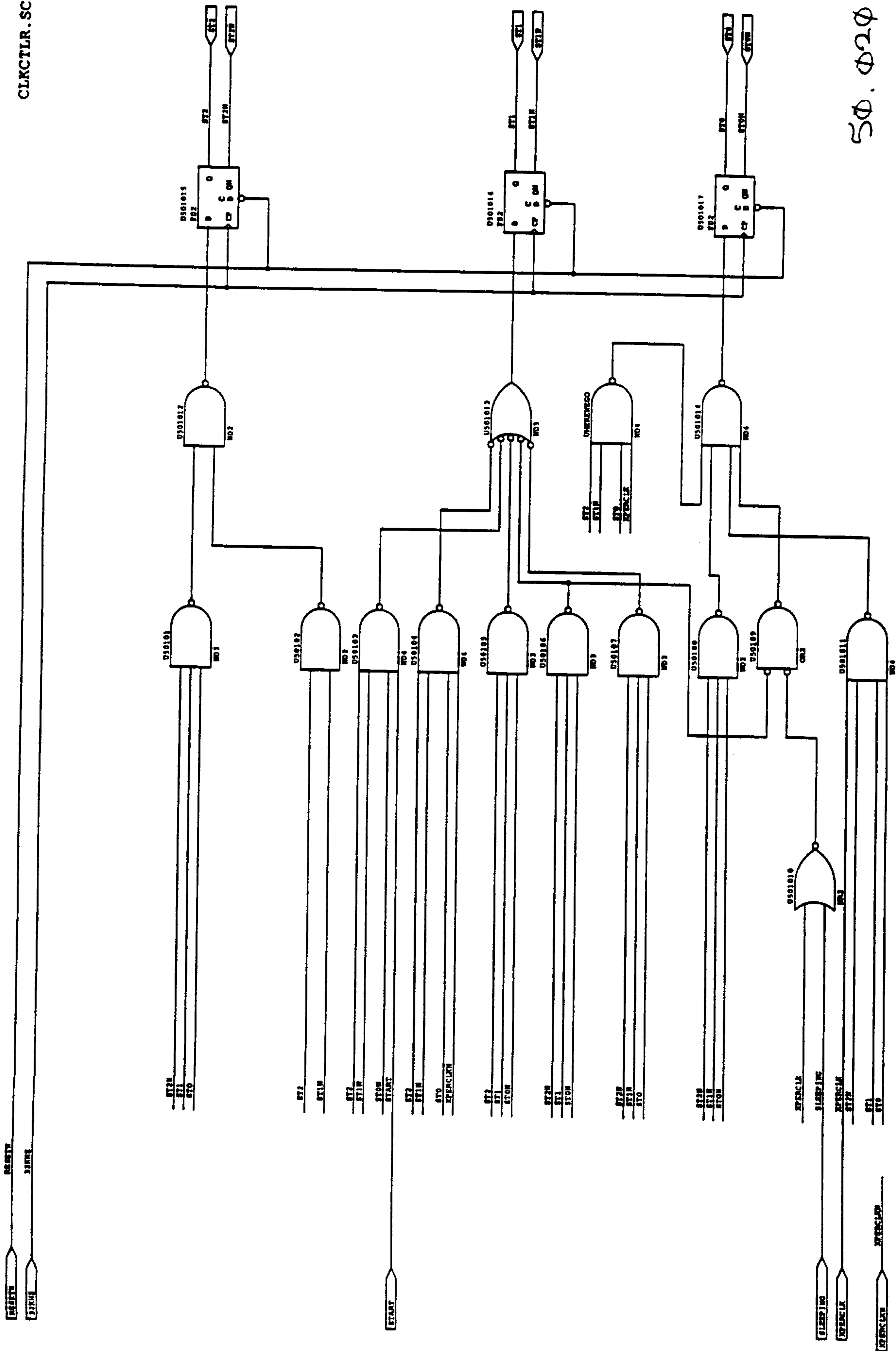


72

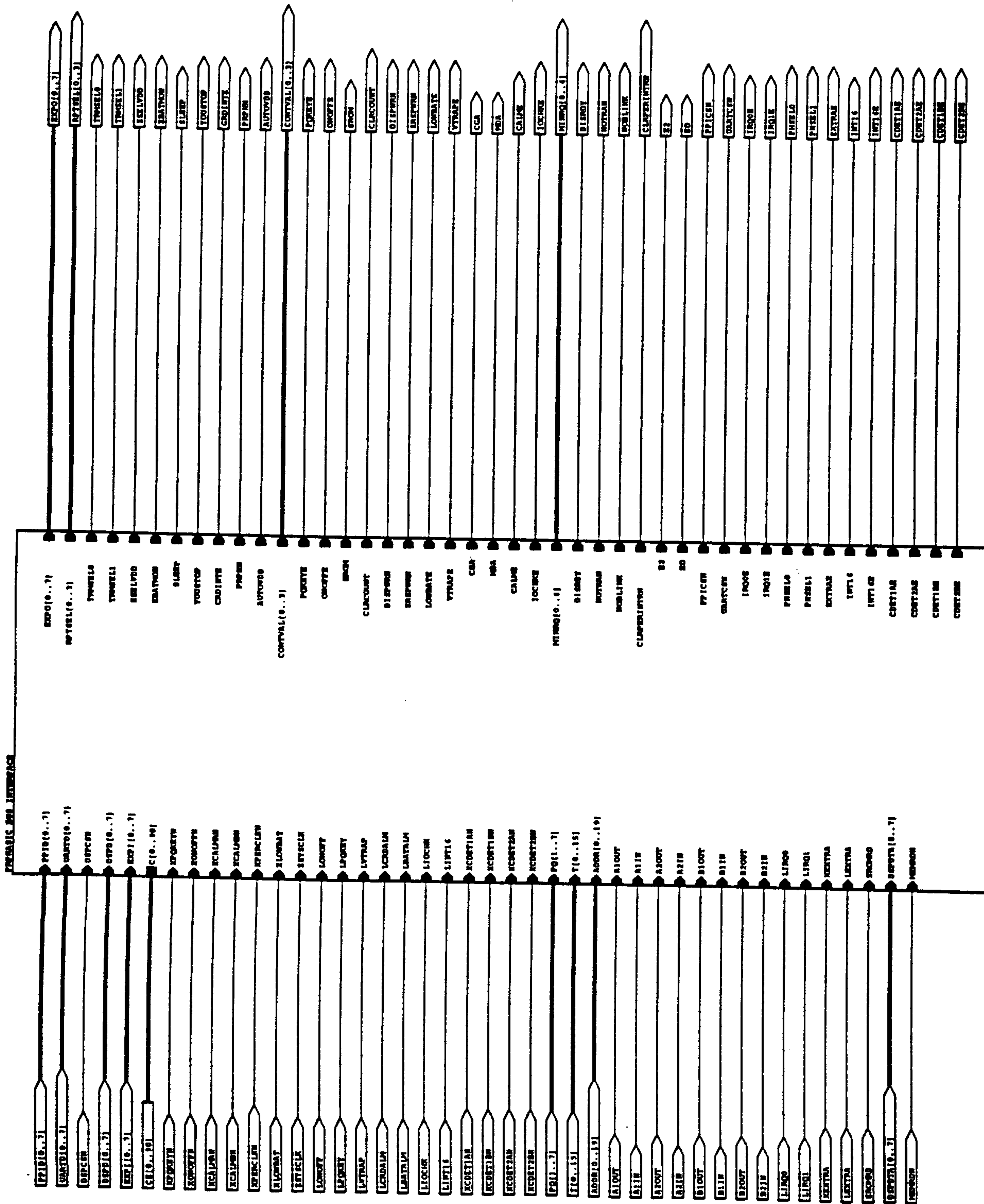
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CLKCTLR.SCH

50.020
Fig. 10 Bj



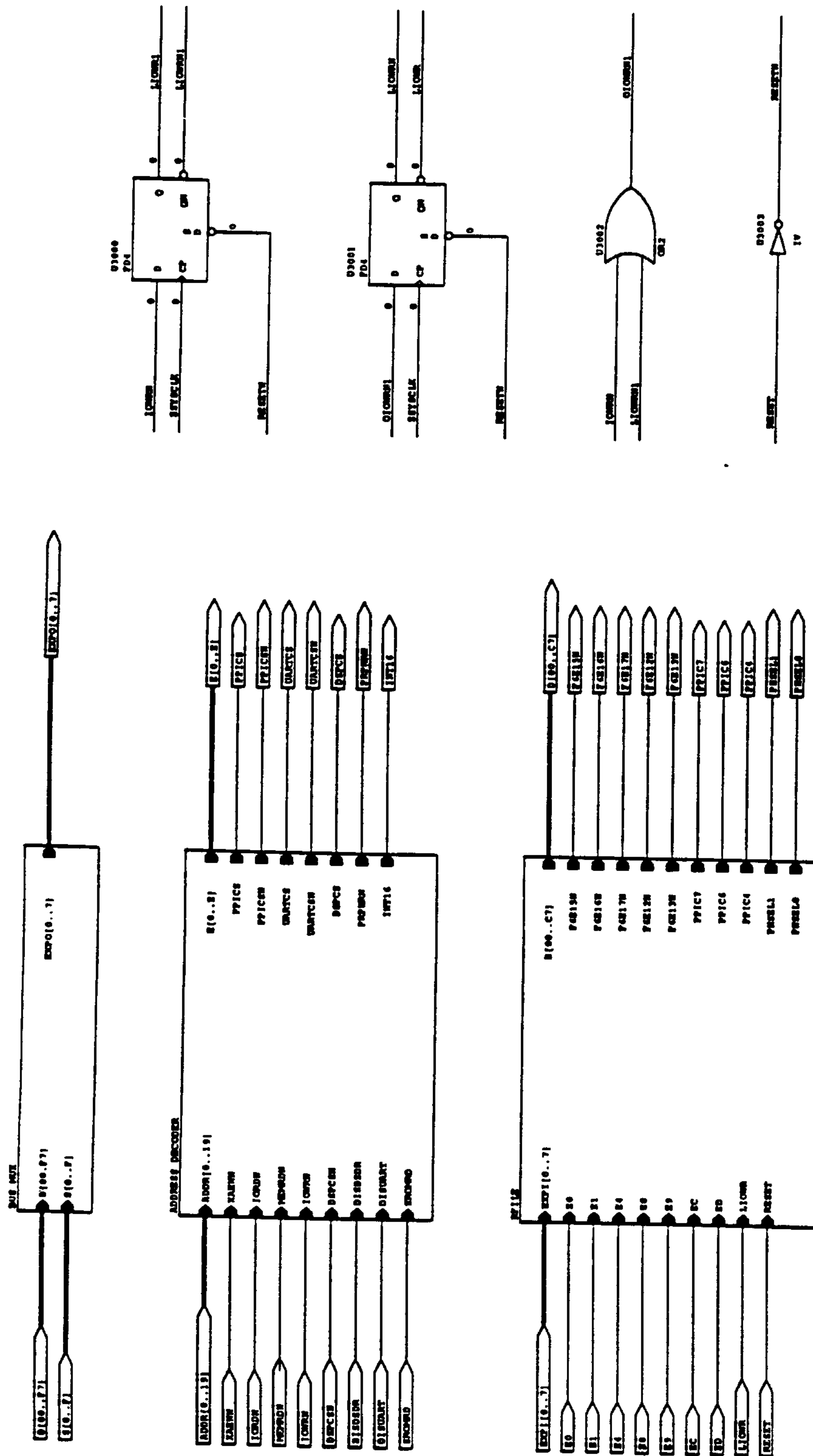
ΦΦ-ΦΦΦ
Fig. 10 BK



74

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60. 010
Fig 10 Bl



74

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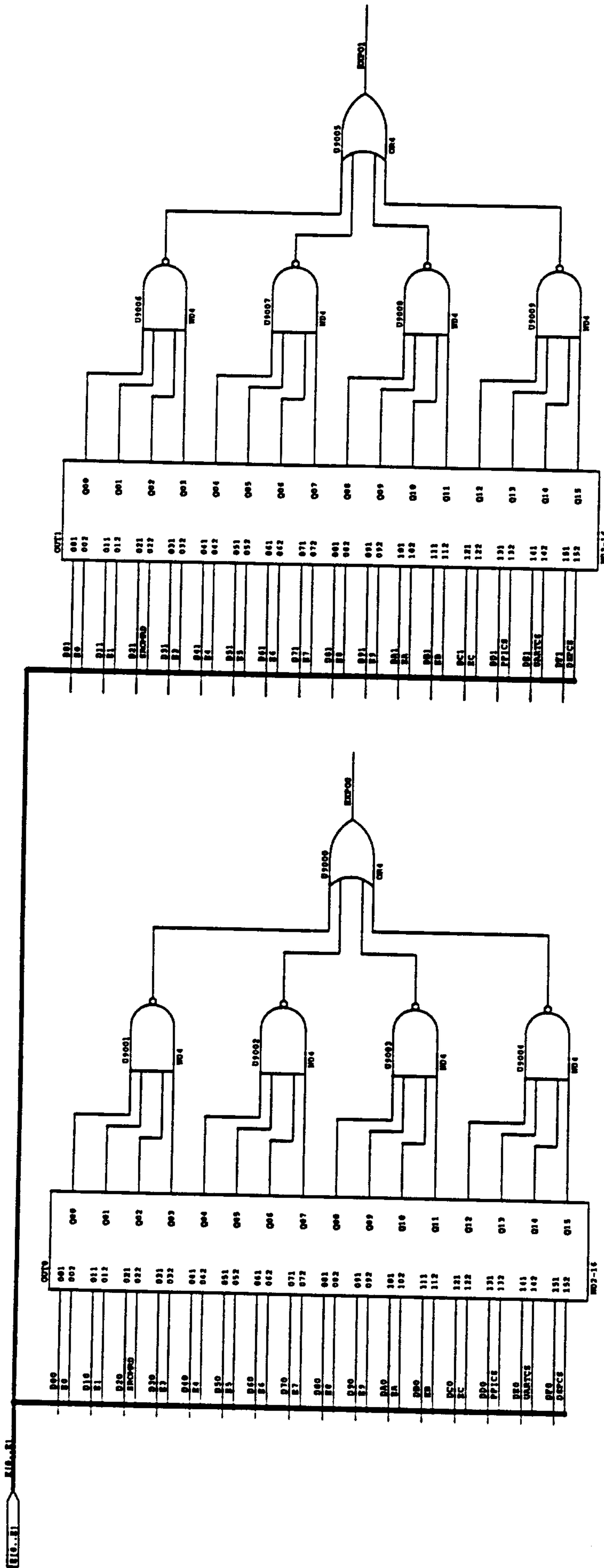
60. 010
Fig 10 Bl

OUTMX1.SCH

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60.020

Fig 10 Bm



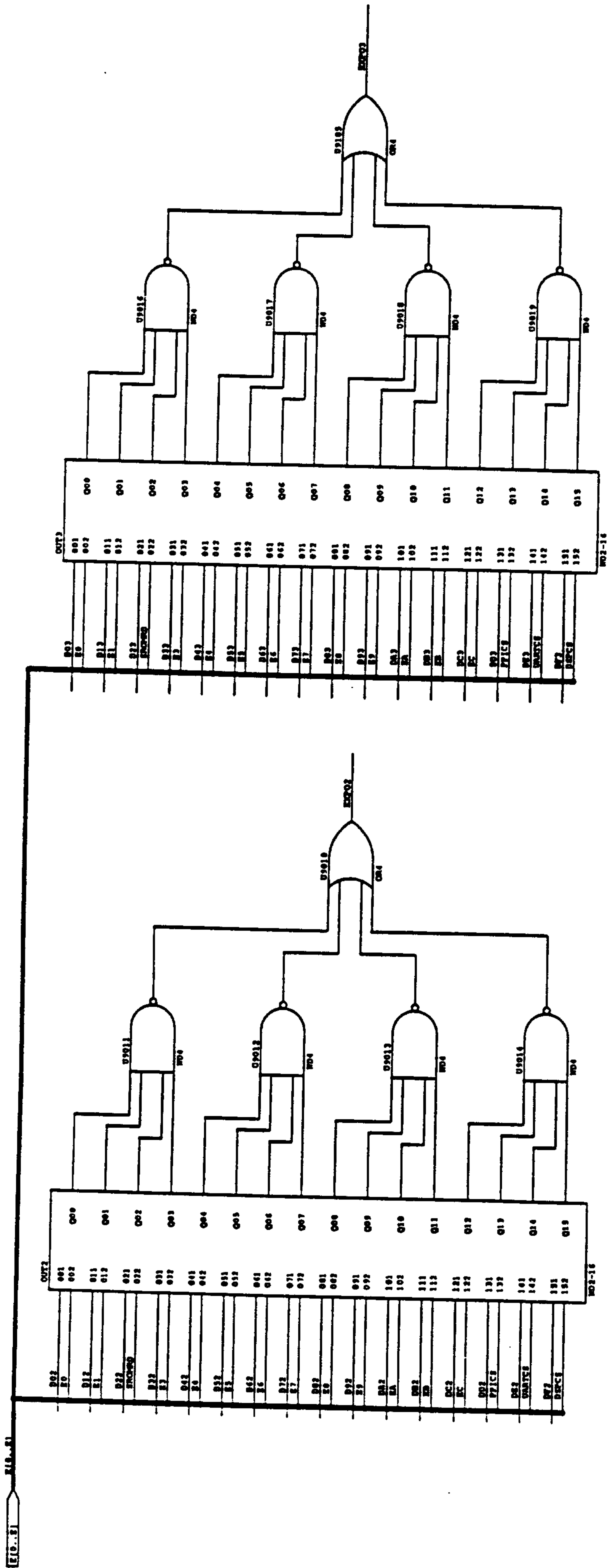
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Fig. 10 Bm

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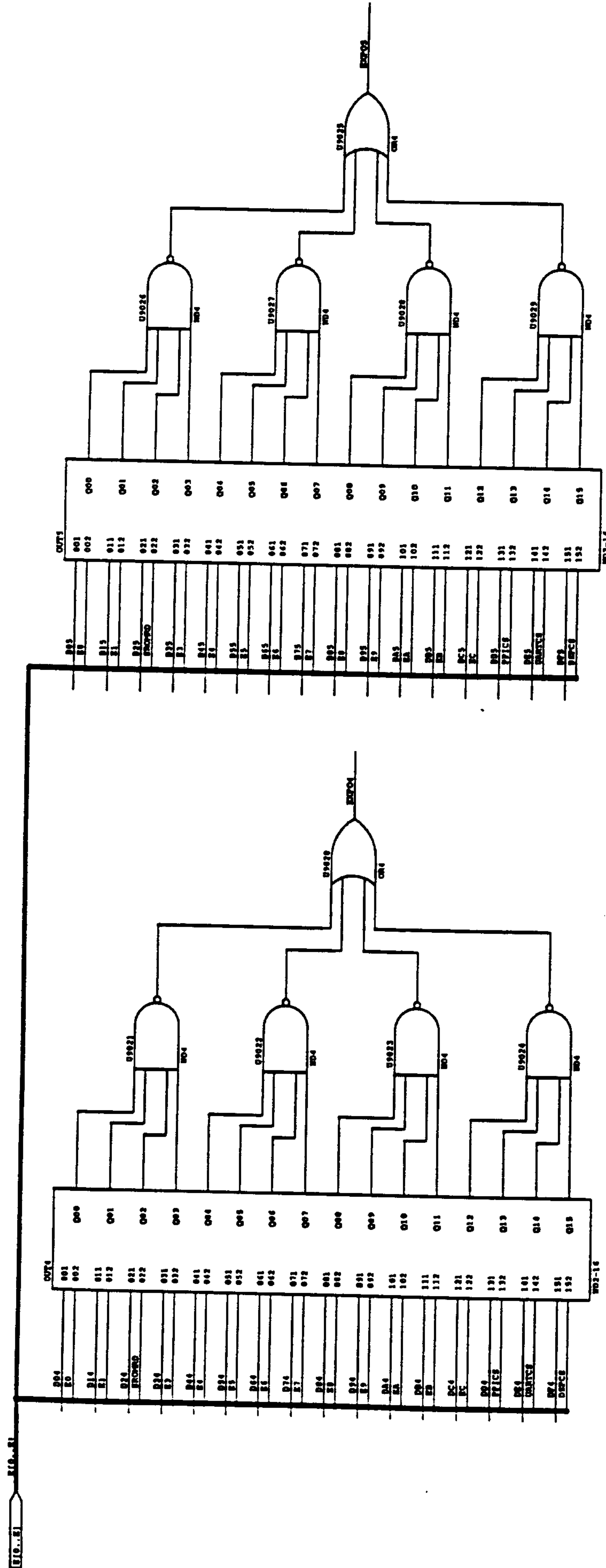
60.030

OUTMUX2.SCH



OUTMX3.SCH

PROCESS
RELIEF
UNITS
DEPCB



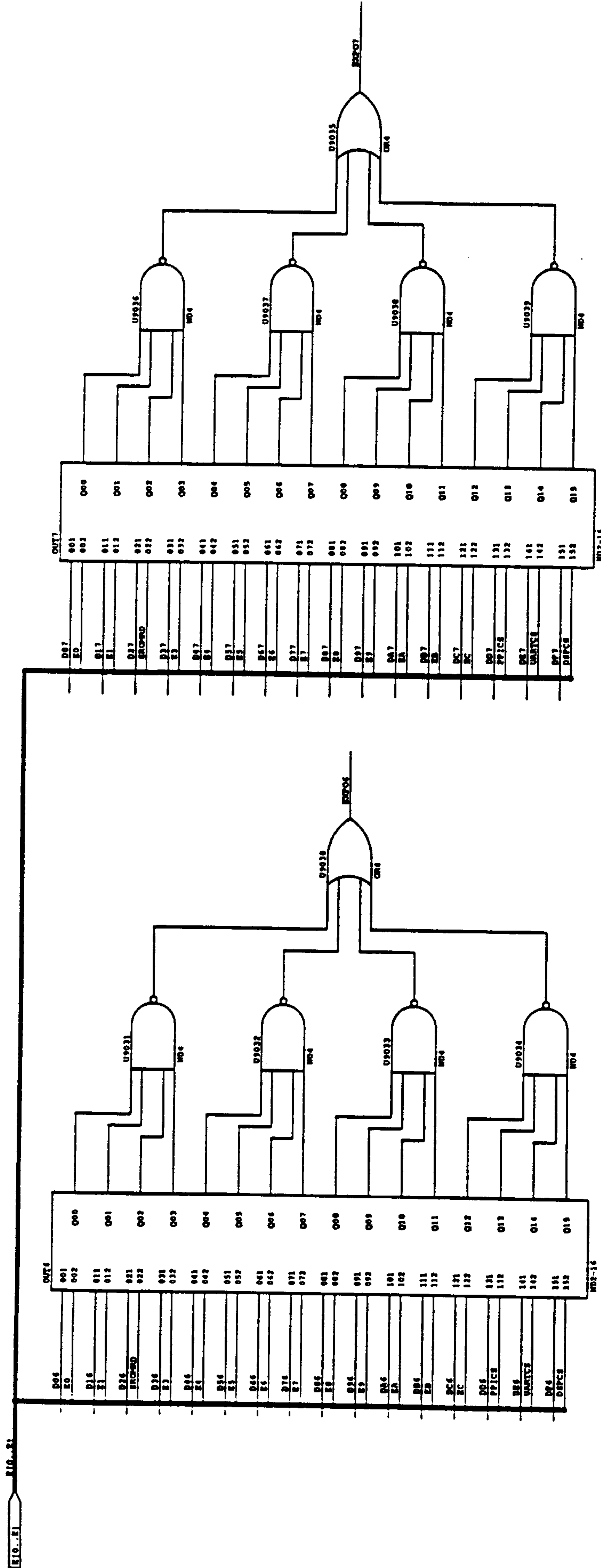
CONFIDENTIAL

68.040

Fig. 10

OUTMX4.SCH

PROCESS
PRICE
QUANTITY
PRICE



CONFIDENTIAL

60.050 © 1988

Fig. 10 b0



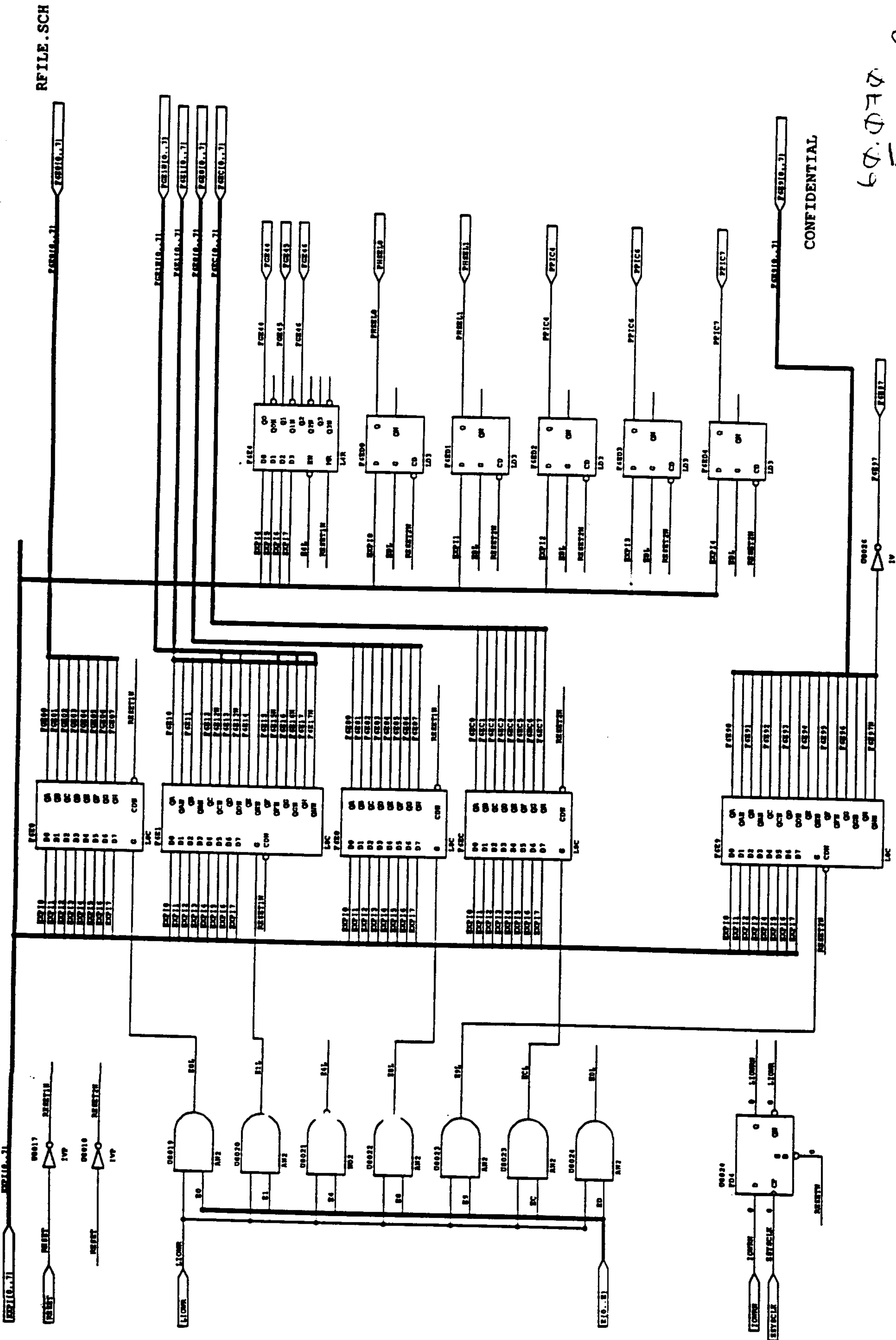
6th. 1860

Fig. 10 Bp

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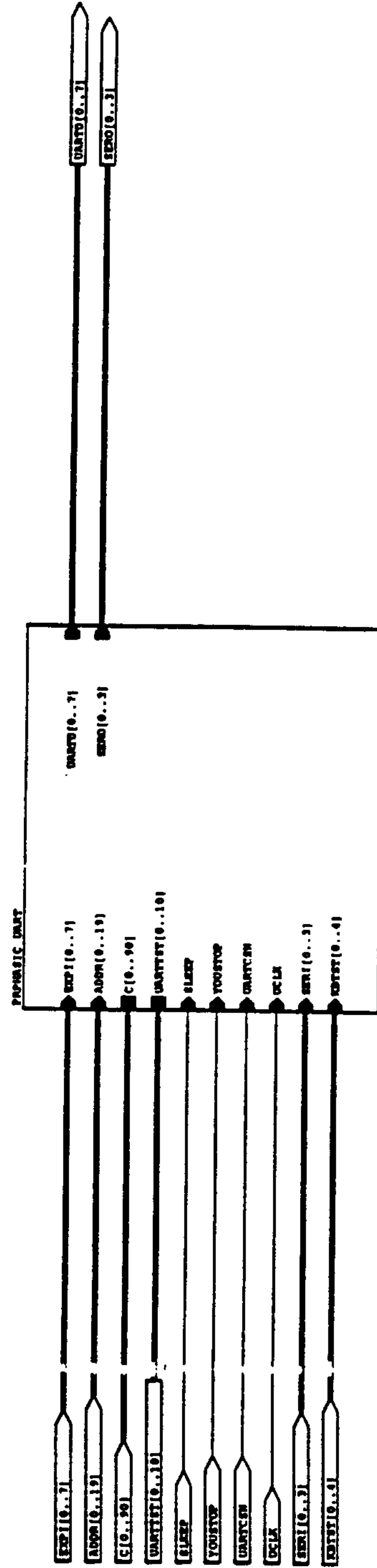
40

60.070
Fig. 10 B2



81

$\phi\phi.\phi=\phi$
Fig 10 Bt



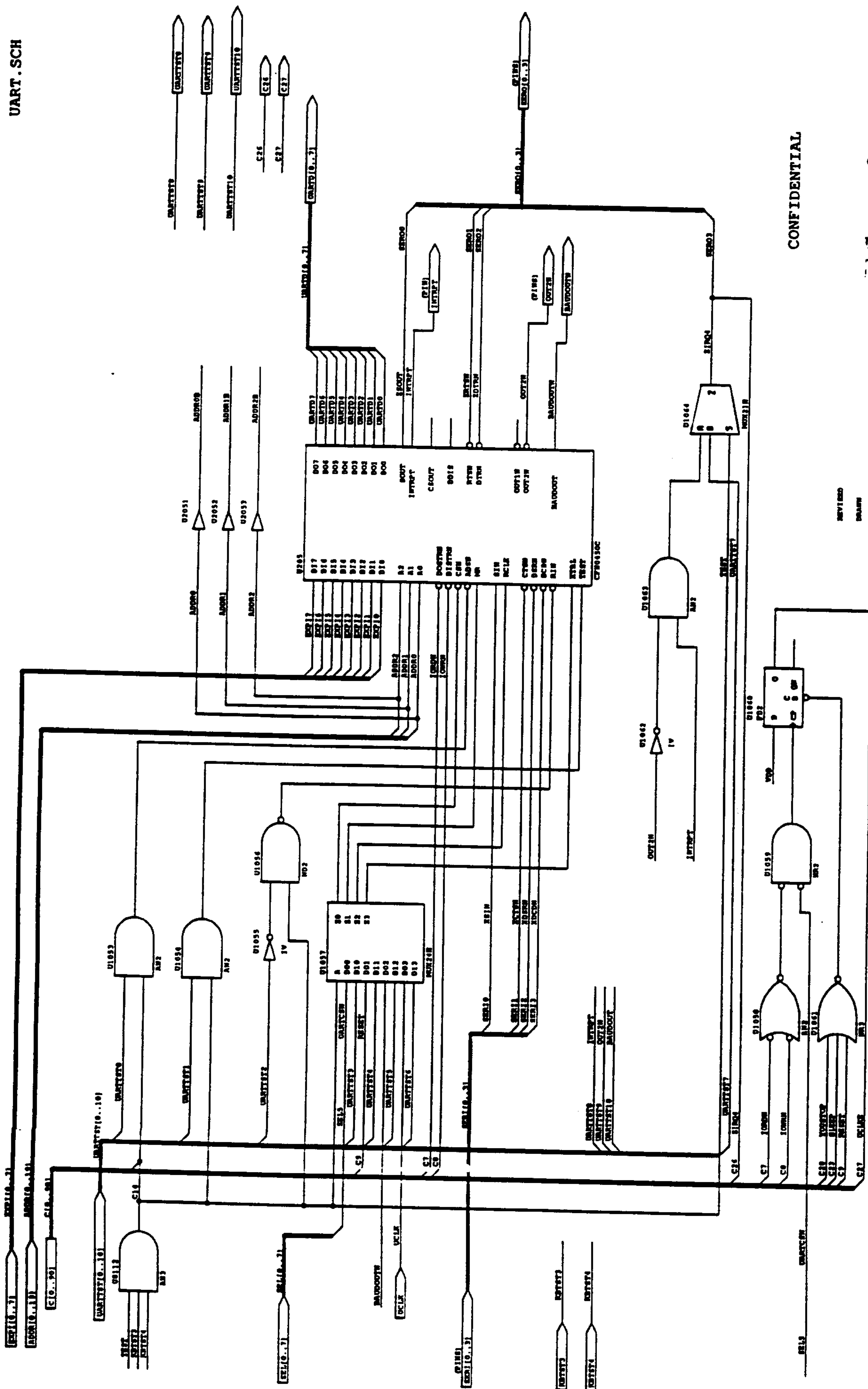
2063558

UART.SCH

92

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710.010
Fig 10Bs



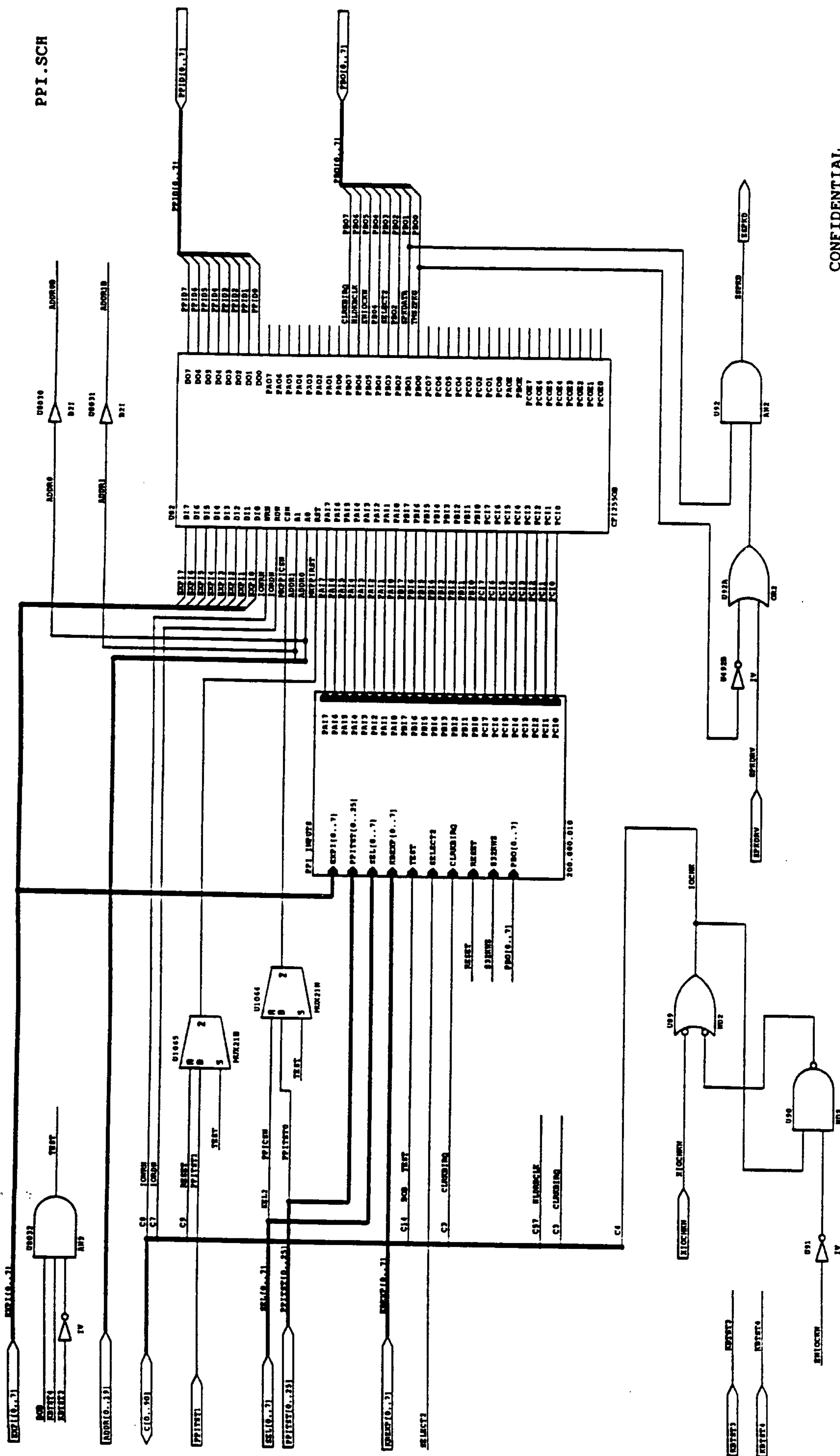
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Fig. 80. $\phi_1 \phi$

Fig. 10 bu

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DESIGNED
DRAWN
APPROVED

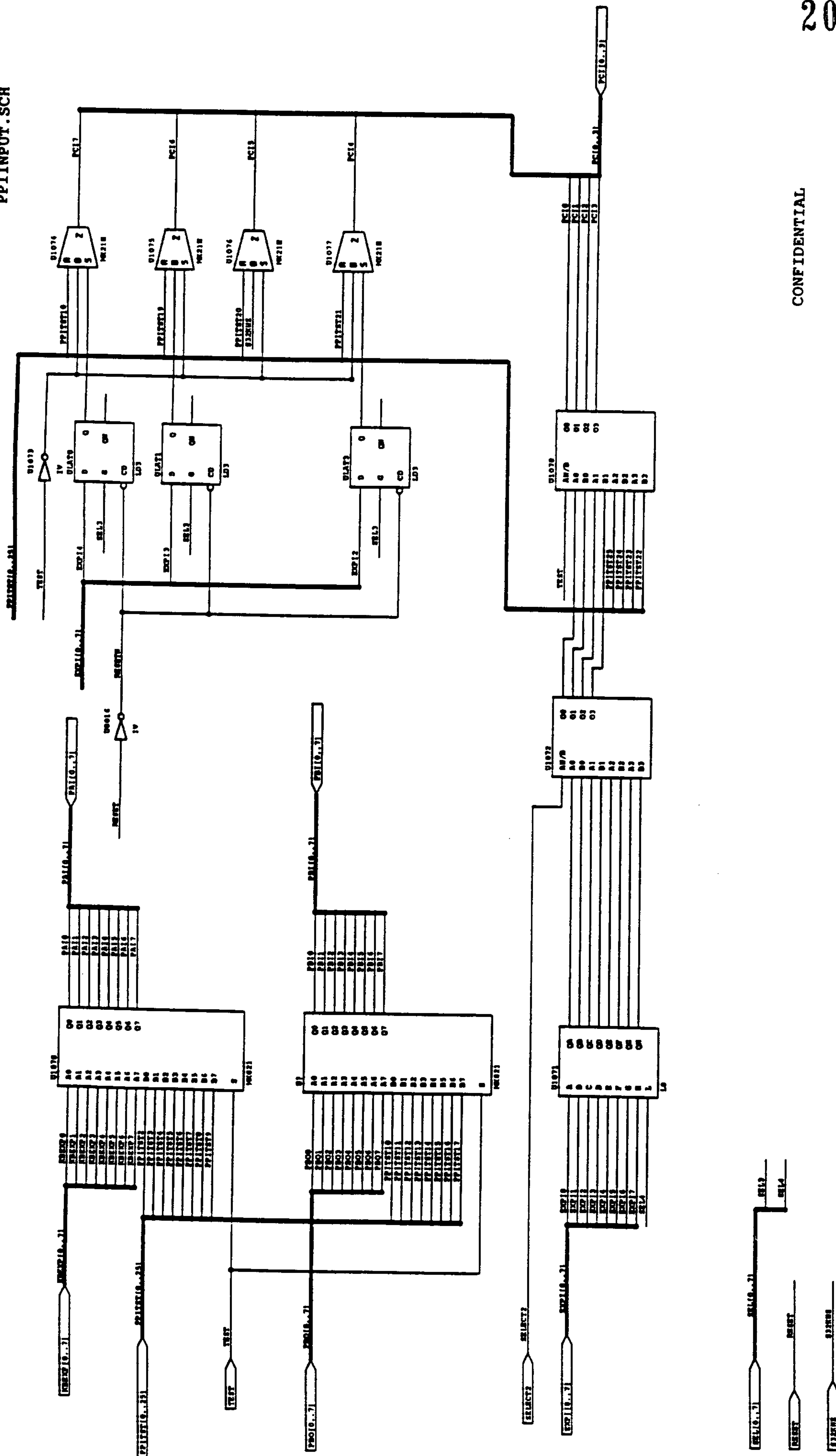


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$\phi\tau\psi, \psi\phi$

Fig. 10bV



86

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Fig. 10Bw

ΦΦ.Φ9Φ

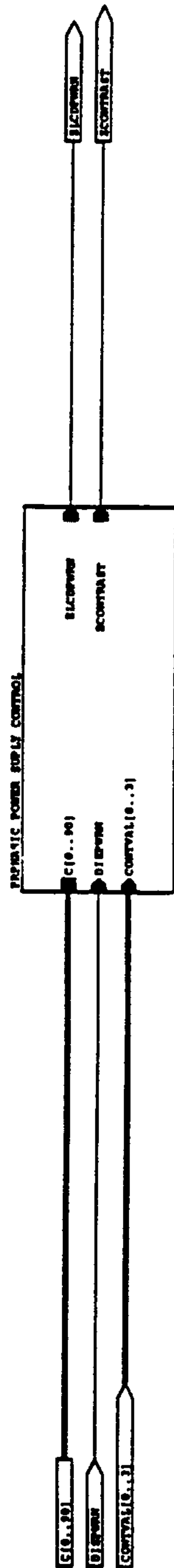
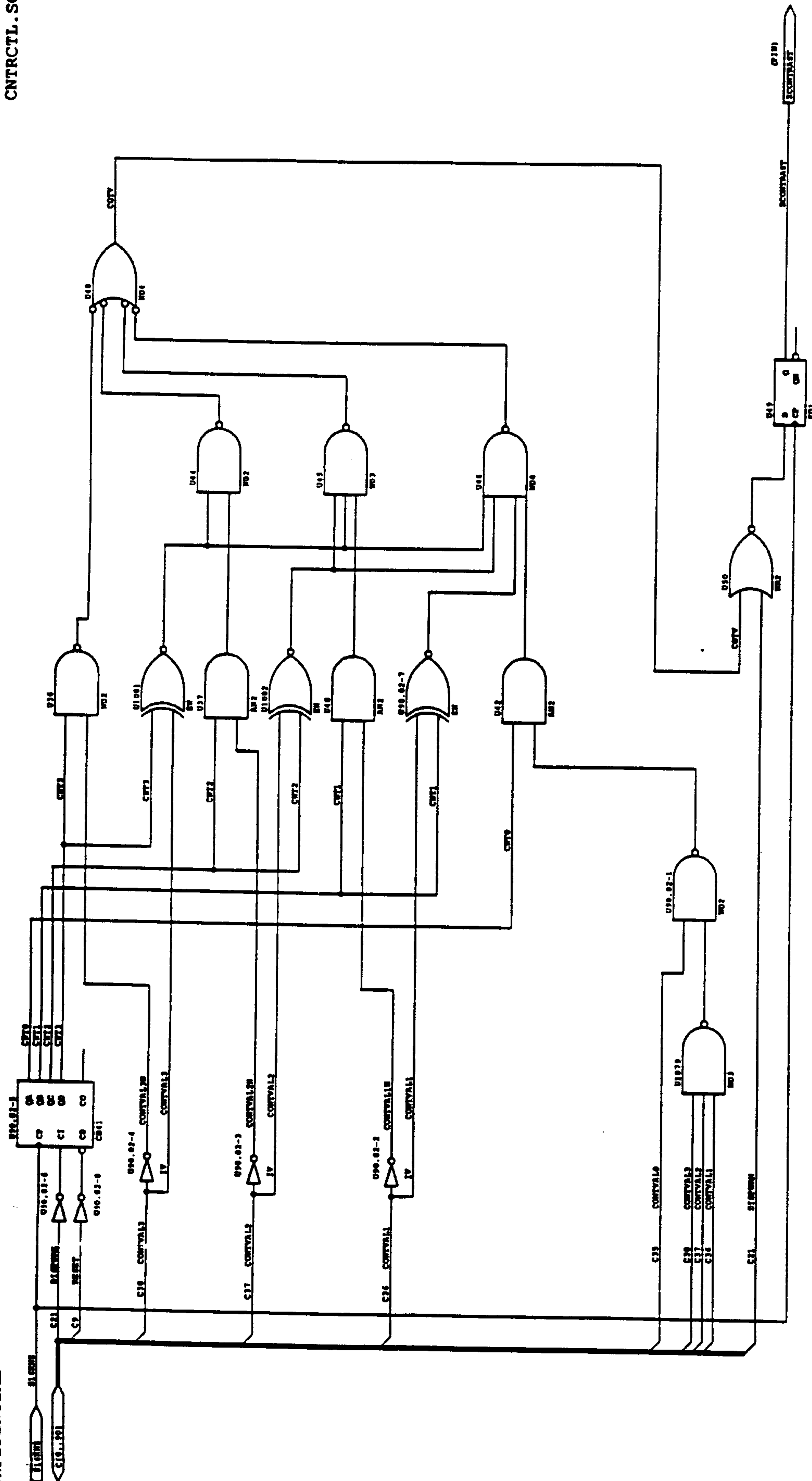


Fig 10 By

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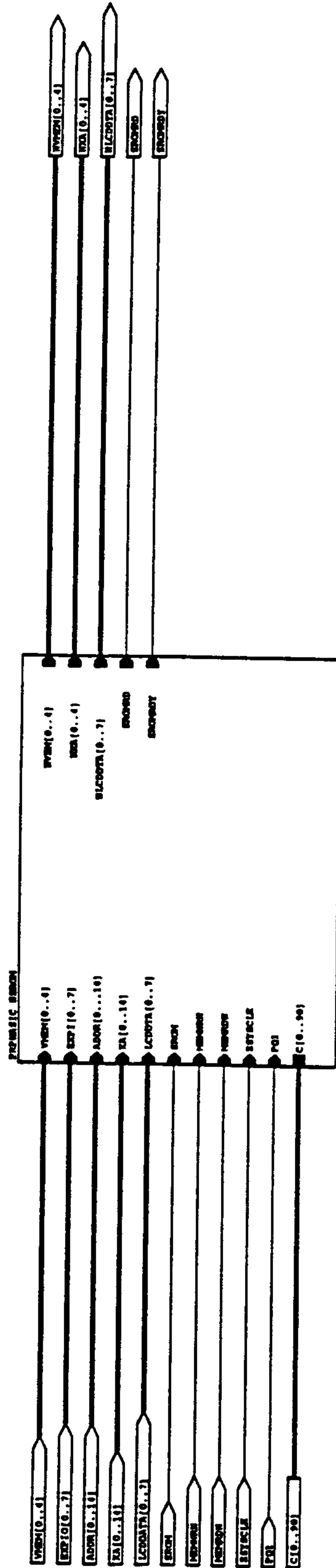
90. 020



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ΦΦ.1ΦΦ

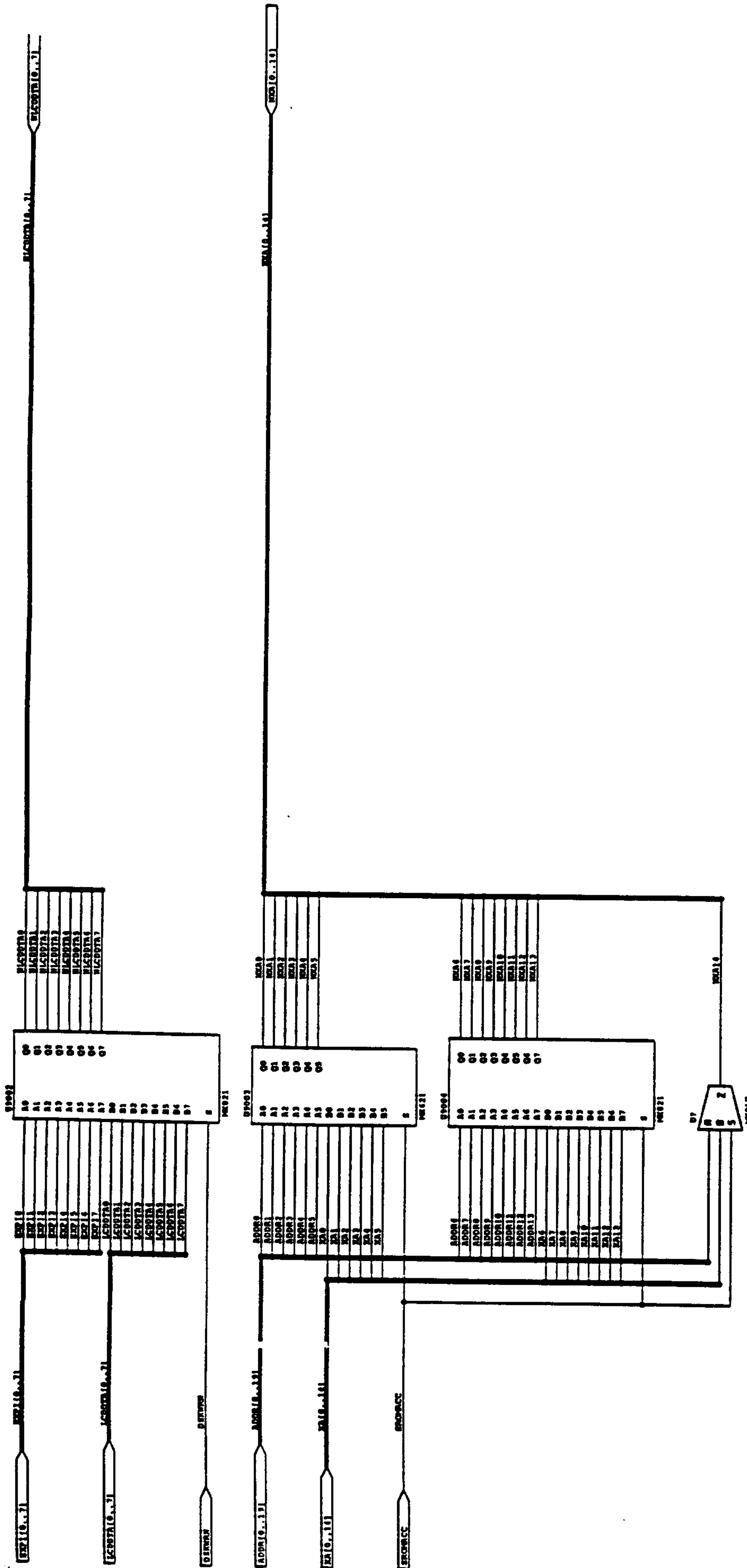
Fig 10 B2

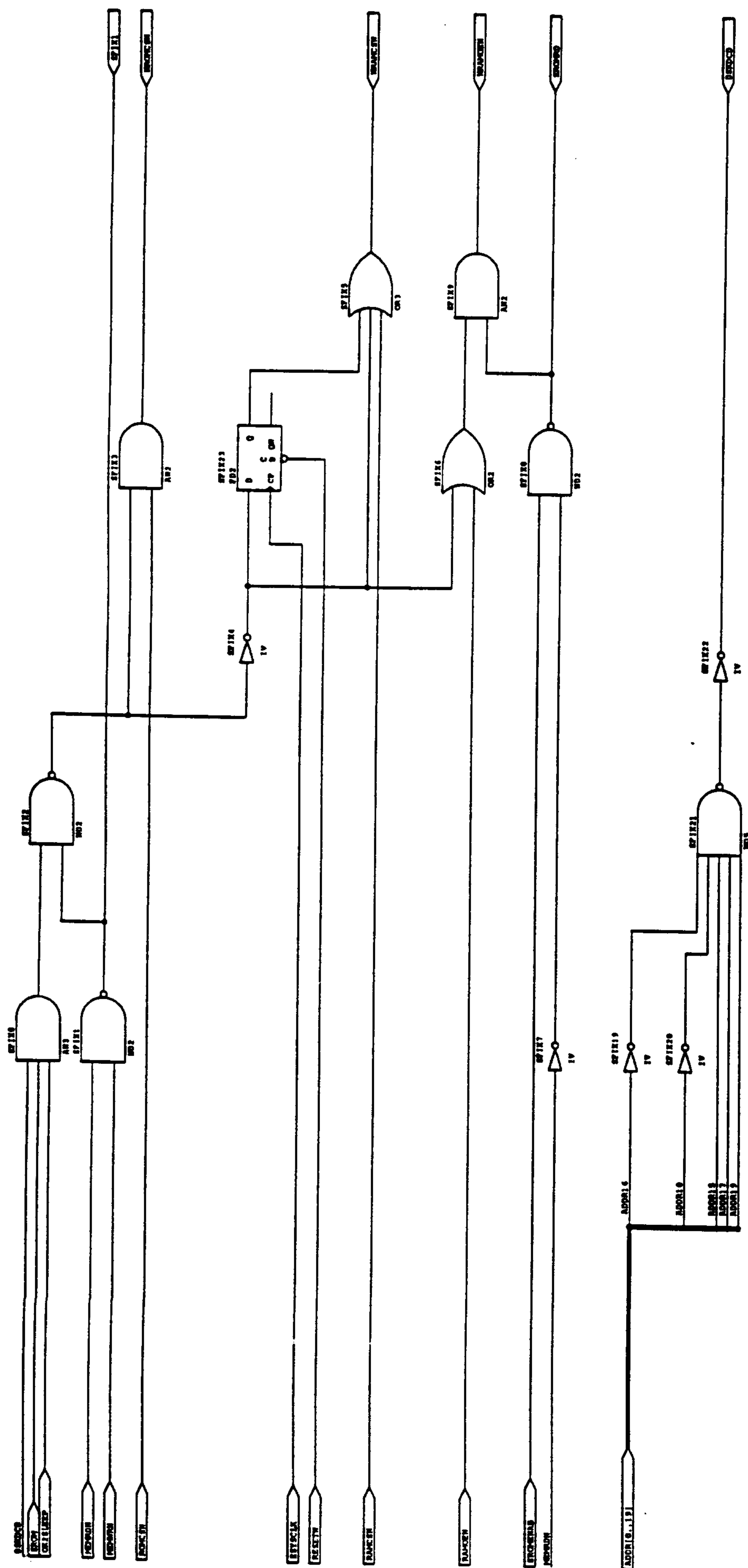


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100.010

Fig. 10 Ca



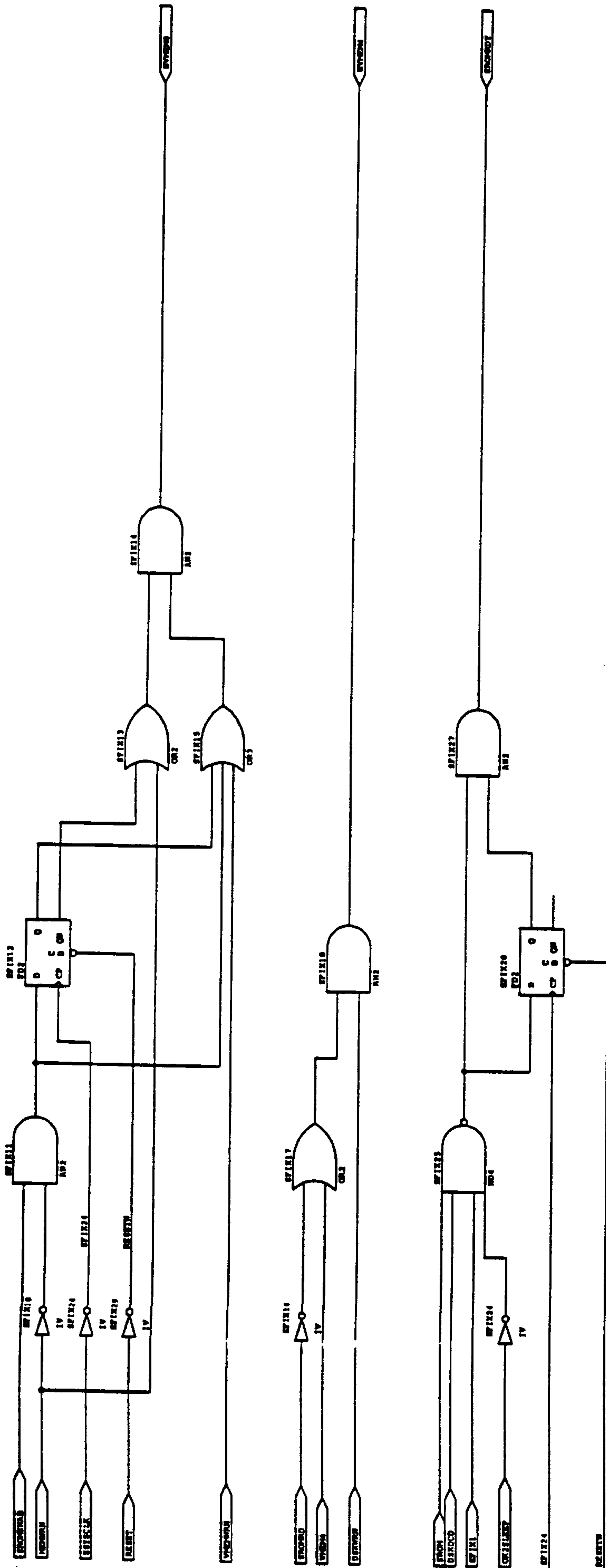


100. 100. 100.

Fig. 10C b

199. 730

Fig. 10 C

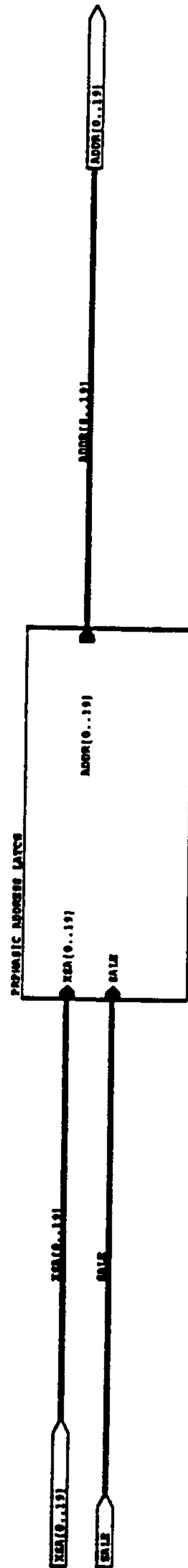


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93

Fig. 10 (a)

Fig. 11 (b)

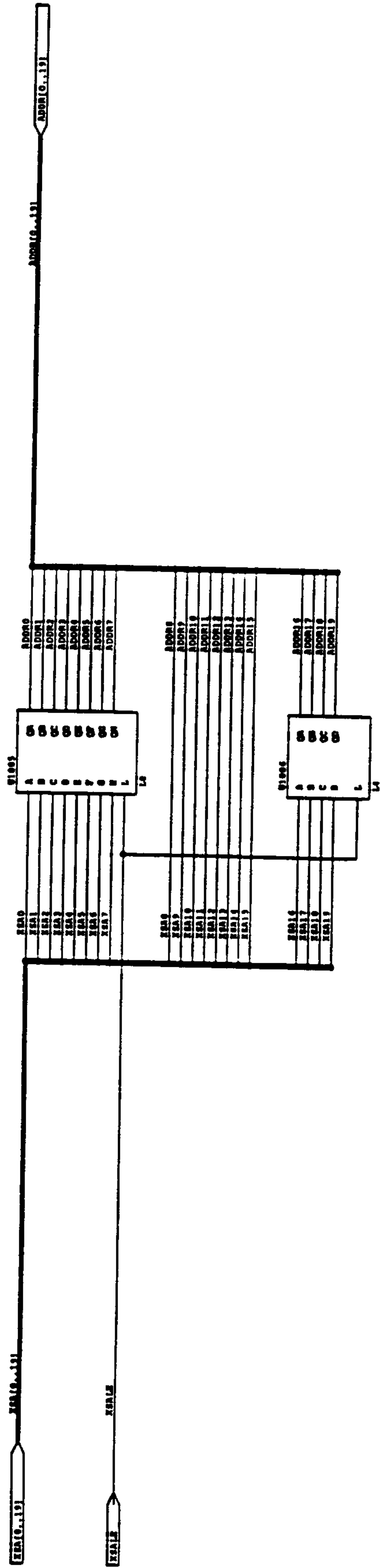


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94

117.010

Fig. 10C

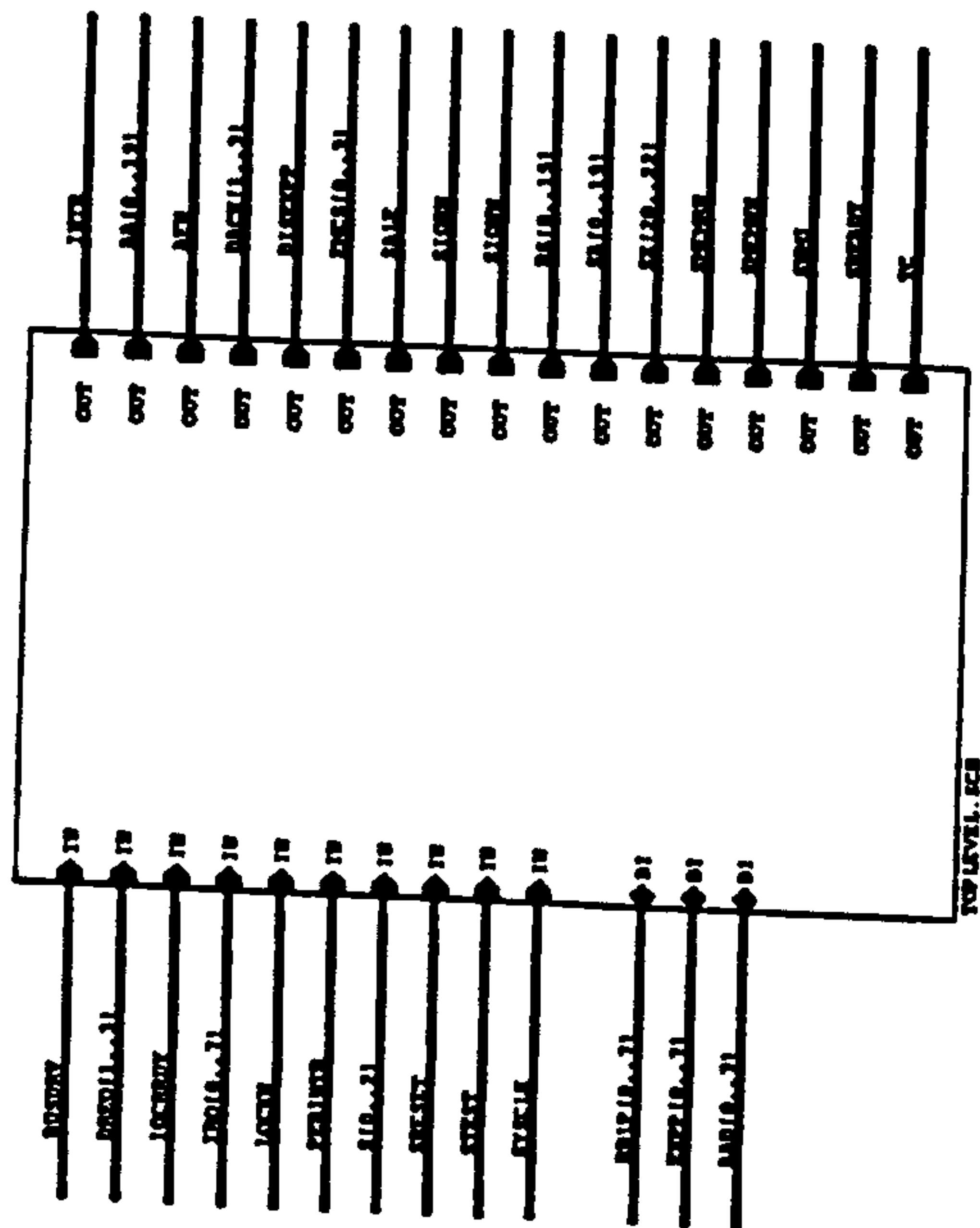


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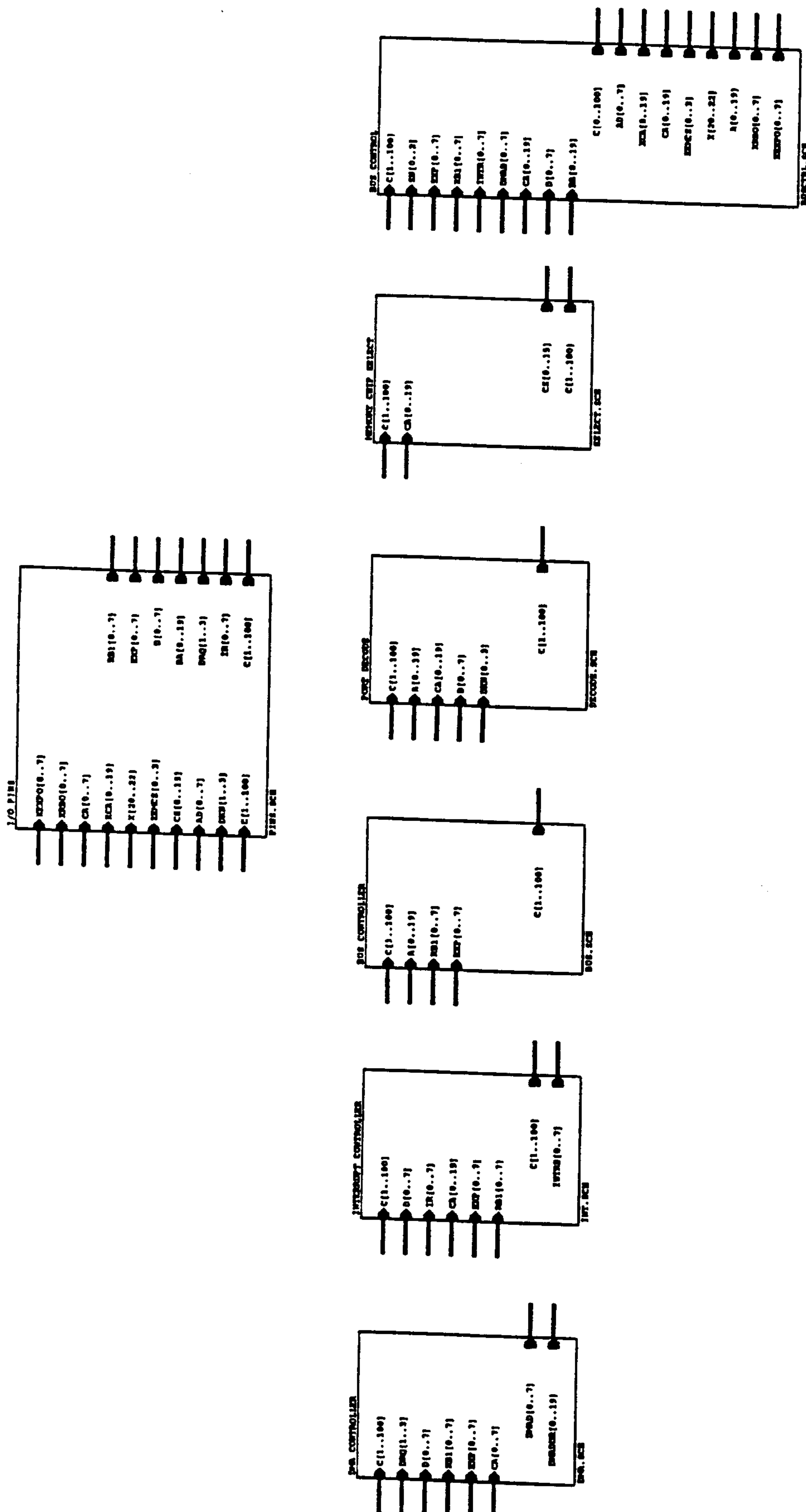
100.600.001

Fig. 11 A



96

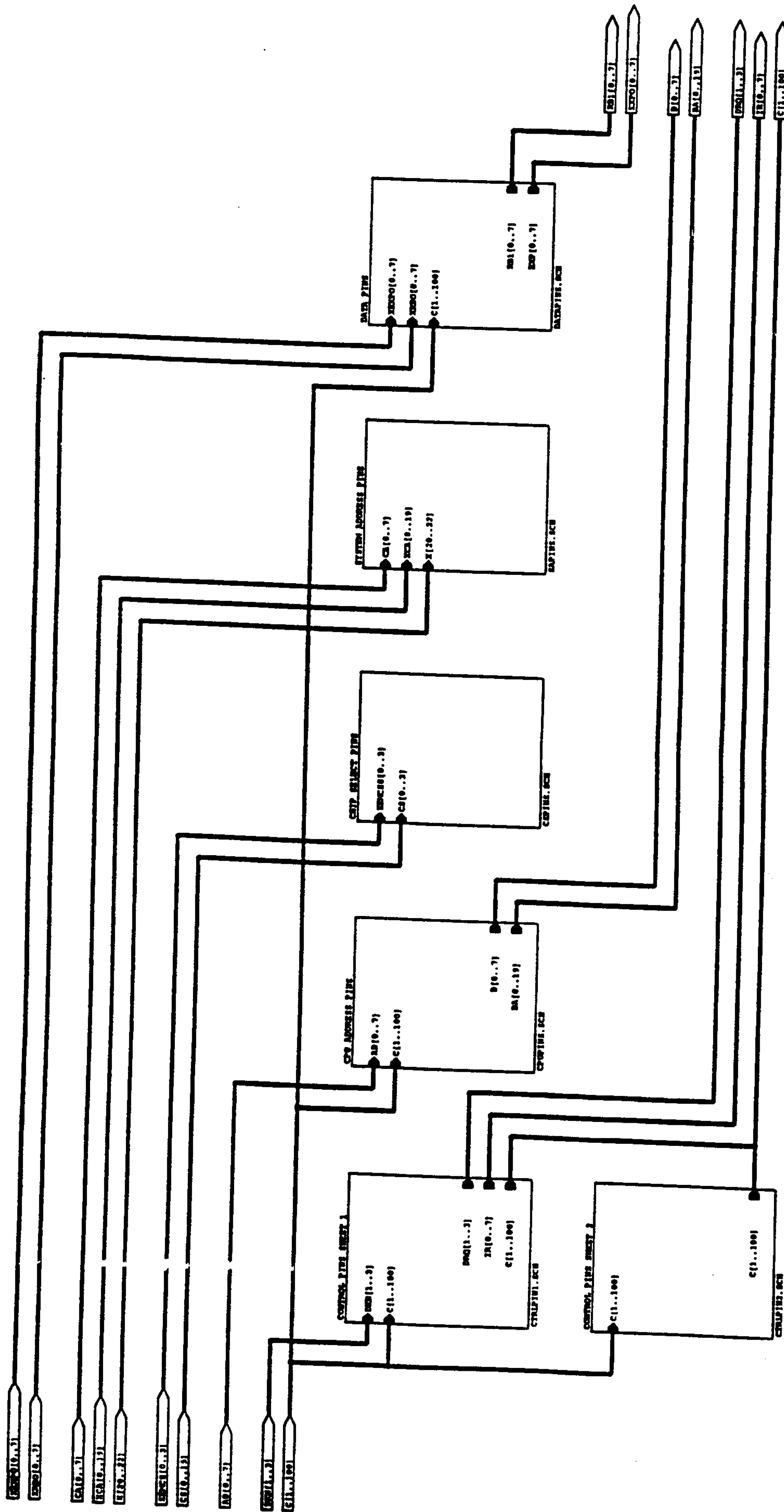
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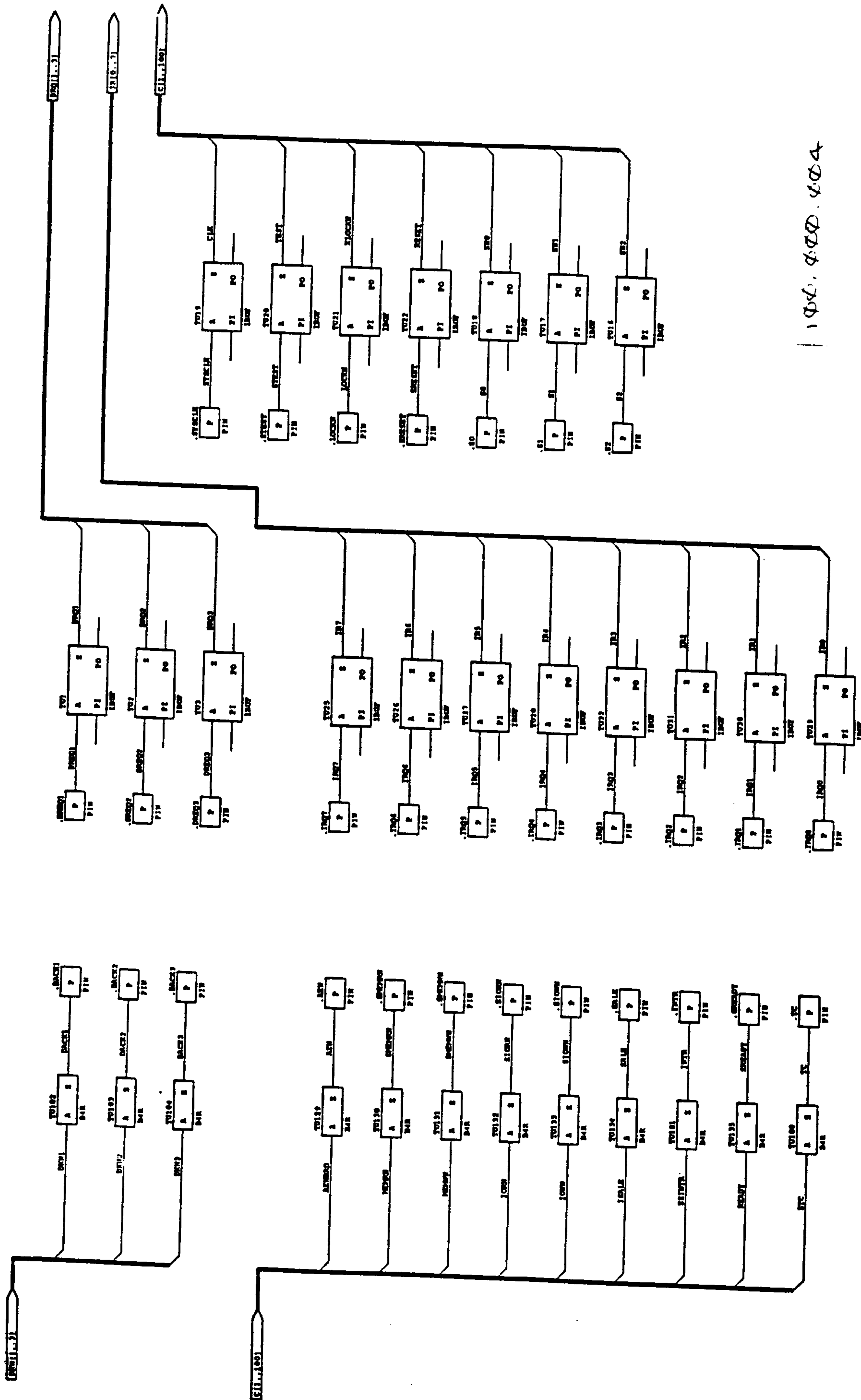
Fig. 11B

97



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Fig. 11 D



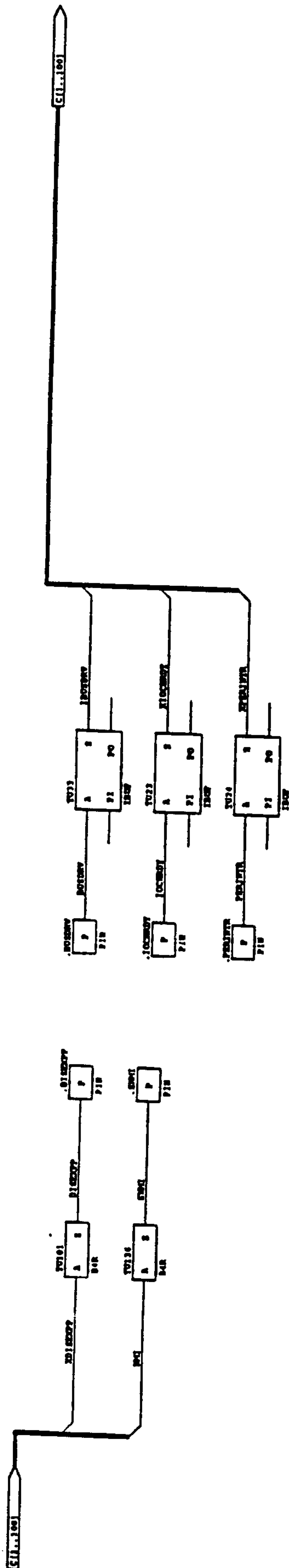
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Fig. 11

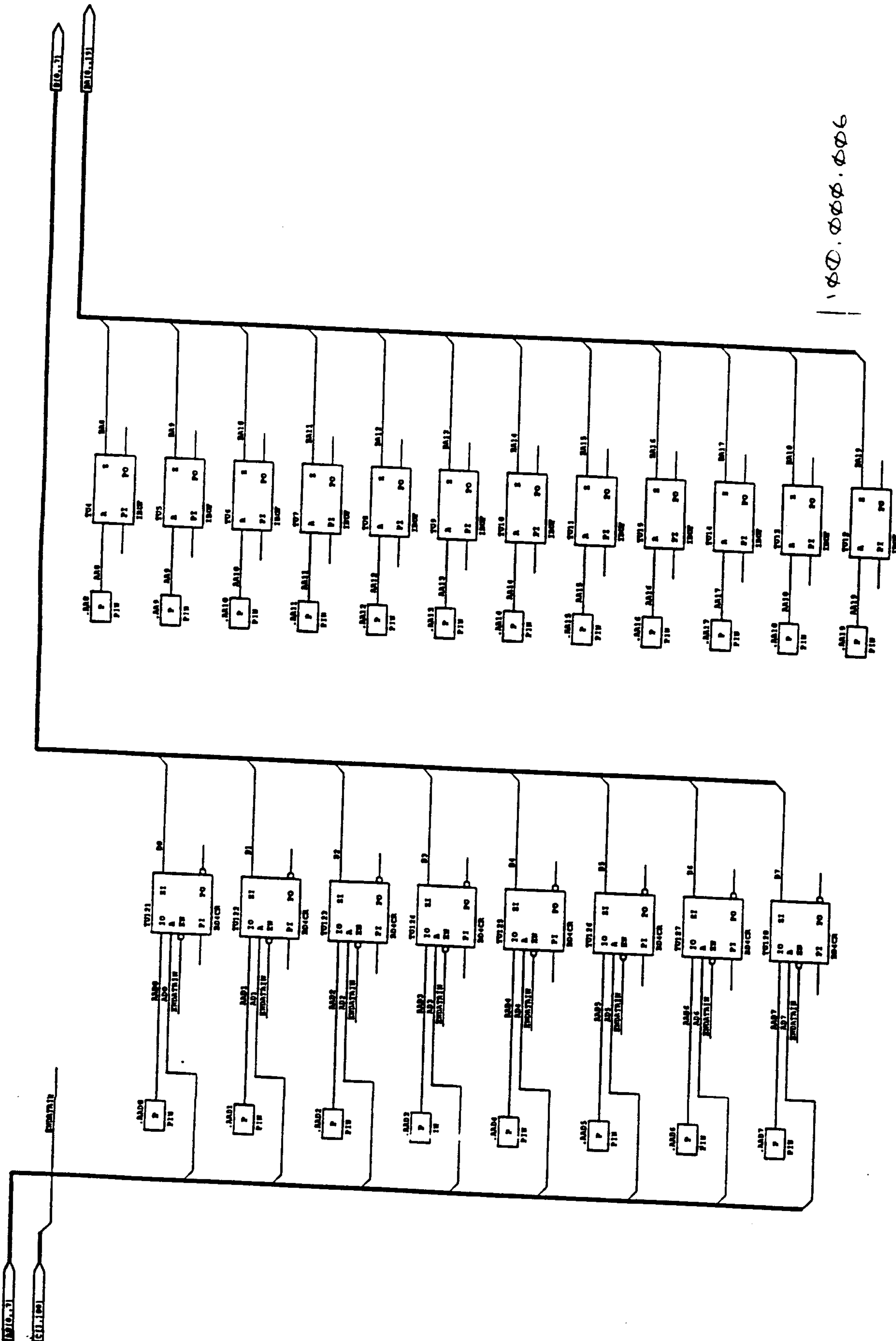
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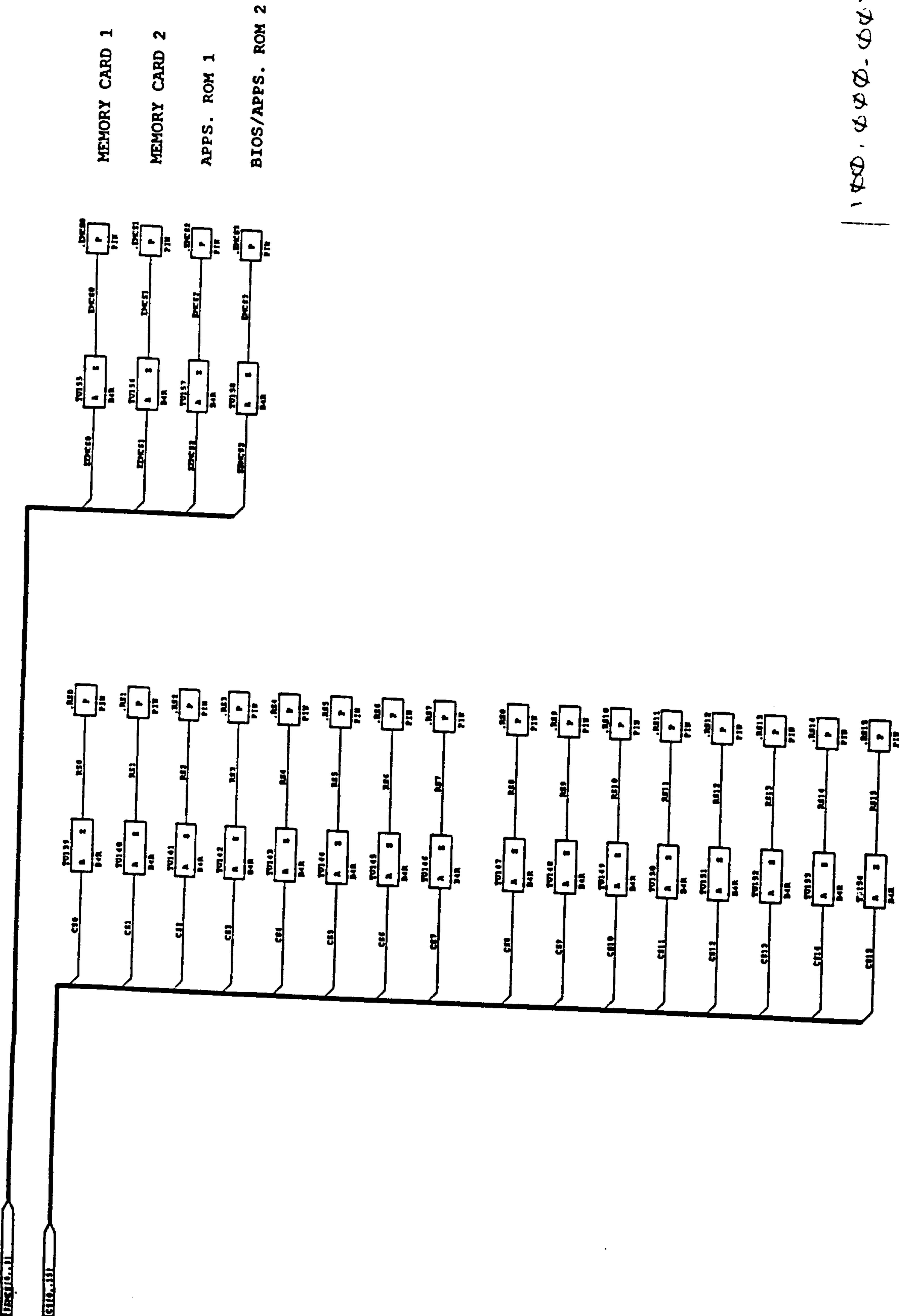
Fig. 11

140.000.006



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Fig. 11G

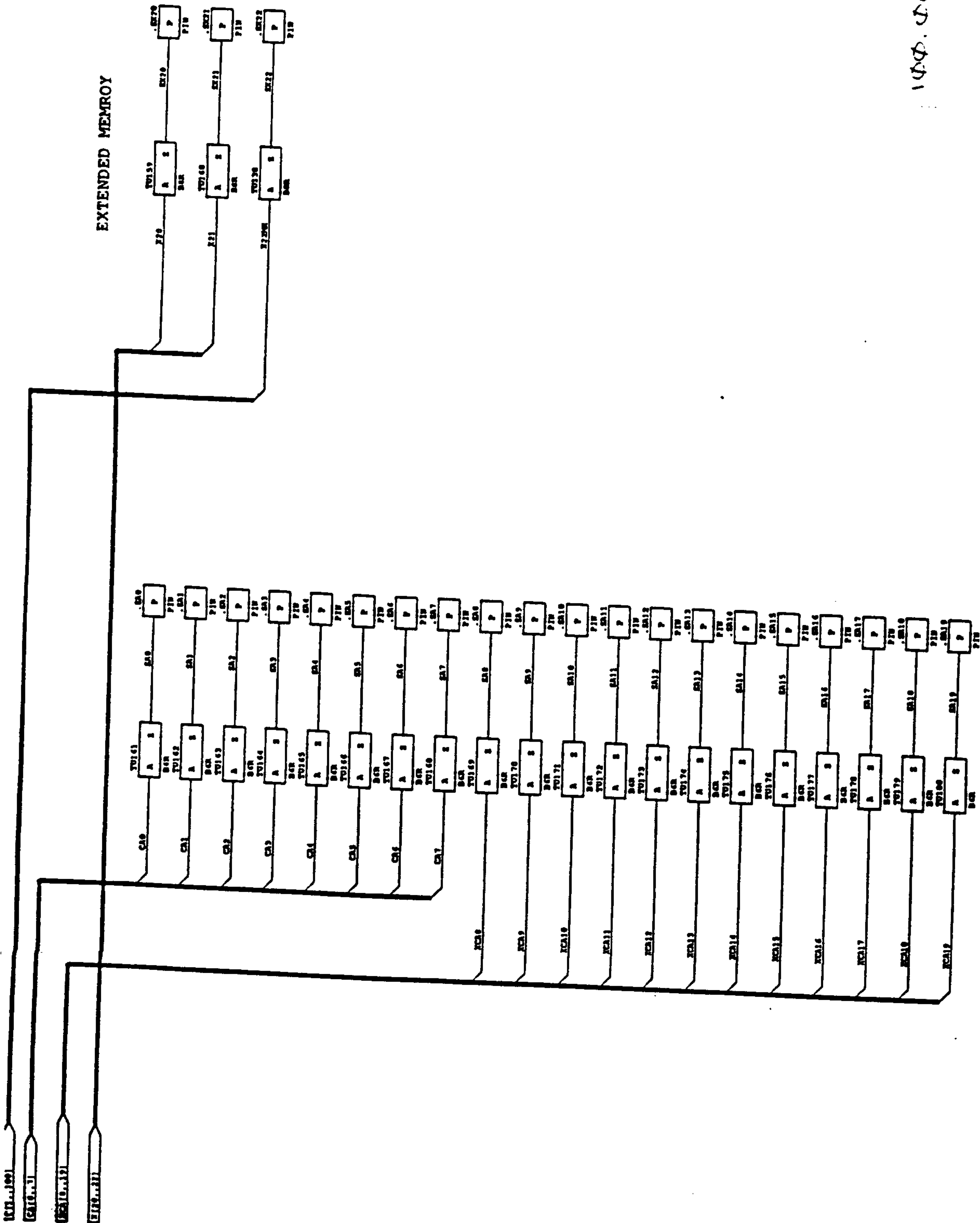


100.000.000

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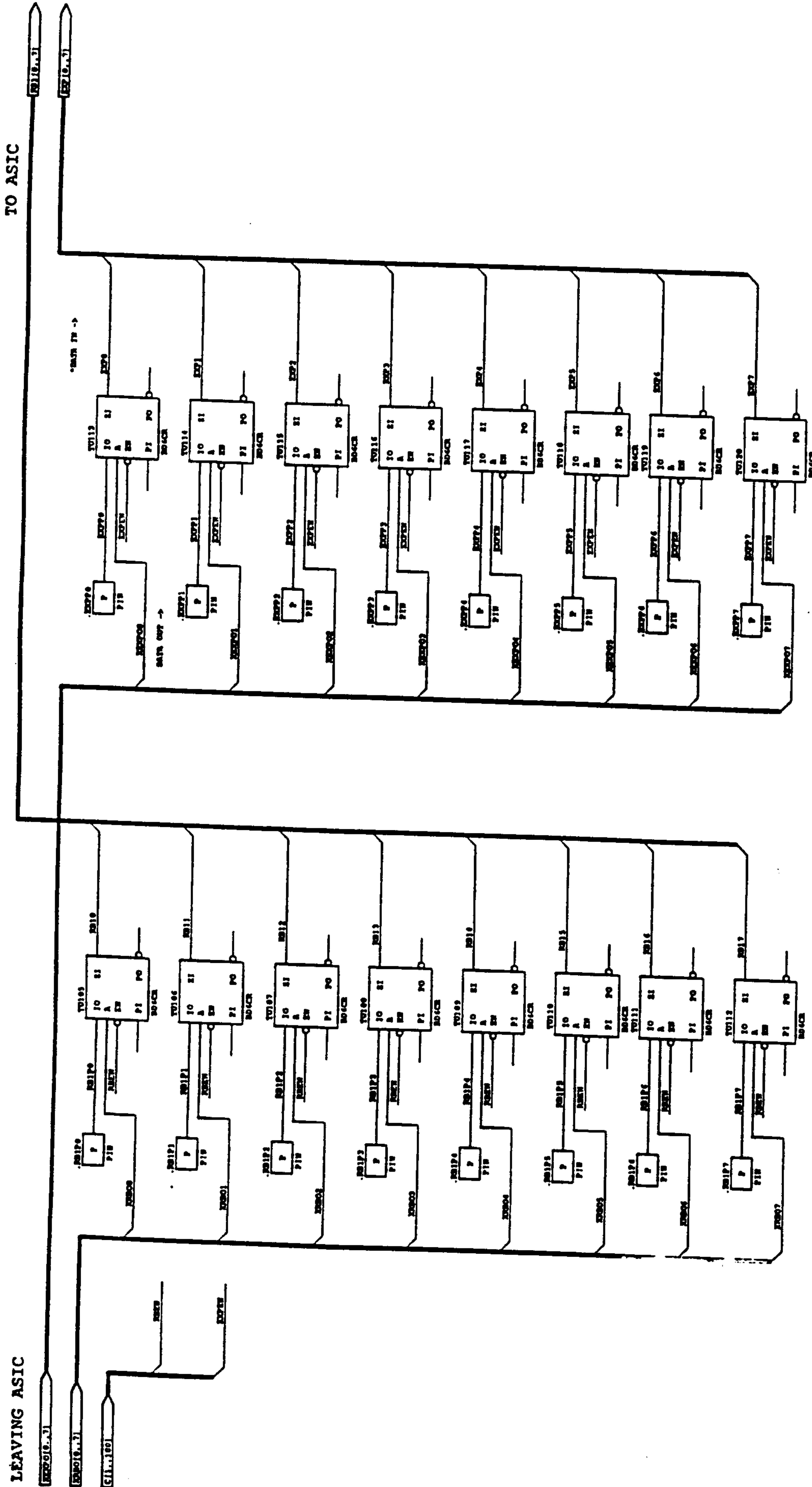
Fig 11H

144, 444, 448



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Fig 11 I

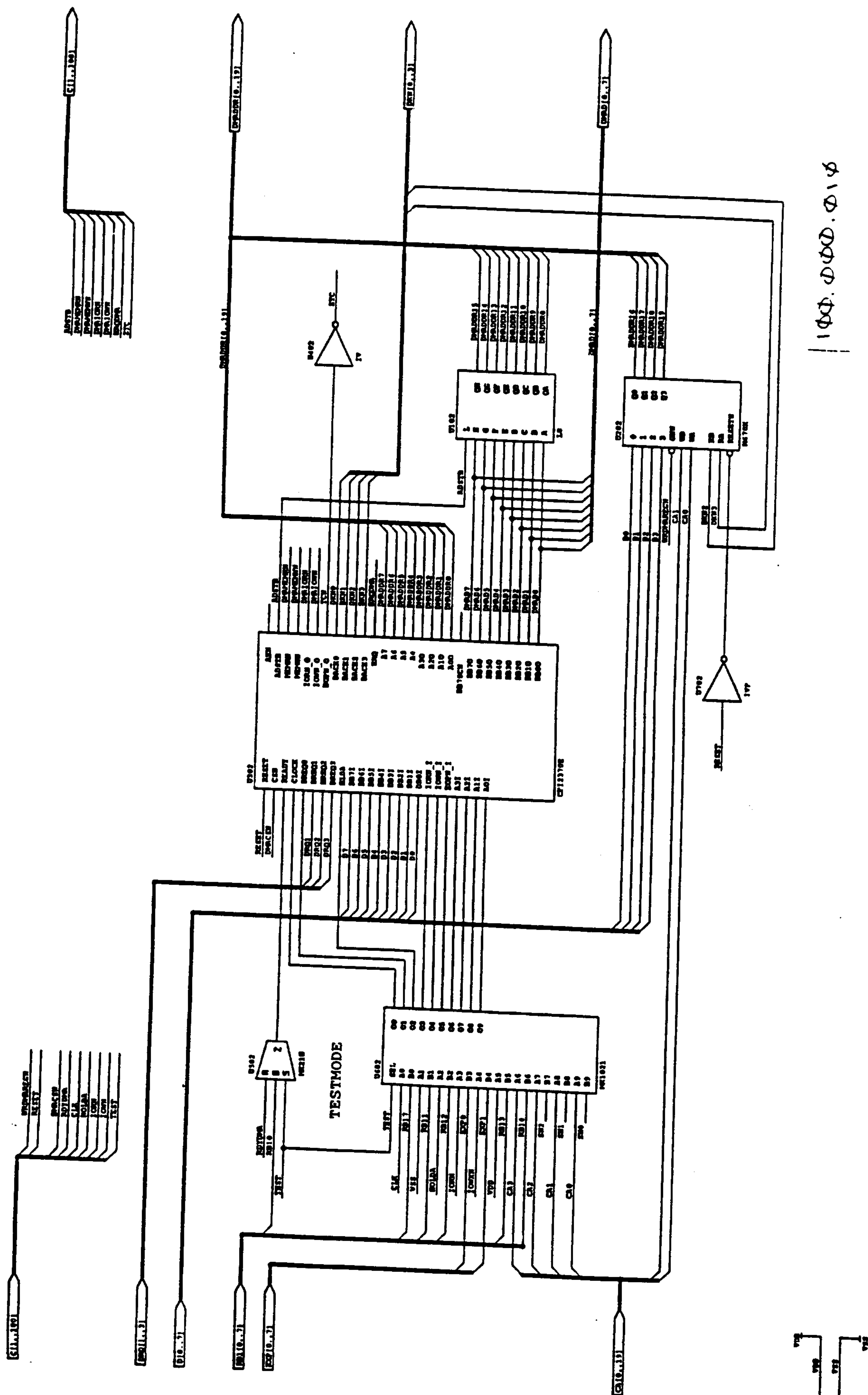


NOTES:

*74LS160 AND 74LS161

140.460.009

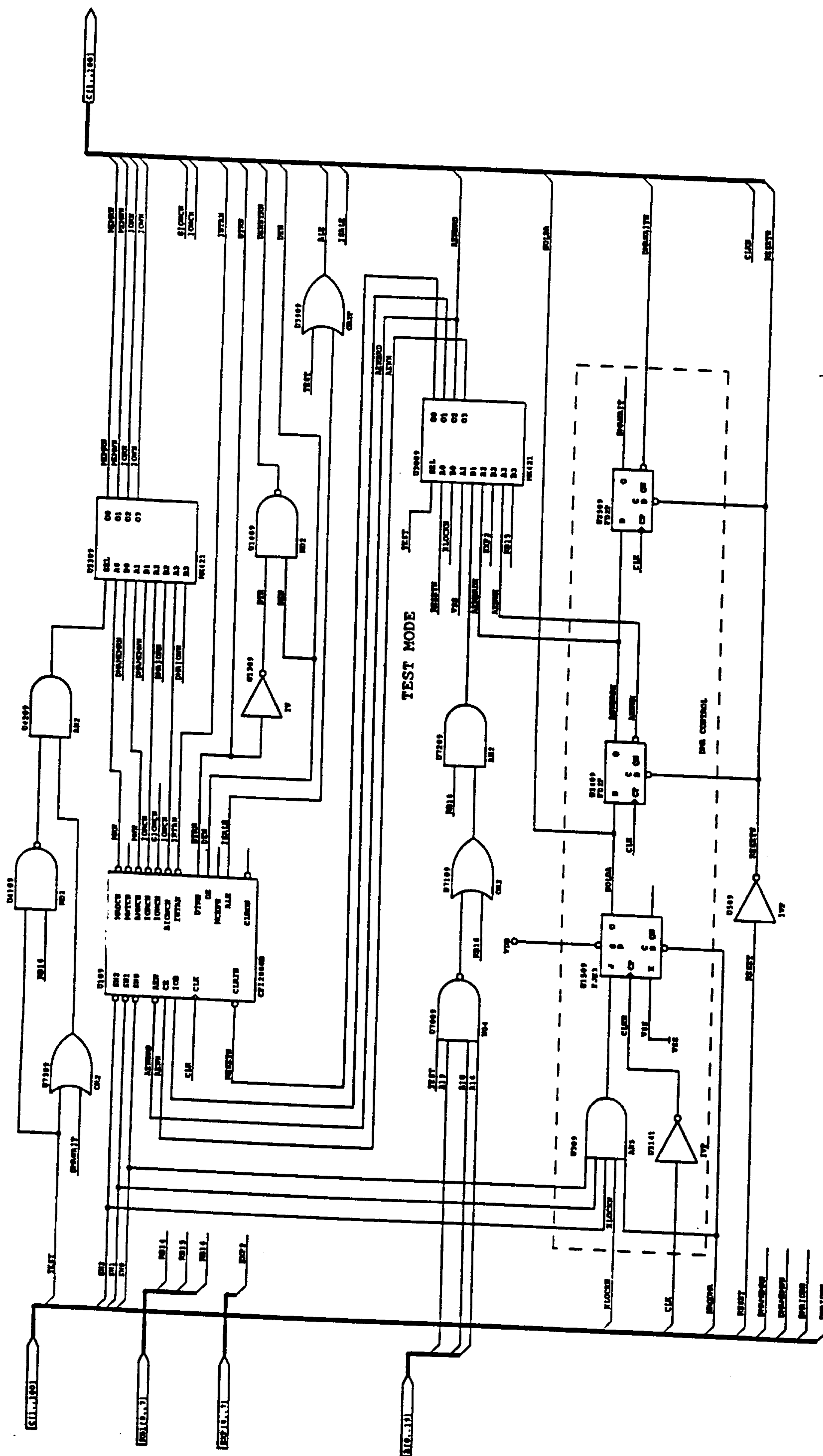
Fig. 5



106

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Fig. 11

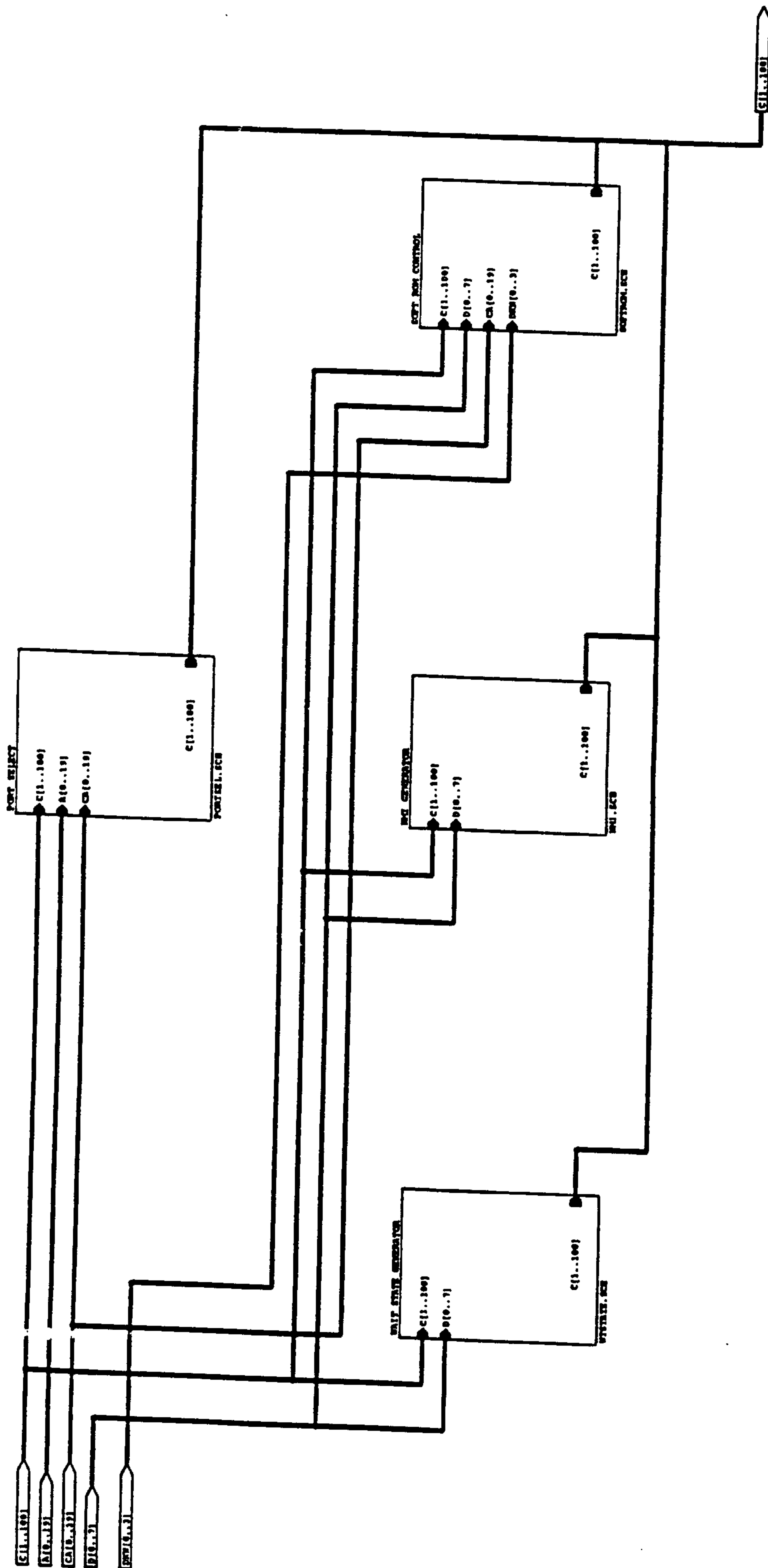


146. 146. 146. 146.

107

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Fig. 11

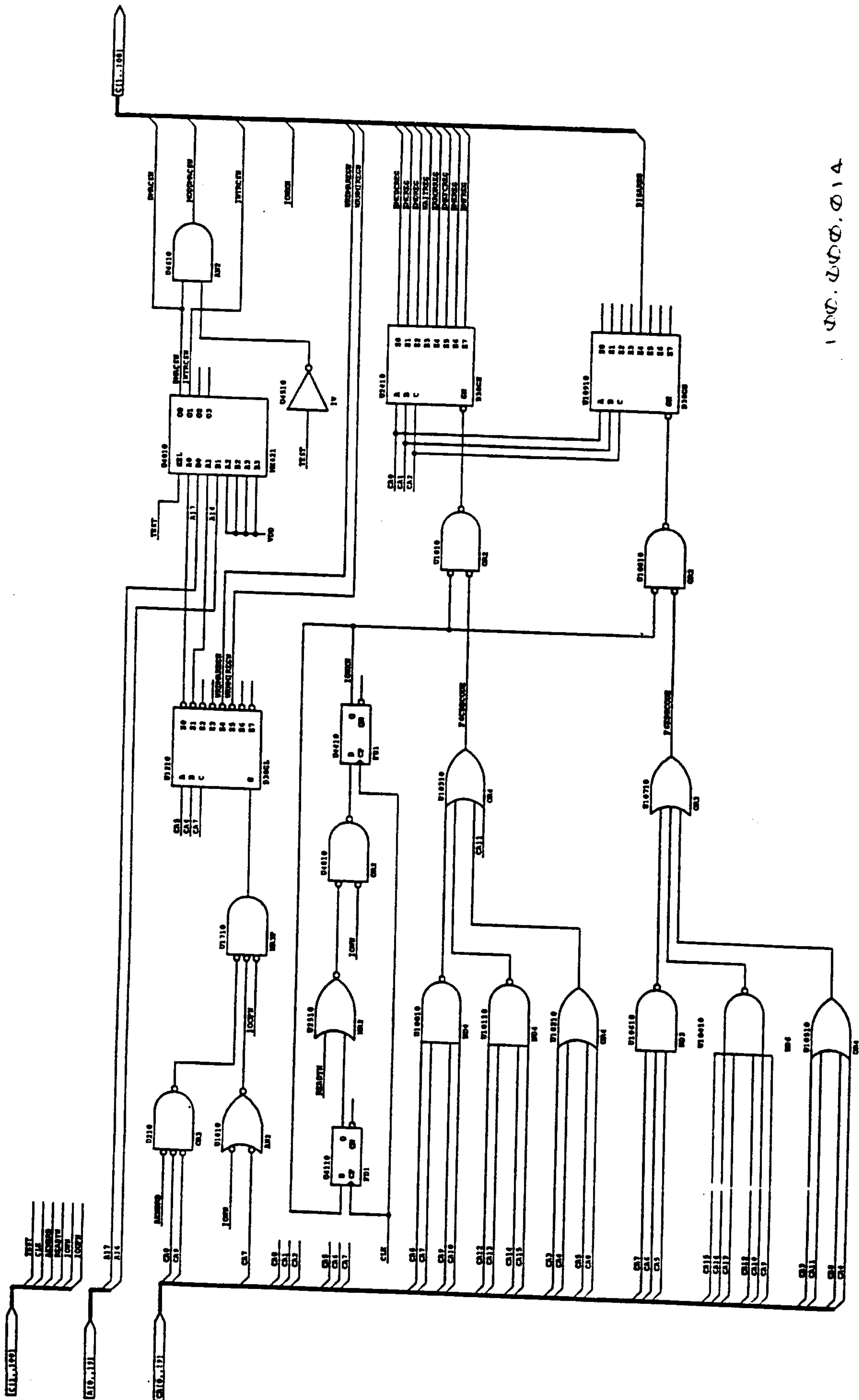


140,444,413

108

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Fig. 11 N



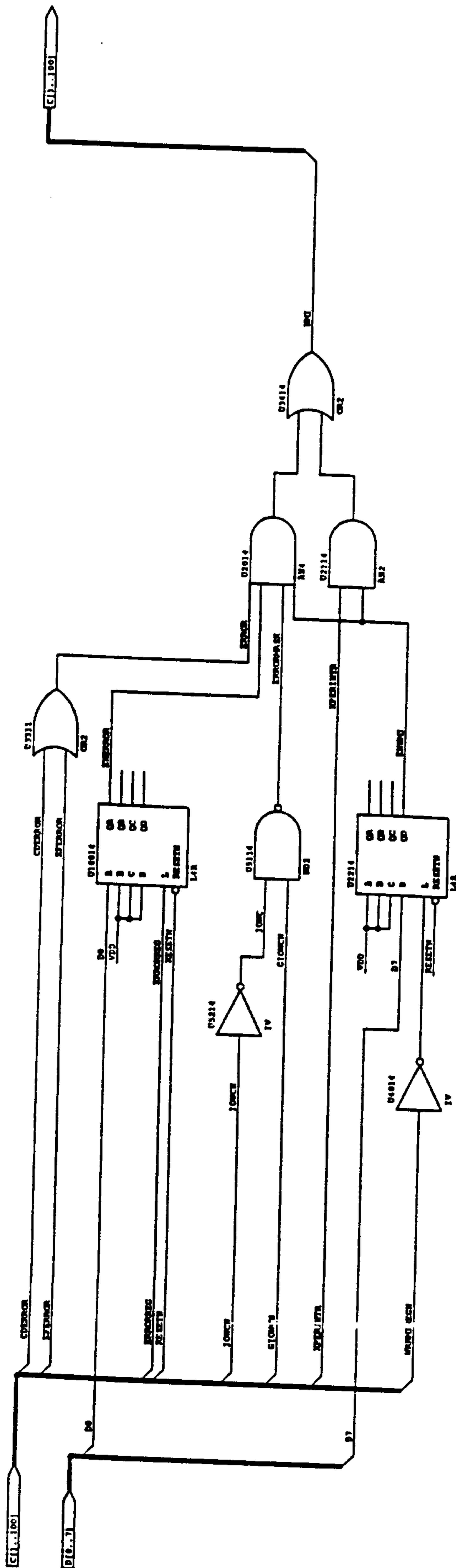
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110

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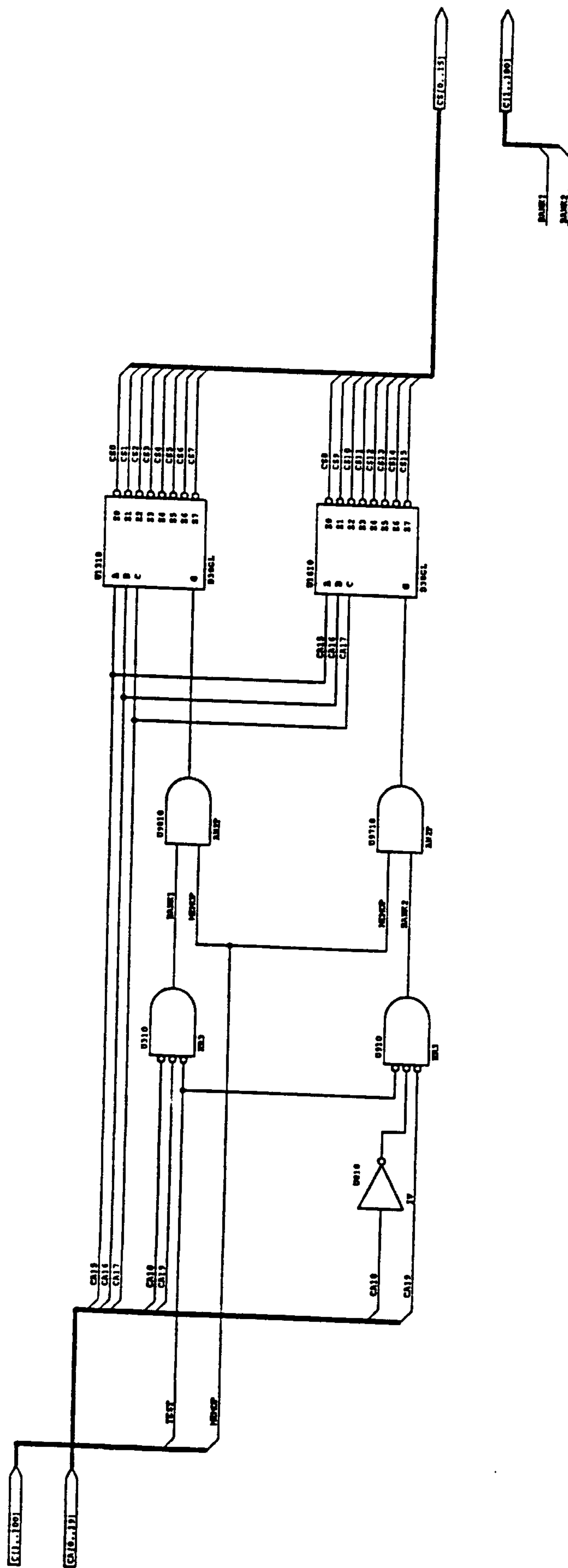
Fig 11a

100...999, 016



112

Fig. 11R

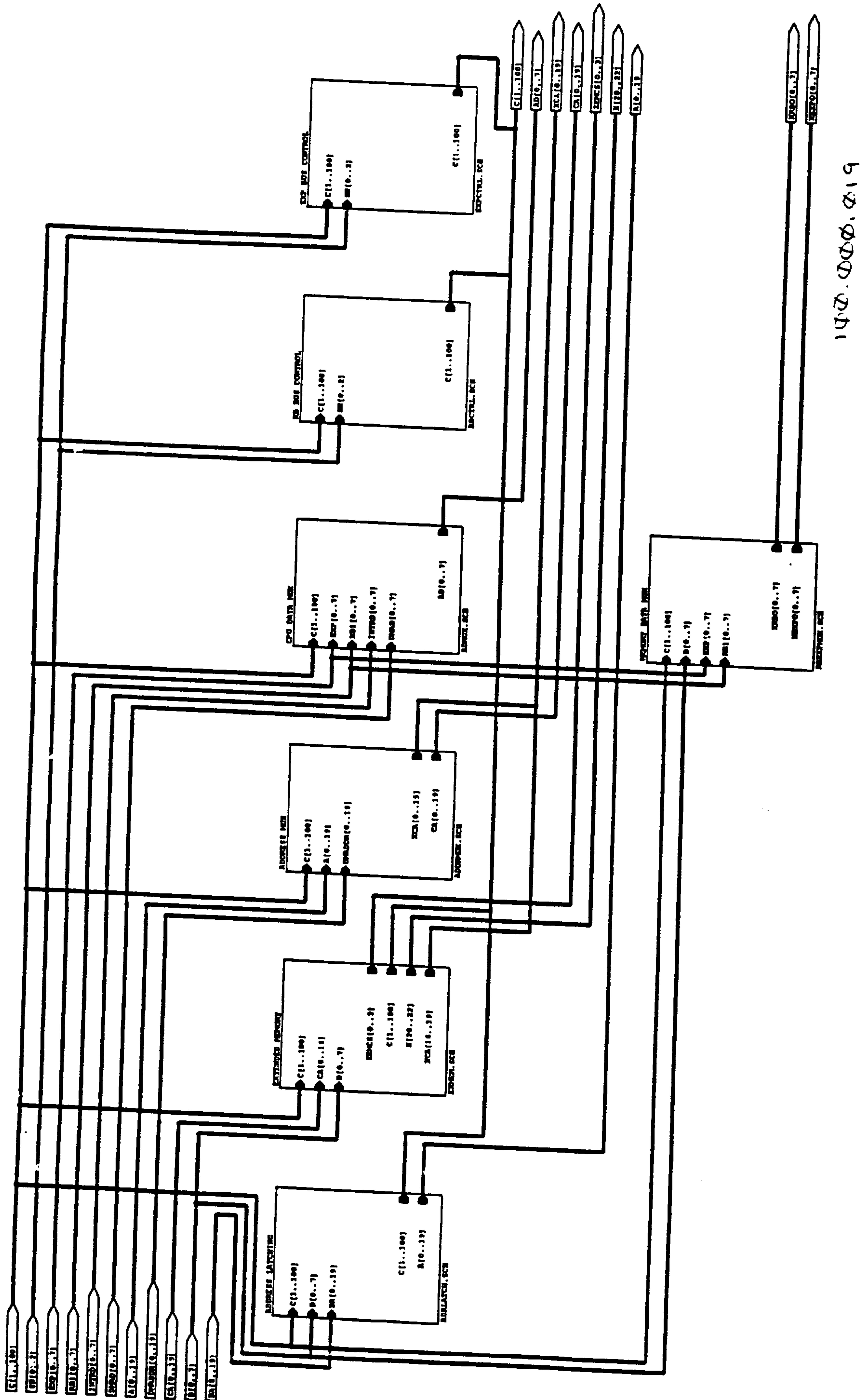


100.000.018

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Fig. 11 S

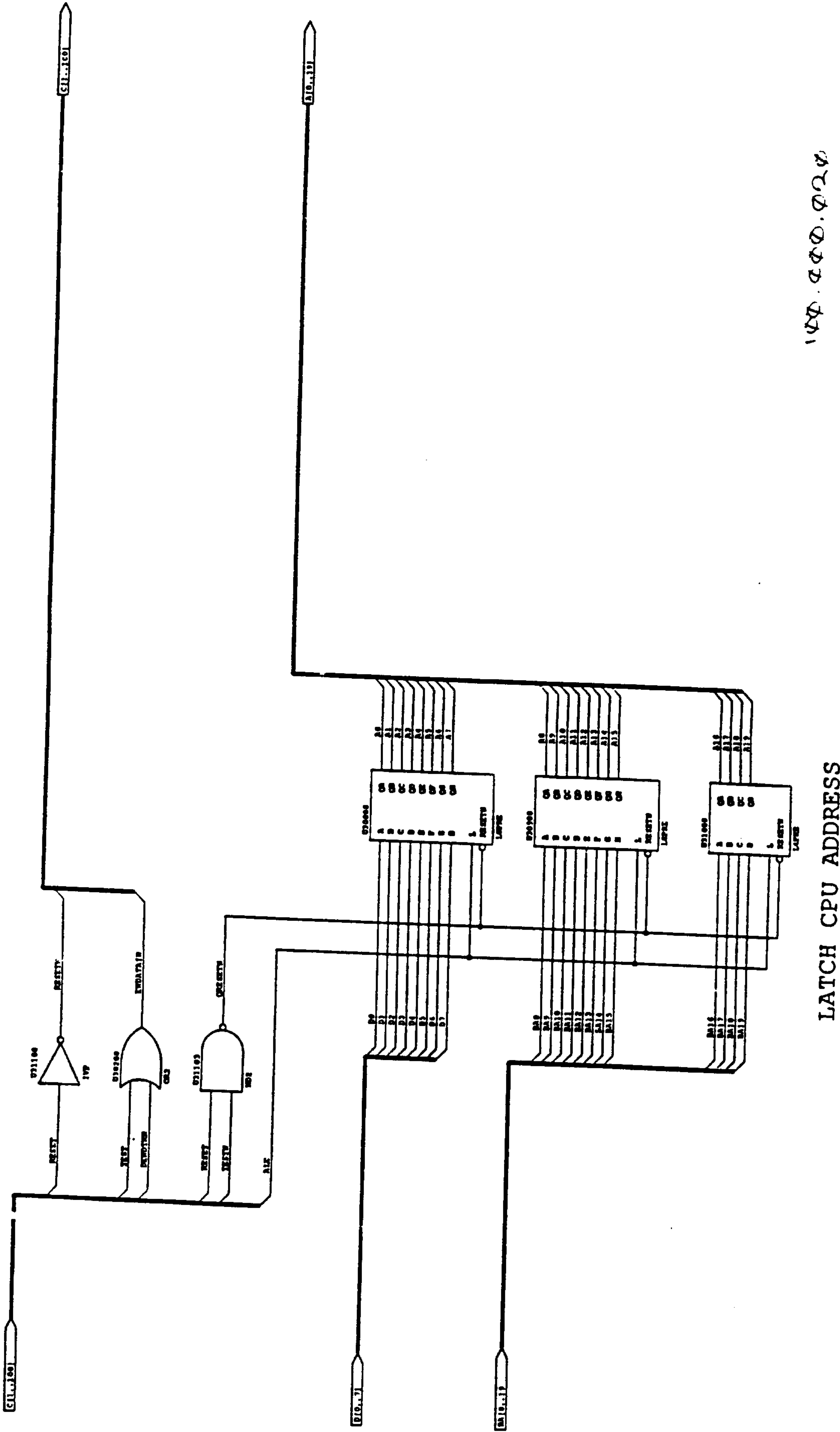


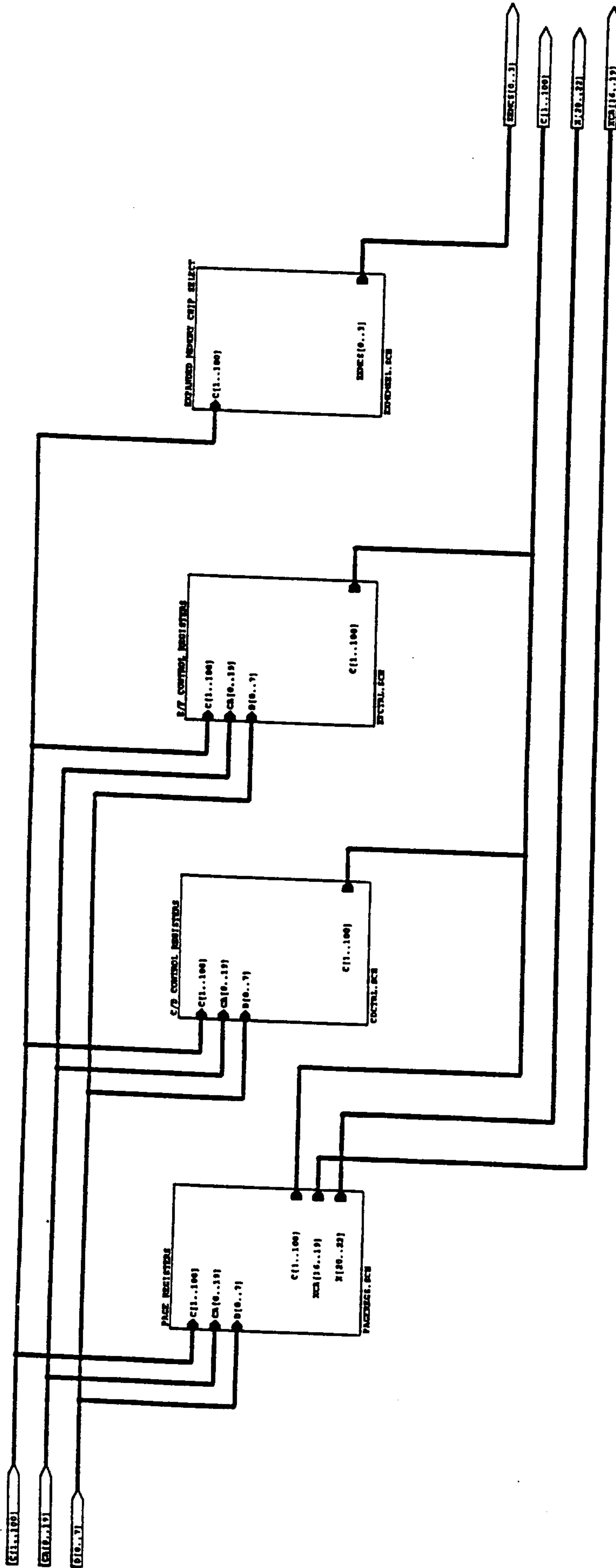
114

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Fig. 11 T

144.444.424



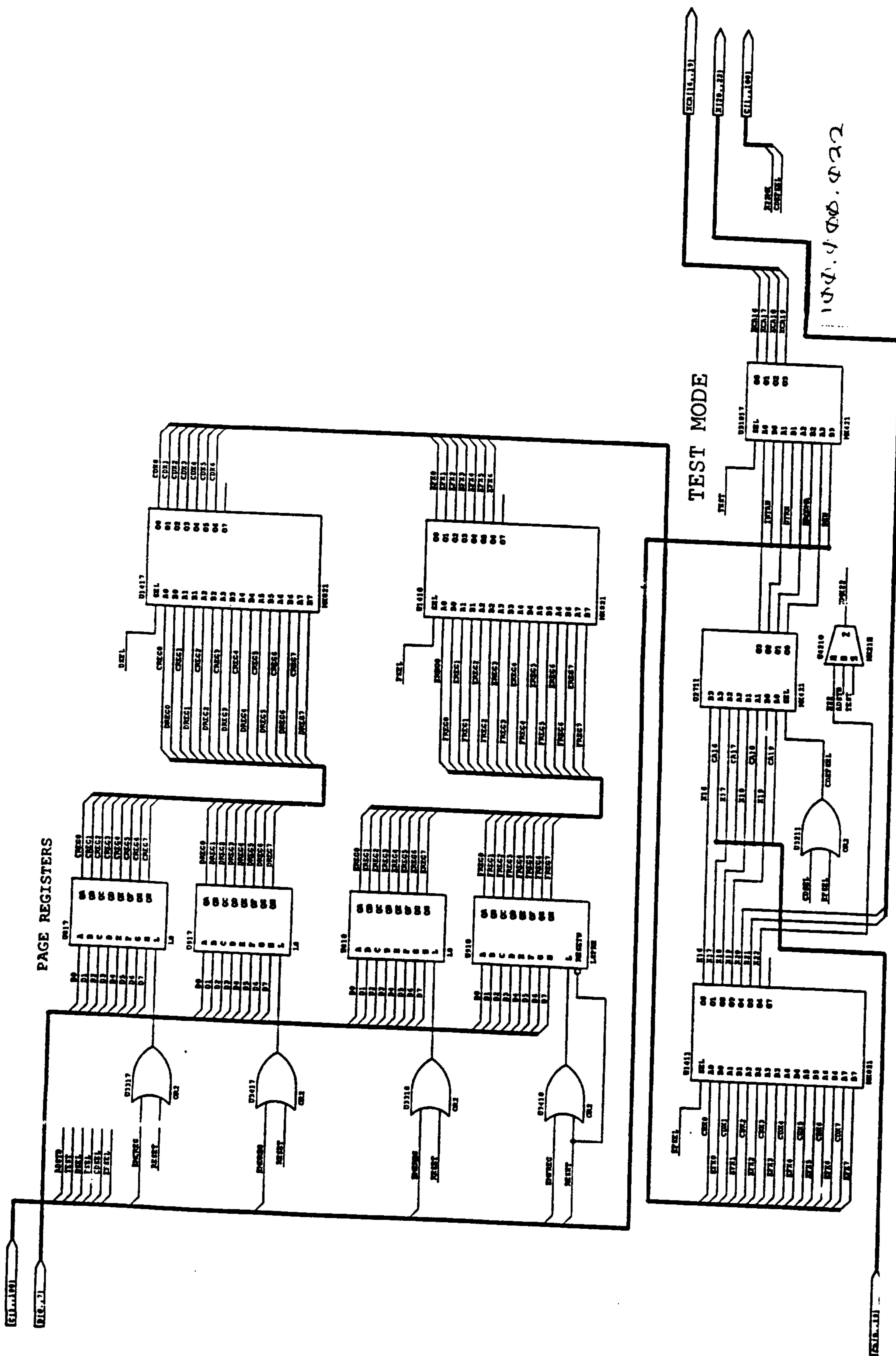


140,000,000

Fig. 11U

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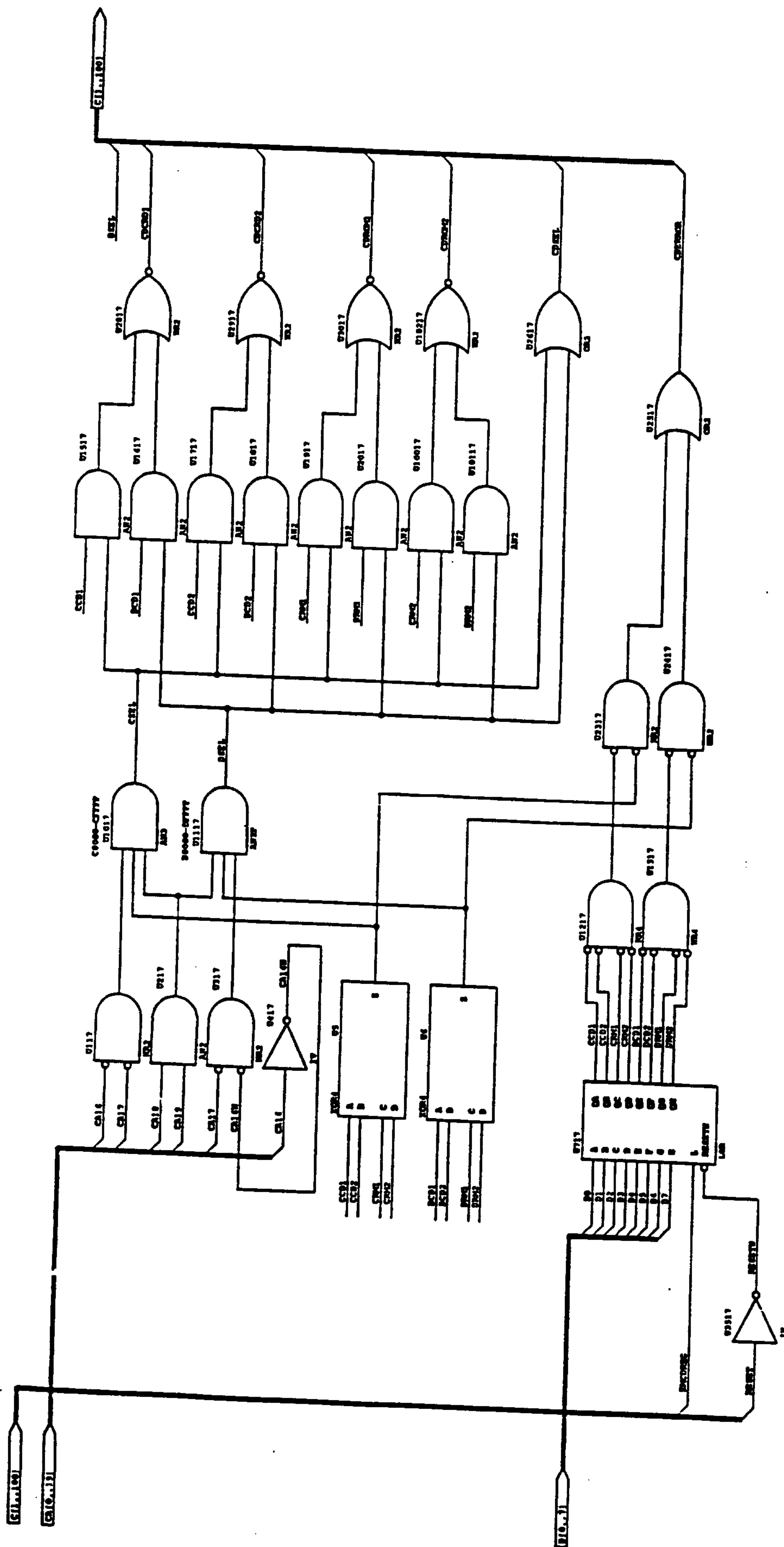
Fig. 11V



417

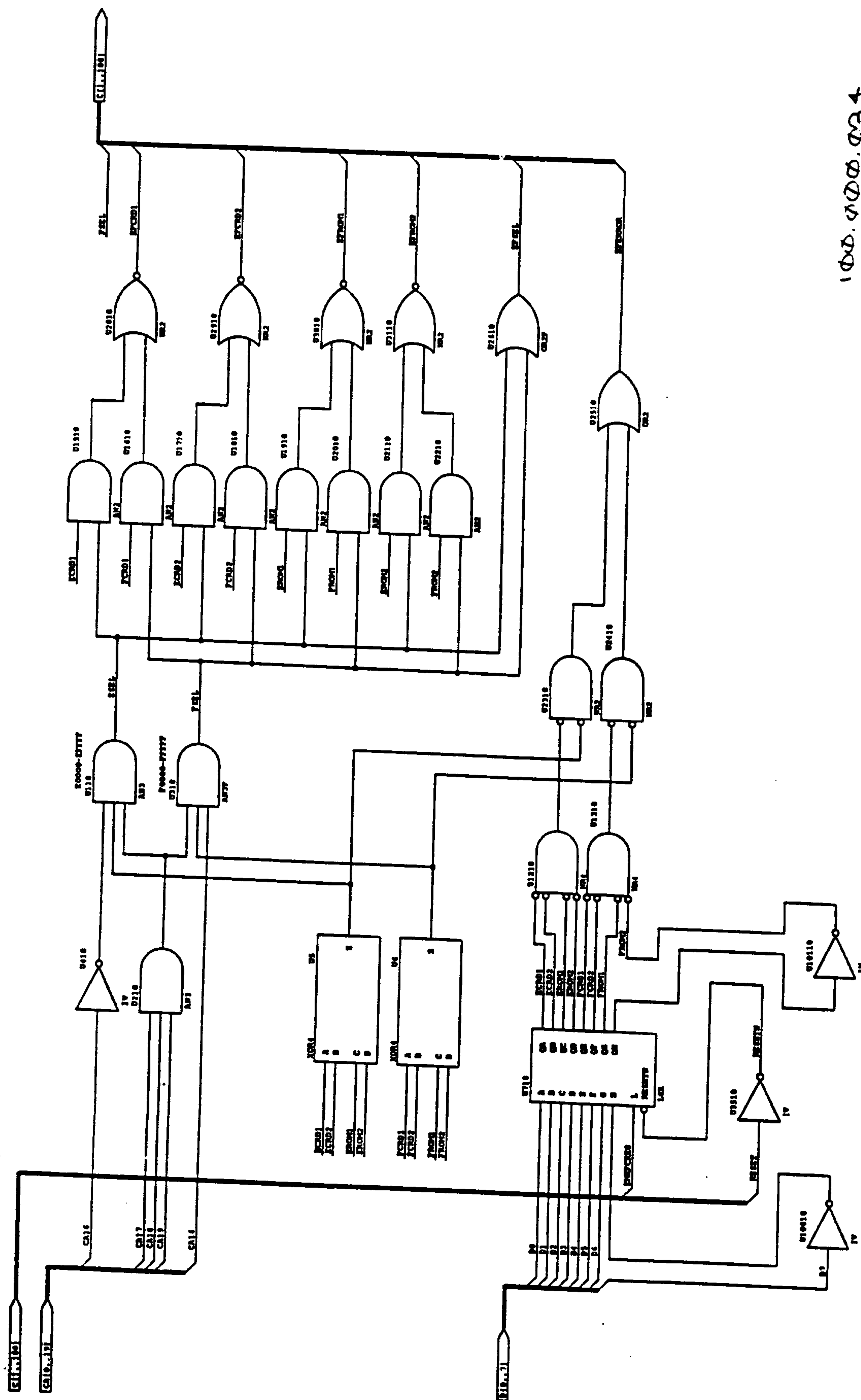
Fig. 11W

100, 400, 423



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1. $\Phi \Psi$. $\Psi \Psi \Psi$. $\Psi \Psi \Psi$



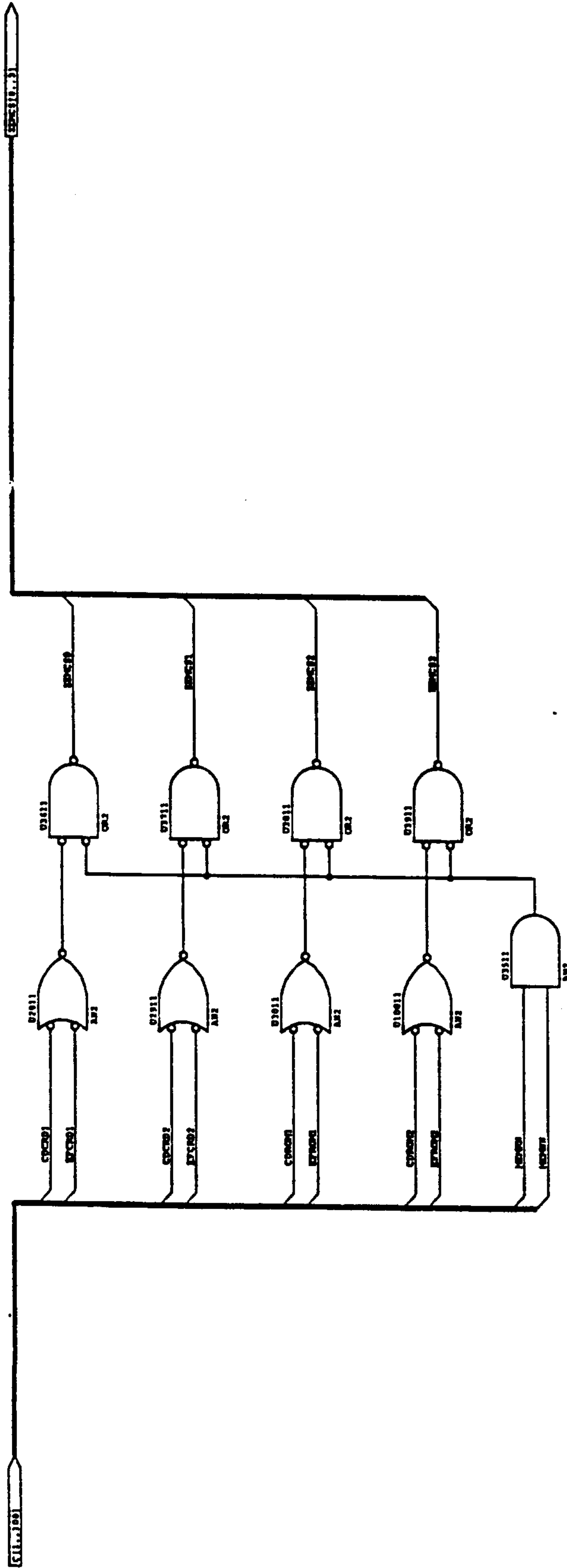
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117

Fig.

140.000.025

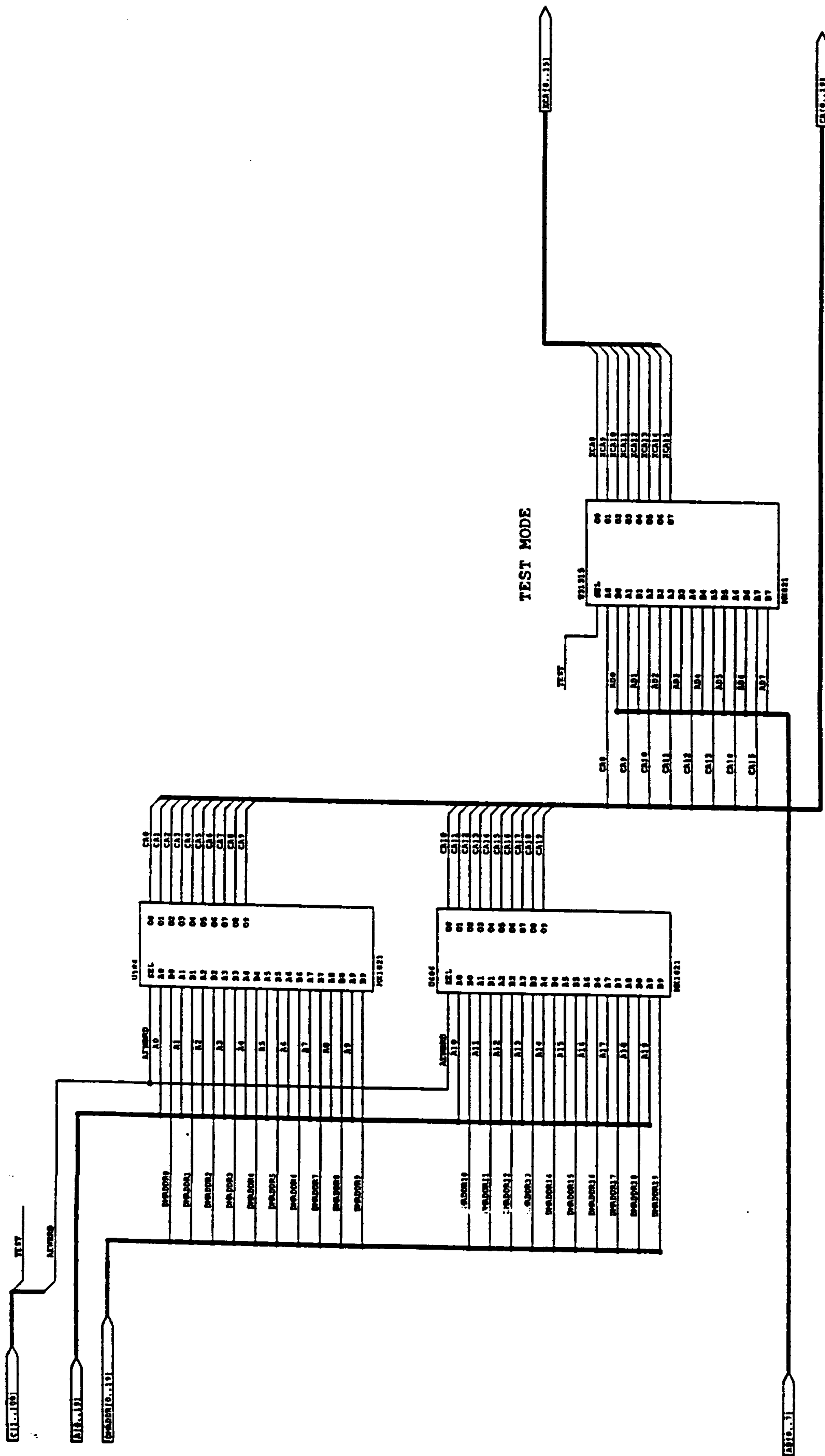


120

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Fig. 11 Z

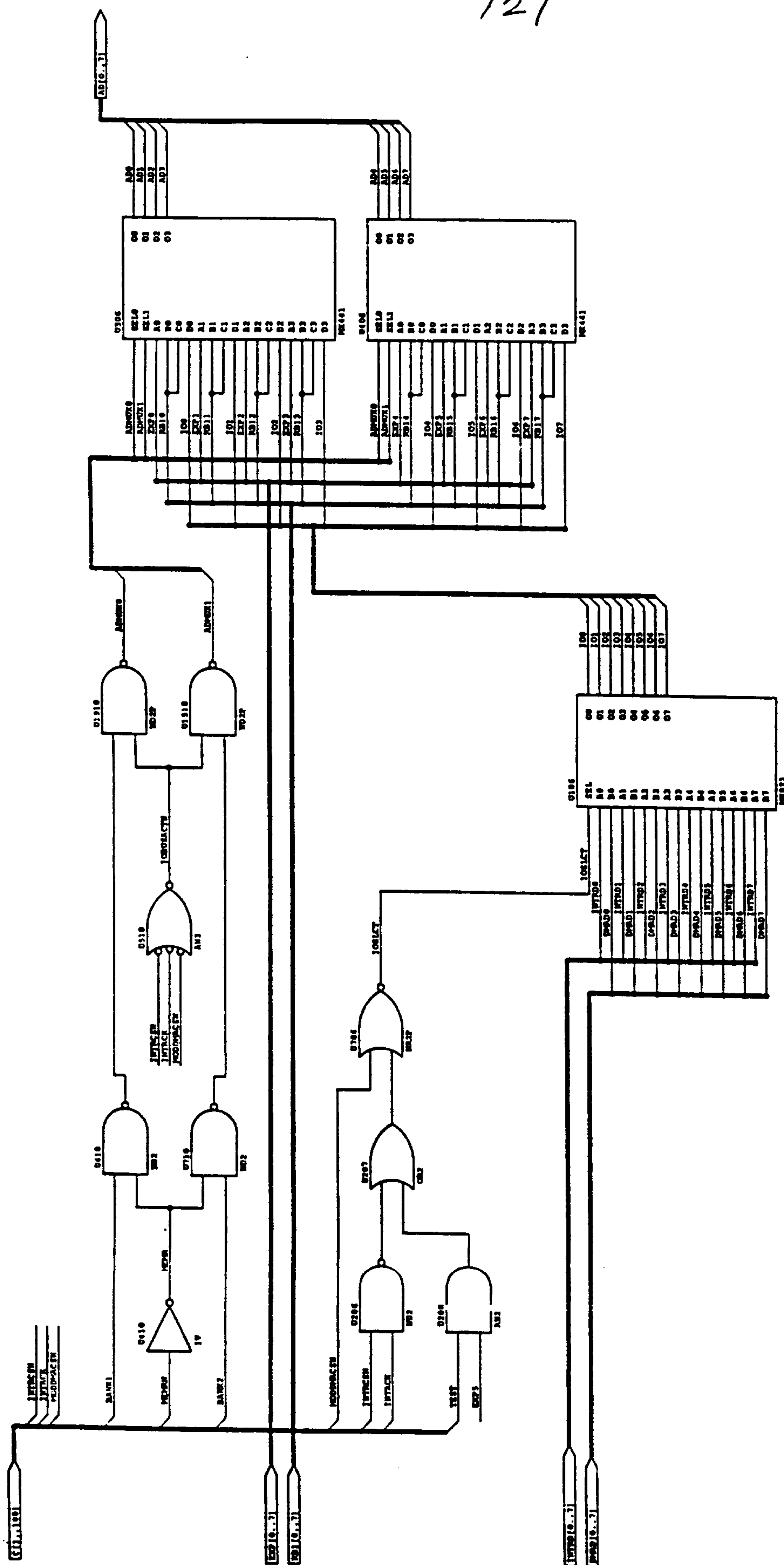
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Fig. 11A

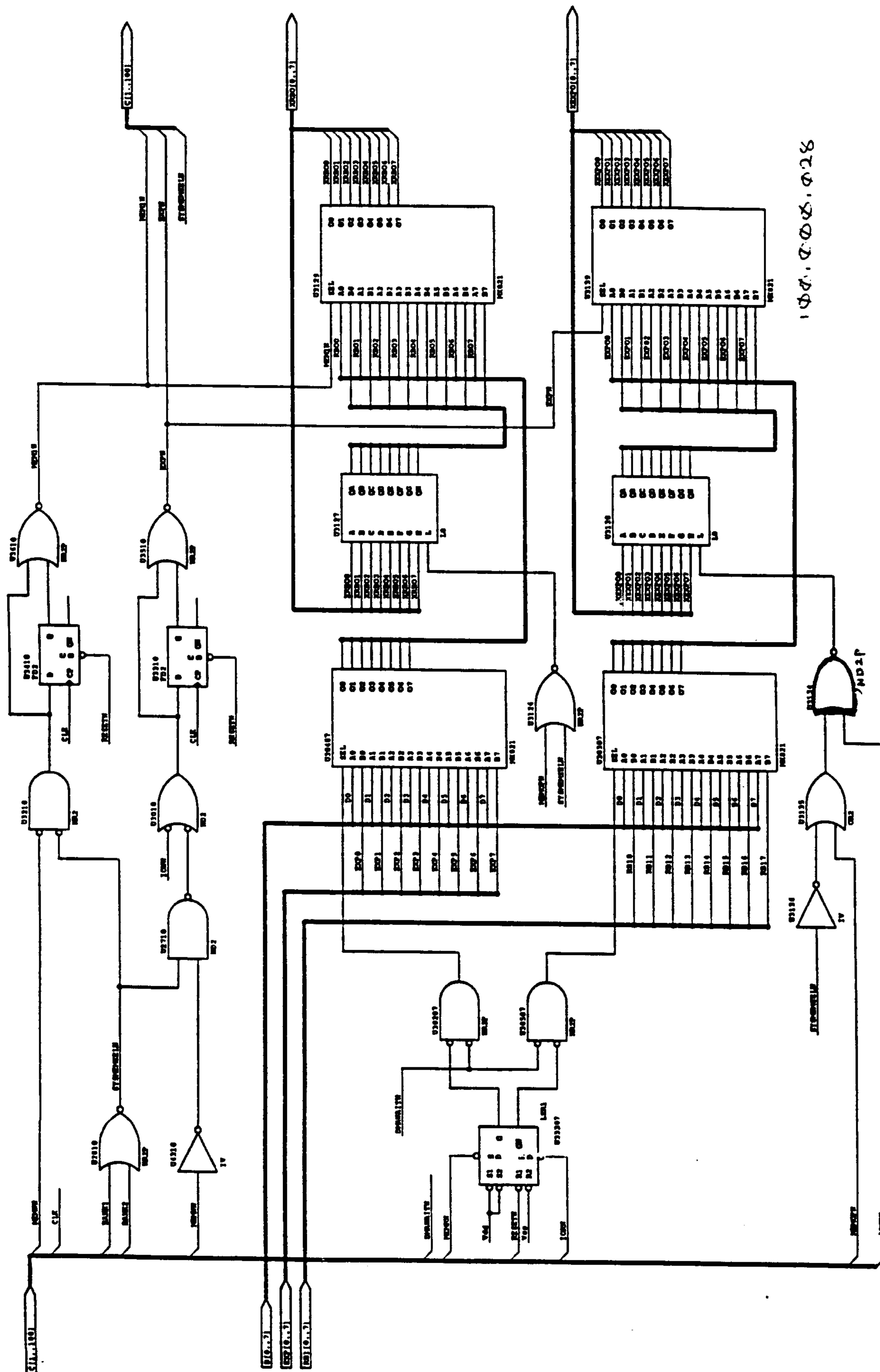
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Fig. 11A

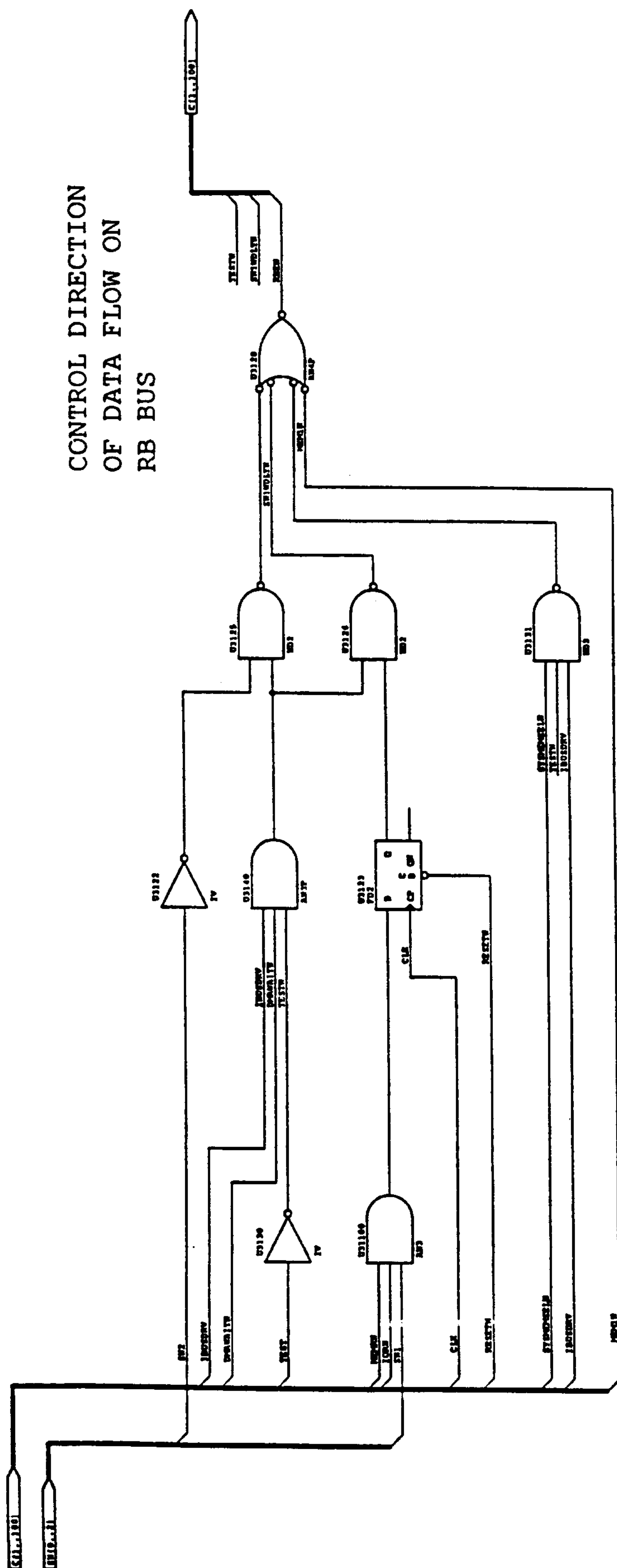


123

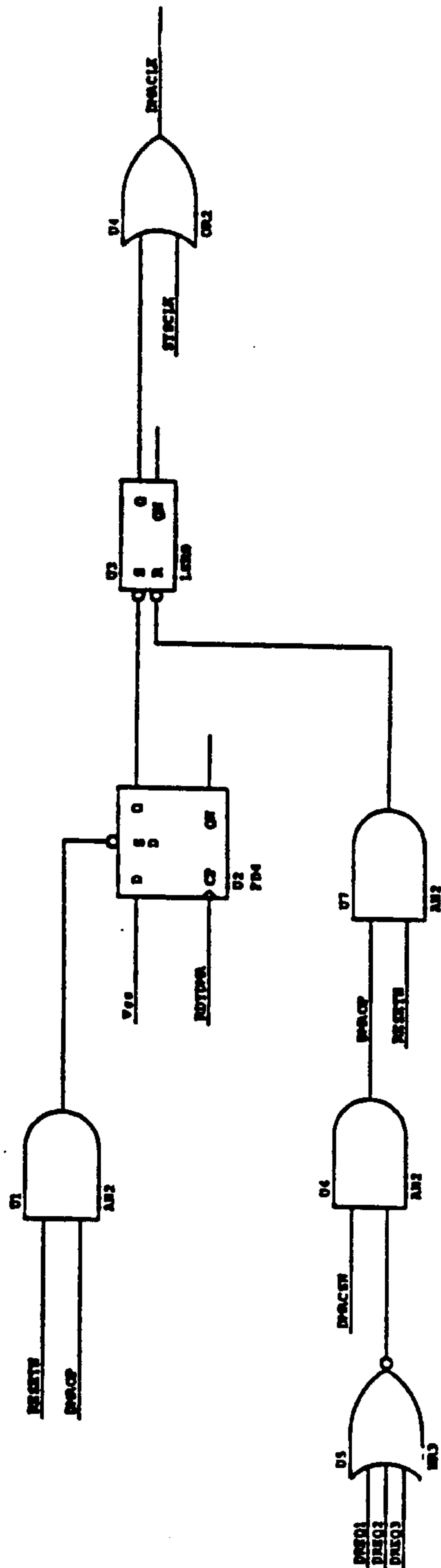
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Fig. 11 AC58

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100.000.030

Fig. 11 Ad