Title: 3D INTERCONNECT WITH PROTRUDING CONTACTS

Abstract: This invention relates to a semiconductor having protruding contacts comprising, a first semiconductor substrate (2) having at least one interconnect (8) located substantially within the first substrate (2), and a second semiconductor substrate (20) having at least one protruding contact point (26) that substantially contacts at least one interconnect (8).
Declarations under Rule 4.17:
— as to the identity of the inventor (Rule 4.17(i))
— as to applicant’s entitlement to apply for and be granted a patent (Rule 4.17(ii))
— as to the applicant’s entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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3D INTERCONNECT WITH PROTRUDING CONTACTS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a semiconductor having protruding contacts comprising, a first semiconductor substrate having at least one interconnect located substantially within the first substrate, and a second semiconductor substrate having at least one protruding contact point that substantially contacts at least one interconnect.

Description of the Related Art

[0002] Prior to the present invention, as set forth in general terms above and more specifically below, it is known in the semiconductor art, that two semiconductor substrates can be joined together at low temperatures by using well-known plasma-enhanced bonding processes. These low-temperature substrate joining techniques can be used to package MEMS (microelectromechanical systems) or NEMS (nanoelectromechanical systems) devices hermetically as well as 3-D wafer stacking. With respect to these low-temperature substrate joining techniques, the surface of the substrates to be joined need to be flat and very smooth (<20A rms surface roughness over 2 μm×2μm). Consequently, the surfaces are usually planarized with chemical mechanical polishing (CMP).

[0003] It is well known that the CMP planarization process creates some unique challenges for wafer-to-wafer interconnect applications since it is difficult to planarize the interconnect plug (or contact points) and the surrounding area evenly. The interconnect between two substrates may fail if dishing on the plugs occurs during the CMP process. Also, plasma-enhanced bonding may fail if the plugs
surfaces are higher than the surrounding area, which prevents the two substrates from contacting at the atomic level.

[0004] It is also known, in the semiconductor art, that compliant intermediate layers (such as BCB (benzocyclobutene)) are often used to adhere two substrates together as well as to form an interconnect at the same time. This approach works fine for many 3-D interconnect applications, but does not work when both 3-D interconnect and hermetic packaging are required since BCB is not hermetic.

[0005] It is further known, in the semiconductor art, that Au bump or solder ball techniques can be used to flip-chip bond one substrate to another. However, none of these techniques provide both a good electrical interconnect between the substrates and hermetic packaging at the wafer level as the bumps or balls tend to cause a standoff between the circuits or substrates. The interconnect density is also limited with this approach.

[0006] Finally, it is known, in the interconnect art, to bond the interconnect to the pad of the circuit device. Typical techniques involve heat, eutectic bonding, electrical bonding, and/or mechanical bonding. However, many of these techniques do not provide an adequate bond for a variety of reasons.

[0007] It is apparent from the above that there exists a need in the semiconductor art for a semiconductor construction technique that works with both 3-D interconnect and hermetic packaging, but which at the same time allows the two substrates to be efficiently bonded so that they contact each other at the atomic level. It is a purpose of this invention to fulfill this and other needs in the art in a manner more apparent to the skilled artisan once given the following disclosure.

**SUMMARY OF THE INVENTION**

[0008] Generally speaking, an embodiment of this invention fulfills these needs by providing a semiconductor having protruding contacts comprising, a first semiconductor substrate having at least one interconnect located substantially within the first substrate, and a second semiconductor substrate having at least one protruding contact point that substantially contacts at least one interconnect.

[0009] In certain preferred embodiments, the first semiconductor substrate includes a CMOS (complementary metal oxide semiconductor) circuit on a top surface and through-silicon interconnect plugs. Also, the first semiconductor substrate may
include an optical MEMS or NEMS device. Also, the surface of the interconnect
that contacts the protruding contact point of the second substrate may be thinned
and chemically mechanically polished.

[00010] In another further preferred embodiment, the second semiconductor
substrate may include CMOS or other high density (nanotechnology devices)
circuitry and at least one protruding contact point. Also, the contact point is formed
by layering various metal and dielectric films, including a compressive dielectric
film, wherein etching is employed to cause the compressive dielectric film to bow up
slightly and create a protruding contact point.

[00011] The preferred semiconductor, according to various embodiments of
the present invention, offers the following advantages: ease of assembly; excellent
electrical contact characteristics; and good durability. In fact, in many of the
preferred embodiments, these factors of ease of assembly and excellent electrical
contact characteristics are optimized to an extent that is considerably higher than
heretofore achieved in prior, known semiconductor devices.

[00012] The above and other features of the present invention, which will
become more apparent as the description proceeds, are best understood by
considering the following detailed description in conjunction with the accompanying
drawings, wherein like characters represent like parts throughout the several views
and in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[00013] Figures 1a and 1b are a schematic illustrations of a semiconductor
substrate having a through-silicon interconnect with Figure 1b illustrating a detailed
view of the end of the through-silicon interconnect, according to one embodiment of
the present invention;

[00014] Figure 2 is a schematic illustration of a second semiconductor
substrate with CMOS circuitry and contact points, to be bonded to the first
substrate, according to the ongoing embodiment of the present invention;

[00015] Figure 3 is a schematic illustration of a patterned sacrificial film prior
to forming a contact pad, according to the ongoing embodiment of the present
invention;
[00016] Figure 4 is a schematic illustration of a deposited compressive film that will form a contact pad, according to the ongoing embodiment of the present invention;

[00017] Figures 5a and 5b are schematic illustrations of a planarized contact pad prior to release, wherein Figure 5a is the cross sectional view and Figure 5b is the top-down view, according to the ongoing embodiment of the present invention;

[00018] Figures 6a and 6b are schematic illustrations of a patterned photoresist that will define the contact pads during a subsequent etching process, wherein Figure 6a is the cross sectional view and Figure 6b is the top-down view, according to the ongoing embodiment of the present invention;

[00019] Figures 7a and 7b are schematic illustrations of a released contact pad after removal of the sacrificial layer wherein Figure 7a is the cross sectional view and Figure 7b is the top-down view, according to the ongoing embodiment of the present invention;

[00020] Figures 8a and 8b are schematic illustrations of the final interconnect assembly formed by plasma bonding substrates one and two together, wherein Figure 8b illustrates a detailed view of a contact point between substrates one and two, according to the ongoing embodiment of the present invention;

[00021] Figure 9 is a schematic illustration of face-to-face bonding with an optical MEMS device, according to another embodiment of the present invention; and

[00022] Figure 10 is a schematic illustration of face-to-back wafer bonding with high density circuitry, according to still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[00023] With reference first to Figure 1, there is illustrated one preferred embodiment for use of the concepts of this invention. Figure 1 illustrates a first semiconductor substrate 2. Substrate 2 includes, in part, complementary metal oxide semiconductor (CMOS) 6, and through silicon interconnect plugs 8. Preferably, substrate 2 may be conventionally thinned and chemically mechanically polished (CMP) on the backside to prepare the plugs 8 for bonding. Also, through silicon interconnect plugs can be constructed of any suitable material such as
tungsten, copper, gold or the like. Finally, each substrate 2 and 20(Fig. 2) may not contain through silicon interconnect plugs 8 and the two substrates can be bonded together face-to-face.

[00024] With respect to Figure 1b, a detailed view of the dished surface 10 of the through silicon interconnect plug 8 is illustrated. The dished surface 10 typically results from the CMP process. It is to be understood that the dished surface 10 that opposes the protruding contact point 26 (Fig. 2) does not have to be recessed, it can be recessed, flat or a released compressively stressed protruding contact, as well.

[00025] With respect to Figure 2, a second semiconductor substrate 20 is illustrated. Substrate 20 includes, in part, substrate backside 22, CMOS 24, and contact points 26. The details of how contact points 26 are fabricated will be discussed in relation to Figures 3-8.

[00026] With respect to Figure 3, patterned semiconductor substrate 20 is illustrated. Substrate 20 includes, in part, CMOS 24, and sacrificial film 32. As shown in Figure 3, CMOS 24 and sacrificial film 32 are conventionally patterned to form a contact pad. Also, sacrificial film 32, preferably, is a silicon film. It is to be understood that the sacrificial layer can be any material that can be selectively etched and removed relative to other layers or materials in the device.

[00027] With respect to Figure 4, semiconductor wafer 20 is illustrated with compressive and contact films deposited. Wafer 20 includes, in part, CMOS 24, sacrificial film 32, compressive dielectric film 42, and metallic contact film 44. As shown in Figure 4, compressive dielectric film 42 and metallic contact film 44 are conventionally deposited on top of sacrificial layer 32 and CMOS 24. Also, compressive dielectric film 42, preferably, is constructed of Si₃N₄. It is to be understood that the compressive film 42 can also be other materials as long as it is compressively stressed in the final device. Finally, metallic contact film 44, preferably, is constructed of any suitable metallic material such as a noble metal (for example, gold) various solder materials, or typical multi-metal layer contact structures such as Cu/Au and Cu/Ni/Au. Finally, it is to be understood that the metal layer 44 could, with the proper materials set, theoretically be the compressive layer, as well.

[00028] With respect to Figures 5a and 5b, semiconductor wafer 20 is illustrated. After contact layers have been deposited on semiconductor wafer 20
(Fig. 4), it is planarized according to a conventional CMP process, such as the Damascene process. As can be seen in Figure 5a, at this point wafer 20 includes, in part, CMOS 24, sacrificial film 32, compressive dielectric film 42, and metallic contact film 44. As can be seen in Figure 5b, only CMOS 24 and metallic film 44 are exposed after the planarization process.

[00029] With respect to Figures 6a and 6b, semiconductor wafer 20 is illustrated with patterned photoresist prior to etching to define the contacts. After semiconductor wafer 20 (Fig. 5) has been planarized, it is patterned and etched, according to conventional techniques. Semiconductor wafer 20 at this point includes, in part, CMOS 24, sacrificial film 32, compressive dielectric film 42, metallic contact film 44, patterning film 62, and contact point 64. Preferably, patterning film 62 is constructed of any suitable material such as any suitable polymeric material for patterning via photo-imaging, embossing, imprinting or other common techniques. As can be seen in Figure 6a, patterning film 62 is conventionally deposited on metallic film 44. Compressive dielectric film 42 and metallic film 44 are then conventionally patterned and etched to form contact point 64. During this patterning and etching process, sacrificial film 32 is also exposed, as shown in Figure 6b. It is to be understood that the contact points can be patterned in other shapes, in addition to rectangular.

[00030] With respect to Figures 7a and 7b, semiconductor wafer 20 is illustrated after removal of sacrificial layer 32. After semiconductor wafer 20 (Fig. 6) has been patterned and etched (Fig 6), it is again etched, according to conventional techniques, such as XeF₂ or SF₆ plasma etching. Semiconductor wafer 20 at this point includes, in part, substrate CMOS 24, compressive dielectric film 42, metallic contact film 44, and released contact pad 72. As can be seen in Figure 7a, released contact pad 72 is formed after sacrificial film 32 is etched away underneath compressive dielectric film 42 and metallic contact film 44. Once the contact points are released, compressive dielectric film 42 causes released contact pad 72 to bow up slightly and protrude from the planarized surface. The patterning film 62 (Fig. 6) is then conventionally stripped. Figure 7b shows a top-down view of semiconductor wafer 20 with CMOS 24 and released contact pad 72 exposed.

[00031] With respect to Figures 8a and 8b, completed semiconductor interconnect assembly 80 is illustrated. After semiconductor wafer 20 (Fig. 7) has been completed, it is then contacted with semiconductor substrate 2 (Fig. 2) in
order to form semiconductor interconnect assembly 80. Semiconductor
interconnect assembly 80 includes, in part, CMOS 6, through silicon interconnect
plugs 8, CMOS 24, and contact points 26. As can be seen in Figure 8a,
semiconductor substrate 2 and semiconductor wafer 20 are conventionally plasma
treated (such as in N₂, O₂ or Ar plasma) and bonded together. It is to be understood
that interconnect assembly 80 maybe located on the top side, the back side or
multiple sides of each substrate 2 (Fig. 1) and 20 (Fig. 2).

[00032] With respect to Figure 8b, contact pad 72 of semiconductor wafer 20
protrudes upwards towards dished surface 10 of plug 8 on semiconductor substrate
2. In this manner, an excellent interconnect is insured even when the surfaces of
the through silicon interconnect plugs 8 are slightly dished.

[00033] With respect to Figure 9, semiconductor 90 is illustrated.
Semiconductor 90 includes, in part, glass substrate 92, CMOS 93, interconnects
94, an optical MEMS or NEMS devices 95, CMOS 96 and released contact pads
97. As illustrated in Figure 9, a face-to-face bonding of the glass substrate and the
MEMS device is achieved through a conventional plasma enhanced bonding
process. In this manner, released contact pads 97 protrude upward towards
interconnect 94 in order to form an excellent interconnect between the two devices
in a similar manner as discussed above with respect to Figures 1-8.

[00034] Finally, with respect to Figure 10, semiconductor 100 is illustrated.
Semiconductor 100 includes, in part, substrate backside or lid 102, through silicon
interconnect plugs 104, substrate backside 106, high density circuitry devices 108,
and released contact pads 110. High density circuitry devices 108 can be,
preferably, nanotechnology devices. As illustrated in Figure 10, lid 102 will not only
provide a cap over substrate 106 and high density circuitry devices 108, but also
increase the number of input-output counts.

[00035] While the present invention has been illustrated with respect to
particular semiconductor devices, it is to be understood that the present invention
can also be utilized in other devices such as, but not limited to, non-CMOS devices
(JetMOS, sensors, etc), NEMS devices, photonics devices, various medical
devices, FLEX circuits, PCBs (Printed Circuit Boards), any type of protruding
contacts to flat contacts, any type of protruding contacts to protruding contacts, and
various multi-layer (2 or more) substrate stacks without deviating from the scope of
the present invention.
[00036] Also, the present invention can be embodied in any computer-readable medium for use by or in connection with an instruction-execution system, apparatus or device such as a computer/processor based system, processor-containing system or other system that can fetch the instructions from the instruction-execution system, apparatus or device, and execute the instructions contained therein. In the context of this disclosure, a "computer-readable medium" can be any means that can store, communicate, propagate or transport a program for use by or in connection with the instruction-execution system, apparatus or device. The computer-readable medium can comprise any one of many physical media such as, for example, electronic, magnetic, optical, electromagnetic, infrared, or semiconductor media. More specific examples of a suitable computer-readable medium would include, but are not limited to, a portable magnetic computer diskette such as floppy diskettes or hard drives, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory, or a portable compact disc. It is to be understood that the computer-readable medium could even be paper or another suitable medium upon which the program is printed, as the program can be electronically captured, via, for instance, optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a single manner, if necessary, and then stored in a computer memory.

[00037] Those skilled in the art will understand that various embodiment of the present invention can be implemented in hardware, software, firmware or combinations thereof. Separate embodiments of the present invention can be implemented using a combination of hardware and software or firmware that is stored in memory and executed by a suitable instruction-execution system. If implemented solely in hardware, as in an alternative embodiment, the present invention can be separately implemented with any or a combination of technologies which are well known in the art (for example, discrete-logic circuits, application-specific integrated circuits (ASICs), programmable-gate arrays (PGAs), field-programmable gate arrays (FPGAs), and/or other later developed technologies. In preferred embodiments, the present invention can be implemented in a combination of software and data executed and stored under the control of a computing device.

[00038] It will be well understood by one having ordinary skill in the art, after having become familiar with the teachings of the present invention, that software
applications may be written in a number of programming languages now known or later developed.

[00039] Once given the above disclosure, many other features, modifications or improvements will become apparent to the skilled artisan. Such features, modifications or improvements are, therefore, considered to be a part of this invention, the scope of which is to be determined by the following claims.

[00040] What is claimed is:
CLAIMS

1. A semiconductor having protruding contacts comprising:
   a first semiconductor substrate (2) having at least one interconnect (8)
   located substantially within the first substrate (2); and
   a second semiconductor substrate (20) having at least one protruding
   contact point (26) that substantially contacts the at least one interconnect (8).

2. The semiconductor, as in Claim 1, wherein the first semiconductor
   substrate (20) is further comprised of:
   a first substrate surface (22); and
   a first complementary metal oxide semiconductor (24) operatively connected
   to the first substrate surface.

3. The semiconductor, as in Claim 1, wherein the at least one
   interconnect (8) is further comprised of:
   a through silicon interconnect plug.

4. The semiconductor, as in Claim 1, wherein the at least one
   interconnect (8) is further comprised of:
   a planar or dished surface (10) located substantially at one end of the
   interconnect (8) such that the dished surface interacts with the protruding contact
   point (26).

5. The semiconductor, as in Claim 1, wherein the second
   semiconductor substrate is further comprised of:
   a second substrate surface (4); and
   a second complementary metal oxide semiconductor (6) operably connected
   to the second substrate surface.
6. The semiconductor, as in Claim 5, wherein the at least one protruding contact point (26) is further comprised of:
   a compressive dielectric film (42) operably connected to the second complementary metal oxide semiconductor (6);
   a metallic film (44) operably connected to the compressive dialectic film (42);
   and
   a released contact pad (72) operatively connected to the metallic contact film (44).

7. The semiconductor, as in Claim 6, wherein the semiconductor is further comprised of:
   a sacrificial film (32) located substantially under the compressive dielectric film (42) such that the sacrificial film (32) is subsequently removed in order to form said protruding contact point (26).

8. The semiconductor, as in Claim 7, wherein the sacrificial film is further comprised of:
   silicon.

9. The semiconductor, as in Claim 6, wherein the compressive dielectric film is further comprised of:
   Si₃N₄.

10. The semiconductor, as in Claim 6, wherein the metallic contact film is further comprised of:
    a noble metal.

11. The semiconductor, as in Claim 6, wherein the metallic contact film is further comprised of:
    a solder material.

12. The semiconductor, as in Claim 1, wherein the first substrate is further comprised of:
    a glass substrate; and
a third complementary metal oxide semiconductor (93) operatively connected to the glass substrate.

13. The semiconductor, as in Claim 1, wherein the second substrate is further comprised of:
   a microelectronic mechanical systems (MEMS) device (95); and
   a fourth complementary metal oxide semiconductor (96) operably connected to the MEMS or NEMS device (95).

14. The semiconductor, as in Claim 1, wherein the first substrate (2) is further comprised of:
   a third substrate (102).

15. The semiconductor, as in Claim 1, wherein the second substrate (20) is further comprised of:
   a fourth substrate (106); and
   at least one high density circuitry device (108) operatively connected to the fourth substrate.

16. The semiconductor, as in Claim 15, wherein the high density circuitry device is further comprised of:
   a nanotechnology device.

17. A method for constructing a semiconductor, comprising the steps of:
   constructing a first semiconductor substrate (2) having at least one interconnect (8) located substantially within the first substrate (2); and
   constructing a second semiconductor substrate (20) having at least one protruding contact point (26) that substantially contacts the at least one interconnect (8).
18. The method, as in Claim 17, wherein the step of constructing the first semiconductor substrate is further comprised of the step of:
   installing a first complementary metal oxide semiconductor (CMOS) (6) substantially within a first substrate (20) such that the CMOS interacts with the at least one interconnect.

19. The method, as in Claim 18, wherein the step of installing the CMOS is further comprised of the step of:
   thinning and polishing a portion of the first substrate.

20. The method, as in Claim 19, wherein the polishing step is further comprised of the step of:
   chemically mechanically polishing the first substrate.

21. The method, as in Claim 17, wherein the step of constructing the second semiconductor substrate is further comprised of the step of:
   installing a second CMOS (24) substantially within a second substrate (20) such that the CMOS interacts with the at least one protruding contact point (26).

22. The method, as in Claim 21, wherein the method is further comprised of the steps of:
   patterning the second CMOS (24); and
   patterning a sacrificial film (32) substantially over the second CMOS (24) in order to form a contact pad.

23. The method, as in Claim 22, wherein the method is further comprised of the steps of:
   depositing a compressive dielectric film (42) substantially over the second CMOS and the sacrificial film (32); and
   depositing a metallic contact film (44) substantially over the compressive dielectric film (42).
24. The method, as in Claim 23, wherein the method is further comprised of the step of:
   planarizing the metallic film (44).

25. The method, as in Claim 24, wherein the planarizing step is further comprised of the step of:
   chemically mechanically polishing the metallic film (44).

26. The method, as in Claim 24, wherein the method is further comprised of the step of:
   patterning a film substantially over the metallic contact film.

27. The method, as in Claim 26, wherein the method is further comprised of the step of:
   patterning and etching the metallic contact film (44) and the compressive dielectric film (42) in order to form a contact point (26).

28. The method, as in Claim 27, wherein the method is further comprised of the step of:
   exposing the sacrificial film (32).

29. The method, as in Claim 28, wherein the method is further comprised of the step of:
   etching the sacrificial film (32) such that the contact point (26) is released which causes the contact pad to bow up slightly and protrude from the planarized surface.

30. The method, as in Claim 29, wherein the method is further comprised of the step of:
   stripping the patterning film from the metallic contact film (44).

31. A system for constructing a semiconductor, comprising:
   means for constructing a first semiconductor substrate having at least one interconnect located substantially within the first substrate; and
means for constructing a second semiconductor substrate (20) having at least one protruding contact point (26) that substantially contacts at least one interconnect (8).

32. The system, as in Claim 31, wherein the means for constructing the first semiconductor substrate (2) is further comprised of:
   means for installing a first complementary metal oxide semiconductor (CMOS) (6) substantially within a first substrate such that the CMOS interacts with the at least one interconnect (8).

33. The system, as in Claim 32, wherein the means for installing the CMOS is further comprised of:
   means for thinning and polishing a portion of the first substrate (2).

34. The system, as in Claim 33, wherein the means for polishing is further comprised of:
   means for chemically mechanically polishing the first substrate (2).

35. The system, as in Claim 31, wherein the means for constructing the second semiconductor substrate is further comprised of:
   means for installing a second CMOS (24) substantially within a second substrate (20) such that the CMOS (24) interacts with the at least one protruding contact point (26).

36. The system as in Claim 35, wherein the system is further comprised of:
   means for patterning the second CMOS (24); and
   means for patterning a sacrificial film (32) substantially over the second CMOS (24) in order to form a contact pad.

37. The system, as in Claim 36, wherein the system is further comprised of:
   means for depositing a compressive dielectric film (42) substantially over the second CMOS (24) and the sacrificial film (32); and
means for depositing a metallic contact film (44) substantially over the compressive dielectric film (42).

38. The system, as in Claim 37, wherein the system is further comprised of:
means for planarizing the metallic contact film (44).

39. The system, as in Claim 38, wherein the means for planarizing is further comprised of:
means for chemically mechanically polishing the metallic contact film (44).

40. The system, as in Claim 37, wherein the system is further comprised of:
means for patterning a film substantially over the metallic contact film (44).

41. The system, as in Claim 40, wherein the system is further comprised of:
means for patterning and etching the metallic contact film (44) and the compressive dielectric film (42) in order to form a contact point (26).

42. The system, as in Claim 41, wherein the system is further comprised of:
means for exposing the sacrificial film (32).

43. The system, as in Claim 42, wherein the system is further comprised of:
means for etching the sacrificial film (32) such that the contact point (26) is released which causes the contact pad to bow up slightly and protrude from the planarized surface.

44. The system, as in Claim 43, wherein the system is further comprised of:
means for stripping the patterning film from the metallic film (44).
Fig. 1
Fig. 2
Fig. 3
SELECTING AN ELLIPTIC CURVE $E_q$ FOR VALIDATING A COMPUTATION ON A SPECIFIED ELLIPTIC CURVE $E_p$

DERIVING A THIRD ELLIPTIC CURVE FROM $E_p$ AND $E_q$

PROJECTING POINTS $P_{in}$ ONTO $E_n$, EACH $P_{in}$ A PROJECTION OF POINTS $[P_{ip}, P_{iop}]$

PERFORMING A COMPUTATION ON $E_n$ USING POINTS $P_{in}$

PERFORMING A COMPUTATION ON $E_q$ USING ONE OR MORE POINTS $P_{iq}$

EXTRACTING FROM THE COMPUTATION ON $E_n$ A PREDICTED RESULT OF THE COMPUTATION TO BE VALIDATED

IF THE PREDICTED RESULT OF THE COMPUTATION ON $E_q$ IS THE ACTUAL RESULT, VALIDATING THE RESULT PREDICTED IN THE PREVIOUS STEP

Fig. 4B

Fig. 4A
500

Fig. 5
Fig. 6
Fig. 7A

Fig. 7B
### Fig. 8A

<table>
<thead>
<tr>
<th>Case</th>
<th>Description</th>
<th>Case avoided if</th>
<th>Input at top of loop</th>
<th>Input</th>
<th>Input</th>
<th>Steps 2.1.1-2.1.3</th>
<th>Steps 2.1.1-2.1.3</th>
<th>Step 2.1.4</th>
<th>Condition step 2.1.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Typical. No adj.</td>
<td>$k_{eq}$</td>
<td>adj</td>
<td>$k_i$</td>
<td>$k_i'$</td>
<td>$k_{eq}'$</td>
<td>$k_{eq} = [2^a k_{eq}]_{eq}$</td>
<td>$</td>
<td>k_{eq}' + k_i'</td>
</tr>
<tr>
<td>1</td>
<td>Multiple of $n_e$ encountered. Adj. propagated</td>
<td>$[2^a(n_e-k_i)]_{eq}$</td>
<td>0</td>
<td>$&gt;0$</td>
<td>$k_i$</td>
<td>0</td>
<td>$[2^a k_{eq}]_{eq}$</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Double encountered. Adj. propagated</td>
<td>$[2^a k_{eq}]_{eq}$</td>
<td>0</td>
<td>$=1$</td>
<td>$k_i$</td>
<td>0</td>
<td>1</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Double encountered and resolved</td>
<td>$[2^a k_{eq}]_{eq}$</td>
<td>0</td>
<td>$&gt;1$</td>
<td>$k_i$</td>
<td>0</td>
<td>$k_i$</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Previous multiple of $n_e$. Adj. propagated</td>
<td>$n_e - 1$</td>
<td>1</td>
<td>$=0$</td>
<td>$2^a$</td>
<td>$k_i = 0$</td>
<td>$n_e - 2^a$</td>
<td>yes</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Previous multiple of $n_e$. Adj. resolved</td>
<td>$n_e - 1$</td>
<td>1</td>
<td>$&gt;0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$n_e - 2^a$</td>
<td>yes</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Previous double, Adj. resolved</td>
<td>$[2(k_{eq} - 1)]<em>{eq}$, $k</em>{eq} = 1$</td>
<td>1</td>
<td>$=0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$2^a$</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Previous double, adj. resolved. Multiple of $n_e$ encountered. Adj. propagated</td>
<td>$n_e &gt; 3*2^{a-1}$</td>
<td>$[2(k_{eq} - 1)]<em>{eq}$, $k</em>{eq} = 1$</td>
<td>1</td>
<td>$&gt;0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$2^a$</td>
<td>no</td>
</tr>
<tr>
<td>8</td>
<td>Previous double, Adj. resolved</td>
<td>$[2(k_{eq} - 1)]<em>{eq}$, $k</em>{eq} &gt; 1$</td>
<td>1</td>
<td>$&gt;0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$[2^a(2k_{eq} - 1)]_{eq}$</td>
<td>no</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Previous double, adj. resolved. Multiple of $n_e$ encountered. Adj. propagated</td>
<td>$n_e &gt; 2^{a+1}(2^a - 1)$</td>
<td>$[2(k_{eq} - 1)]<em>{eq}$, $k</em>{eq} &gt; 1$</td>
<td>1</td>
<td>$&gt;0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$[2^a(2k_{eq} - 1)]_{eq}$</td>
<td>no</td>
</tr>
<tr>
<td>10</td>
<td>Previous double, Adj. resolved. New double encountered. Adj. propagated</td>
<td>$n_e &gt; 2^{a+1}(2^a - 1)$</td>
<td>$[2(k_{eq} - 1)]<em>{eq}$, $k</em>{eq} &gt; 1$</td>
<td>1</td>
<td>$&gt;0$</td>
<td>$2^a$</td>
<td>$k_i$</td>
<td>$[2^a(2k_{eq} - 1)]_{eq}$</td>
<td>no</td>
</tr>
</tbody>
</table>

Legend: $|x|_{eq}$ represents $x \mod n_e$
<table>
<thead>
<tr>
<th>Case</th>
<th>Condition step 2.1.5</th>
<th>Result after 2.1.5</th>
<th>Result after 2.1.5</th>
<th>Step 2.1.6</th>
<th>Condition step 2.1.7</th>
<th>Result after 2.1.7</th>
<th>Result after 2.1.7</th>
<th>Step 2.1.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>yes</td>
<td>0</td>
<td>1</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>no</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>no</td>
<td>k_i</td>
<td>0</td>
<td>[2^k_i mod n_q]</td>
<td>no</td>
<td>no</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>yes</td>
<td>k_i - 1</td>
<td>1</td>
<td>n_q - 1</td>
<td>yes</td>
<td>no</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>yes</td>
<td>k_i - 1</td>
<td>1</td>
<td>2k_i - 1</td>
<td>no</td>
<td>no</td>
<td>0</td>
<td>2k_i</td>
</tr>
<tr>
<td>4</td>
<td>no</td>
<td>2^k_i - 1</td>
<td>1</td>
<td>n_q - 1</td>
<td>yes</td>
<td>no</td>
<td>0</td>
<td>n_q - 1</td>
</tr>
<tr>
<td>5</td>
<td>no</td>
<td>2^k_i - 1</td>
<td>k_i + 1</td>
<td>n_q - 1</td>
<td>no</td>
<td>no</td>
<td>k_i + 1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>yes</td>
<td>2^k_i - 1</td>
<td>k_i + 1</td>
<td>2^k_i + 1</td>
<td>no</td>
<td>k_i + 1</td>
<td>0</td>
<td>2^k_i + 1</td>
</tr>
<tr>
<td>7</td>
<td>yes</td>
<td>2^k_i - 1</td>
<td>k_i + 1</td>
<td>2^k_i - 1</td>
<td>yes</td>
<td>k_i</td>
<td>n_q - 1</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>no</td>
<td>2^k_i</td>
<td>[2^k_i mod n_q]</td>
<td>no</td>
<td>no</td>
<td>k_i</td>
<td>0</td>
<td>[2^k_i mod n_q]</td>
</tr>
<tr>
<td>9</td>
<td>no</td>
<td>2^k_i</td>
<td>[2^k_i mod n_q]</td>
<td>yes</td>
<td>no</td>
<td>k_i - 1</td>
<td>1</td>
<td>n_q - 1</td>
</tr>
<tr>
<td>10</td>
<td>no</td>
<td>2^k_i</td>
<td>[2^k_i mod n_q]</td>
<td>no</td>
<td>yes</td>
<td>k_i - 1</td>
<td>1</td>
<td>2k_i - 1</td>
</tr>
</tbody>
</table>

Legend: |x|{mod n_q} represents x mod n_q.
<table>
<thead>
<tr>
<th>Input at top of loop</th>
<th>Input</th>
<th>Input</th>
<th>Steps 2.1.1</th>
<th>Steps 2.1.3</th>
<th>Condition step 2.1.5</th>
<th>Condition step 2.1.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>j</td>
<td>(k_{eq})</td>
<td>(adj)</td>
<td>(k_0)</td>
<td>(k'_1)</td>
<td>(k'_2)</td>
<td>(k_{eq}=\lfloor k_{adj} \rfloor)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>no</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>no</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>no</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>no</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>yes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Result after 2.1.5</th>
<th>Result after 2.1.5</th>
<th>Step 2.1.6</th>
<th>Condition step 2.1.7</th>
<th>Condition step 2.1.7</th>
<th>Result after 2.1.7</th>
<th>Result after 2.1.7</th>
<th>Step 2.1.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>j</td>
<td>(k'_1)</td>
<td>(k'_2)</td>
<td>(k_{eq}=\lfloor k_{adj} \rfloor)</td>
<td>(</td>
<td>k_{eq}+k'_2</td>
<td>_{eq}=0?)</td>
<td>(k_{eq}=k'_1?)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>no</td>
<td>no</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>3</td>
<td>no</td>
<td>no</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>no</td>
<td>yes</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>yes</td>
<td>no</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>1</td>
<td>4</td>
<td>yes</td>
<td>no</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Legend: \(|x|_{eq}\) represents \(x \mod n_{eq}\)

**Fig. 9**
<table>
<thead>
<tr>
<th>w</th>
<th>( n_q )</th>
<th>( Pr(m) )</th>
<th>( Pr(e) )</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>37</td>
<td>72.1%</td>
<td>73.7%</td>
<td>-2.2%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>81.4%</td>
<td>83.2%</td>
<td>-2.2%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>92.2%</td>
<td>92.4%</td>
<td>-0.2%</td>
</tr>
<tr>
<td>2</td>
<td>37</td>
<td>78.2%</td>
<td>77.9%</td>
<td>0.4%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>86.7%</td>
<td>86.1%</td>
<td>0.7%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>94.2%</td>
<td>94.2%</td>
<td>0%</td>
</tr>
<tr>
<td>4</td>
<td>37</td>
<td>85.7%</td>
<td>85.5%</td>
<td>0.2%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>91.3%</td>
<td>91.1%</td>
<td>0.2%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>95.9%</td>
<td>95.6%</td>
<td>0.3%</td>
</tr>
</tbody>
</table>

**Legend:**
- \( Pr(m) \) - Measured Probability
- \( Pr(e) \) - Estimated Probability
- Error - Approximation error: \( \text{Error} = (Pr(m) - Pr(e))/Pr(m) \)

**Fig. 10**
<table>
<thead>
<tr>
<th>w</th>
<th>$n_q$</th>
<th>$Pr(m)$</th>
<th>$Pr(e)$</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>37</td>
<td>0.44%</td>
<td>0.55%</td>
<td>-25.0%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>3.7%</td>
<td>4.4%</td>
<td>-18.9%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>21.5%</td>
<td>22.8%</td>
<td>-6.0%</td>
</tr>
<tr>
<td></td>
<td>$2^{16}$.15</td>
<td>99.74%</td>
<td>99.73%</td>
<td>0.01%</td>
</tr>
<tr>
<td></td>
<td>$2^{32}$.5</td>
<td>100%</td>
<td>99.999999627%</td>
<td>$37 \times 10^{-9}$%</td>
</tr>
<tr>
<td>2</td>
<td>37</td>
<td>1.8%</td>
<td>2.0%</td>
<td>-11.1%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>8.6%</td>
<td>9.5%</td>
<td>-10.5%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>32.2%</td>
<td>33.0%</td>
<td>-2.5%</td>
</tr>
<tr>
<td></td>
<td>$2^{16}$.15</td>
<td>99.84%</td>
<td>99.80%</td>
<td>0.04%</td>
</tr>
<tr>
<td></td>
<td>$2^{32}$.5</td>
<td>100%</td>
<td>99.999999721%</td>
<td>$28 \times 10^{-9}$%</td>
</tr>
<tr>
<td>4</td>
<td>37</td>
<td>8.1%</td>
<td>8.6%</td>
<td>-6.2%</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>22.6%</td>
<td>23.0%</td>
<td>-1.8%</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>49.5%</td>
<td>49.7%</td>
<td>-0.4%</td>
</tr>
<tr>
<td></td>
<td>$2^{16}$.15</td>
<td>99.87%</td>
<td>99.88%</td>
<td>0.01%</td>
</tr>
<tr>
<td></td>
<td>$2^{32}$.5</td>
<td>100%</td>
<td>99.999999825%</td>
<td>$18 \times 10^{-9}$%</td>
</tr>
</tbody>
</table>

Legend:
- $Pr(m)$ - Measured Probability
- $Pr(e)$ - Estimated Probability
- Error - Approximation error: Error = ($Pr(m)$ - $Pr(e)$)/$Pr(m)$

Fig. 11
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

HO1L23/48  HO1L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

HO1L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 6 278 181 B1 (MALEY READING G) 21 August 2001 (2001-08-21) abstract; figures 6,9,10</td>
<td>1,3,4, 13,17,31</td>
</tr>
<tr>
<td>A</td>
<td>column 6, line 57 - line 67 column 8, line 9 - line 13 column 8, line 39 - column 9, line 5</td>
<td>2,5-12, 14-16, 18-30, 32-44</td>
</tr>
<tr>
<td>X</td>
<td>WO 2004/059720 A (INTERNATIONAL BUSINESS MACHINES CORPORATION; POGGE, H.; BERNHARD; YU,) 15 July 2004 (2004-07-15) abstract; figures 1C-1H claims 1,2,14</td>
<td>1,13,17, 31</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
  *A* document defining the general state of the art which is not considered to be of particular relevance
  *E* earlier document but published on or after the international filing date
  *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  *O* document referring to an oral disclosure, use, exhibition or other means
  *P* document published prior to the international filing date but later than the priority date claimed

**Date of the actual completion of the international search** 23 February 2006

**Date of mailing of the international search report** 06/03/2006

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentanden 2 NL-2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3015

Authorized officer

Favre, P.
### DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>abstract; figures 1-11</td>
<td></td>
</tr>
<tr>
<td></td>
<td>abstract; figure 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>column 2, line 15 - column 3, line 49</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>US 5 627 106 A (HSU ET AL) 6 May 1997 (1997-05-06)</td>
<td>1,17,31</td>
</tr>
<tr>
<td></td>
<td>abstract; figures 8-12</td>
<td></td>
</tr>
<tr>
<td></td>
<td>column 1, line 45 - column 2, line 26</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>US 5 998 292 A (BLACK ET AL) 7 December 1999 (1999-12-07)</td>
<td>1,13</td>
</tr>
<tr>
<td></td>
<td>abstract; figures 4(E),4(F)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>abstract; figure 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>paragraph '0015!' - paragraph '0025!'</td>
<td></td>
</tr>
<tr>
<td>Patent document cited in search report</td>
<td>Publication date</td>
<td>Patent family member(s)</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----------------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>US 6278181 B1</td>
<td>21-08-2001</td>
<td>NONE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>EP 1573799 A1</td>
</tr>
<tr>
<td>US 2003019836 A1</td>
<td>30-01-2003</td>
<td>CN 1400697 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DE 10231172 A1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GB 2383188 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 2003078075 A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SG 104332 A1</td>
</tr>
<tr>
<td>US 5424245 A</td>
<td>13-06-1995</td>
<td>NONE</td>
</tr>
<tr>
<td>US 5627106 A</td>
<td>06-05-1997</td>
<td>NONE</td>
</tr>
<tr>
<td>US 5998292 A</td>
<td>07-12-1999</td>
<td>TW 401611 B</td>
</tr>
<tr>
<td>US 2002074637 A1</td>
<td>20-06-2002</td>
<td>NONE</td>
</tr>
</tbody>
</table>