

United States Patent

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[54] THIN-FILM BEAM-LEAD RESISTORS
7 Claims. 6 Drawing Figs.

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29/583, 29/621

[51] Int. Cl. H01c 7/00,
H01c 17/00

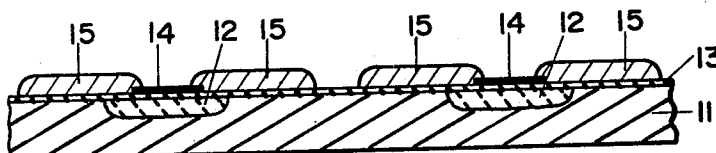
[50] **Field of Search**..... 29/610,
614, 616, 617, 619, 578, 583; 29/620, 621

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ABSTRACT: Thin-film beam-lead resistors are fabricated for use in hybrid microcircuits by a sequence of steps beginning with the formation of a substrate member having an array of dielectric islands coplanar with and supported by a matrix material that is selectively etchable in the presence of the dielectric islands. A refractory dielectric layer is then deposited on the substrate to cover the islands and the surrounding coplanar matrix material. A thin-film resistance element is then deposited on each portion of the dielectric layer that covers a dielectric island. Conductive terminal pairs are then deposited in contact with spaced-apart locations on each resistance element, followed by the step of removing the matrix material, together with contiguous portions of the dielectric layer to separate the completed resistor assemblies.



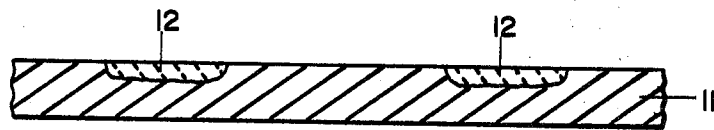


FIG 1

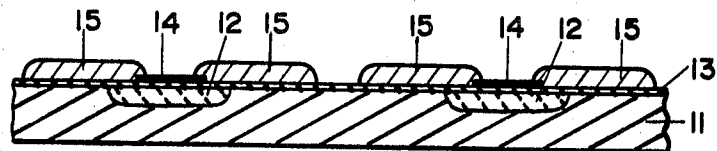


FIG 2

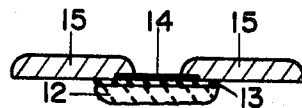


FIG 3

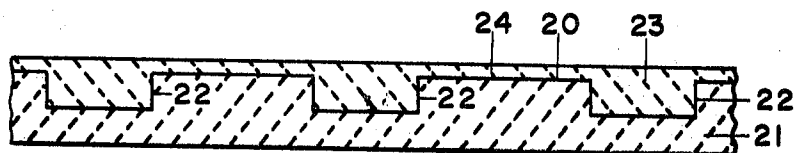


FIG 4

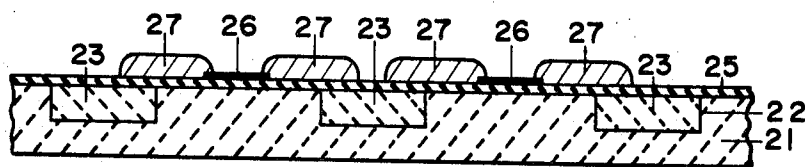


FIG 5

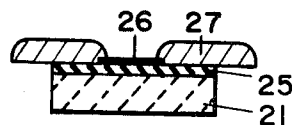


FIG 6

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THIN-FILM BEAM-LEAD RESISTORS

BACKGROUND OF THE INVENTION

This invention relates to the fabrication of thin-film resistors for use in hybrid microcircuits, and more particularly to a method of forming dielectric islands of glass, or its equivalent, as a substrate material in the fabrication of thin film resistors having "beam-lead" terminals for interconnection with hybrid microcircuits.

Various techniques for the fabrication of beam-lead devices on oxidized silicon surfaces have been proposed in the past. It is also known to fabricate thin-film resistors on glass substrates; but the fabrication of thin-film resistors by either of these techniques has certain disadvantages. A thin-film resistance element deposited on an oxidized silicon surface introduces a certain amount of shunt capacitance at high-frequency operating conditions. Prior techniques for substituting glass substrates have not been satisfactory for high-volume microphotolithographic batch-processing methods, due in part to the lack of suitable technology for the formation of contact terminals.

THE INVENTION

It is an object of the present invention to provide a technique for the fabrication of thin-film beam-lead resistor assemblies characterized by improved performance under high-frequency operating conditions.

It is a more particular object of the invention to provide a suitable method for the manufacture of thin-film resistance elements on glass substrates with integral beam-lead contacts.

A primary feature of the invention lies in the step of forming a substrate having an array of dielectric islands coplanar with and supported by a matrix material that is selectively etchable in the presence of said islands. Two separate means of forming such a substrate are provided.

In accordance with one embodiment, a planar-surfaced silicon body is selectively etched to provide a plurality of cavities therein of a suitable size to serve as resistor substrates. These cavities are then filled with an insulator composition having a softening point about 750° C. A slight overfilling of the cavities is essential at this point in order to facilitate the subsequent smoothing of the insulator-filled regions and the surrounding silicon by mechanical lapping to coplanarize the surfaces of the insulator regions with the surface of the surrounding silicon matrix.

In accordance with an alternate embodiment, a suitable substrate is provided by a sequence of steps beginning with the etching of a quartz or sapphire wafer to form a network of channels surrounding an array of islands having coplanar surfaces. A filler material is then placed in the channel network, including a slight excess fill, in order to facilitate subsequent smoothing of the surfaces to coplanarize the filler material with the island surfaces.

It is an additional feature of the invention to deposit a layer of dielectric material over the coplanarized substrate surfaces in order to provide a suitable base for the subsequent deposition of the resistance element and the beam-lead material.

Another feature of the invention, characteristic of either of the above embodiments, lies in the further steps of depositing a thin-film resistance element on each portion of the dielectric layer covering the less-readily-etchable substrate areas, i.e., the island portions thereof, depositing conductive terminal pairs in contact with spaced-apart locations of each resistance element, and then removing the matrix material and contiguous portions of the dielectric layer to separate the completed resistor assemblies.

The invention is embodied in a method for fabricating thin-film resistor assemblies beginning with the step of providing a substrate having an array of dielectric islands coplanar with and supported by a matrix material that is selectively etchable in the presence of such islands. A refractory dielectric layer is then deposited to cover the islands and the coplanar matrix

material. A thin-film resistance material is then patterned on each portion of the dielectric layer which covers a dielectric island. Conductive terminal pairs are then deposited, for example, by vacuum evaporation, in contact with spaced-apart locations on each resistance element, followed by the step of removing the matrix material, together with contiguous portions of the dielectric layer, to separate the completed resistor assemblies.

A more particular aspect to the invention is embodied in a method for fabricating thin-film resistor assemblies, beginning with the step of selectively etching a planar-surfaced silicon body to provide a plurality of cavities therein of a suitable size for forming resistor substrates. The cavities are then filled with an insulator composition having a softening point above 750° C. The insulator-filled regions in the surrounding silicon are smoothed, for example, by mechanical lapping, to coplanarize the surfaces of the insulator regions with the surrounding silicon surfaces. A layer of dielectric material is then deposited over the coplanarized surfaces, followed by the step of depositing a thin-film resistance element on each portion of the dielectric layer which covers an insulator region. Conductive terminal pairs are then deposited in contact with spaced-apart locations on each resistant element, followed by the step of removing the silicon body and contiguous portions of the dielectric layer, to separate the completed resistor assemblies.

A further embodiment of the invention begins with the step of providing a quartz or sapphire substrate with a network of channels surrounding an array of islands having coplanar surfaces. A filler material is then placed in the channel network, including at least a slight overfill. The resulting surfaces are then smoothed, for example by mechanical lapping, to coplanarize the filler material with the island surface. A refractory dielectric layer is then deposited on the coplanarized surfaces followed by the step of depositing a thin-film resistance element on each portion of the dielectric layer which covers a substrate island. Conductive terminal pairs are then deposited in contact with spaced-apart locations on each resistance element. Sufficient substrate material is then removed from the reverse side thereof to expose the filler material, and finally the filler layer is selectively removed to separate the completed resistor assemblies.

THE DRAWINGS

FIGS. 1—3 are greatly enlarged cross-sectional views illustrating the fabrication of a thin-film beam-lead resistor assembly in accordance with one embodiment of the invention; and

FIGS. 4—6 are greatly enlarged cross-sectional views illustrating the fabrication of a thin-film beam-lead resistor in accordance with an alternate embodiment of the invention.

In FIG. 1, silicon wafer 11 having a thickness of 5 to 15 mils is selectively etched by known procedures to form an array of cavities or pockets 12 of a suitable size for forming the resistor substrates; that is, about 25 to 75 mils in diameter, assuming the pockets are generally circular, and 25 to 75 mils on each side, in case of rectangular cavities. The etched surface of the wafer is then covered with a suitable glass composition, for example, by melting-in a high temperature compatible vitreous frit. The glass should have a softening point above 750° C. and a coefficient of thermal expansion approximately equal to that of the silicon base. Some overfilling of the cavity is essential in order to insure a complete fill, and to facilitate the formation of a single flat surface by means of mechanical lapping and polishing to remove excess glass.

As shown in FIG. 2, a film of silicon dioxide, or other dielectric refractory material, is deposited over the surface of the structure of FIG. 1 to provide a thickness of 1,000 to 10,000 angstroms, and preferably about 4,000 to 6,000 angstroms. The silicon dioxide may be deposited by RF sputtering or by gas-plating techniques, such as by contacting the substrate surface with the vaporous stream of silane plus oxygen.

A thin-film resistance element 14 is then patterned on refractory dielectric layer 13, directly above filled pockets or cavities 12. Examples of suitable thin-film resistance materials include nickel-chromium alloys, tantalum carbide, boron silicide, tin nitride, molybdenum boride, and many others known in the art.

A thick layer of metallization is then deposited to form conductive terminal pairs 15. Preferably, the terminals or leads 15 include successive layers of titanium, platinum and gold. For example, an initial layer of titanium 1,000 to 5,000 angstroms thick, is covered by a layer of platinum of the same thickness and then with a gold layer many times thicker, preferably in excess of about 100,000 angstroms thick. Other useful metal combinations for the fabrication of the conductive terminal pairs include molybdenum-gold, tantalum-gold, titanium-gold, titanium-silver-gold, titanium-copper, and chromium-nickel. Still others are known in the art.

Thereafter, the reverse side of the wafer is removed by selective etching, for example, with an aqueous mixture of nitric and hydrofluoric acids. Once the silicon is completely removed, the contiguous portions of refractory dielectric layer 13 are exposed and are subjected to further etching, for example, with HF in order to complete the isolation of each separate resistor assembly, such as illustrated in FIG. 3.

In FIG. 4, an alternate embodiment of the invention is illustrated, beginning with the selective etching of quartz of sapphire substrate 21 to provide a channel network 22 surrounding an array of islands 20 having coplanar surfaces. The etched side of substrate 21 is then covered by a suitable filler 23, such as a glass frit or silver chloride, including at least a slight overfill 24. The filler surface is then lapped and polished to remove all excess material and thereby coplanarize the surfaces of islands 20 with the filler surfaces in the channel network.

Then, as shown in FIG. 5, a refractory dielectric layer 25, such as silicon dioxide, for example, is deposited over the coplanarized surfaces of the substrate. Layer 25 may be formed in the same manner as layer 13 of the above-described embodiment. Also, as previously described, thin-film resistance elements 26 are deposited directly over the surfaces of the quartz or sapphire substrate islands, followed by the deposition of thick conductive terminal layers 27. The same examples of resistance materials and leads as listed above are used.

The reverse side of the structure shown in FIG. 5 is then subjected to mechanical lapping and polishing to remove the quartz until filler material 23, within the channel network, is exposed. With the upper surface of the wafer protected by wax, or other masking material, filler 23 is removed by selective etching, for example with HF, which leaves the sapphire (or quartz) relatively unaffected. Those portions of dielectric layer 25 immediately contiguous the glass network channel are also etched away, thereby separating the individual resistor assemblies, such as illustrated by FIG. 6.

I claim:

1. A method for fabricating thin-film resistor assemblies comprising:

- a. selectively etching a planar-surfaced silicon body to provide a plurality of cavities therein of a suitable size for forming resistor substrates;
- b. filling said cavities with an insulator composition having a softening point of 750° C.;
- c. smoothing the said insulator-filled regions and the surrounding silicon to coplanarize the surfaces of the insulator regions with the surrounding silicon surfaces;
- d. depositing a layer of dielectric refractory material on the coplanarized surfaces;
- e. depositing a thin-film resistance element on each portion of the dielectric layer which covers an insulator region;
- f. depositing conductive terminal pairs in contact with spaced-apart locations on each resistance element; and
- g. removing the silicon body and contiguous portions of the dielectric layer to separate the completed resistor assemblies.

2. A method as defined by claim 2 wherein said cavities measure 25 to 75 mils on each side at the surface of the silicon body and are etched to a depth of 5 to 15 mils.

3. A method as defined by claim 2 wherein said insulator composition is a high-temperature glass.

4. A method as defined by claim 2 wherein said dielectric layer is silicon dioxide.

5. A method as defined by claim 2 wherein said resistance element is selected from the group consisting of nickel-chromium alloys, tantalum carbide, boron silicide, tin nitride and molybdenum boride.

6. A method as defined by claim 2 wherein said terminal pairs are patterned to extend beyond the periphery of each respective insulator region, and are provided with sufficient strength to be self-supporting.

7. A method for fabricating thin-film resistor assemblies comprising:

- a. providing a quartz or sapphire substrate with a network of channels surrounding an array of islands having coplanar surfaces;
- b. placing a filler material on the channel network;
- c. smoothing the resulting surfaces to coplanarize the filler material with the island surfaces;
- d. depositing a refractory dielectric layer on the coplanarized surfaces;
- e. depositing a thin-film resistance element on each portion of the dielectric layer which covers a substrate island;
- f. depositing conductive terminal pairs in contact with spaced-apart locations on each resistance element;
- g. removing sufficient substrate from the reverse side thereof to expose said filler material; and
- h. removing said filler and the contiguous portions of said dielectric layer to separate the completed resistor assemblies.