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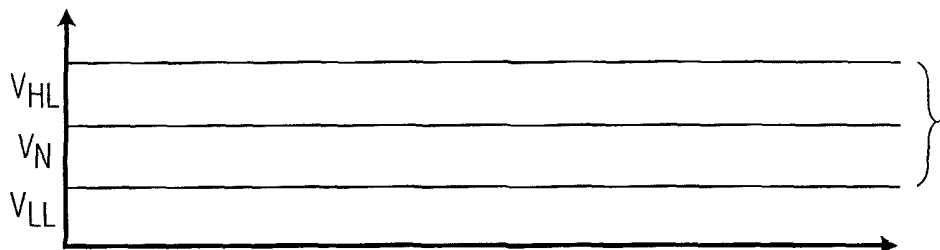
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(54) Title: LATCHING ELECTRONIC CIRCUIT FOR RANDOM NUMBER GENERATION



(57) Abstract: A physical random number generator has a bi-stable latch that operates to generate a random number bit in response to a reception of one or more voltage input signals and a clock signal. A voltage source provides the voltage input signal(s) for provoking the bi-stable latch into a metastable state. A clock provides the clock signal for triggering the bi-stable latch. When triggered, the bi-stable latch latches the random number bit as a function of its metastable state provoked by the voltage input signal(s).

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB 03/03231

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F7/58

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, COMPENDEX, INSPEC, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 963 104 A (BUER MARK LEONARD) 5 October 1999 (1999-10-05) column 5, line 29 -column 9, line 39; figures 2-5	1-20
P, X	--- KINNEMENT D J; CHESTER E G: "Design of an on-chip random number generator using metastability" ESSCIRC 2002 PROCEEDINGS ON THE 28TH EUROPEAN SOLID-STATE CIRCUIT CONFERENCE, 24 - 26 September 2002, pages 595-598, XP002273019 Firenze, Italy the whole document --- -/--	1-20

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BELLIDO M J ET AL: "A simple binary random number generator: new approaches for CMOS VLSI" CIRCUITS AND SYSTEMS, 1992., PROCEEDINGS OF THE 35TH MIDWEST SYMPOSIUM ON WASHINGTON, DC, USA 9-12 AUG. 1992, NEW YORK, NY, USA, IEEE, US, 9 August 1992 (1992-08-09), pages 127-129, XP010057783 ISBN: 0-7803-0510-8 the whole document ---	
A	WALKER S ET AL: "Evaluating metastability in electronic circuits for random number generation" IEEE COMPUTER SOCIETY WORKSHOP VLSI 2001, 19 - 20 April 2001, pages 99-101, XP010541763 the whole document -----	

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