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(54) **ELECTRONIC DRIVER CIRCUIT AND METHOD FOR DRIVING A DISTRIBUTED MACH-ZEHNDER MODULATOR (MZM) WITH DRIVER DELAY COMPENSATION**

ELEKTRONISCHE TREIBERSCHALTUNG UND VERFAHREN ZUM TREIBEN EINES VERTEILTEN MACH-ZEHNDER-MODULATORS (MZM) MIT TREIBERVERZÖGERUNGSKOMPENSATION

CIRCUIT D'ATTAQUE ÉLECTRONIQUE ET PROCÉDÉ D'ATTAQUE D'UN MODULATEUR MACH-ZEHNDER DISTRIBUÉ (MZM) AVEC COMPENSATION DE RETARD DU CIRCUIT D'ATTAQUE

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Description

BACKGROUND

[0001] A Mach-Zehnder Modulator (MZM) splits a received optical input (e.g., optical signal) into portions. One portion is provided to a first arm (e.g., waveguide) while the other portion is provided to a second arm. Phase change is applied to the optical signal portion propagating through one or both arms such that when the optical signal portions are later recombined, either constructive or destructive interference occurs. The phase change applied to the optical signal portions is a function of an electrical input voltage provided by an electronic driver circuit coupled to the MZM.

[0002] A segmented MZM contains multiple electrical inputs applied along one or both of the arms. Each electrical input is supplied with an electrical input voltage by the electronic driver circuit. A major challenge in designing a segmented MZM is ensuring that electrical signals received from the electronic driver circuit and optical signals propagating through the arms are aligned given that their respective velocities are different. This is readily apparent when comparing the optical index of a silicon waveguide, which is 4, to the electrical index of a silicon dioxide interlayer dielectric, which is 2. Because the electrical signal is faster than the optical signal, a common approach is to insert additional delay into the electronic driver circuit.

[0003] One known method to introduce delay into the electronic driver circuit is to use transmission lines. Transmission lines offer very accurate delay with precise delay control, but they have a number of drawbacks. For example, transmission lines require controlled impedance design and are prone to cross-talk. In addition, the routing of transmission lines requires complicated meandering. As a result, transmission line patterns are large, which may directly translate into higher cost. Further, transmission lines need higher power amplifiers, typically implementing analog-based topologies, to drive and receive.

[0004] In addition, buffer stages are usually implemented to drive large capacitive loads, and hence they normally have gate widths that increase in size with each additional stage. However, implementing delay buffer stages with increasingly fanned-out widths results in large delays on the order of 20 picoseconds (ps) and correspondingly poor precision on the order of 10 ps over process/voltage/temperature (PVT) corners. For silicon photonic applications, the amount of delay desired falls into an awkward region of being too small to achieve using normal active delay techniques and too large to achieve passively without considering transmission line effects. Therefore, a major problem is how to achieve an active delay that is much smaller than is normally available.

[0005] EP 0347759 relates to a speed enhancement technique for CMOS circuits. EP 0690577 relates to a

fast propagation technique in CMOS integrated circuits.

SUMMARY

[0006] Various aspects of the present disclosure have been defined in the independent claims. Further technical features of each of these aspects have been defined in the respective dependent claims.

[0007] These and other features will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of this disclosure, reference is now made to the following brief description, taken in connection with the accompanying drawings and detailed description, wherein like reference numerals represent like parts.

FIG. 1 is a schematic diagram of a segmented MZM coupled to a conventional electronic driver circuit.

FIG. 2 is a schematic diagram of an embodiment electronic driver circuit configured to drive a segmented MZM.

FIG. 3 is a schematic diagram of a CMOS inverter in the buffers of the embodiment electronic driver circuit.

FIG. 4 is a circuit model of a p-channel metal-oxide-semiconductor (PMOS) within the CMOS inserter.

FIG. 5 is a circuit model of an n-channel metal-oxide-semiconductor (NMOS) within the CMOS inserter.

FIG. 6 is a functional circuit model of the embodiment electronic driver circuit of Figure 2.

FIG. 7A is a first portion of the functional circuit model of Figure 6 illustrating a first time delay between the first and second outputs of the embodiment electronic driver circuit of Figure 2.

FIG. 7B is a second portion of the functional circuit model of Figure 6 illustrating a second time delay between the second and third outputs of the embodiment electronic driver circuit of Figure 2.

FIG. 8 is table comparing delay due to PVT variation across different transistor sizing conditions under pre-simulated models and excluding fixed delay.

FIG. 9 is table comparing delay due to PVT variation across different transistor sizing conditions under post-simulated models.

FIG. 10 is a flowchart of an embodiment method of driving a segmented MZM.

DETAILED DESCRIPTION

[0009] It should be understood at the outset that although an illustrative implementation of one or more embodiments are provided below, the disclosed systems and/or methods may be implemented using any number

of techniques, whether currently known or in existence. The disclosure should in no way be limited to the illustrative implementations, drawings, and techniques illustrated below, including the exemplary designs and implementations illustrated and described herein, but may be modified within the scope of the appended claims.

[0010] Disclosed herein is an electronic driver circuit configured to drive a segmented MZM. As will be more fully explained below, the electronic driver circuit generates delays using decreasingly sized delay buffer stages. Specifically, accurate and precise delay is accomplished by implementing CMOS delay buffer stages with sequentially decreasing gate widths to introduce the small amount of additional delay desired. This scheme avoids a transmission line design that calls for a large space, a more complicated design, and higher power consumption. With the electronic driver circuit disclosed herein, delay compensation is demonstrated as precise to within 3 ps across a designed 8 ps total delay under PVT corners. This is significantly better than the typical 100% error range that would otherwise be achieved with active delay. In addition, substantial delay time matching between individual segments in both optical and electrical domains is achieved. The techniques disclosed herein are directly applicable to high-speed optical communications at 25 Giga bits per second (GBPS) per channel and beyond.

[0011] Figure 1 depicts a conventional electronic driver circuit 100 coupled to a segmented MZM 102. The MZM 102 is configured to split an optical input (e.g., an optical signal) into a first portion and a second portion. The first portion of the optical input is routed to and propagates through a first arm 104 (e.g., waveguide) of the MZM 102 while the second portion of the optical input is routed to and propagates through a second arm 106 of the MZM 102. In Figure 1, a phase change is applied to the first portion of the input signal propagating through the first arm 104. The amount of phase change is a function of the electrical input voltage provided at a first segment 108, a second segment 110, and a third segment 112 by the conventional electronic driver circuit 100 coupled to the MZM 102. While three segments are illustrated, the first arm 104 may include any number of segments. Due to the phase change applied to the first portion of the input signal propagating through the first arm 104, when both portions of the input signal are later recombined, either constructive or destructive interference occurs at the optical output. Unfortunately, ensuring that the electrical signals from the conventional electronic driver circuit 100 are aligned with the optical signals of the MZM 102 is challenging.

[0012] Figure 2 depicts an embodiment electronic driver circuit 200 configured to drive a segmented MZM such as, for example, the MZM 102 of Figure 1. Figure 2 represents a single-channel of a multi-channel (e.g., 4-channel) distributed electronic driver circuit where each channel operates similarly. In other words, the electronic driver circuit 200 may include any number of channels. In an

embodiment, a driver circuit similar to driver circuit 200 may be operably coupled to each arm of an MZM in order to simultaneously change the phase of each arm.

[0013] In an embodiment, the electronic driver circuit 200 includes a first output buffer 202 (e.g., buffer amplifier) disposed between a first delay stage 204 and a second delay stage 206, a second output buffer 208 disposed between the second delay stage 206 and a third delay stage 210, and a third output buffer 212 following the third delay stage 210. The first delay stage 204 is configured to receive an input signal (e.g., an electrical signal) from a particular channel (e.g., channel 1). The first delay stage 204 is also configured to output an electrical signal to the first output buffer 202 and subsequently to a first segment (e.g., the first segment 108 in Figure 1) and to the second delay stage 206. The second delay stage 206 receives an electrical signal from the first delay stage 204. The second delay stage 206 is configured to output an electrical signal to the second output buffer 208 and subsequently to a second segment (e.g., the second segment 110 in Figure 1) and to the third delay stage 210. The third delay stage 210 receives an electrical signal from the second delay stage 206. The third delay stage 210 is configured to output an electrical signal to the third output buffer 212 and subsequently to a third delay stage (e.g., the third segment 112 in Figure 1) and to the dummy load 214. In an embodiment, the dummy load 214 permits the design of delay stages (e.g., the second and third delay stages 206, 210) to be similar. While three delay stages 204, 206, 210 and three output buffers 202, 208, 212 are illustrated in Figure 2, any number of delay stages and output buffers may be employed within the electronic driver circuit 200. As will be more fully explained below, each of the delay stages 204, 206, 210 in Figure 2 is configured to add a delay to the electrical signal received by that stage.

[0014] In an embodiment, the second delay stage 206 and the third delay stage 210 in Figure 2 each include a metal trace 216. The metal traces 216 are configured to provide a passive fixed delay. In an embodiment, the metal traces 216 have a length of about 650 micrometers (μm), which corresponds to about 4 ps of passive fixed delay. The metal traces 216 also serve to connect outputs of delay stages to inputs of delay stages together in series, but do not act as a transmission line. As known to those skilled in the art, transmission line effects can be neglected as long as the metal trace length is a small percentage of wavelength. Considering a frequency content up to about 25 Giga Hertz (GHz), a wavelength with effective dielectric constant of 4 is calculated to be about 6,000 μm . Generally, lengths less than $1/10^{\text{th}}$ of the wavelength may be treated as lumped, which in this example limits lengths to 600 μm . In an embodiment, the metal traces 216 are about 650 μm long. As such, transmission line effect may be safely neglected.

[0015] The first delay stage 204 includes a first delay buffer 218, the second delay stage 206 includes a second delay buffer 220, and the third delay stage 210 includes

a third delay buffer 222. As will be more fully explained below, the delay buffers 218, 220, 222 are configured to provide an active delay. In an embodiment, each of the first, second, and third delay buffers 218, 220, 222 provides about 4 ps of active delay. In an embodiment, a total delay of 8 ps is desired from a delay stage (e.g., delay stage 204, 206), with 4 ps being fixed delay and coming from a passive metal trace (e.g., metal trace 216) and another 4 ps being active delay and coming from a delay buffer (e.g., delay buffer 218, 220, 222). In an embodiment, each of the first, second, and third delay buffers 218, 220, 222 and the first, second, and third output buffers 202, 208, 212 is implemented as a CMOS inverter.

[0016] FIG. 3 depicts a CMOS inverter 300 suitable for use as the delay buffers and the output buffers disclosed herein. The CMOS inverter 300 includes a PMOS transistor 302 and NMOS transistor 304. In the CMOS inverter 300, the gates and drains of the NMOS transistor 304 and the PMOS transistor 302 are coupled together, the source of the PMOS transistor 302 is coupled to a voltage supply, and the source of the NMOS transistor 304 is coupled to ground. Each transistor type provides an input capacitance load at the gate. Although the PMOS transistor 302 and NMOS transistor 304 are inherently different, inverters are designed to give symmetric rise/fall times.

[0017] In an embodiment, the gate width of each CMOS inverter 300 used as an output buffer (e.g., output buffers 202, 208, 212) is the same. In other words, the gate width of the CMOS inverter 300 in the first output buffer 202 is equivalent to the gate width of the CMOS inverter 300 in the second output buffer 208. Likewise, the gate width of the CMOS inverter 300 in the second output buffer 208 is equivalent to the gate width of the CMOS inverter 300 in the third output buffer 212. In an embodiment, the gate width of each of the CMOS inverters 300 used as an output buffer is small (e.g., between about 5 microns and 10 microns).

[0018] In an embodiment, the gate width of each CMOS inverter 300 used as a delay buffer (e.g., delay buffers 218, 220, 222) gets smaller with each successive delay stage. In other words, the gate width of the CMOS inverter 300 in the third delay buffer 222 is smaller than the gate width of the CMOS inverter 300 in the second delay buffer 220. Likewise, the gate width of the CMOS inverter 300 in the second delay buffer 220 is smaller than the gate width of the CMOS inverter 300 in the first delay buffer 218. This concept is represented by the sizes of the triangles used in Figure 2 to represent the first, second, and third delay buffers 218, 220, 222. The sequentially-decreasing gate width configuration takes advantage of the fact that the input capacitance of a delay buffer is proportional, and the output resistance is inversely proportional, to the gate width. As will be more fully explained below, the use of ever smaller gate widths of the delay buffers in the successive delay stages 204, 206, 210 also takes advantage of the fact that delay on

the n^{th} output is approximately proportional to the product of the resistance (R) and the capacitance (C) in addition to the product of the output resistance on the n^{th} delay buffer and the input capacitance of the $(n+1)^{\text{th}}$ delay buffer.

[0019] To aid in the understanding of why sequentially decreasing gate sizes provide a small delay time, equivalent circuit transistor models may be helpful. In that regard, the small-signal circuit model 400 for the PMOS transistor 302 and the small-signal circuit model 500 for the NMOS transistor 304 are provided in Figures 4 and 5, respectively. Each of the models 400, 500 contains a gate (G), a source (S), and a drain (D). The models 400, 500 are similar in that they both include a gate capacitance (e.g., C_{gp}, C_{gn}) and channel resistance (e.g., R_{op}, R_{on}). The models 400, 500 also each include a transconductance element 402, 502, respectively, that outputs current as a function of the voltage between gate and source. Input capacitance increases proportionally with gate width, and output channel resistance is inversely proportional to gate width.

[0020] With CMOS topologies, only one transistor is intended to be on at any given time, and practically, this is a good assumption as only one transistor is on about 95% of the time. Further, the transconductance element 402, 502 for each transistor can be dropped from a delay circuit model. Therefore, as a first-order model for the block-diagram in Figure 2, the models shown in Figures 4 and 5 can be generalized to the delay circuit model 600 shown in Figure 6. As shown, C_n and R_n (where n is an integer 1, 2, 3 ...) are the effective input capacitance and output resistance of the n^{th} delay buffer stage, respectively. C_b is the input capacitance presented by the output buffer. The value of C_b is independent of R_n/C_n and is instead controlled by the gate width of the output buffer stages and is intentionally designed with a small gate width to limit its effect on delay. The delay circuit model 600 also includes metal traces 616 (or other fixed passive delay elements) similar to the metal traces 216 in Figure 2.

[0021] The active delay may be approximated as RC delay where R is the equivalent channel resistance, and C is comprised of the gate capacitances of the output buffer that follows immediately. The relevant circuit model portions 700, 702 from the circuit model 600 that are needed to calculate the delay are illustrated in Figures 7A and 7B, respectively. As shown in Fig. 7A, the active delay between first and second outputs (e.g., between input of the first output buffer 202 and the input of the second output buffer 208 in Figure 2) is not related to the product of R₁ and C₁ (Figure 6), but rather it is related to the product of R₁ and C₂. In order to minimize the active delay time, the R and C components need to be simultaneously reduced. R₁ is made smaller by using a wider gate width in an early delay stage. Similarly, C₂ is made smaller by having a narrower gate width in a later delay stage. In this manner, each sequential delay stage has a decreasing width to length (W/L) ratio, which leads to

a reduced RC time-constant. This means that by using CMOS gates with successively decreasing size for each stage, a much smaller active delay is achieved relative to other known methods of generating active delay.

[0022] It can be observed that delay using the disclosed topology comprises an active delay contribution (e.g., provided by delay buffers) plus a passive fixed delay (e.g., provided by metal traces). For RC time constant, a factor of 2.2 is used to calculate 10% to 90% rise/fall delay time. Hence, total time delay between stages may be calculated as shown in Figures 7A and 7B. For example, total time delay may be approximated as $T_1 = 2.2 (R_1)(C_b + C_2) + \text{fixed delay}$, and $T_2 = 2.2 (R_2)(C_b + C_3) + \text{fixed delay}$.

[0023] Using the design disclosed herein, the total delay may be controlled as a function of the scaling factor between stages (e.g., delay stages 204, 206, 210 in Figure 2). For example, using delay buffers (e.g., delay buffers 218, 220, 222 in Figure 2) having gate widths of 4w, 2w, and w, respectively, where w is some unit gate width for PMOS/NMOS devices. In this case, the gate width of the delay buffer in each of the successive delay stages is reduced by a factor of 2. If a smaller active delay is desired, delay buffer dimensions may be changed to 16w, 4w, w, respectively, such that the gate width of the delay buffer in each successive stage is reduced by a factor of 4. With such a change, output resistance is reduced to 1/4 while input capacitance doubles to cause the net effect of delay to scale by half. Those skilled in the art will recognize that due to output buffer load C_b , metal trace parasitic elements, and/or additional parasitic elements not in the model, time delay may not be reduced by exactly half. Similarly, due to the additional loading, time delay between the first and second output buffers may be slightly different from delay between second and third output buffers. Gate widths may be tuned accordingly. In an embodiment, the gate widths of the delay buffers range between about 120 microns (the largest gate width of the first stage) and 30 microns (the smallest gate width for the last stage).

[0024] As power consumption is proportional to fCV^2 , where f is frequency, C is capacitance, and V is voltage, increasing first stage gate width causes increasingly more power consumption. This is further aggravated by the possibility that additional pre-buffer stages may be required to drive such a large first stage. This indicates that from a power consumption perspective, it may be preferable to err on having slightly more delay rather than less.

[0025] Only active delay is sensitive to PVT corners, while passive delay is relatively insensitive to PVT. The concepts disclosed herein exploit the fixed delay insensitivity such that each delay segment is designed to maximize fixed delay and minimize active delay time. A smaller time-constant from the active devices allows less variation over PVT, which means more precise delay. Minimum gate lengths are used to maintain the fastest possible switching speed.

[0026] For comparison, pre-layout simulated models that do not include the fixed delay section are provided in table 800 of Figure 8. In order to maintain high yield, analysis is performed across all PVT corner cases. Variations in the physical process that affect gate dimensions, mobility, or other transistor features may result in slower or faster transistor action. Higher supply voltage similarly allows faster switching by allowing higher current. Lower temperature increases mobility that also allows faster switching. In the simulation results presented in Figure 8, process is varied across Slow-Slow (SS), Typical-Typical (TT), and Fast-Fast (FF); supply voltage is varied from 0.95V, 1V, to 1.05V; and temperature is varied from -40 °C, +50 °C, to +120 °C.

[0027] In Figure 8, the last row represents the actual design for the delay between the outputs of delay buffers (e.g., between the input of first output buffer 202 and the input of the second output buffer 208 in Figure 2). As expected, this scenario provides smallest delay and smallest delay variation on an absolute time (e.g., picosecond (ps)) basis. In the increasingly sized case, transistor sizes for the first and third delay stages (e.g., the first delay stage 204 and the third delay stage 210 in Figure 2) are swapped. It can be clearly seen that increasingly sized delay buffers shows larger total delay as well as larger absolute variation in delay as compared to the decreasingly sized delay buffers. The scenario with the equally-sized delay buffers assumes that the sizing of the second delay stage (e.g., the second delay stage 206) is also used for both the first and third delay stages. For the equally-sized delay buffers, actual size is not a major factor, as changing gate width will simultaneously change R and C in opposite directions.

[0028] Post-layout simulated models including layout parasitic effects and fixed delay are presented in table 900 of Figure 9. This simulation represents all known effects in the model and may take several days to run to completion. Results show decreasingly sized delay buffers show variation to be within 3.1 ps or 37.58% against the mean across all corners. Comparison with equally-sized delay buffer stages with the second delay stage sizing from the actual design applied to both the first and third stages is also provided. Consistent with pre-layout simulation trends, the equally sized delay buffer stage design shows larger variation on both an absolute and percent basis than the decreasingly sized delay buffer stage design and has high nominal delay above 10 ps with over 4.5 ps of variation.

[0029] Figure 10 depicts a method 1000 of driving a modulator such as a segmented MZM. The method 1000 may be implemented when there is a desire to delay electrical signals so that they are aligned with the optical signals propagating through the segmented MZM. In block 1002, a first delayed electrical signal is generated at first delay stage from a received electrical signal using a first CMOS inverter having a first gate width. In block 1004, the first delayed electrical signal is output to a first output buffer and a second delay stage. In block 1006, a second

delayed electrical signal is generated at the second delay stage from the first delayed electrical signal using a passive delay element and a second CMOS inverter. The second CMOS inverter has a second gate width smaller than the first gate width of the first CMOS inverter. In block 1008, the second delayed electrical signal is output to a second output buffer.

[0030] From the foregoing, those skilled in the art will appreciate that a new circuit for delay compensation in a distributed MZM driver employing decreasingly sized delay buffer stages is disclosed. The circuit has the advantage of being compact, providing accurate delay, and remaining precise over PVT corners to allow high yield. Moreover, the circuit is simple to design once the technique is understood.

[0031] While several embodiments have been provided in the present disclosure, it should be understood that the disclosed systems and methods might be embodied in many other specific forms without departing from the scope of the appended claims. The present examples are to be considered as illustrative and not restrictive, and the intention is not to be limited to the details given herein. For example, the various elements or components may be combined or integrated in another system or certain features may be omitted, or not implemented.

[0032] In addition, techniques, systems, subsystems, and methods described and illustrated in the various embodiments as discrete or separate may be combined or integrated with other systems, modules, techniques, or methods without departing from the scope of the claims. Other items shown or discussed as coupled or directly coupled or communicating with each other may be indirectly coupled or communicating through some interface, device, or intermediate component whether electrically, mechanically, or otherwise. Other examples of changes, substitutions, and alterations are ascertainable by one skilled in the art and could be made without departing from the scope of the claims.

Claims

1. An electronic driver circuit for a Mach-Zehnder modulator, comprising:

a first delay buffer (218) implemented as a first complementary metal-oxide-semiconductor (CMOS) inverter having a first gate width, wherein the first CMOS inverter is configured to produce a first delayed electrical signal from a received electrical signal and output said first delayed electrical signal to a first output buffer (202) and subsequently to a first segment (108) of the modulator; and

a second delay buffer (220) following the first delay buffer (218), wherein the second delay buffer (220) is implemented as a second CMOS inverter having a second gate width smaller than

the first gate width of the first CMOS inverter, and wherein the second CMOS inverter is configured to produce a second delayed electrical signal from the first delayed electrical signal produced by the first CMOS inverter and output said second delayed electrical signal to a second output buffer (208) and subsequently to a second segment (110) of the modulator;

wherein, the electronic driver circuit further comprises a third delay buffer (222) following the second delay buffer (220), the third delay buffer (222) implemented as a third CMOS inverter having a third gate width smaller than the second gate width of the second CMOS inverter, wherein the third CMOS inverter produces a third delayed electrical signal from the second delayed electrical signal produced by the second CMOS inverter and output said third delayed electrical signal to a third output buffer (212) and subsequently to a third segment (112) of the modulator; and

wherein the first delayed electrical signal is provided to a first output buffer (202), the second delayed electrical signal is provided to a second output buffer (208), and the third delayed electrical signal is provided to a third output buffer (212); and

wherein the second delay buffer (220) includes a first metal trace operably coupled to the second CMOS inverter and the third delay buffer (222) includes a second metal trace operably coupled to the second CMOS inverter.

2. The electronic driver circuit of claim 1, wherein each of the first output buffer (202), the second output buffer (208), and the third output buffer (212) are implemented as an output CMOS inverter.
3. The electronic driver circuit of claim 1, wherein the first CMOS inverter, the second CMOS inverter, and the third CMOS inverter each produce an active delay, and wherein the first metal trace and the second metal trace each produce a passive delay.
4. The electronic driver circuit of claim 3, wherein the active delay is 4 picoseconds (ps) and the passive delay is 4 ps.
5. The electronic driver circuit of any one of claims 1 to 4, wherein the first gate width is $4w$, the second gate width is $2w$, and the third gate width is w , where w is a unit gate width, such that the gate width of each of the successive buffer stages is reduced by a factor of 2.
6. The electronic driver circuit of any one of claims 1 to 4, wherein the first gate width is $16w$, the second gate width is $4w$, and the third gate width is w , where

w is a unit gate width, such that the gate width of each of the successive buffer stages is reduced by a factor of 4.

7. A method of driving a Mach-Zehnder modulator, comprising:

generating, at first delay stage (204), a first delayed electrical signal from a received electrical signal using a first complementary metal-oxide-semiconductor (CMOS) inverter (218; 300) having a first gate width; 10
outputting the first delayed electrical signal to a first output buffer (202) and subsequently to a first segment of the modulator and a second delay stage (206); 15
generating, at the second delay stage, a second delayed electrical signal from the first delayed electrical signal using a passive delay element (216) and a second CMOS inverter (220), the second CMOS inverter having a second gate width smaller than the first gate width of the first CMOS inverter; and 20
outputting the second delayed electrical signal to a second output buffer (208) and subsequently to a second segment of the modulator; 25
wherein, the method further comprises outputting the second delayed electrical signal to a third delay stage (210) and generating, at the third delay stage, a third delayed electrical signal from the second delayed electrical signal using another passive delay element (216) and a third CMOS inverter (222), the third CMOS inverter having a third gate width smaller than the second gate width of the second CMOS inverter; 30
wherein, the method further comprises outputting the third electrical signal to a third output buffer (212) and subsequently to a third segment of the modulator; 35
wherein the first output buffer, the second output buffer, and the third output buffer are each implemented as an output CMOS inverter, and wherein each of the passive delay elements is a metal trace. 40
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Patentansprüche

1. Elektronische Treiberschaltung für einen Mach-Zehnder-Modulator, umfassend:

einen ersten Verzögerungspuffer (218), der als ein erster komplementärer Metalloxid-Halbleiter (*complementary metal-oxide-semiconductor*-CMOS)-Inverter implementiert ist, der eine erste Gate-Breite aufweist, wobei der erste CMOS-Inverter konfiguriert ist, um ein erstes verzögertes elektrisches Signal aus einem empfangenen 50
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elektrischen Signal zu produzieren und das erste verzögerte elektrische Signal an einen ersten Ausgabepuffer (202) und anschließend an ein erstes Segment (108) des Modulators auszugeben; und

einen zweiten Verzögerungspuffer (220), der dem ersten Verzögerungspuffer (218) folgt, wobei der zweite Verzögerungspuffer (220) als ein zweiter CMOS-Inverter implementiert ist, der eine zweite Gate-Breite aufweist, die kleiner als die erste Gate-Breite des ersten CMOS-Inverters ist, und wobei der zweite CMOS-Inverter konfiguriert ist, um ein zweites verzögertes elektrisches Signal aus dem ersten verzögerten elektrischen Signal zu produzieren, das durch den ersten CMOS-Inverter produziert wird, und das zweite verzögerte elektrische Signal an einen zweiten Ausgabepuffer (208) und anschließend an ein zweites Segment (110) des Modulators auszugeben; 10
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wobei die elektronische Treiberschaltung ferner einen dritten Verzögerungspuffer (222) umfasst, der dem zweiten Verzögerungspuffer (220) folgt, wobei der dritte Verzögerungspuffer (222) als ein dritter CMOS-Inverter implementiert ist, der eine dritte Gate-Breite aufweist, die kleiner als die zweite Gate-Breite des zweiten CMOS-Inverters ist, wobei der dritte CMOS-Inverter ein drittes verzögertes elektrisches Signal aus dem zweiten verzögerten elektrischen Signal produziert, das durch den zweiten CMOS-Inverter produziert wird, und das dritte verzögerte elektrische Signal an einen dritten Ausgabepuffer (212) und anschließend an ein drittes Segment (112) des Modulators ausgibt; und 30
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wobei das erste verzögerte elektrische Signal einem ersten Ausgabepuffer (202) bereitgestellt wird, das zweite verzögerte elektrische Signal einem zweiten Ausgabepuffer (208) bereitgestellt wird und das dritte verzögerte elektrische Signal einem dritten Ausgabepuffer (212) bereitgestellt wird; und 50
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2. Elektronische Treiberschaltung nach Anspruch 1, wobei jeweils der erste Ausgabepuffer (202), der zweite Ausgabepuffer (208) und der dritte Ausgabepuffer (212) als ein Ausgabe-CMOS-Inverter implementiert ist. 50
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3. Elektronische Treiberschaltung nach Anspruch 1, wobei der erste CMOS-Inverter, der zweite CMOS-Inverter und der dritte CMOS-Inverter jeweils eine 50
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aktive Verzögerung produzieren und wobei die erste Metallspur und die zweite Metallspur jeweils eine passive Verzögerung produzieren.

4. Elektronische Treiberschaltung nach Anspruch 3, wobei die aktive Verzögerung 4 Picosekunden (ps) und die passive Verzögerung 4 ps beträgt. 5
5. Elektronische Treiberschaltung nach einem der Ansprüche 1 bis 4, wobei die erste Gate-Breite 4 w, die zweite Gate-Breite 2 w und die dritte Gate-Breite w beträgt, wobei w eine Einheits-Gate-Breite derart ist, dass die Gate-Breite jeder der aufeinanderfolgenden Pufferstufen um den Faktor 2 reduziert wird. 10
6. Elektronische Treiberschaltung nach einem der Ansprüche 1 bis 4, wobei die erste Gate-Breite 16 w, die zweite Gate-Breite 4 w und die dritte Gate-Breite w beträgt, wobei w eine Einheits-Gate-Breite derart ist, dass die Gate-Breite jeder der aufeinanderfolgenden Pufferstufen um den Faktor 4 reduziert wird. 20
7. Verfahren zum Antreiben eines Mach-Zehnder-Modulators, umfassend: 25

Erzeugen, in einer ersten Verzögerungsstufe (204), eines ersten verzögerten elektrischen Signals aus einem empfangenen elektrischen Signal unter Verwendung eines ersten komplementären Metalloxid-Halbleiter(CMOS)-Inverters (218; 300), der eine erste Gate-Breite aufweist; 30

Ausgeben des ersten verzögerten elektrischen Signals an einen ersten Ausgabepuffer (202) und anschließend an ein erstes Segment des Modulators und eine zweite Verzögerungsstufe (206); 35

Erzeugen, in der zweiten Verzögerungsstufe, eines zweiten verzögerten elektrischen Signals aus dem ersten verzögerten elektrischen Signal unter Verwendung eines passiven Verzögerungselements (216) und eines zweiten CMOS-Inverters (220), wobei der zweite CMOS-Inverter eine zweite Gate-Breite aufweist, die kleiner als die erste Gate-Breite des ersten CMOS-Inverters ist; und 40

Ausgeben des zweiten verzögerten elektrischen Signals an einen zweiten Ausgabepuffer (208) und anschließend an ein zweites Segment des Modulators; wobei das Verfahren ferner das Ausgeben des zweiten verzögerten elektrischen Signals an eine dritte Verzögerungsstufe (210) und das Erzeugen, in der dritten Verzögerungsstufe, eines dritten verzögerten elektrischen Signals aus dem zweiten verzögerten elektrischen Signal unter Verwendung eines anderen passiven Verzögerungselements (216) und eines dritten CMOS-Inverters (222) um- 45 50 55

fasst, wobei der dritte CMOS-Inverter eine dritte Gate-Breite aufweist, die kleiner als die zweite Gate-Breite des zweiten CMOS-Inverters ist; wobei das Verfahren ferner das Ausgeben des dritten elektrischen Signals an einen dritten Ausgabepuffer (212) und anschließend an ein drittes Segment des Modulators umfasst; wobei der erste Ausgabepuffer, der zweite Ausgabepuffer und der dritte Ausgabepuffer jeweils als ein Ausgabe-CMOS-Inverter implementiert ist und wobei jedes der passiven Verzögerungselemente eine Metallspur ist.

15 Revendications

1. Circuit d'attaque électronique pour un modulateur de Mach-Zehnder, comprenant : 20

un premier tampon de retard (218) mis en place en tant que premier onduleur semi-conducteur à oxyde métallique complémentaire (CMOS) ayant une première largeur de porte, le premier onduleur CMOS étant configuré pour produire un premier signal électrique retardé à partir d'un signal électrique reçu et pour émettre ledit premier signal électrique retardé vers un premier tampon de sortie (202) et ensuite vers un premier segment (108) du modulateur ; et 25

un deuxième tampon de retard (220) à la suite du premier tampon de retard (218), le deuxième tampon de retard (220) étant mis en place en tant que deuxième onduleur CMOS ayant une deuxième largeur de porte inférieure à la première largeur de porte du premier onduleur CMOS, et le deuxième onduleur CMOS étant configuré pour produire un deuxième signal électrique retardé à partir du premier signal électrique retardé produit par le premier onduleur CMOS et pour émettre ledit deuxième signal électrique retardé vers un deuxième tampon de sortie (208) et ensuite vers un deuxième segment (110) du modulateur ; 30 35 40

le circuit d'attaque électronique comprenant en outre un troisième tampon de retard (222) à la suite du deuxième tampon de retard (220), le troisième tampon de retard (222) mis en place en tant que troisième onduleur CMOS ayant une troisième largeur de porte inférieure à la deuxième largeur de porte du deuxième onduleur CMOS, le troisième onduleur CMOS produisant un troisième signal électrique retardé à partir du deuxième signal électrique retardé produit par le deuxième onduleur CMOS et émettant ledit troisième signal électrique retardé vers un troisième tampon de sortie (212) et ensuite vers un troisième segment (112) du modulateur ; et le premier signal électrique retardé étant fourni 45 50 55

- à un premier tampon de sortie (202), le deuxième signal électrique retardé est fourni à un deuxième tampon de sortie (208), et le troisième signal électrique retardé est fourni à un troisième tampon de sortie (212) ; et 5
- le deuxième tampon de retard (220) comportant une première trace métallique couplée de manière fonctionnelle au deuxième onduleur CMOS et le troisième tampon de retard (222) comporte une seconde trace métallique couplée de manière fonctionnelle au deuxième onduleur CMOS. 10
2. Circuit d'attaque électronique selon la revendication 1, dans lequel chacun des premier tampon de sortie (202), deuxième tampon de sortie (208) et troisième tampon de sortie (212) sont mis en place en tant qu'onduleur CMOS de sortie. 15
3. Circuit d'attaque électronique selon la revendication 1, le premier onduleur CMOS, le deuxième onduleur CMOS et le troisième onduleur CMOS produisant chacun un retard actif, et la première trace métallique et la seconde trace métallique produisant chacune un retard passif. 20 25
4. Circuit d'attaque électronique selon la revendication 3, le retard actif étant de 4 picosecondes (ps) et le retard passif étant de 4 ps. 30
5. Circuit d'attaque électronique selon l'une quelconque des revendications 1 à 4, la première largeur de porte étant de $4w$, la deuxième largeur de porte étant de $2w$ et la troisième largeur de porte étant w , où w est une unité de largeur de porte, de telle sorte que la largeur de porte de chacun des étages tampons successifs est réduite d'un facteur de 2. 35
6. Circuit d'attaque électronique selon l'une quelconque des revendications 1 à 4, la première largeur de porte étant de $16w$, la deuxième largeur de porte étant de $4w$ et la troisième largeur de porte étant w , où w est une unité de largeur de porte, de telle sorte que la largeur de porte de chacun des étages tampons successifs est réduite d'un facteur de 4. 40 45
7. Procédé de commande d'un modulateur de Mach-Zehnder, comprenant :
- la génération, au niveau du premier étage de retard (204), d'un premier signal électrique retardé à partir d'un signal électrique reçu à l'aide d'un premier onduleur semi-conducteur à oxyde métallique complémentaire (CMOS) (218 ; 300) ayant une première largeur de porte ; 50 55
- l'émission du premier signal électrique retardé vers un premier tampon de sortie (202) et ensuite vers un premier segment du modulateur

et un deuxième étage de retard (206) ;

la génération, au niveau du deuxième étage de retard, d'un deuxième signal électrique retardé à partir du premier signal électrique retardé à l'aide d'un élément de retard passif (216) et d'un deuxième onduleur CMOS (220), le deuxième onduleur CMOS ayant une deuxième largeur de porte plus petite que la première largeur de porte du premier onduleur CMOS ; et

l'émission du deuxième signal électrique retardé vers un deuxième tampon de sortie (208) et ensuite vers un deuxième segment du modulateur ;

le procédé comprenant en outre l'émission du deuxième signal électrique retardé vers un troisième étage de retard (210) et

la génération, au niveau du troisième étage de retard, d'un troisième signal électrique retardé à partir du deuxième signal électrique retardé à l'aide d'un autre élément de retard passif (216) et d'un troisième onduleur CMOS (222),

le troisième onduleur CMOS ayant une troisième largeur de porte plus petite que la deuxième largeur de porte du deuxième onduleur CMOS ;

le procédé comprenant en outre l'émission du troisième signal électrique vers un troisième tampon de sortie (212) et ensuite vers un troisième segment du modulateur ;

le premier tampon de sortie, le deuxième tampon de sortie et le troisième tampon de sortie étant chacun mis en place en tant qu'onduleur CMOS de sortie, et chacun des éléments de retard passifs étant une trace métallique.

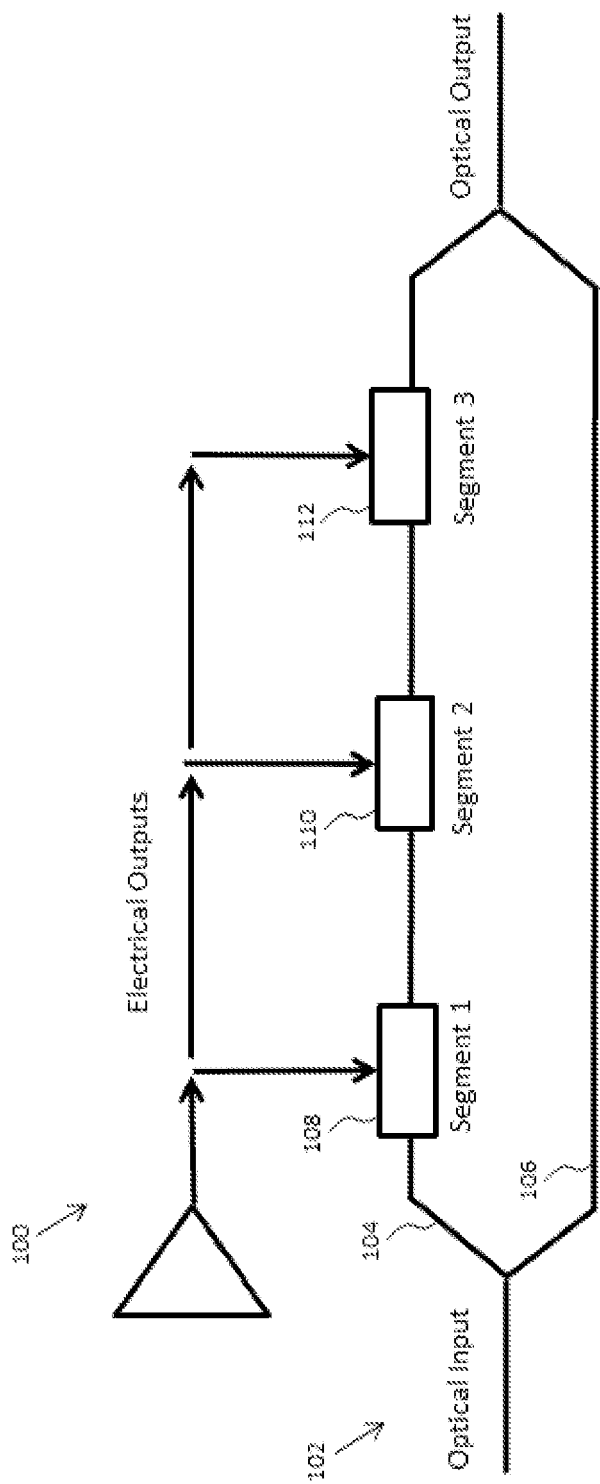


Fig. 1

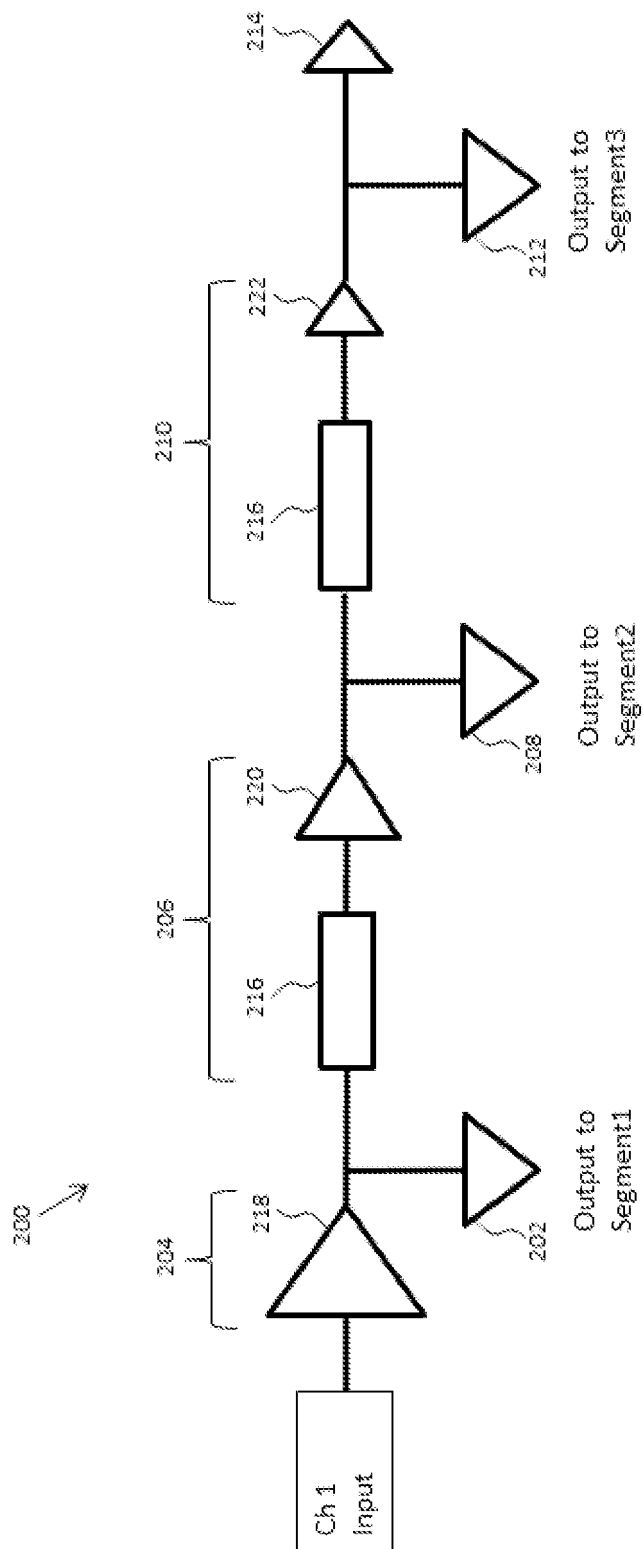


Fig. 2

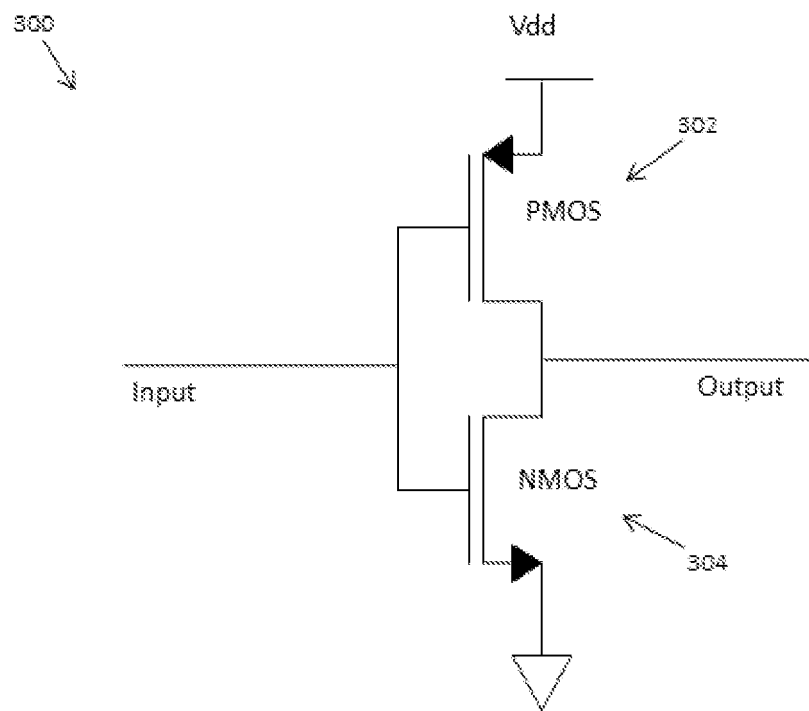


Fig. 3

PMOS

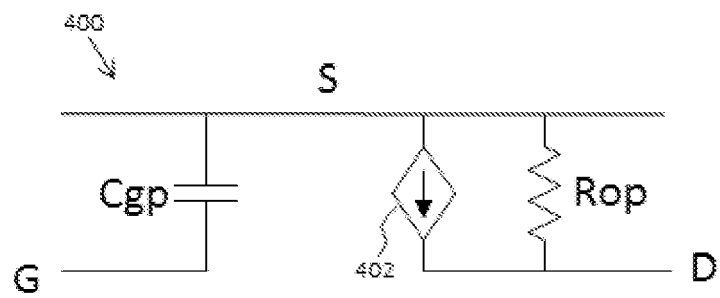


Fig. 4

NMOS

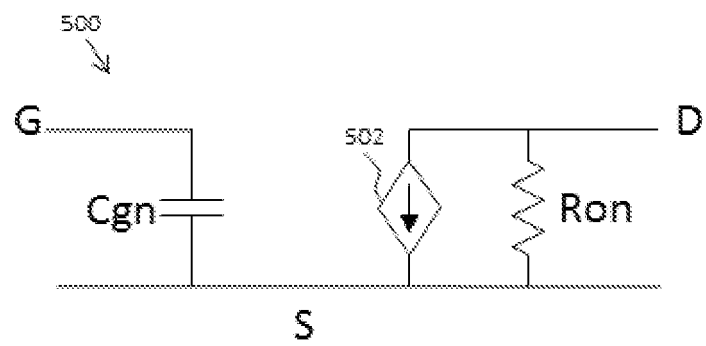


Fig. 5

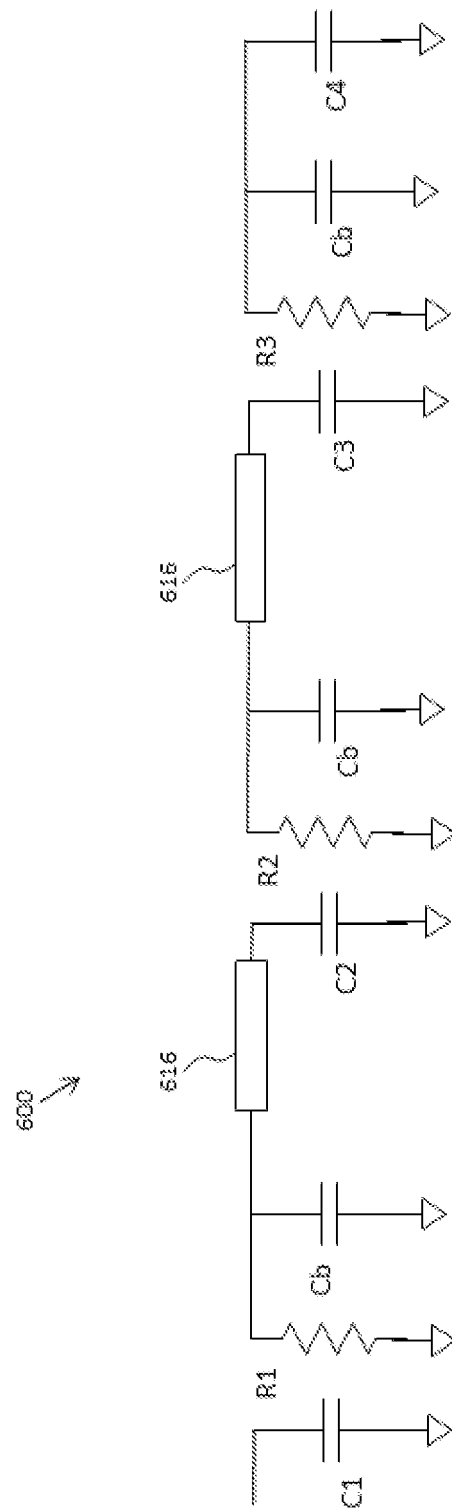


Fig. 6

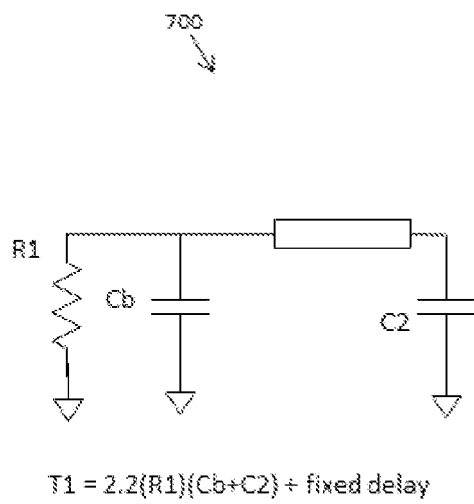


Fig. 7A

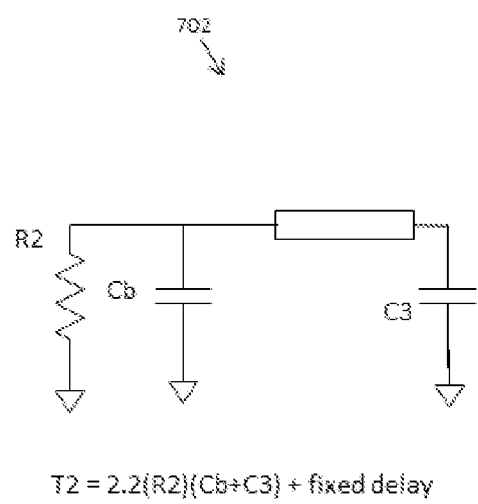


Fig. 7B

800
↙

Pre-Sim Condition	Min (ps)	Max (ps)	Variation (ps)
Increasingly sized delay buffers	4.2	6.95	2.75
Equally-sized delay buffers	3.38	5.68	2.3
Decreasingly sized delay buffers	2.34	3.72	1.38

Fig. 8

900
↙

Post-Sim Condition	Min (ps)	Max (ps)	Mean (ps)	Variation (ps)	Variation (%)
Equally-sized delay buffers	8.372	12.91	10.641	4.54	42.67%
Decreasingly sized delay buffers	6.7	9.8	8.25	3.1	37.58%

Fig. 9

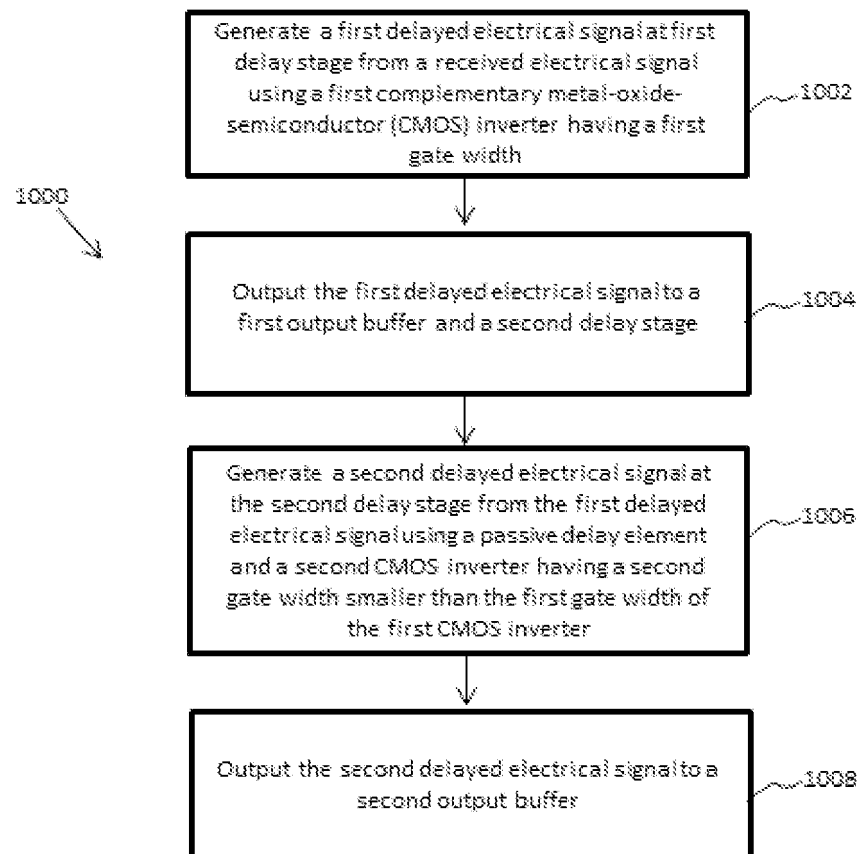


Fig. 10

REFERENCES CITED IN THE DESCRIPTION

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