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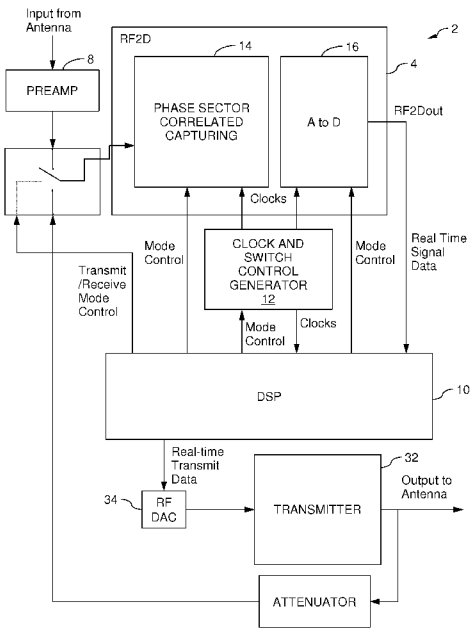

(57) Abstract: Values representative of modulation signal components are extracted from a modulated signal. The modulated signal contains a modulation signal. A local clock signal is developed which correlates in time to the modulated signal and has a plurality of non-overlapping phase sectors per cycle. Signal values are acquired from the modulated signal, separately for at least one phase sector of one cycle of the local clock signal. At least two signal values from the same local clock cycle, but different phase sectors are combined to obtain at least one combined signal value representative of a modulation signal component.

INTERLEAVED PHASE SECTOR BASED RF SIGNAL DECIMATION

BACKGROUND

[001] There are many different modulation schemes used to modulate a Radio Frequency (RF) carrier or an Intermediate Frequency (IF) carrier with a lower frequency modulation signal. There are different advantages and disadvantages to each of the commonly used methods. There are also many different wireless formats or standards used within the wireless product marketplace today. These standards differ not only in modulation technique used, but also in the bandwidth utilized by the wireless system, the RF bandwidth of a single channel, and the use, or not, of various spread spectrum techniques, such as CDMA (Code Division Multiple Access), frequency hoping techniques, or, most recently gaining in popularity, OFDM (Orthogonal Frequency Division Multiplexing). An idealized goal of a Software Defined Radio (SDR) system is to be able to transmit and receive using any of these techniques and to be able to switch between them by merely changing the software code running on such an SDR system.

[002] Cognitive Radio Systems, as currently envisioned within the R&D community, include plans for flexible transceiver's, which can adjust to band utilization variations as needed, changing frequency bands, modulation techniques, and transmission bandwidths as required to make best use of the current RF environment. This discussion continues, yet currently there is not even a cost effective or efficient method to implement a fully flexible SDR.

[003] Given the lack of fully flexible SDR technology, each of the many differing modulation techniques and wireless standards have historically required different customized analog front-end receiver blocks and customized back-end analog transmitter blocks for each bandwidth, modulation technique, or wireless standard accommodated. The concept of SDR has often been put forth with the promise of a single circuit block that could, under software control, be able to operate and provide competitive performance, while working with any of the current wireless transmission schemes. Yet this promise remains unfulfilled.

[004] The roadblocks to achieving fully flexible SDR solutions have been many. The use of IF stages, creating difficult to manage spurs, and image frequency artifacts, also create overly complex matrices of usability limitations. Each combination of center frequency, bandwidth, and modulation scheme has required specific design attention despite a theoretically programmable feature selection. Quadrature modulation and all schemes which make use of phase variation add a great deal of complexity to both reception and transmission. Maintaining orthogonality and minimizing mismatches between the I and Q channels are ongoing challenges. Conventional zero IF approaches to the SDR challenge attempt to simplify the IF complexities, but compound the I/Q mismatch and orthogonality issues and typically degrade noise performance as well. Real solutions to the SDR challenge have seemed perennially imminent, while remaining ethereal.

DESCRIPTION OF THE DRAWINGS

[005] Figure 1 is a system block diagram showing one embodiment of the present invention implemented in a phase sector based software defined radio.

[006] Figure 2 is a timing signals chart for quadrature and phase sector processing.

[007] Figure 3a is a diagram illustrating one embodiment of a phase sector distributed integrator of the present invention.

[008] Figure 3b is a timing diagram for the diagram of Figure 3a.

[009] Figure 4 is a diagram illustrating one embodiment of alternating blocks as phase sector distributed integrators with a charge responding A to D.

[0010] Figures 5a-b are a flow chart showing one embodiment of the present invention method for extracting values representative of modulation signal components from a modulated signal.

[0011] Figure 6 is a flow chart showing one embodiment of a method for accumulating a modulated signal with a capacitive device.

[0012] Figure 7 is a flow chart showing one embodiment of accumulating and combining accumulated values.

[0013] Figure 8 is a flow chart showing an alternate embodiment of accumulating and combining accumulated values.

[0014] Figure 9 is a flow chart showing another embodiment of accumulating and combining accumulated values.

[0015] Figure 10 is a flow chart showing one embodiment of a method for continuously accumulating charge.

[0016] Figure 11 is a flow chart showing a method for using the alternating blocks of Figure 4.

[0017] Figure 12 is a flow chart showing one embodiment for the method of the present invention including a transmit mode.

[0018] Figure 13 is a flow chart illustrating one embodiment for altering a local clock signal.

[0019] Figure 14 is a diagram illustrating one embodiment of alternating blocks as phase sector correlated decimation filters, combining sampled values by accumulation, and passing accumulated values to a charge responding A to D.

DETAILED DESCRIPTION

[0020] There are many common terms used in the RF industry which are generally understood to have consistent meanings, but which can, by usage or by application, have slightly varying scope or specific meaning. For clarity, there are three terms which will now be defined very specifically, which in some cases will be used in place of more common usage meanings or terms, other such specific terms will be described upon initial use. A modulated signal is one such term, carrier signal is another, and modulation signal is another. A modulated signal is a signal which includes information representative of a modulation signal, which is superimposed, encoded, or modulated onto a carrier signal to become the modulated signal, and from which the original modulation signal can be recovered by some means. Generally, most if not all Radio Frequency (RF) signals are modulated signals, as are all Intermediate Frequency (IF) signals. The carrier signal is a single frequency sinusoidal waveform, generally higher in frequency than any of the spectral content

of the modulation signal. The modulation signal is a signal superimposed on a carrier using any of a wide variety of modulation techniques common in the art.

[0021] Developing a more ideal receiver solution for SDR has resulted in various novel methods, blocks, circuits, and systems. Although the present invention is not limited in scope to SDR applications. Figure 1, shows a top level block diagram of a Phase Sector Based Software Defined Radio, (PSB-SDR) system 2, based on these developments. The RF2D block 4, a novel development, is an input block that receives a wide-band modulated signal from a wide-band amplifier 8, or perhaps directly from an antenna, and outputs to a DSP block 10 a wide-band stream of data where each piece of data is representative of a modulation component and where the data is phase sector correlated. A modulation signal component here is any quantity, value, or signal, which when combined with other modulation signal components, can form a representation of a modulation signal. A representation of a modulation signal thus formed is then referred to as a reconstructed modulation signal.

[0022] To understand phase sector correlation, phase sector must first be understood and defined. A phase sector represents a span of the phase of a local clock signal, which remains essentially constant from one clock cycle to the next in the phase angle of the local clock at which it begins and in the phase angle of the local clock at which it ends. Each cycle of the local clock signal has multiple phase sectors. While it is not necessary that phase sectors be contiguous, where every possible phase angle of the local clock is thereby included in one or another phase sector; it is desirable that phase sectors remain non-overlapping so that no two phase sectors both include any one phase angle of the local clock. Generally, it is intended that phase sectors be nearly contiguous, so that every phase be included in one or another phase sector, except for transition phases at the beginning or end of a phase sector. However, it is possible to have phase sectors which have significant gaps between them, yet they should never overlap.

[0023] The local clock signal is an approximately constant frequency signal, generated by a local oscillator block 12, or timing system, where local means within the context of the receiver system, which during the normal operation of receiving a signal is intended to be at the same frequency and in a constant phase relative to the carrier signal used to construct the modulated signal input to the RF2D block 4. Generally, the actual carrier is generated at the transmitter, and the pure carrier signal itself is therefore not generally available at the receiver. Furthermore, the carrier signal is not necessarily even present within the modulated signal, depending on modulation and transmission scheme. There are various methods used to establish the correct frequency and phase for a local clock. Most methods use some form or other of either a phase or a frequency locked loop system. Such phase lock is generally achieved by first defining some window of time, established by timing format, during which the modulated signal can be relied upon to be representative of the carrier frequency, and to be at some known reference phase. However, precisely how this works can vary substantially from one system to another. The system herein described is an SDR system intended to be capable of receiving essentially any transmitted signal. It is therefore necessary for the system to be capable of all methods of frequency or phase lock.

[0024] In the most general case, the most that can be relied upon is that the local clock, when in proper frequency and phase relationship relative to the source carrier, can generally be said to be correlated in time to the modulated signal. It is important to note however, that this is not always a strong mathematical correlation in the strictest sense. Where the carrier is suppressed (not transmitted) and if the modulation factor is high (a statistically high percentage of the modulation range is utilized) this means there may not be very much of the carrier frequency contained in the modulated signal, such that the mathematical correlation may not be very high at all. In such cases, as long as the signal content of the modulated signal can still effectively be demodulated by any means, using the local clock at a frequency near

or in the band of the modulated signal, then the local clock signal can still be considered as correlated in time with the modulated signal.

[0025] The term correlation is used far more strictly and quite differently for the term phase sector correlation. Here, unlike with the local clock whose correlation in time with the modulated signal might be quite low mathematically, yet still be considered correlated, phase sector correlation is intended to indicate a very high level of mathematical correlation, virtually 100%. Each phase sector amounts to a window of time during which the modulated signal gets acquired or captured, with the value captured becoming associated only with the phase sector active during the time of capture. The fact that phase sectors are non-overlapping ensures that any instantaneous time value of the input signal gets included in only one phase sector. This maintains the independence of the modulated signal values so captured and the significance of the phase sectors as separate from one another. Signal transmitted or received within a phase sectors span remains isolated and separated from signal transmitted or received during other phase sectors.

[0026] Phase sector correlation can now be understood and signal or data can be understood to be phase sector correlated whenever all data or signal captured during any one phase sector is collected or captured and kept separate from data or signal captured or collected during any other phase sector. Wherever this separation is maintained, the data or signal can be said to be phase sector correlated. Again, this correlation is a type of correlation where a high mathematical correlation is important in order for it to be phase sector correlated. In fact, phase sector correlation indicates a case where full correlation is virtually assured by design or by definition.

[0027] The data stream output of the RF2D converter block 4, RF2Dout, has an adjustable data rate, f_RF2Dout, adjustable under the control of the DSP 10 and generally chosen to be fast enough to at least provide Nyquist rate data relative to the widest band information present in the incoming signal. In this way, no loss of bandwidth in the data or signal received occurs within the RF2D block 10. It is

important to note however, that it would be possible to allow a reduction in bandwidth, if so desired, within the RF2D block merely by selecting an RF2Dout speed slower than the Nyquist rate relative to the widest band information present in the incoming signal.

[0028] The first processing block within the RF2D block 4, is a discrete time processing block called Phase Sector Correlated Capturing (PSCC) 14, where the modulated signal input to the RF2D block 4 is broken up into discrete time segments and thereby sampled or acquired according to phase sector and then processed without yet being converted to a digital or binary representation of the signal. As such, the signal in this first stage still has full analog signal resolution, where the effective resolution is limited only by a noise floor present. This noise floor is formed as a combination of local circuit processing noise and noise present in the incoming signal. In one embodiment, this discrete time block also includes multiple channels of low-pass filters, which act like discrete time decimation filters on the input data. There is one filter for each phase sector. Each of these phase sector correlated decimation filters has a decimation rate that is variable depending on the number of local clock cycles over which the sampled values are acquired. The simplest discrete time filter for this application is implemented by simply adding up (or "accumulating") the captured signal values (or "sampled values"), separately by phase sector, from one cycle to the next. In this way, each value captured during any one phase sector of one cycle of the clock is simply added together with signal values captured during the same phase sector of subsequent clock cycles.

[0029] This low pass filtering is most simply achieved by the adding up, or the accumulation, of the phase sector correlated values from one clock cycle to the next. This most typically accumulates one additional value per phase sector, once for every local clock cycle that occurs during the entirety of one full RF2Dout cycle period. Once accumulated, this results in one value passed to the DSP for each phase sector per RF2Dout cycle period. Since this occurs within a discrete time analog resolution block, the noise which is typically random or white in nature would

tend to add up stochastically, whereas the signal tends to add up linearly. This yields a profound advantage for this methodology. This means the signal to noise ratio tends to improve as the signal is accumulated, by a factor roughly equal to the square root of the down-conversion factor, where the down-conversion factor is the RF or local clock rate divided by the RF2Dout rate, f_RF2Dout. This accumulation of values from one clock cycle to values accumulated from other clock cycles can generally be done with any value combining system, and is probably most simply implemented using switched capacitor techniques.

[0030] Another option, rather than down-conversion, is to pass the signal captured for each phase sector to the A to D 16 at full speed, one value per phase sector per local clock cycle. This amounts to f_RF2Dout = Fclk, where Fclk is the frequency of the local clock, which is most typically equal in frequency to the carrier frequency of the modulated signal. This would require that the DSP 10 process values coming in from the A to D 16 at a rate equal to the number of phase sectors per clock cycle times the Fclk rate. For a quadrature signal, that would be at least four times the Fclk rate. Depending upon the carrier frequency involved, that can become a large amount of individual pieces of data processed very quickly, in effect using up a great deal of the DSP block's processing power. This can also generate quite a speed challenge for the A to D block 16. Under some signal conditions this might be the preferred processing method, particularly where Fclk is not too high, but in most conditions, it is more desirable to reduce the input signal rate to the DSP 10, using the down-conversion option. In fact, in many systems this down-conversion capability is a fundamental enabler, without which, such a system simply cannot be made to work fast enough.

[0031] For a flexible and programmable system, as this PSB-SDR system 2 is intended to be, it is generally desirable to be able to capture data nearly continuously. In order to avoid regular dumping intervals during which the input signal is ignored, the RF2D block 4, in one embodiment, includes two identical discrete time processing input blocks, one receiving input values, while the other is

dumping its values to a subsequent block, usually the A to D block 16. Figure 4 illustrates one embodiment of these two blocks 18, 20 (accumulation blocks) for a phase sector integration capturing system, described below. Each of these two blocks also has their value reinitialized during its dumping period, reinitialized to a level which the A to D 16 would receive and interpret as a zero value. This occurs after it has dumped its value to the A to D 16 but before it is reconnected to new input for its subsequent acquisition phase. In this embodiment, these two blocks are included within in the Phase Sector Correlated Capturing block 14 of Figure 1. These two blocks then alternate roles on alternate RF2Dout cycles. This allows the system to collect signal for every local clock cycle. Ultimately, this provides a better signal to noise ratio of the resulting recovered modulation signal, for any given modulated signal input, than a scheme which ignores any number of cycles of modulated signal input. This also potentially avoids, or at least minimizes potential aliasing problems, and the complexities of managing adjustable anti-aliasing filters.

[0032] Regardless of the carrier frequency of the incoming modulated signal, regardless of its bandwidth, regardless of the modulation scheme utilized, and regardless of the information the modulation contains; there is some selection of the Fclk/RF2Dout down-conversion factor, the number of phase sectors per clock cycle, and the selection of local clock frequency; such that the resulting digitized phase sector correlated values can be passed to the DSP block 10, containing the information necessary to fully decode, demodulate, filter, and present data in whatever form most desirable, for any RF signal which can be transmitted, and to do so in a way which provides the best signal to noise ratio possible. Because of this, this system is capable of the full flexibility envisioned in the original concept of SDR, as no conventional or prior art circuits or systems have been.

[0033] It is instructive to consider one specific type of modulation, to see how PSCC provides benefits for a specific case. Quadrature modulation is used for many different systems, 8QAM, 16QAM, and 32QAM to name a specific few, and countless others. Quadrature modulation is also key to consider because the

quadrature relationship of the I and Q signals adds the significance of phase variation, as well as generally adding complexity to the demodulation process. A quadrature modulated signal is most simply processed using PSCC, with four phase sectors per local clock cycle. Figure 2 includes waveforms, which show the timing for each of four equally sized phase sectors at (a), (b), (c), and (d). In order to have these timing relationships, a phase lock condition between the carrier that formed the modulated signal and the local clock must exist. It is simplest to merely assume that this condition does exist for now. Such a phase lock condition can be accomplished through conventional means, using a phase locked loop, but a much preferable enhanced method for achieving this phase lock flexibly is also discussed further below.

[0034] Simple impulse sampling may not provide the best signal to noise ratio, but is the most common method of acquiring a discrete time representation of a signal, and therefore an interesting case to consider. Applying PSCC to simple impulse sampling results in a technique described below as Phase Sector Impulse Sampling, or PSIS Impulse sampling must be done at regular intervals. This, in combination with phase sector correlation, requires that each phase sector include an equal number of evenly time-spaced samples. For a four phase sector or quadrature case, this necessitates an integer multiple of four samples per Fclk cycle. The simplest case is again the best to consider, which is just the single sample per phase sector case. The only remaining choice then is where to phase the impulse sample within the phase sector. Aligning each impulse sample time with the center of its phase sector, becomes the case to consider, for reasons which become more apparent as phase locking is considered, as described in greater detail below.

[0035] Phase Sector Impulse Sampling, PSIS operates by first acquiring a sampled value using an impulse sampling method. This is done for the PSIS system shown in Figure 14 for each of four phase sectors, during the time when each of the sampling switches, SWa, SWb, SWc, SWd are closed. During each of these respective intervals, the sample capacitors Ca, Cb, Cc, Cd, each acquire whatever

charge is necessary so that the voltage on the sample capacitor closely matches the input signal voltage by the end of the sample interval. This acquired charge then becomes the sampled value. It is instructive to note, that generally, with the use of switch-cap circuits, it is important to consider, and to factor out of the signal, any variation in offset voltages present at the input of op amps. These techniques are well understood in the art, so for simplicity, these details have been left out of Figure 14. Any of these offset cancellation techniques could be used in conjunction with this circuit without altering its functionality pertaining to the concepts herein presented.

[0036] Once a sampled value is thus acquired on each of capacitors, the sampling switch is then shut off. Each of the respective complement switches, SWa_BAR, SWb_BAR, SWc_BAR, SWd_BAR then transfers the charge on the sample capacitor, the sampled value, to the accumulation capacitor of either the block 1 or the block 2 decimation filter, whichever one is in capture mode. Note that in the drawing SWa_BAR is designated by the letters SWa with a line above it to designate the BAR notation, indicating that the timing for SWa_BAR is the inverse of the timing for SWa. It is also important to note, that the timing for each of the complement switches is non-overlapping with that of the sampling switches, as is typical for most switched capacitor circuits, so that no sampling switch and its respective complement switch are ever on at the same time. The timing of the sampling switches relative to each other can be seen in Figure 3b. However, it is important to note, that the timing of signals a b c and d of Figure 2 are arranged to show the intervals of each phase sector, but these are NOT phased the same as the switch control signals for the PSIS system. The effective moment of impulse sampling occurs at the end of the sampling interval. This should occur at the moments of impulse sampling shown in Figure 2e, which as previously described, should occur at the center of a phase sector, as shown in Figure 2, for the case where only one sample is captured per phase sector.

[0037] Each accumulation type decimation filter of Figure 14 then continues to accumulate sample values by phase sector during one entire cycle of the f_RF2Dout clock, At the end of that clock period the decimation filter which had been capturing, switches to transfer mode, and begins passing the accumulated values for each phase sector to the A to D, one value at a time. While the other decimation filter block is then put into capture mode, and begins accumulating sampled values.

[0038] There are various uses of capacitors made throughout the circuits, systems, and blocks of the PSB-SDR 2. Each capacitor as described here and throughout this writing could be replaced with a capacitive device. A capacitive device, being any device or plurality of devices generally having two or more terminals, which has capacitance between two terminals such that it behaves like a conventional capacitor, in a manner sufficient so as to allow the circuit or system to behave approximately as it would if a capacitor were in its place, generally having an amount of charge stored on the device equal to the voltage across the device multiplied by its capacitance. For simplicity, the term capacitor will be generally used, with the understanding that it could be replaced by any capacitive device.

[0039] Figure 2 (e) shows an incoming modulated signal, having an all in-phase (I) signal, which means that the I component is maximized, and the quadrature (Q) component is zero. While a real RF signal would have phase variation, there are only three full cycles of the modulated signal shown. The bandwidth limitations on most RF signals, would not allow the modulated signal to vary significantly in phase over three cycles, so the pure sine wave shown for Figure 2 (e) is reasonably realistic over the time window shown. For this case, the impulse samples are also shown in Figure 2 (e), where there are four impulse samples per cycle of the modulated signal. From left to right, these impulse samples shown in Figure 2 (e) are for phase sectors A, B, C, D, A, B, C, D, A, B, C, D. PSCC allows for multiple impulse samples to be accumulated over multiple Fclk cycles, as long as the accumulation is done separately for each phase sector, yielding a separate accumulated value for each phase sector, and so that any values accumulated are

captured within the same phase sector, although probably over multiple cycles. This accumulation, for the PSIS case, can be accomplished with the addition of a switched-capacitor circuit designed for this purpose, Figure 14 shows two such blocks. Here each switched capacitor filter provides an analog decimation filter, separately for each phase sector, accumulating the sum of the values captured on a capacitor, for later transfer to the A to D block 16. For the signal state shown in Figure 2 (e), all of the phase sector A values would be accumulated into a single value along with those from subsequent cycles, for however many local clock cycles are included in a single RF2Dout cycle. Accumulation is the simplest approach, but a more complex switched capacitor filter could also be used here to achieve steeper band response features.

[0040] From Figure 2 (e), it is plain to see that all of the phase sector A values are identical, as are all of the phase sectors B, C, and D values respectively. This is a direct result of the bandwidth being too narrow for the phase of the modulated signal to vary too quickly, in combination with the modulated signal having the same frequency as the Fclk. As described above, the down-conversion ratio of Fclk/RF2Dout would normally be chosen so that the bandwidth of the resulting RF2D output data would not be significantly reduced, which means generally, that there would not be much variation in the values of all of the A phase sector values over the time of their accumulation. Naturally, this also applies to the B, C, and D values respectively.

[0041] Each of the values for phase sectors A, B, C, and D, whether combined over multiple Fclk cycles or not, gets transferred and converted to a digital value by the same A to D converter 16, with resulting digital values then made available to the DSP 10, while their phase sector correlation also is provided to the DSP 10, so that each value is still identified by the A to D as data resulting from phase sector A, B, C or D. Mixing of these phase sector correlated values can then be easily performed by the DSP. The I or in-phase signal can be formed by adding data from the A and B phase sectors and subtracting the data from the C and D phase sectors, or I = A +

B - C - D, where A, B, C, and D now represent digital values collected during each of their respective phase sectors, possibly over multiple Fclk cycles. The Q or quadrature signal is similarly developed by combining the phase sector values as follows, Q = B + C - A - D. In this way, each of these combinations yields one value for I and one value for Q per cycle of RF2Dout.

[0042] The conventional approach to performing a phase locked loop (PLL) function is to use a phase comparator that compares the phase of a received modulated signal to that of the local clock, usually during a predefined reference period discerned from receiving a signal with the proper timing format. The phase comparator most conventionally uses a four quadrant multiplier or an exclusive-OR block that essentially implements a binary type multiplication on the two input signals, where one is the local clock and the other is the received modulated signal, where the multiplier is only on during a predefined phase reference period. When not on, the output of this phase comparator is disabled and a low pass filter, most often just a single capacitor, holds its voltage unaltered until the next predefined reference period occurs. This type of phase comparator tends to cause a phase lock loop to lock with the two inputs to the phase comparator in quadrature with one another that is 90 degrees out of phase, which results in an equal period of charging the hold capacitor as discharging it per local clock cycle, during the predefined reference period. The output of this phase comparator is often that of a charge-pump, charging or discharging the hold capacitor in response to the relative phase of the local clock and reference period signal. The voltage on the capacitor then typically becomes the control voltage input for a voltage controlled oscillator.

[0043] This same functionality can be achieved, using phase sector correlated capturing as applied to a quadrature modulation case, by employing a digital low pass filter technique on the post conversion mixed Q signal, developed within the DSP, or, alternately, by acting on a separately developed control signal having control signal values developed within the DSP from accumulated values previously discussed. This low pass filtering would then be done to obtain a control value or

voltage to be applied as a control input to the local oscillator, thereby controlling its frequency, as with a convention Voltage Controlled Oscillator, (VCO), and thereby forming a PLL 10. Alternately, some of the low pass function could be reserved for an analog final stage, which could be a charge pump type design, either charging or discharging a hold capacitor, similar to that of a conventional PLL phase comparator output and VCO control input, but with the signal driving it being a digitally low pass filtered version of the Q signal. This digital low pass and/or charge pump could then be programmed, under the control of the DSP 10, to be enabled only during the correct reference period, thereby again creating an effective sample hold on the phase comparator output. The voltage on the hold capacitor is then applied to a VCO, and so controls the oscillator frequency used to develop the local clock, and the timing of the four phase sectors. This now essentially forms a fully programmable PLL. The programming for this could be changed, the precise filter response of the low-pass could be changed as with the rest of the features of this SDR system 2, to accommodate any signal/modulation format, now including the timing details of the desired phase reference period. The programming could also be changed in response to signal conditions, by having a control signal evaluator, probably formed merely by program steps operating within the DSP, which can evaluate the control signal described above, before it is low pass filtered, or any of the other signals otherwise developed within the DSP, comparing the signals to any number of characterization metrics, many determined by mere mathematical processing of the control signal, to determine what the low pass filter characteristics should be, or to determine how the control signal is processed in developing the control value or voltage used to control the VCO.

[0044] Mixing the accumulated values after any down-conversion desired, and after A to D conversion has taken place, constitutes a novel methodology called Post Conversion Mixing. This Post Conversion Mixing is advantageous in every way, as it provides for virtually no mismatch between either the I and Q channels, nor between either of those and the phase detection mixing traditionally used to provide

the control voltage to control the voltage controlled local oscillator of the PLL. All of this mixing is now done post down-conversion and post analog to digital conversion, and is therefore acting on data which has been processed through a single analog block and a single analog to digital conversion process. I and Q are now formed by mathematically mixing identical data. This leaves essentially no place for I/Q mismatch to occur within the receiver. This is a major advancement over conventional techniques.

[0045] Previously, a method implementing PSCC using standard impulse sampling techniques was described, PSIS. An alternative is to use Phase Sector Integration Capturing (PSIC), a novel technique capable of improved noise performance and capable of continuous signal capturing, a further enhancement to be described in detail below.

[0046] The most straight-forward or simplest way of implementing Phase Sector Integration Capturing, is to consider Figure 3a, a phase sector distributed integrator 22. For Figure 3a, this block 22 and its signal timing is arranged to show a specific case of Phase Sector Integration Capturing, and a special case of Phase Sector Distributed Integrator, where the system is set up to perform quadrature detection. Similarly to the description above considering the use of impulse sampling, this arrangement includes a specific selection where there are four phase sectors per local clock cycle, and where the phase relationship between the local clock and the incoming modulated signal is phase locked, just as in the impulse sampling case, in a manner and with a static phase relationships consistent with that of traditional quadrature signal detection methods.

[0047] The input signal, a modulated signal, which might be received directly from an antenna, or from a very wide-band amplified version of signal present at the antenna, or perhaps an attenuated output of a transmitter, is applied to one side of a resistor Rin, where the other side of the resistor is connected to the inverting input of an ideal op-amp 24. The positive input 26 to the op-amp is connected to a DC voltage reference level, which might be ground, and is certainly an effective AC

ground. The output 28 of the op-amp is connected to four switches, SWa, SWb, SWc, SWd (for the quadrature case), where only one of the switches is closed or on at any one time. The other side of each switch is connected to one side of a capacitor, Ca, Cb, Cc, Cd, with the other side of the capacitor Ca, Cb, Cc, Cd connected back to the inverting input 30. Each switch SWa, SWb, SWc, SWd is connected to its own capacitor Ca, Cb, Cc, Cd. In this way, because of the switches SWa, SWb, SWc, SWd, only one of the capacitors Ca, Cb, Cc, Cd is connected at any one time. While one of the switches SWa, SWb, SWc, SWd is closed, the op-amp 24 acts on the capacitor Ca, Cb, Cc, Cd through the switch SWa, SWb, SWc, SWd, providing whatever voltage is required to keep the inverting input of the op-amp 24 essentially and approximately equal to the positive input 26 of the op-amp 24. Since the inverting input node is then maintained at a constant voltage, in this case at ground, any signal present at the input side of the resistor Rin, is converted into a current through the resistor Rin. This current has no where to go except through the capacitor Ca, Cd, Cc, Cd having its related switch SWa, SWb, SWc, SWd on. In this way each capacitor Ca, Cd, Cc, Cd, is charged with a current that is a replica of the input signal, and thereby the charge on the capacitor Ca, Cd, Cc, Cd becomes proportional to, and a replica of, the integral of the input signal during the period when its associated switch SWa, SWb, SWc, SWd is on. In this way, this block 22 becomes essentially a phase sector accumulator, accumulating a value, in this case charge, over each non-overlapping, timing system developed phase sector.

[0048] Each of the four switches SWa, SWb, SWc, SWd is then sequentially turned on, after the other switches SWa, SWb, SWc, SWd are all off, so that there is no overlapping time period where more than one switch is on. This prevents charge representing signal, which has correctly been acquired onto one capacitor Ca, Cd, Cc, Cd, from being altered by signal during a different phase of clock, or by charge on an alternate capacitor Ca, Cd, Cc, Cd. The timing of the turning on of each of the switches SWa, SWb, SWc, SWd is sequentially arranged, so that any one switches

SWa, SWb, SWc, SWd period of on time, always follows the on period of the same other switch SWa, SWb, SWc, SWd. So, each switch and capacitor combination A, B, C, and D, is named so that the time when switch SWa is on always follows when switch SWd is on, SWb always follows SWa, SWc always follows SWb, and SWd always follows SWc, these four periods together complete one full cycle of the local clock.

[0049] As described above, the circuit from Figure 3a operates so as to integrate the input signal current, and thereby store a charge on each of the capacitors, which is proportional to the integral of the input signal over the period where the switch associated with that capacitor is on. This then results in charges, referred to as Qa, Qb, Qc, and Qd, which are the charges representative of accumulated values, specifically analog accumulated values, on each of the four capacitors Ca, Cb, Cc, Cd of Figure 3a, during periods A, B, C, and D, respectively. Figure 3b shows the timing of SWa, SWb, SWc, and SWd.

[0050] After as few as one full cycle (or perhaps after multiple cycles) each of the capacitors Ca, Cb, Cc, Cd, which have now accumulated a signal related charge as an accumulated value, are then dumped into a charge responding A to D converter 16, where a digitized accumulated value is developed, which is directly proportional to the amount of charge accumulated on each capacitor Ca, Cb, Cc, Cd. A separate A to D output value is acquired for each phase sector value, one for the charge accumulated during each of quadrature phase sectors A, B, C, and D.

[0051] If the conversion to digital is done at the end of every local clock cycle, there is one digital value for each quadrature phase A, B, C, and D, for each local clock cycle. However, if the integration continues over multiple local clock cycles, then there is only one digital value generated for each quadrature phase A, B, C, and D, for each multiplicity of local clock cycles. The number of cycles over which the integration continues before executing an A to D on the integrated values, becomes the down conversion factor. If the integration continues over five cycles, then the accumulated value converted by the A to D 16 is first integrated for each

quadrature phase, over five cycles, and the value converted to digital is effectively an average of the input signals integration by phase sector, over the five cycles. This effectively executes a down conversion by a factor of five. This means the A to D 16 does not have to execute an A to D nearly as quickly. Furthermore, as before with the impulse sampled case, the data is averaged, so any random noise is reduced, while the signal in effect, gets larger because of the ongoing integration. None of the desired pass band data is lost unless the down-conversion factor becomes large enough to result in a restriction of the bandwidth to a value that is narrower than that of the data contained in the modulation of the modulated signal. Ideally, the down-conversion factor is chosen so as to make the bandwidth just large enough to avoid significantly limiting the bandwidth of the data. The exact bandwidth chosen would likely be chosen to provide the best signal to noise ratio of the resulting data.

[0052] If a local clock circuit which generates the full cycle described above, is synchronous (at the same frequency) with the carrier frequency of a modulated signal present at the input of the circuit of Figure 3a and if the static phase relationship between the local clock and incoming modulated signal is correctly set, the analog accumulated value represented by the charge accumulated on each of the capacitors Ca, Cb, Cc, Cd, after one full cycle, could then be selectively combined together in the correct polarities, and thereby reconstruct one RF cycle's worth of demodulated I and Q base-band signals, for that cycle.

[0053] Phase Sector Integration Capturing can be used in this way, to achieve modulation signal values, using analog discrete time methods. Selectively combining each of the capacitors charge values, with the correct polarity selection for each, amounts to the mixing function, and thereby reconstructs analog discrete time in-phase or quadrature signal values. This combining can be accomplished using any accumulated value combining system. Where the processing block is analog, the values are usually charges, and the combining is most commonly implemented using switched-capacitor techniques. Where the combining is

accomplished using digital values, the accumulated values are just digital values in active memory, and the accumulated value combining system generally becomes a mathematical step executed by a program running on within a DSP block. Considering the case where analog modulation signal values are formed before digitization, this is done for each clock cycle, according to Qi = Qa + Qb – Qc - Qd, and Qq = Qb + Qc - Qa - Qd, where the charges Qi and Qq so formed are now representative of modulation signal values, analog modulation signal values, with Qi as a charge representing an in-phase modulation value, a single cycles reconstruction of the in-phase modulation, and with Qq representing a quadrature modulation value, a single cycles reconstruction of the quadrature modulation.

[0054] As described earlier however, there is great advantage in performing this mixing function in a post conversion manner instead. The point here is that these analog accumulated values contain the significance of the quadrature and in-phase signal components, and that this is one alternate and novel way that this Phase Sector Integration Capturing technique could be used. If this system were used this way, where discrete time analog modulation values are formed, it is also possible to then further combine these already mixed analog values, using a modulation value combining system, which would combine modulation values from multiple clock cycles, inherently creating a discrete time filter. This modulation value combining system could also be implemented within the DSP block, merely by performing the correct mathematical operations on digitized modulation values. Where implemented, this modulation value combining system would most typically be used to create a low pass, discrete time, or digital decimation filter.

[0055] The distributive property of multiplication over addition also applies over accumulation and suggests that if charge is accumulated first by phase sector and the accumulated values are then combined together in the correct polarity, that the resultant can be no different than if the values are first multiplied by the correct polarity and then accumulated all at once. Conventional mixing is achieved by multiplying the modulated signal by the correct polarity, and then accumulating all at

once. This is necessarily done separately for I and Q, once multiplying by the in-phase clock, Figure 2 (f), and once by the quadrature clock, Figure 2 (g). Each of these mixers outputs then get separately low pass filtered, similar to integration over its reject band, which is essentially accumulated all at once, without regard to phase sectors. Phase Sector Integrated Capturing can achieve the same resultants, but in a way that provides much greater flexibility by accumulating by phase sector first, then combining in the correct polarity to achieve modulation signal values.

[0056] For full flexibility, selective combining of accumulated values can be performed on digital accumulated values, after digitizing the analog accumulated values. The option of reconstructing the modulation signal value before digitization, by selectively combining the analog accumulated values, has already been described. Alternately, under some signal conditions, some portions of this selective combining might be performed before the A to D, with others left until after the conversion to digital. In some cases, this can be done by merely reconnecting using switched-capacitor techniques, the capacitors of Figure 4, during different phase sectors of the four phase sector clock. This combines multiple phase sector accumulated values before the A to D conversion.

[0057] One novel and advantageous case of this, an alternate value combining system, is to again selectively combine the four phase sector correlated analog accumulated values, but now to obtain two analog accumulated values to be A to D converted for each local clock cycle, the charge values Q1 = Qb - Qd, and Q2 = Qa - Qc. This is particularly advantageous if frequency content slower than the desired signal were present as a large interfering signal. In this way the large interfering signal can be canceled, before it uses up range of the A to D converter 16. This is most directly accomplished using switched-capacitor type techniques, by reconnecting the integrating capacitors of Figure 4, or perhaps by connecting the two non adjacent phase sectors to be combined, both to the charge responding A to D simultaneously. This option reduces the A to D conversion rate to two values per cycle, while also maintaining the benefits of post conversion mixing for the I and Q

reconstructed modulation signals. This is another alternate enhancement of the current invention and is achieved by arranging clocking and switching of the capacitors of Figure 4 so that two of the charging phases are combined and only two complete charge integrations are accomplished per full cycle of the clock, with each being a combination of two non-adjacent quadrature phase sectors of the full cycle clock. The I and Q signals can then be post conversion mixed using the digital modulation signal values obtained from performing the A to D conversion on Q1 and Q2, and where now Qip = Q1 + Q2 = Qa + Qb – Qc – Qd, and Qq = Q1 – Q2 = Qb + Qc – Qa – Qd.

[0058] This alternate combining system is one of several ways the RF2D 4 can be setup to accumulate and operate on the modulated signal, the accumulated values, and the modulation signal values. Different setups are likely to yield better signal to noise ratio than others, depending on signal conditions. These signal conditions can include a large set a variables, strong or weak signal, whether or not there is a strong interfering signal nearby in frequency or physically near the receiver so that it is overwhelming the desired signal, or whether or not there is rapidly changing fading conditions, just to name a few. The program running in the DSP 10 can adjust the selection of setups, to get the best signal to noise ratio, under current signal conditions.

[0059] As previously mentioned, it is intended here that there be no time during which more than one of the four switches SWa, SWb, SWc, SWd are simultaneously on. Given the imperfections of real timing and variations, it is difficult to avoid any simultaneous on time, without also providing for a period of time, however short, when all of the switches SWa, SWb, SWc, SWd are intentionally off. This would of course create a period of time, however short, where the input signal is ignored. This can lead directly to aliasing. One way of overcoming this is to make use of parasitic capacitance at the inverting input 30 of the op-amp 24. During any period where all of the switches are off, a transitory period, the parasitic capacitance at the inverting input of the op-amp 24, representing an auxiliary capacitive device, will

begin to accumulate charge, and allow the voltage at the inverting input 30 to rise slightly. The charging of this auxiliary capacitive device continues until the next phase sector begins. As long as the next phase sector switch SWa, SWb, SWc, SWd turns on before this voltage rises too far, the voltage would be pulled right back to within its proper operating range as soon as the next switch turns on, while the charge that was accumulated by the parasitic capacitor at the inverting input would be redistributed exactly, onto the integrating capacitor Ca, Cb, Cc, Cd whose switch SWa, SWb, SWc, SWd is now on. In this way, after the switching transients have settled, the now on capacitor Ca, Cb, Cc, Cd would hold the same charge as if its switch SWa, SWb, SWc, SWd had been turned on fully at exactly the instant the previous switch SWa, SWb, SWc, SWd had been turned fully off.

[0060] Operating a Phase Sector Integration Capturing system in this way, assuring that there is no period of time during which the input signal is ignored by subsequent processing, is an advantage referred to as Continuous Signal Capturing. One major reason why this is so advantageous is that this completely avoids any need for anti-aliasing filters, and avoids the complexities of managing adjustable anti-aliasing filters otherwise required for a fully flexible receiver. Continuous Signal Capturing is achieved by performing continuous accumulation on the input signal. Whenever the input signal is no longer accumulated on the most recently charging integration capacitor Ca, Cb, Cc, Cd , it is now effectively becomes accumulated on the subsequent phase sector's capacitor Ca, Cb, Cc, Cd. Using another circuit architecture might require using one or more capacitive devices devoted to this auxiliary capacitive device's purpose, but with the Phase Sector Distributed Integrator circuit configuration, this parasitic input capacitance at the non-inverting input 26 of the op-amp 24 accomplishes this added feature, without the addition of a device devoted to this purpose. There are also other ways of accomplishing continuous signal capturing, though they are more complex in nature. This however, does not detract from the novelty of this entire methodology.

[0061] Another valuable enhancement to Phase Sector Integration Capturing, novel to Phase Sector Integration Capturing, is the fact that by selecting to accumulate the modulated signal input over multiple cycles of the local clock, a Phase Sector Distributed Integrator block can accumulate phase sector correlated values for phase sectors, A, B, C, and D, which represent low pass filtered, or decimation filtered accumulated values. In this way, the charge stored on capacitor Ca gets added to, by additional charge during a second phase A of a subsequent full cycle, and by each phase A of multiple subsequent full cycles. The charge already on capacitor Cb gets added to by a second and multiple subsequent phase B portions of second or multiple full cycles of the set of four switches. Capacitors Cc and Cd also, can thereby integrate charge over multiple full cycles of the set of four switches SWa, SWb, SWc, SWd. Charges accumulated in this way are still phase sector correlated, with each capacitor Ca, Cb, Cc, Cd accumulating charge only during its active phase sector of each local clock cycle. This is similar to the low pass filter used in conjunction with the impulse sampling method previously described, the simplest of which just adds up the input samples. However, with this integrating block, there is no additional circuitry required, and no additional components being clocked at the fastest clock rate, effectively 4 times the local clock rate. The same integrating capacitors Ca, Cb, Cc, Cd just continue to add up the charge over multiple local clock cycles. Just as with the impulse sampled input, the signal adds up over multiple local clock cycles, and the resulting integrated charge can be made available to a subsequent A to D converter 16 at a much slower, down-converted rate. There is also the same improvement in signal to noise ratio resulting from the averaging of the phase sector correlated charge components over time, as they are integrated onto each of their respective capacitors Ca, Cb, Cc, Cd, linearly compounding the amount of charge that is in response to the signal, while adding only stochastically, the amount of charge that is present on the each capacitor Ca, Cb, Cc, Cd due to noise.

[0062] While band narrowing does occur as a result of integrating the input signal over multiple full cycles of A, B, C, and D phases, this band narrowing is a function of the down-conversion factor, which is just Fclk/f_RF2Dout, and which is under the control of the DSP 10. As before, this down-conversion factor can be chosen so as to not narrow the band of the information contained in the modulated signal, or it can be chosen to narrow the band, if so desired.

[0063] Subsequently, both I and Q are first formed after digitization has occurred using a single A to D block 16. I and Q are formed in the DSP 10 by combining, in the right polarity, the values collected during each of the quadrature phase sectors. This again constitutes Post Conversion Mixing with all of the same advantages as previously described, all profound in several ways. The mixing and filtering to provide the control voltage for the voltage controlled oscillator portion of the PLL is also the same as previously described.

[0064] Various methods of reconstructing a modulation signal have been discussed here. Each of the methods discussed has some combination of RF environment or receiving conditions under which it might represent the best method of signal reception. This PSB-SDR system is capable of switching between all of these methods as signals are being received. This switching can be done in some cases by changing the signals clocking various switched-capacitor circuits, in some cases by switching different components in or out of the circuits, and in many cases by merely altering the program steps that are being applied to the digitized signals as they propagate through the DSP block. These choices can all be made under program control, by any programmable control unit, which most typically is just the DSP block. This can be done in response to a modulation signal evaluator, which is most likely constituted by lines of code in the program running on the DSP, but might also be implemented in some cases, by dedicated hardware circuitry. In either case, this modulation signal evaluator can evaluate the reconstructed modulation signal relative to any number of characterization metrics, many determined by mere mathematical processing of the reconstructed modulation signal, which could be

done by any processing system, but generally for this PSB-SDR system, the processing system is the DSP block.

[0065] Everything described to this point has mostly been describing the various features of this PSB-SDR system 2 as applied to achieve a receiver, receiving a modulated signal. The transmitter portion of a radio system can also be greatly enhanced by all of the previously described techniques. A number of conventional transmitter methods and techniques can be applied to this system, while managed from the DSP block 10 of this PSB-SDR 2. This system provides for a relatively wide-band, and thereby a relatively fast, acquisition of reconstructed I and Q modulation signal values from a modulated signal. This enables the use of a closed loop feedback system, which is amply stable, incorporating the transmitter block in the loop. For transmit mode, a transmit/receive mode control, generally a control signal or control bit from the DSP block 10, switches the modulated signal input to the PSCC block 14 from a received signal over to an attenuated version of the transmitter's output. The PSCC block 14 then provides reasonably quick feedback to the DSP block 10, so that it can compare the actual transmit signal to a desired transmit signal and make calculated adjustments to the signals driving the transmit block 32, as necessary to achieve the desired transmit signal at the output of the transmitter 32. In this way, the output of the transmitter 32 is in effect regulated to match the desired signal, so that the desired transmit signal is achieved at the output of the transmitter 32, greatly mitigating non-linearities, and thermal non-idealities, of the transmit block 32. Conventional systems have not been able to take this approach, because conventional systems have much too much delay in any signal path which reconstructs a modulation signal or component from a modulated signal by conventional means.

[0066] The digital transmission values that are output from the DSP 10 are converted to analog values by the RF DAC 34. This DAC 34 also includes a fast Phase Sector Distributed Output block, which steps through various analog phase sector correlated output values, providing each value in the form of either a current

or a voltage proportional to this phase sector correlated output value to the transmitter 32 for transmission. The values that are distributed for each phase sector are generally updated much more slowly, by a digital to analog conversion of the data provided by the DSP 10. Because of this arrangement, the data update rate out of the DSP 10 does not have a full RF transmission rate, but can have an update rate more on the order of the bandwidth of the resulting RF transmission, rather than up at the carrier frequency.

[0067] This PSB-SDR system 2 provides for a zero IF, direct RF down-conversion technique, which converts as directly as possible, an RF band-constrained signal located at a center frequency, to a clocked parallel data stream. The center frequency at which RF information is down-converted from is determined by the frequency of the local clock, Fclk. This local clock is developed by the local clock generation block 12, under the control of the DSP 10. A down-conversion factor is given by the ratio of the local clock to the frequency of the complete cycle output rate of the A to D conversion block 16, or Fclk/f_RF2Dout. This ratio is an integer ratio, also controlled by the DSP block 10. One block within the PSB-SDR 2, the RF2D 14, essentially performs an RF to digital conversion. The output of this block 4 is a stream of multiple bit wide data, provided to the DSP block 10. The PSB-SDR 2 incorporates a transmitter 32, also controlled by the DSP 10, with a reconstructed modulation signal generated by the RF2D block 4 from the output of the transmitter fed back to the DSP 10, allowing the DSP 10 to maintain closed loop control of the transmitted output signal. This system is capable of receiving and transmitting in accordance with any transmission or wireless standard, requiring only programming to do so, and is limited in RF application only by the operational bandwidth limitations imposed by the semiconductor process into which it is fabricated.

[0068] Figures 5a-13 are flow charts representing steps of various embodiments of aspects of the present invention. Although the steps represented in these Figures are presented in a specific order, the technology presented herein can be performed in any variation of this order. Furthermore, additional steps may be executed

between the steps illustrated in these Figures. Although many of the following described enhancements are equally applicable to PSIS and PSIC, for simplicity the descriptions will use only the “accumulated value” terminology of PSIC. The PSIS terminology “sampled value” may be directly substituted for “accumulated value” in those descriptions to apply them to the PSIS approach.

[0069] Figures 5a-b are a flow chart representing steps of one embodiment method for extracting values representative of modulation signal components from a modulated signal. A local clock signal is developed 50, which correlates in time to the modulated signal and has a plurality of non-overlapping phase sectors per cycle.

[0070] The modulated signal is accumulated 52 into an accumulated value, separately for at least one phase sector of one cycle of the local clock signal. In one embodiment, the modulated signal is accumulated by analog means and the accumulated values are analog accumulated values. Each accumulated value is representative of a modulation signal component. The modulated signal accumulated is of an amount representative of the mathematical integral of the modulated signal during each phase sector of the local clock over which the modulated signal is accumulated.

[0071] In one embodiment, each accumulated value represents the amount accumulated over one phase sector. In an alternative embodiment, at least one accumulated value includes amounts accumulated in either polarity, selectively, over multiple phase sectors of one cycle of the local clock.

[0072] Figure 6 illustrates one embodiment for accumulating the modulated signal into an accumulated value. A capacitive device is charged 80 with the modulated signal such that the accumulated charge on the capacitive device is the accumulated value. The charging process 80 is repeated 82 for as many clock cycles and phase sectors as desired. The accumulated value is then transferred 84 to an analog to digital converter and the capacitive device is reinitialized 86.

[0073] Returning to Figures 5a-b, the accumulating step is repeated 54 during multiple cycles of the local clock. In one embodiment, at least one accumulated

value includes amounts accumulated during multiple cycles of the local clock. In one embodiment, the accumulated values include amounts accumulated during the same phase sector of multiple cycles of the local clock.

[0074] In one embodiment, accumulating the modulated signal into an accumulated value includes a switched capacitor filter accumulating the modulated signal over multiple clock cycles. In one embodiment, the switched capacitor filter is a low pass filter.

[0075] In one embodiment, the accumulated values are selectively combined 58, 64 to obtain at least one modulation signal value representative of the modulation signal. Selectively combining 58, 64 the accumulated values includes selecting whether to combine any accumulated values, which accumulated values to combine, and whether to add or subtract the accumulated values. In one embodiment, analog accumulated values are selectively combined 58 to obtain analog modulation signal values representative of the modulation signal and the analog modulation signal values are digitized 60 to obtain digital modulation signal values representative of the modulation signal.

[0076] In an alternative embodiment, analog accumulated values are digitized 62 to obtain digitized accumulated values and the digitized accumulated values are selectively combined 64 to obtain digital modulation signal values representative of the modulation signal.

[0077] The accumulating and combining steps are repeated 66 over multiple cycles of the local clock signal. In one embodiment, the resulting modulation signal values are selectively combined 68 to reconstruct the modulation signal. Selectively combining 68 the modulation signal values includes selecting whether to combine any modulation signal values, which modulation signal values to combine, and whether to add or subtract the modulation signal values.

[0078] In one embodiment, signal conditions of the reconstructed modulation signal are evaluated 70. The manner of selectively combining 68 the resulting

modulation signal values is altered 72, as necessary or desirable, based on the signal conditions.

[0079] In one embodiment, the accumulated values are evaluated 74 and the manner of selectively combining 58, 64 the accumulated values is altered 76 based on the evaluation 74. In one embodiment, the accumulated values are selectively combined 58, 64 as directed by an instruction from a programmable control unit, of which the digital signal processor 10 is one example.

[0080] In another embodiment, the manner of developing 50 the local clock signal is altered 78 based on the evaluation 74. Altering 78 the manner of developing the local clock signal includes selectively altering the number of phase sectors per cycle, frequency, and phase of the local clock signal.

[0081] Figure 7 illustrates one embodiment where the modulation signal includes in-phase and quadrature signals and the accumulated values form in-phase and quadrature signal components or are combined to form in-phase and quadrature signal components. There are four phase sectors per cycle.

[0082] The modulated signal is accumulated 88, 90, 92, 94 separately during each phase sector of one cycle of the local clock signal, into first, second, third, and fourth accumulated values. The first, second, third, and fourth values are selectively combined 96 to obtain an in-phase value representative of the in-phase signal. The first, second, third, and fourth values are also selectively combined 98 to obtain a quadrature value representative of the quadrature signal.

[0083] Figure 8 shows an alternative embodiment for obtaining the in-phase and quadrature values. The first and third values are combined 100 and the second and fourth values are combined 102. In one embodiment, combining 100 the first and third values includes during the first and third phase sectors of the local clock signal charging a first capacitive device with the modulated signal and combining 102 the second and fourth values includes during the second and fourth phase sectors of the local clock signal charging a second capacitive device with the modulated signal.

[0084] The combined first and third values are digitized 104 and the combined second and fourth values are digitized 106. The digitized combined second and fourth values are combined 108 with the digitized combined first and third values to obtain the in-phase values and the digitized combined second and fourth values are combined 110 with the digitized combined first and third values to obtain the quadrature values.

[0085] Figure 9 illustrates another embodiment for accumulating the modulated signal where there are four phase sectors per cycle. During the first phase sector of the local clock signal, a first capacitive device is charged 112 with the modulated signal. During the second phase sector of the local clock signal, a second capacitive device is charged 114 with the modulated signal. During the third phase sector of the local clock signal, a third capacitive device is charged 116 with the modulated signal. During the fourth phase sector of the local clock signal, a fourth capacitive device is charged 118 with the modulated signal.

[0086] In one embodiment, the modulated signal is continuously accumulated over a plurality of cycles of the local clock so that there are no intervals during the plurality of cycles wherein the modulated signal is not accumulated. Figure 10 illustrates one embodiment for continuously accumulating the modulated signal. For the first accumulated value, a first capacitive device is charged 120 with the modulated signal. An auxiliary capacitive device is charged 122 with the modulated signal during the transitory period between phase sectors. For the second accumulated value, a second capacitive device is charged 124 with the modulated signal. The accumulated charge on the auxiliary capacitive device is transferred 126 to the second capacitive device while the second capacitive device is charging 124.

[0087] The auxiliary capacitive device is charged 128 with the modulated signal during the transitory period between charging the second capacitive device and the third capacitive device. The third capacitive device is charged 130 with the modulated signal. The accumulated charge on the auxiliary capacitive device is

transferred 132 to the third capacitive device while the third capacitive device is charging 130.

[0088] The auxiliary capacitive device is charged 134 with the modulated signal during the transitory period between charging the third capacitive device and the fourth capacitive device. The fourth capacitive device is charged 136 with the modulated signal. The accumulated charge on the auxiliary capacitive device is transferred 138 to the fourth capacitive device while the fourth capacitive device is charging 138.

[0089] The auxiliary capacitive device is charged 140 with the modulated signal during the transitory period between charging the fourth capacitive device and the first capacitive device. The first capacitive device is charged 120 with the modulated signal. The accumulated charge on the auxiliary capacitive device is transferred 142 to the first capacitive device while the first capacitive device is charging 120. Although the preceding description refers to only one auxiliary capacitive device, multiple auxiliary capacitive devices may be used to accomplish this capture and transfer of charge accumulated between phase sectors.

[0090] Figure 11 illustrates an alternate embodiment for accumulating the modulated signal into an accumulated value. A first accumulation block is activated 144. When activated, the first accumulation block accumulates 146 the modulated signal into an accumulated value. While the first accumulation block is accumulating 146, an accumulated value is transferred 148 from a second accumulation block. The second accumulation block is activated 150. When activated, the second accumulation block accumulates 152 the modulated signal into an accumulated value. While the second accumulation block is accumulating 152, an accumulated value is transferred 154 from the first accumulation block.

[0091] Figure 12 illustrates one embodiment for the method of the present invention including a transmit mode. The present invention is useful in both a receive mode and a transmit mode and may be selectively switched 156 between the modes. In one embodiment, a single digital signal processing system selectively

switches 156 between the transmit and receive modes, supplying data to a transmitter to transmit, and obtaining data from a receiver.

[0092] In the receive mode, the modulated signal is a received 158 modulated signal. In the transmit mode, a transmit signal is generated 160 and the modulated signal is generated 162 by attenuating the transmit signal. In the transmit mode, a desired transmission modulation signal is compared 164 to a selectable combination of the accumulated values. The generation 160 of the transmit signal is regulated 164 with the comparison between the desired transmission modulation signal and the selectable combination of the accumulated values.

[0093] Figure 13 illustrates an alternate embodiment for altering the local clock signal. The accumulated values are selectively combined 166 to obtain at least one control signal value representative of a control signal. The accumulating and combining steps are repeated 168 over multiple cycles of the local clock signal. The resulting control signal values are selectively combined 170 to construct a control signal. Signal conditions of the control signal are evaluated 172. The manner of developing the local clock signal is altered 174 based on the signal conditions.

[0094] The methods and systems disclosed herein accomplish the highest goal of SDR, to provide hardware which provides fully flexible reception and transmission, in any programmable format, of any modulated signal, and without compromising performance.

[0095] The foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention embraces all such alternatives, modifications, and variances that fall within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method for extracting values representative of modulation signal components from a modulated signal, the modulated signal containing a modulation signal, the method comprising:

developing a local clock signal which correlates in time to the modulated signal and has a plurality of non-overlapping phase sectors per cycle;

acquiring at least one analog signal value from the modulated signal, separately for at least one phase sector of one cycle of the local clock signal; and

combining at least two analog signal values from the same clock cycle, but different phase sectors to obtain at least one analog combined signal value representative of a modulation signal component.

2. The method of claim 1 wherein:

acquiring at least one analog signal value includes sampling the modulated signal to acquire at least one analog sampled value and

combining at least two analog signal values from the same clock cycle, but different phase sectors to obtain at least one analog combined signal value representative of a modulation signal component includes combining at least two analog sampled values from the same clock cycle, but different phase sectors to obtain at least one analog combined sampled value representative of a modulation sampled component.

3. The method of claim 1 wherein at least one analog combined signal value includes amounts combined in either polarity, selectively, over multiple phase sectors of one cycle of the local clock.

4. The method of claim 1 further including:

repeating the acquiring and combining steps over multiple cycles of the local clock signal and

combining at least one analog combined signal value from at least two different cycles of the local clock, to obtain at least one filtered analog signal value representative of a modulation signal component.

5. The method of claim 4 wherein the number of the at least two different cycles of the local clock is variable to achieve an analog decimation filter having a variable decimation rate.

6. The method of claim 1 further including:

digitizing the analog combined signal values to obtain digitized combined signal values and

selectively combining the digitized combined signal values to obtain digital modulation signal values representative of the modulation signal.

7. The method of claim 1 wherein:

the modulation signal includes in-phase and quadrature signals;

the plurality of phase sectors per cycle is four phase sectors per cycle;

acquiring at least one analog signal value from the modulated signal includes acquiring first, second, third, and fourth analog signal values; and further including

selectively combining the first, second, third, and fourth analog signal values to obtain an in-phase value representative of the in-phase signal and selectively combining the first, second, third, and fourth analog signal values to obtain a quadrature value representative of the quadrature signal.

8. The method of claim 7 further including:

combining the first and third analog signal values;

combining the second and fourth analog signal values;

digitizing the combined first and third analog signal values;

digitizing the combined second and fourth analog signal values;

wherein combining the first, second, third, and fourth analog signal values to obtain the in-phase value includes combining the digitized combined second and fourth signal values with the digitized combined first and third signal values; and

wherein combining the first, second, third, and fourth analog signal values to obtain the quadrature value includes combining the digitized combined second and fourth signal values with the digitized combined first and third signal values.

9. The method of claim 8 wherein acquiring at least one analog signal value from the modulated signal includes:

during the first phase sector of the local clock signal, charging a first capacitive device with the modulated signal;

during the second phase sector of the local clock signal, charging a second capacitive device with the modulated signal;

during the third phase sector of the local clock signal, charging a third capacitive device with the modulated signal; and

during the fourth phase sector of the local clock signal, charging a fourth capacitive device with the modulated signal.

10. The method of claim 9 wherein:

combining the first and third analog signal values includes charging a first combining capacitive device with the charge from the first and third capacitive devices and

combining the second and fourth analog signal values includes charging a second combining capacitive device with the charge from the second and fourth capacitive devices.

11. A system for extracting values representative of modulation signal components from a modulated signal, the modulated signal containing a modulation signal, the system comprising:

a timing system configured to develop a local clock signal which correlates in time to the modulated signal, and has a plurality of non-overlapping phase sectors per cycle;

a phase sector correlated capturing block configured to acquire at least one analog signal value, separately for at least one phase sector of one cycle of the local clock signal; and

a signal value combining system configured to combine at least two analog signal values from the same clock cycle, but different phase sectors to obtain at least one analog combined signal value representative of a modulation signal component.

12. The system of claim 11 wherein:

acquiring at least one analog signal value includes sampling the modulated signal to acquire at least one sampled value and

combining at least two analog signal values from the same clock cycle, but different phase sectors to obtain at least one analog combined signal value representative of a modulation signal component includes combining at least two analog sampled values from the same clock cycle, but different phase sectors to obtain at least one analog combined sampled value representative of a modulation signal component.

13. The system of claim 11 wherein at least one analog signal value includes amounts acquired in either polarity, selectively, over multiple phase sectors of one cycle of the local clock.

14. The system of claim 11 wherein the phase sector correlated capturing block is further configured to repeat the sampling step over multiple cycles of the local clock and the signal value combining system is further configured to:

repeat the combining step over multiple cycles of the local clock signal and

combine at least one analog combined signal value from at least two different cycles of the local clock, to obtain at least one filtered analog signal value representative of a modulation signal component.

15. The system of claim 14 wherein the number of the at least two different cycles of the local clock is variable and wherein the signal combining system includes an analog decimation filter having a variable decimation rate.

16. The system of claim 11 wherein the signal value combining system includes:

an analog to digital converter configured to digitize the analog signal values to obtain digitized signal values and

a digital signal value combining system configured to selectively combine the digitized signal values to obtain digital modulation signal values representative of the modulation signal.

17. The system of claim 11 wherein:

the modulation signal includes in-phase and quadrature signals;

the plurality of phase sectors per cycle is four phase sectors per cycle;

acquiring at least one analog signal value from the modulated signal includes acquiring first, second, third, and fourth analog signal values; and

the signal value combining system is further configured to selectively combine the first, second, third, and fourth values to obtain an in-phase value representative of the in-phase signal and selectively combining the first, second, third, and fourth values to obtain a quadrature value representative of the quadrature signal.

18. The system of claim 17 wherein the signal value combining system includes:

an alternate value combining system configured to combine the first value with the third value and the second value with the fourth value;

an analog to digital converter system configured to digitize the combined first and third and combined second and fourth values; and

a processing system configured to combine the digitized combined first and third values with the digitized combined second and fourth values to obtain an in-phase value representative of the in-phase signal and to combine the digitized combined first and third values with the digitized combined second and fourth values to obtain a quadrature value representative of the quadrature signal.

19. The system of claim 18 wherein the alternate value combining system includes:

a first capacitive device configured to charge during the first and third phase sectors of the local clock signal and

a second capacitive device configured to charge during the second and fourth phase sectors of the local clock signal.

20. The system of claim 19 wherein the phase sector correlated capturing block includes:

a first capacitive device configured to charge during the first phase sector of the local clock signal,

a second capacitive device configured to charge during the second phase sector of the local clock signal,

a third capacitive device configured to charge during the third phase sector of the local clock signal, and

a fourth capacitive device configured to charge during the fourth phase sector of the local clock signal.

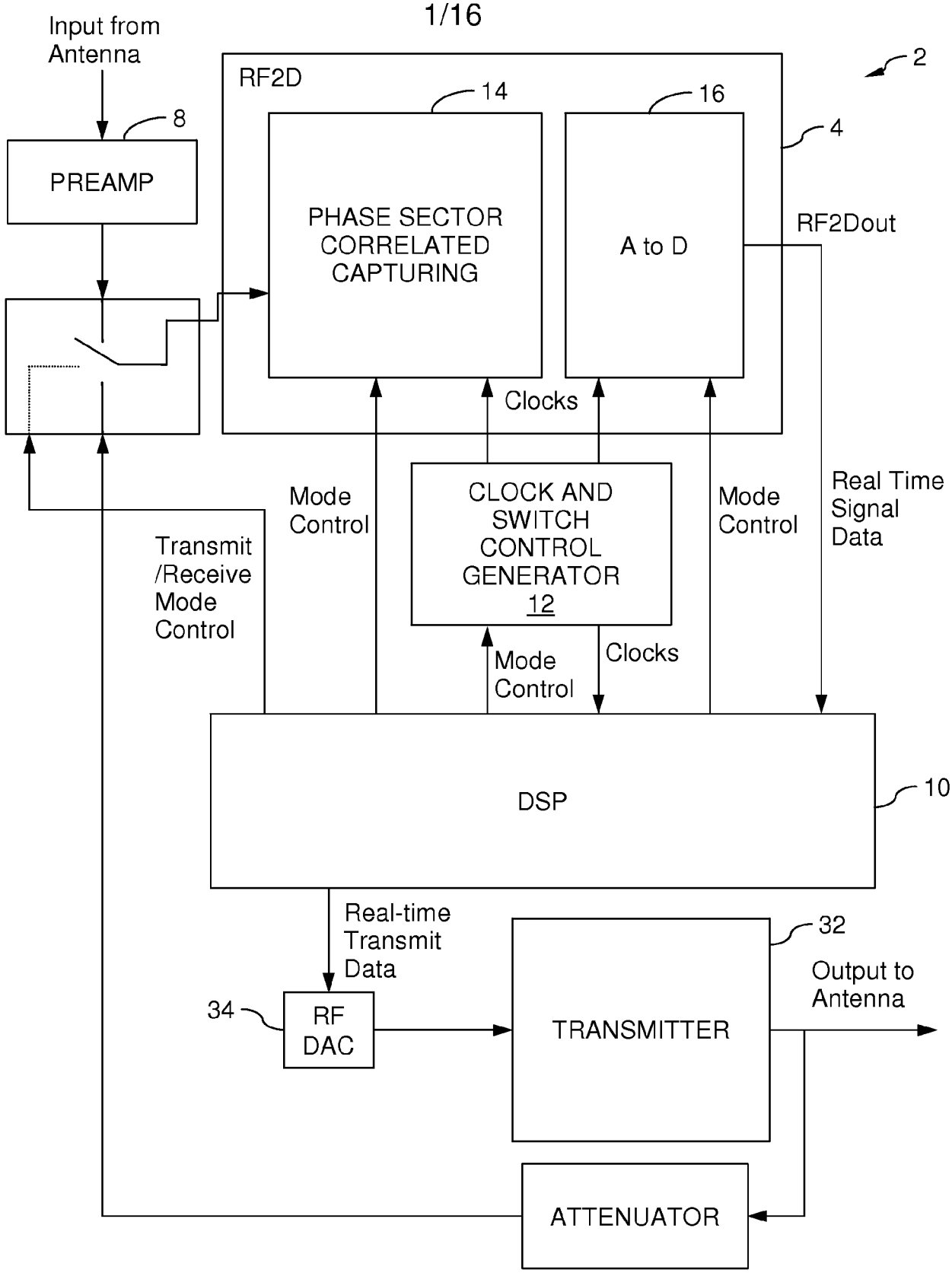
Input from Antenna
8
PREAMP
RF2D
14
16
2
4
PHASE SECTOR CORRELATED CAPTURING
A to D
RF2Dout
Clocks
Mode Control
CLOCK AND SWITCH CONTROL GENERATOR 12
Mode Control
Real Time Signal Data
Transmit /Receive Mode Control
Mode Control
Clocks
DSP
10
Real-time Transmit Data
32
Output to Antenna
34
RF DAC
TRANSMITTER
ATTENUATOR

Fig. 1

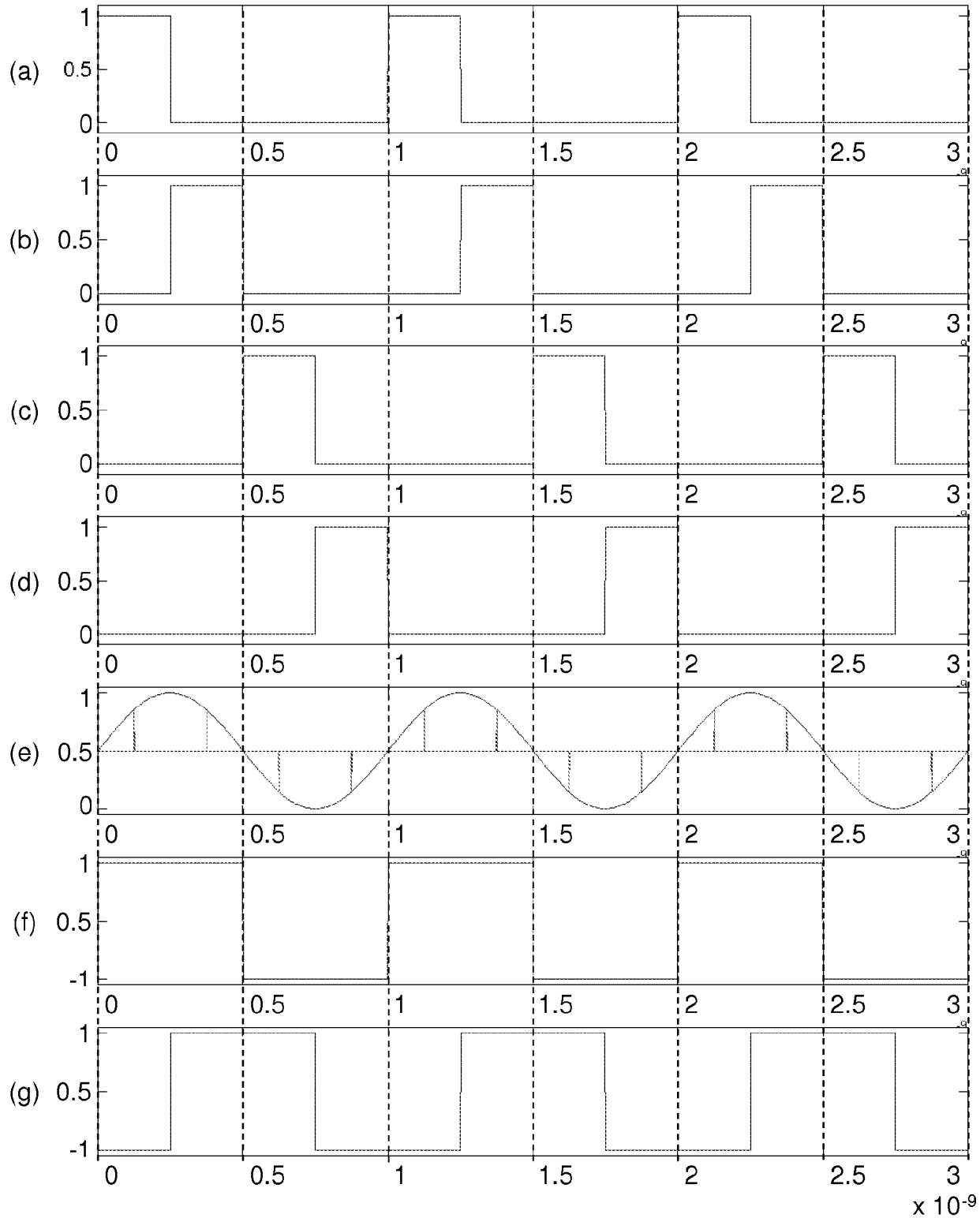

Fig. 2

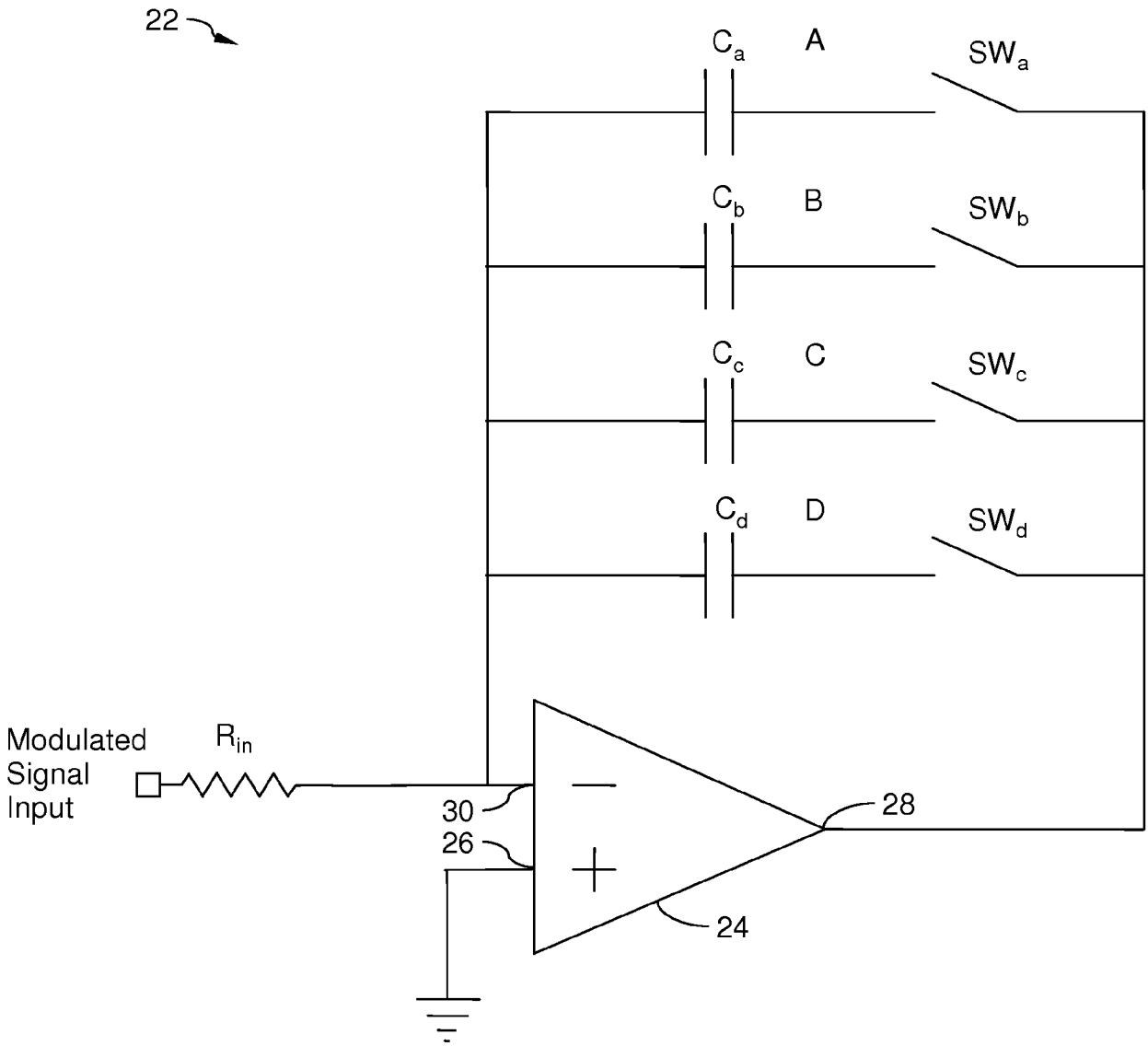
22
C_a
A
SW_a
C_b
B
SW_b
C_c
C
SW_c
C_d
D
SW_d
Modulated Signal Input
R_{in}
30
26
28
24

Fig. 3a

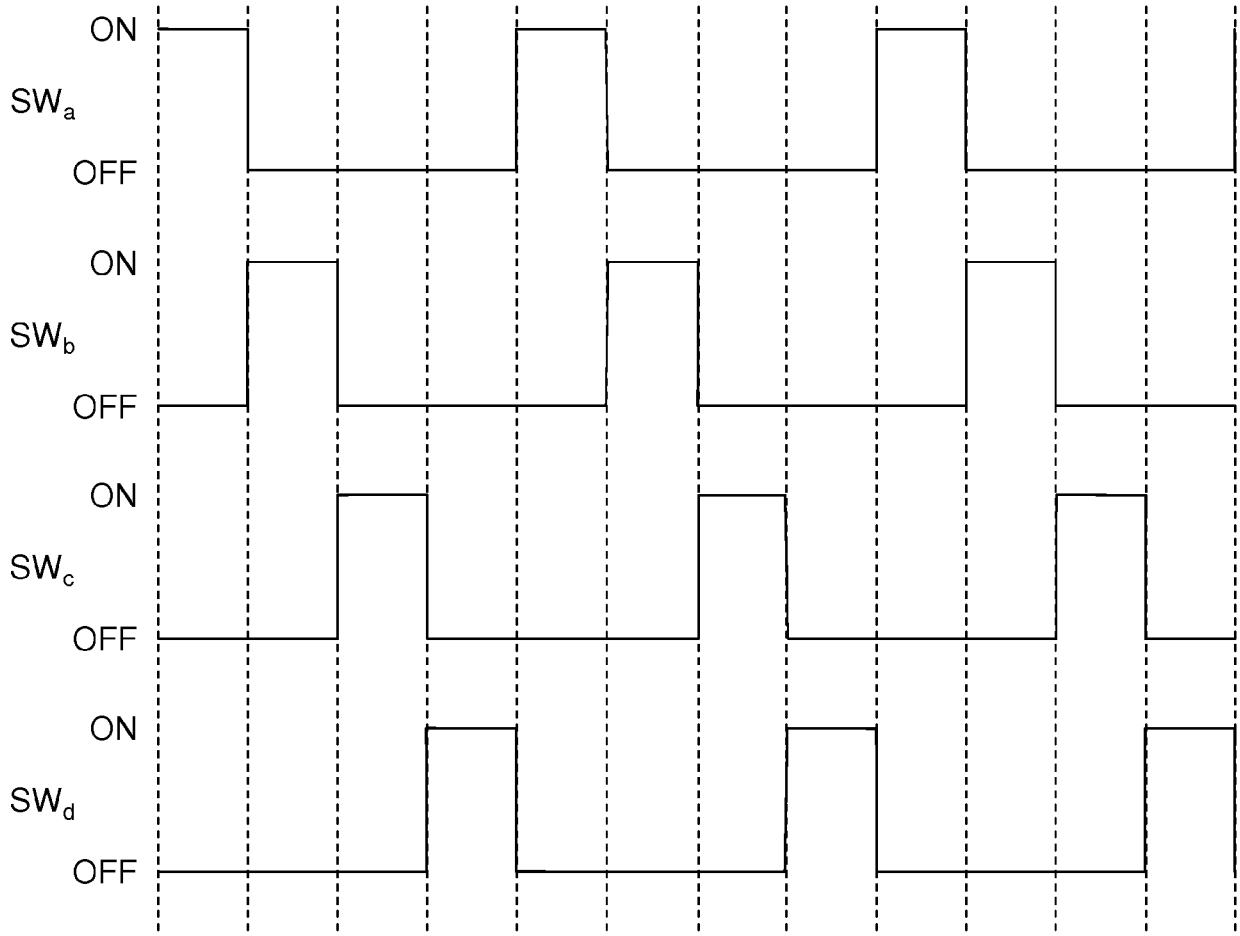

Fig. 3b

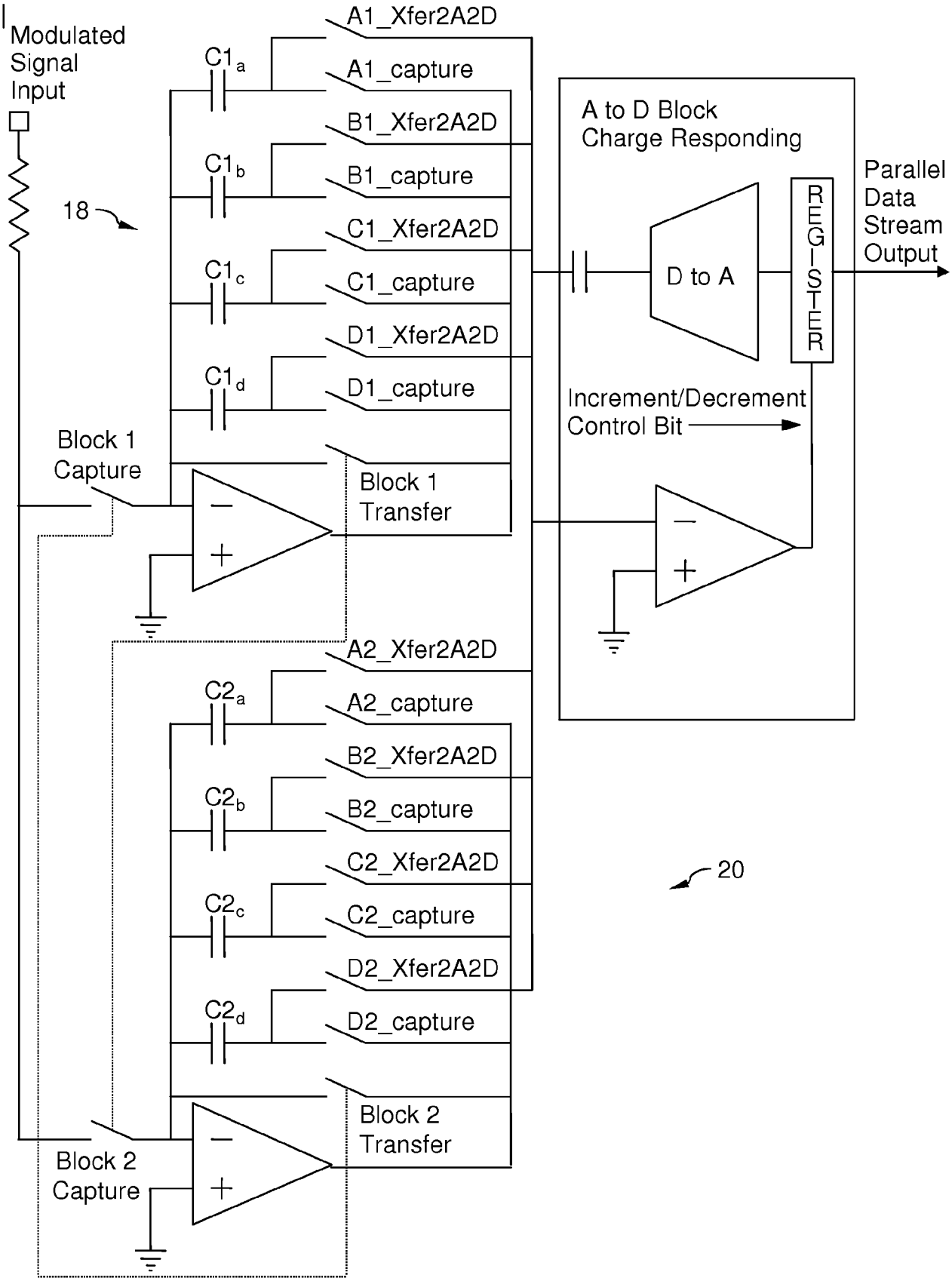
Modulated Signal Input
18
A1_Xfer2A2D
A1_capture
B1_Xfer2A2D
B1_capture
C1_Xfer2A2D
C1_capture
D1_Xfer2A2D
D1_capture
C1a
C1b
C1c
C1d
Block 1 Capture
Block 1 Transfer
A2_Xfer2A2D
A2_capture
B2_Xfer2A2D
B2_capture
C2_Xfer2A2D
C2_capture
D2_Xfer2A2D
D2_capture
C2a
C2b
C2c
C2d
Block 2 Capture
Block 2 Transfer
A to D Block Charge Responding
D to A
REGISTER
Parallel Data Stream Output
Increment/Decrement Control Bit
20

Fig. 4

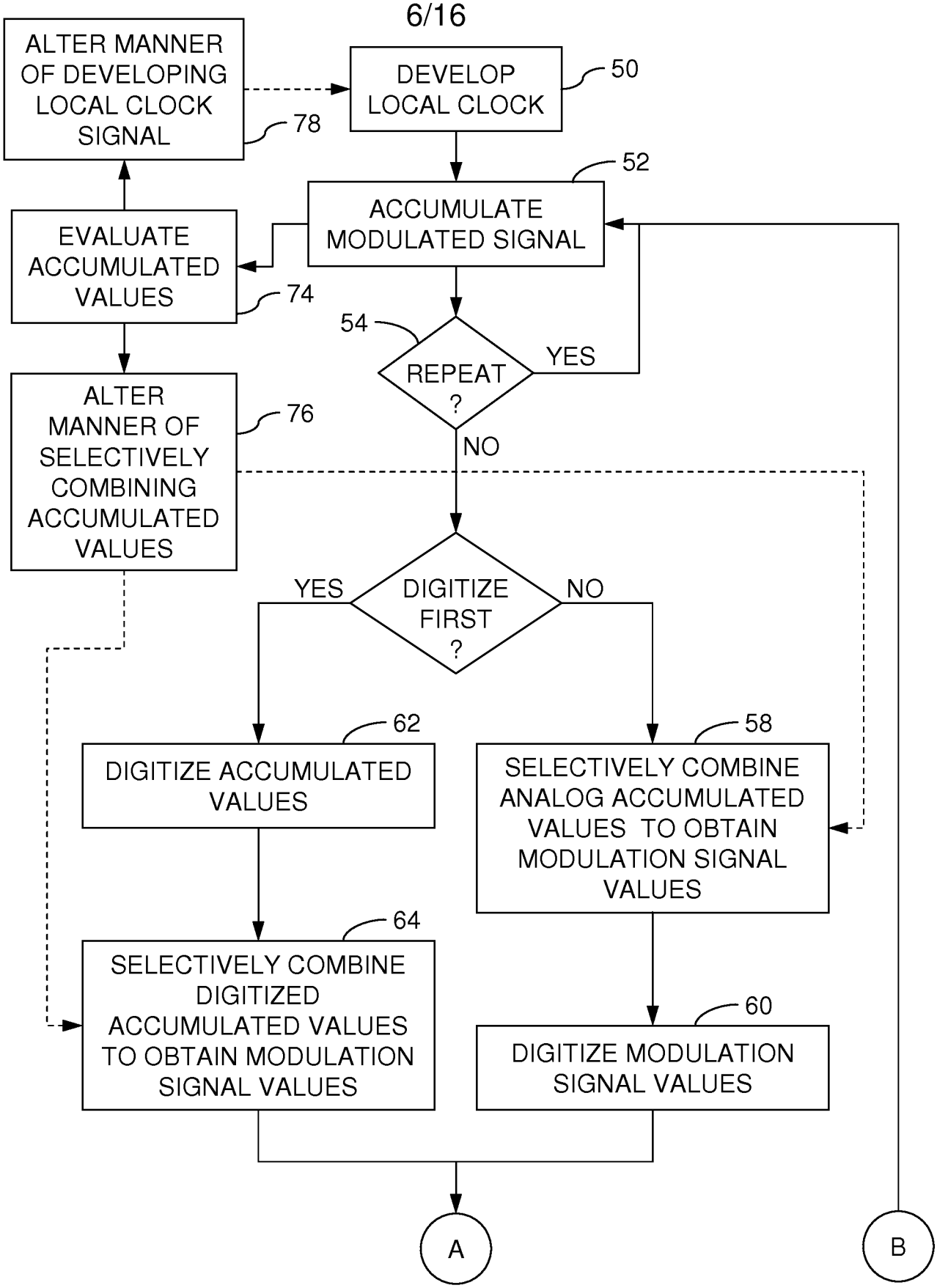
ALTER MANNER OF DEVELOPING LOCAL CLOCK SIGNAL
78
DEVELOP LOCAL CLOCK
50
52
ACCUMULATE MODULATED SIGNAL
EVALUATE ACCUMULATED VALUES
74
54
REPEAT ?
YES
NO
ALTER MANNER OF SELECTIVELY COMBINING ACCUMULATED VALUES
76
YES
DIGITIZE FIRST ?
NO
62
DIGITIZE ACCUMULATED VALUES
58
SELECTIVELY COMBINE ANALOG ACCUMULATED VALUES TO OBTAIN MODULATION SIGNAL VALUES
64
SELECTIVELY COMBINE DIGITIZED ACCUMULATED VALUES TO OBTAIN MODULATION SIGNAL VALUES
60
DIGITIZE MODULATION SIGNAL VALUES
A
B

Fig. 5a

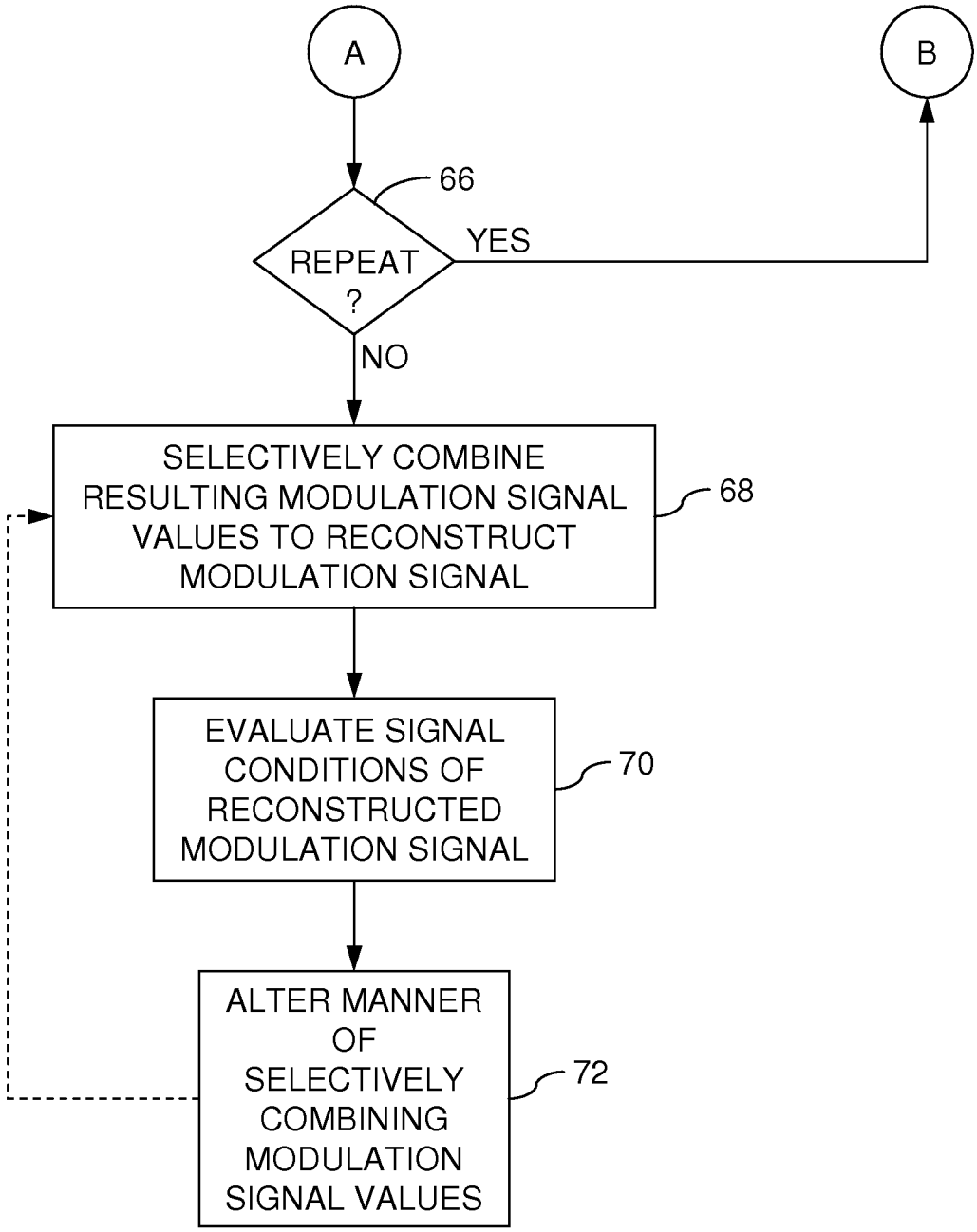
A
B
66
REPEAT ?
YES
NO
SELECTIVELY COMBINE RESULTING MODULATION SIGNAL VALUES TO RECONSTRUCT MODULATION SIGNAL
68
EVALUATE SIGNAL CONDITIONS OF RECONSTRUCTED MODULATION SIGNAL
70
ALTER MANNER OF SELECTIVELY COMBINING MODULATION SIGNAL VALUES
72

Fig. 5b

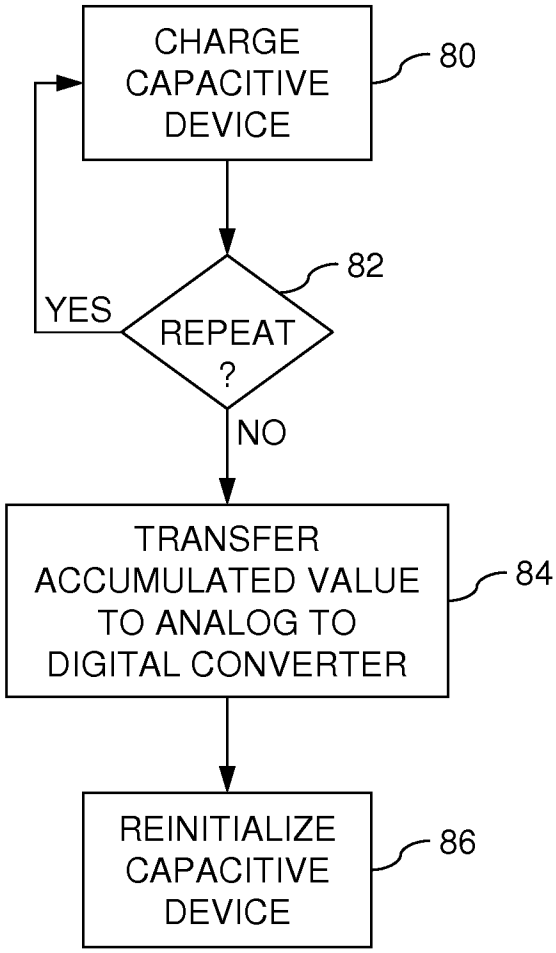
CHARGE CAPACITIVE DEVICE
80
82
YES
REPEAT ?
NO
TRANSFER ACCUMULATED VALUE TO ANALOG TO DIGITAL CONVERTER
84
REINITIALIZE CAPACITIVE DEVICE
86

Fig. 6

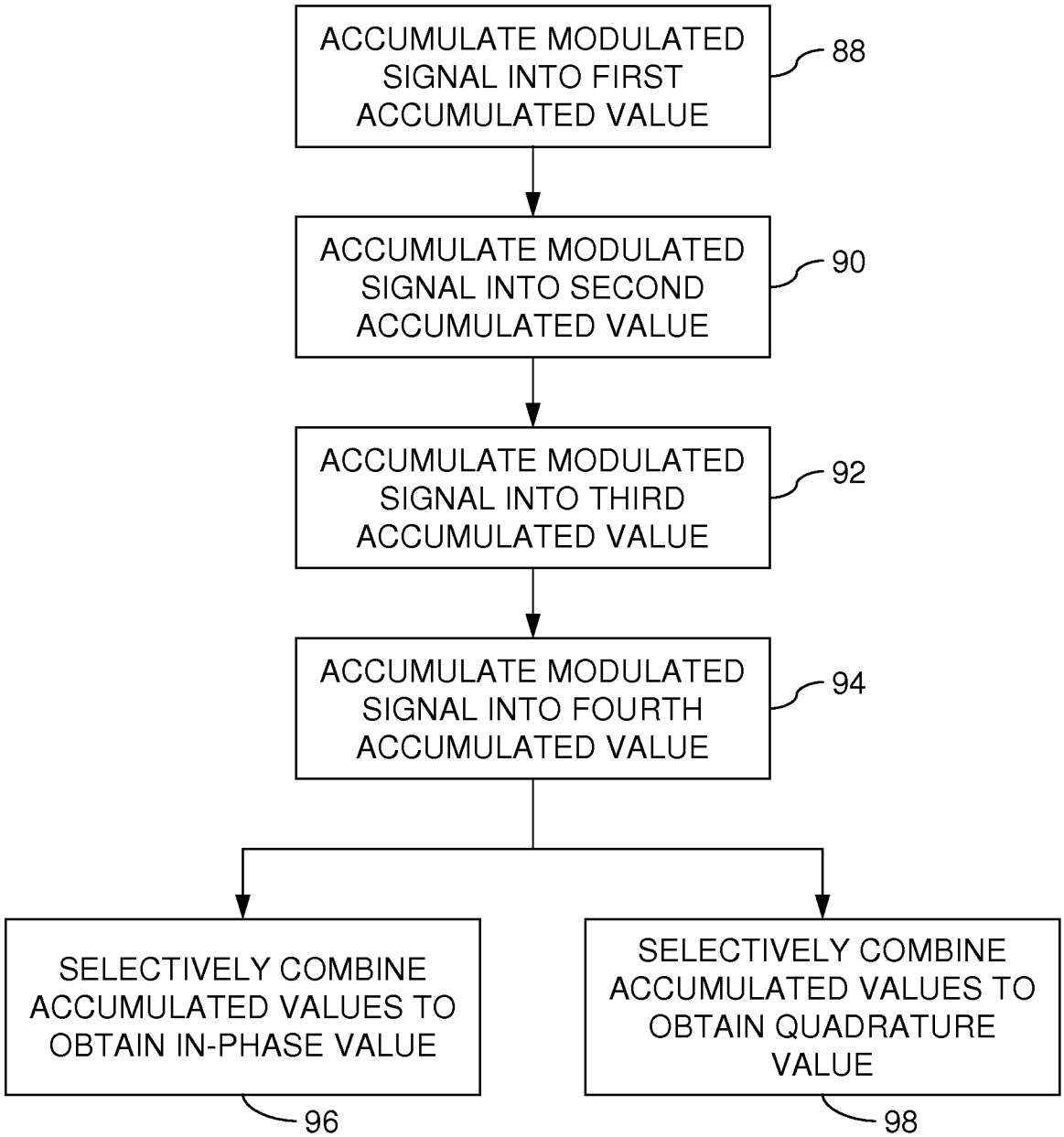
ACCUMULATE MODULATED SIGNAL INTO FIRST ACCUMULATED VALUE
88
ACCUMULATE MODULATED SIGNAL INTO SECOND ACCUMULATED VALUE
90
ACCUMULATE MODULATED SIGNAL INTO THIRD ACCUMULATED VALUE
92
ACCUMULATE MODULATED SIGNAL INTO FOURTH ACCUMULATED VALUE
94
SELECTIVELY COMBINE ACCUMULATED VALUES TO OBTAIN IN-PHASE VALUE
96
SELECTIVELY COMBINE ACCUMULATED VALUES TO OBTAIN QUADRATURE VALUE
98

Fig. 7

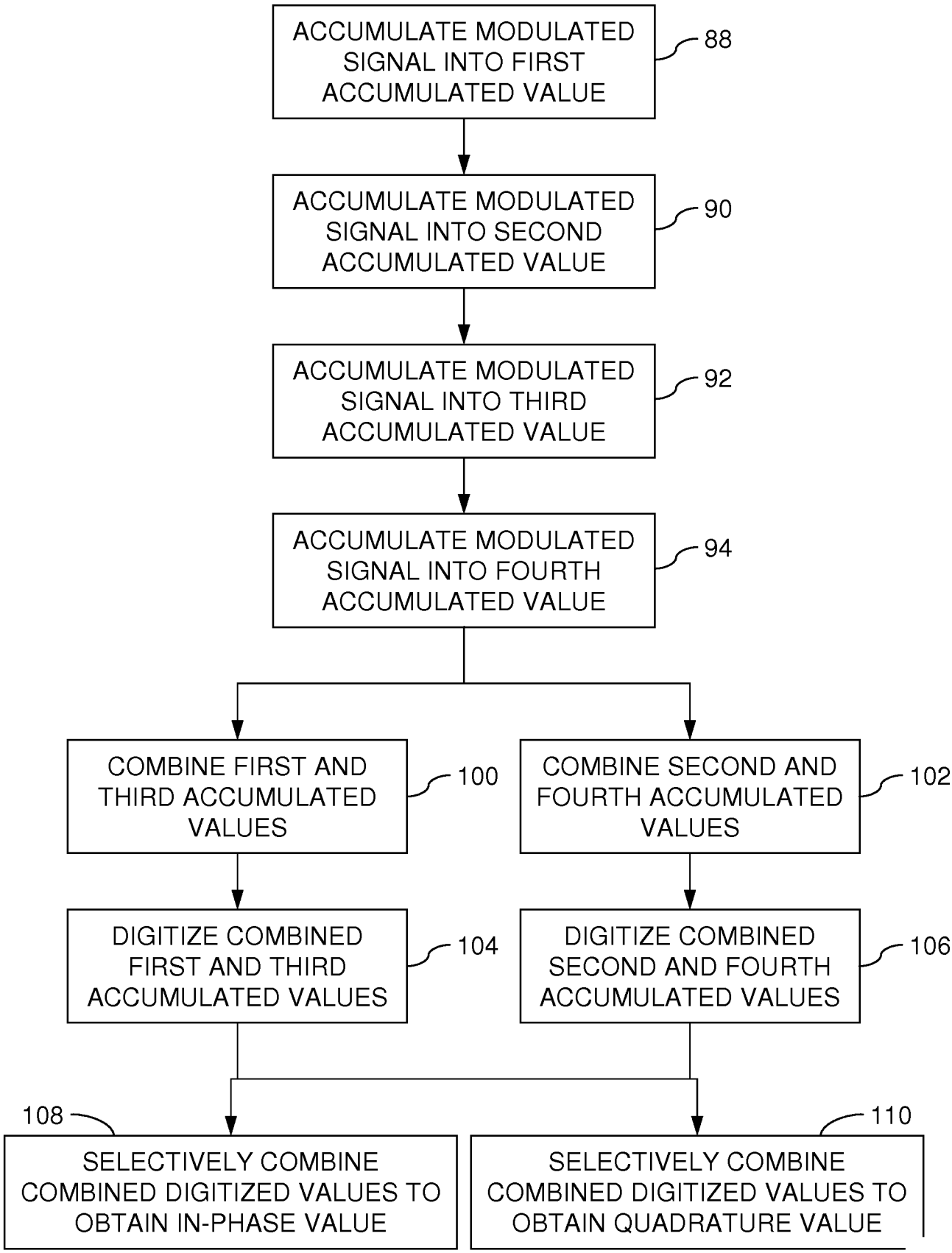
ACCUMULATE MODULATED SIGNAL INTO FIRST ACCUMULATED VALUE
88
ACCUMULATE MODULATED SIGNAL INTO SECOND ACCUMULATED VALUE
90
ACCUMULATE MODULATED SIGNAL INTO THIRD ACCUMULATED VALUE
92
ACCUMULATE MODULATED SIGNAL INTO FOURTH ACCUMULATED VALUE
94
COMBINE FIRST AND THIRD ACCUMULATED VALUES
100
COMBINE SECOND AND FOURTH ACCUMULATED VALUES
102
DIGITIZE COMBINED FIRST AND THIRD ACCUMULATED VALUES
104
DIGITIZE COMBINED SECOND AND FOURTH ACCUMULATED VALUES
106
108
SELECTIVELY COMBINE COMBINED DIGITIZED VALUES TO OBTAIN IN-PHASE VALUE
110
SELECTIVELY COMBINE COMBINED DIGITIZED VALUES TO OBTAIN QUADRATURE VALUE

Fig. 8

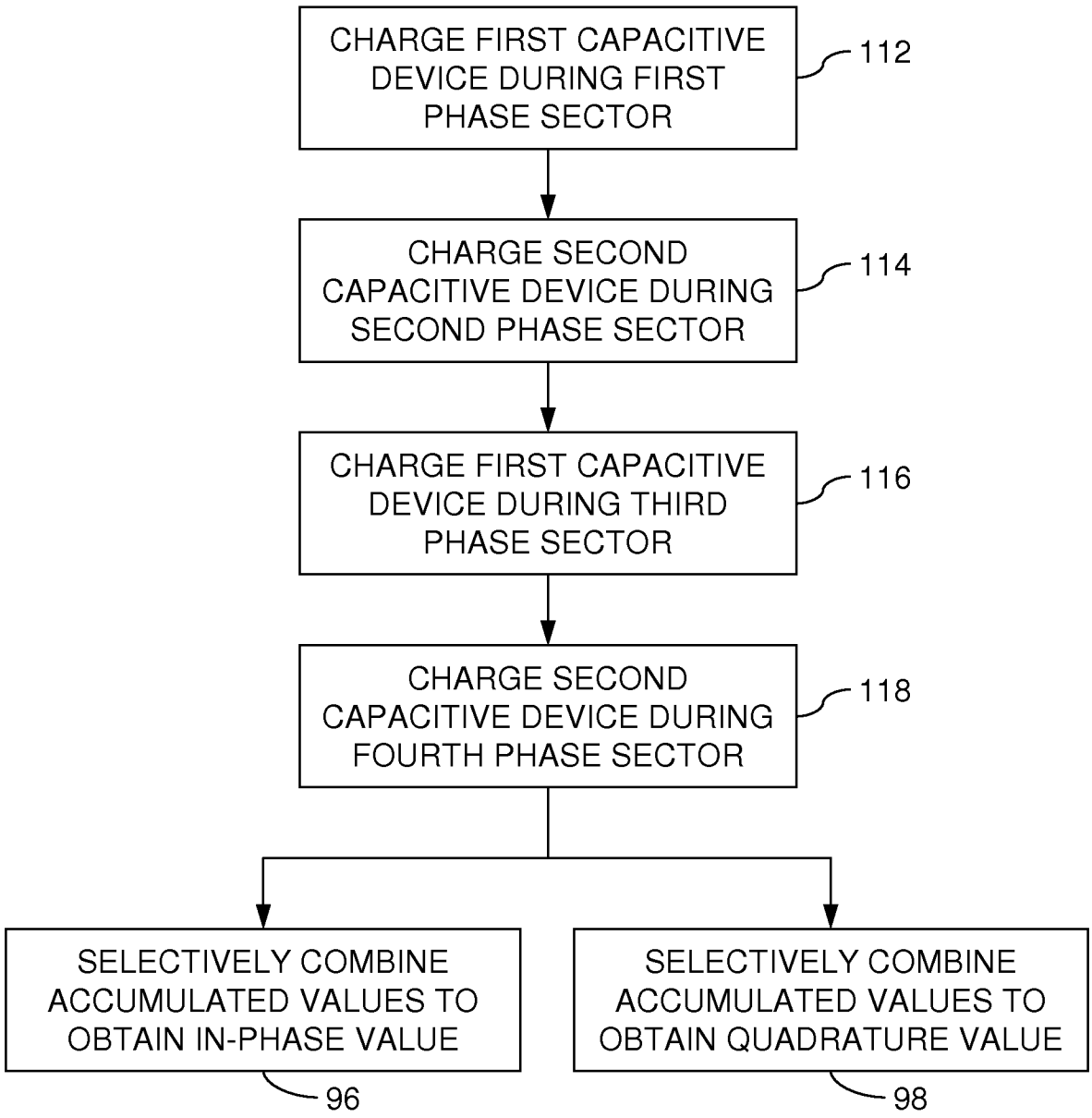
CHARGE FIRST CAPACITIVE DEVICE DURING FIRST PHASE SECTOR
112
CHARGE SECOND CAPACITIVE DEVICE DURING SECOND PHASE SECTOR
114
CHARGE FIRST CAPACITIVE DEVICE DURING THIRD PHASE SECTOR
116
CHARGE SECOND CAPACITIVE DEVICE DURING FOURTH PHASE SECTOR
118
SELECTIVELY COMBINE ACCUMULATED VALUES TO OBTAIN IN-PHASE VALUE
96
SELECTIVELY COMBINE ACCUMULATED VALUES TO OBTAIN QUADRATURE VALUE
98

Fig. 9

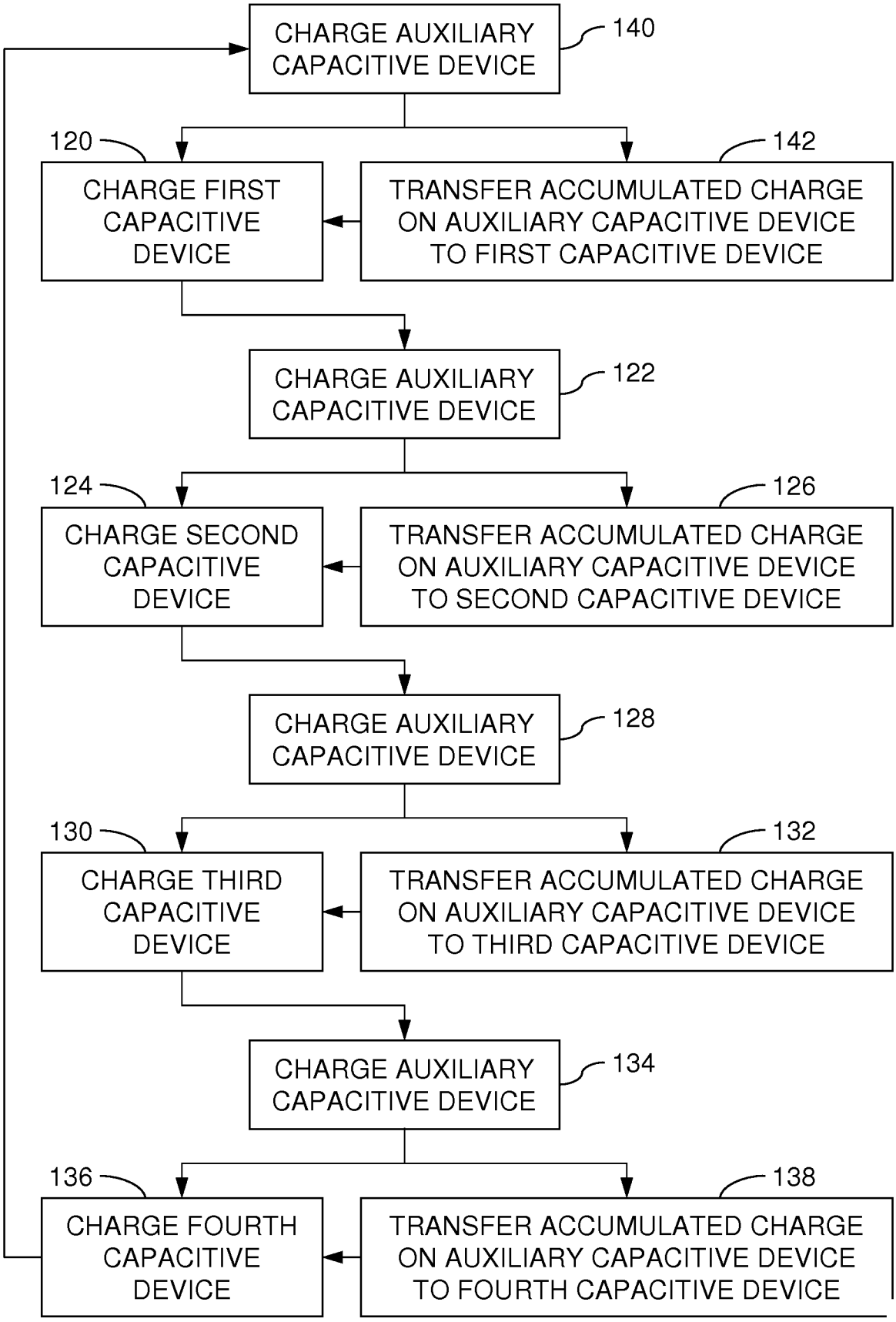
CHARGE AUXILIARY CAPACITIVE DEVICE
140
120
CHARGE FIRST CAPACITIVE DEVICE
142
TRANSFER ACCUMULATED CHARGE ON AUXILIARY CAPACITIVE DEVICE TO FIRST CAPACITIVE DEVICE
CHARGE AUXILIARY CAPACITIVE DEVICE
122
124
CHARGE SECOND CAPACITIVE DEVICE
126
TRANSFER ACCUMULATED CHARGE ON AUXILIARY CAPACITIVE DEVICE TO SECOND CAPACITIVE DEVICE
CHARGE AUXILIARY CAPACITIVE DEVICE
128
130
CHARGE THIRD CAPACITIVE DEVICE
132
TRANSFER ACCUMULATED CHARGE ON AUXILIARY CAPACITIVE DEVICE TO THIRD CAPACITIVE DEVICE
CHARGE AUXILIARY CAPACITIVE DEVICE
134
136
CHARGE FOURTH CAPACITIVE DEVICE
138
TRANSFER ACCUMULATED CHARGE ON AUXILIARY CAPACITIVE DEVICE TO FOURTH CAPACITIVE DEVICE

Fig. 10

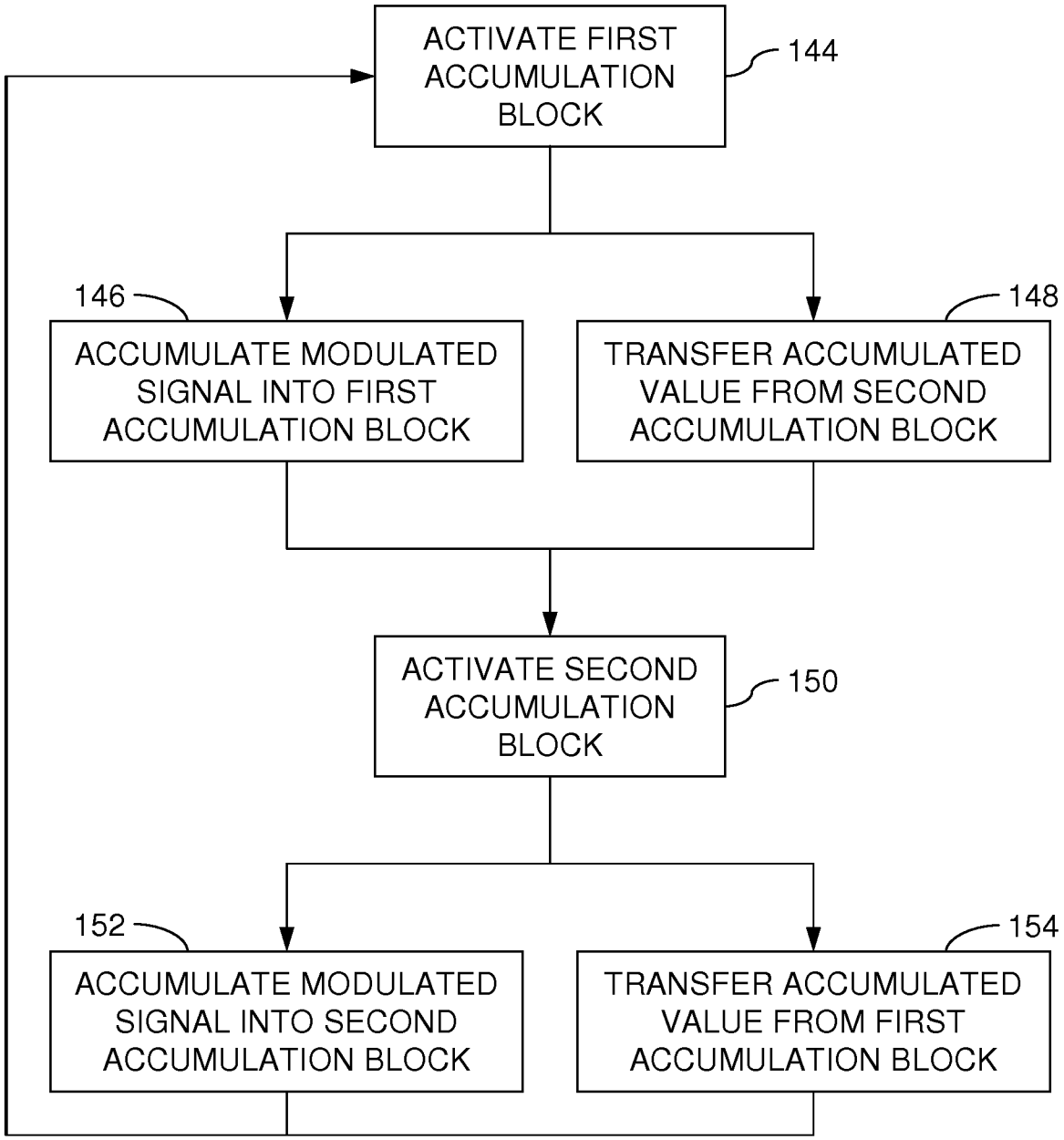
ACTIVATE FIRST ACCUMULATION BLOCK
144
146
ACCUMULATE MODULATED SIGNAL INTO FIRST ACCUMULATION BLOCK
148
TRANSFER ACCUMULATED VALUE FROM SECOND ACCUMULATION BLOCK
ACTIVATE SECOND ACCUMULATION BLOCK
150
152
ACCUMULATE MODULATED SIGNAL INTO SECOND ACCUMULATION BLOCK
154
TRANSFER ACCUMULATED VALUE FROM FIRST ACCUMULATION BLOCK

Fig. 11

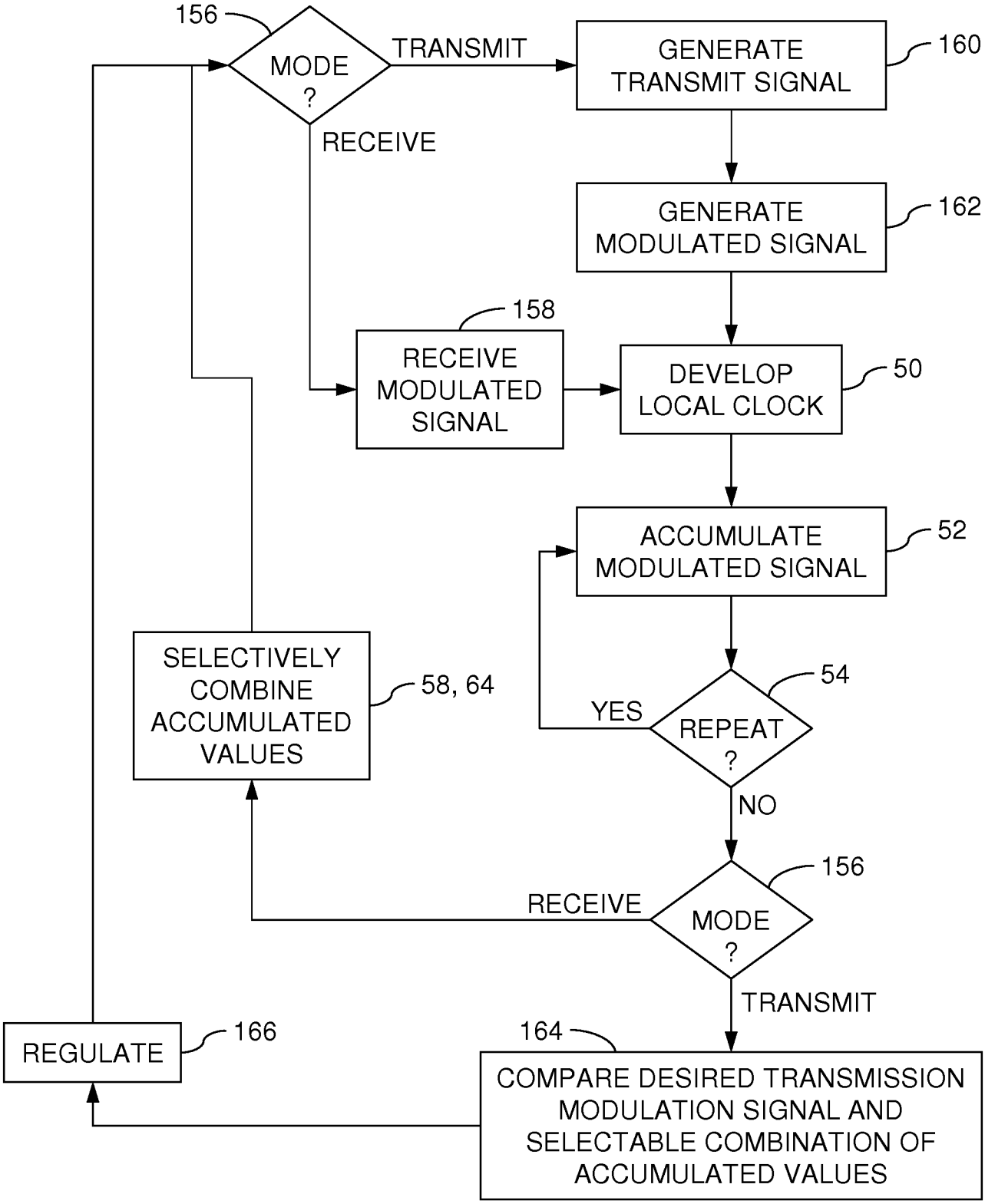
156
MODE ?
TRANSMIT
RECEIVE
GENERATE TRANSMIT SIGNAL
160
GENERATE MODULATED SIGNAL
162
158
RECEIVE MODULATED SIGNAL
DEVELOP LOCAL CLOCK
50
ACCUMULATE MODULATED SIGNAL
52
SELECTIVELY COMBINE ACCUMULATED VALUES
58, 64
YES
REPEAT ?
54
NO
156
RECEIVE
MODE ?
TRANSMIT
REGULATE
166
164
COMPARE DESIRED TRANSMISSION MODULATION SIGNAL AND SELECTABLE COMBINATION OF ACCUMULATED VALUES

Fig. 12

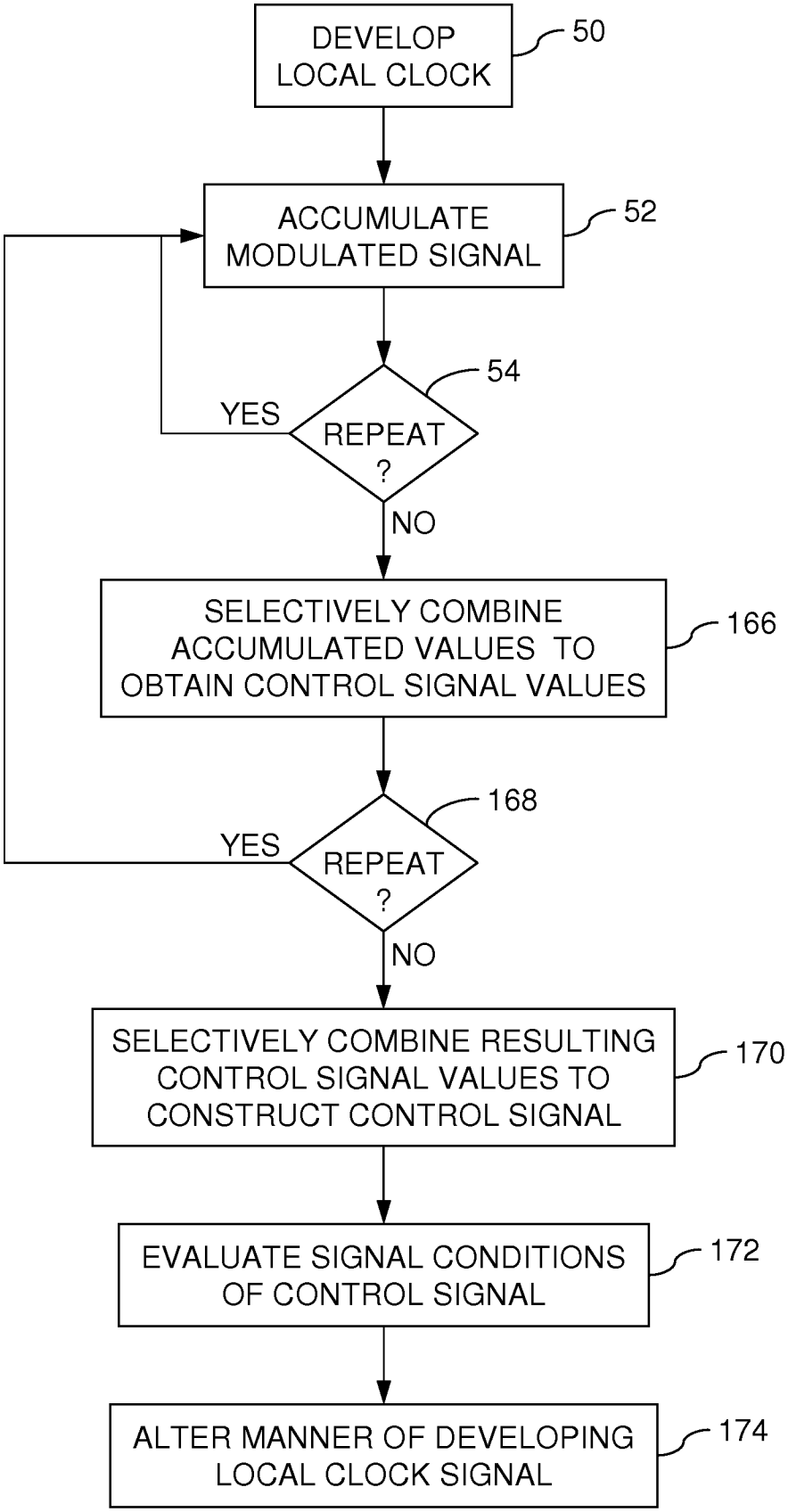
DEVELOP LOCAL CLOCK
50
ACCUMULATE MODULATED SIGNAL
52
54
YES
REPEAT ?
NO
SELECTIVELY COMBINE ACCUMULATED VALUES TO OBTAIN CONTROL SIGNAL VALUES
166
168
YES
REPEAT ?
NO
SELECTIVELY COMBINE RESULTING CONTROL SIGNAL VALUES TO CONSTRUCT CONTROL SIGNAL
170
EVALUATE SIGNAL CONDITIONS OF CONTROL SIGNAL
172
ALTER MANNER OF DEVELOPING LOCAL CLOCK SIGNAL
174

Fig. 13

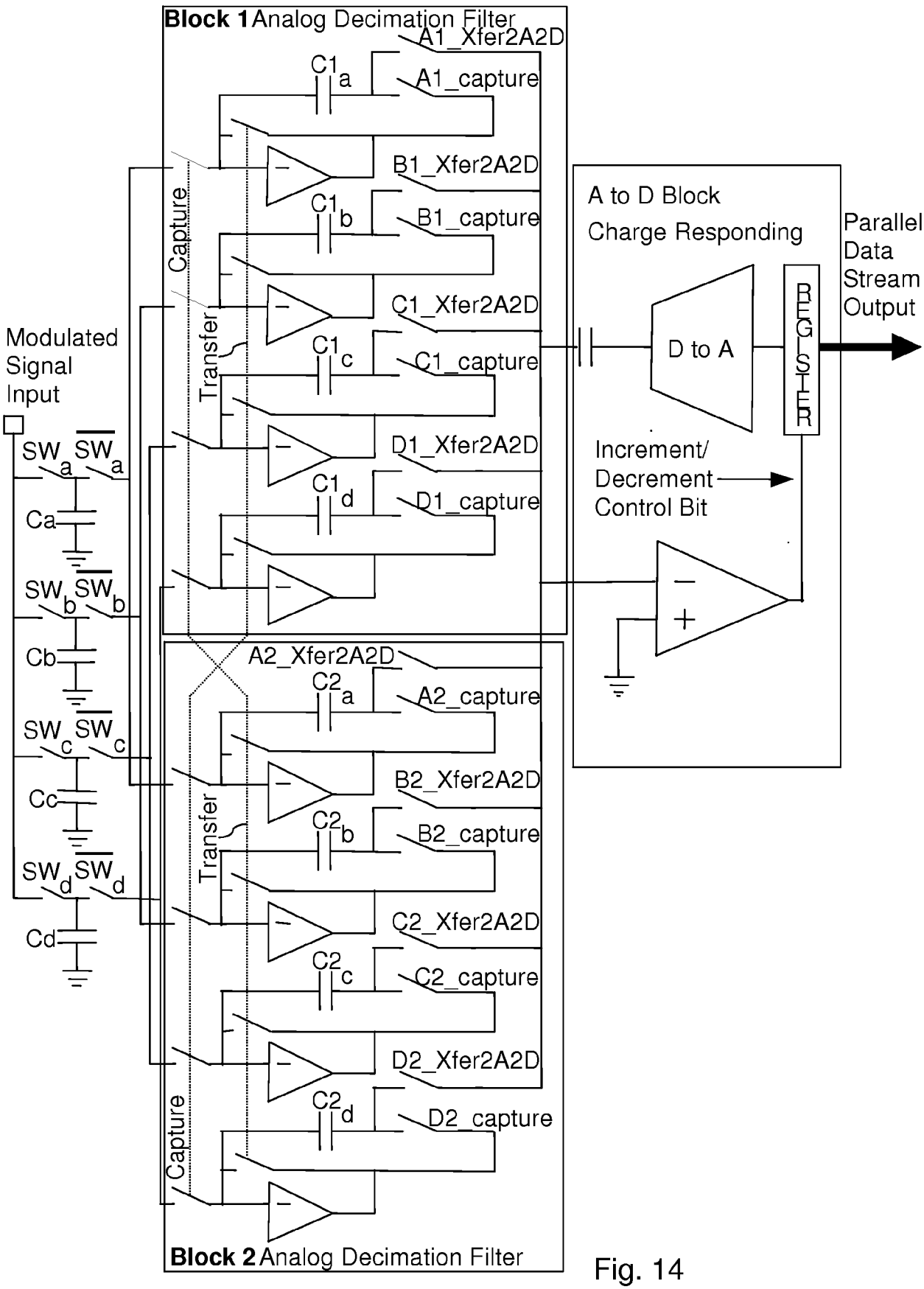
Block 1 Analog Decimation Filter
A1_Xfer2A2D
C1a
A1_capture
B1_Xfer2A2D
C1b
B1_capture
C1_Xfer2A2D
C1c
C1_capture
D1_Xfer2A2D
C1d
D1_capture
Capture
Transfer
Modulated Signal Input
SWa SWa
Ca
SWb SWb
Cb
SWc SWc
Cc
SWd SWd
Cd
A to D Block Charge Responding
D to A
REGISTER
Parallel Data Stream Output
Increment/ Decrement Control Bit
A2_Xfer2A2D
C2a
A2_capture
B2_Xfer2A2D
C2b
B2_capture
C2_Xfer2A2D
C2c
C2_capture
D2_Xfer2A2D
C2d
D2_capture
Transfer
Capture
Block 2 Analog Decimation Filter

Fig. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/064769

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H04B 1/00 (2013.01)
USPC - 455/130
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H04B 1/00, 1/02, 1/04, 1/26 (2013.01)
USPC - 455/130, 131, 307

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
CPC - H04B 1/00, 1/02, 1/04, 1/26 (2013.01)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Orbit, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 6,397,048 B1 (TODA) 28 May 2002 (28.05.2002) entire document	1-6,11-16 ---- 7-10,17-20
Y	US 6,337,888 B1 (HUANG et al) 08 January 2002 (08.01.2002) entire document	7-10,17-20
Y	EP0208817 B1 (AUSTIN) 19 December 1990 (19.12.1990) entire document	9,10,19,20
A	US 2009/0028269 A1 (PINKNEY) 29 January 2009 (29.01.2009) entire document	1-20
A	US 7,812,750 B2 (LAKDAWALA et al) 12 October 2010 (12.10.2010) entire document	1-20
A	US 6,181,740 B1 (YASUDA) 30 January 2001 (30.01.2001) entire document	1-20

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 January 2014	17 JAN 2014

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)