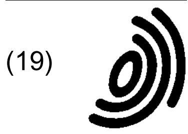
(19) 

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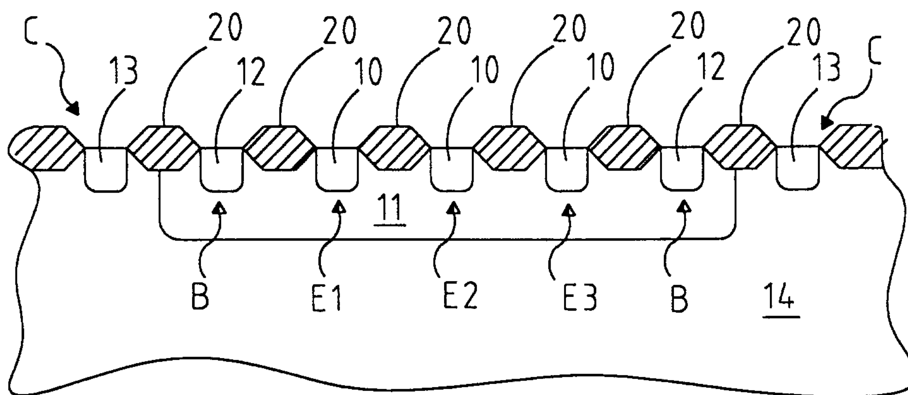
(54) **Multiemitter bipolar transistor for bandgap reference circuits**

(57) The present invention relates a transistor comprising a substrate region (14) of a first type (P) of conductivity in a semiconductor material layer of the same type (P) of conductivity, at least a first contact region (13) of said first type (P+) of conductivity inside said substrate region (14) and adjacent to a first terminal (C) of said transistor, a well (11) of second type (N) of conductivity placed inside said substrate region (14), characterized in that said well (11) of second type (N) of conductivity comprises at least a second contact region (12) of a second type of conductivity (N+) adjacent to a region of a second terminal (B) of said transistor, and a plurality of third contact regions (10) of said first type of conductivity (P+) adjacent to a plurality of regions of a third terminal (E1, ..., E3) of said transistor interposed each one (10) other (12) by proper insulating shapes (20).



EP 1 220 321 A1

Description

[0001] The present invention relates to a multiemitter bipolar transistor for bandgap reference circuits, particularly to a multiemitter vertical bipolar transistor to be used as reference in bandgap circuits.

[0002] In the modern microelectronic devices based on CMOS technology voltages are internally produced and used, such as, for example, negative voltages and / or high voltages, distinct from supply voltage.

[0003] The circuits for the management of the various produced voltages need of a precise and stable voltage reference both at the supply voltage oscillations and at the temperature changes. A reference of such a nature is obtained by means of a circuit known as "bandgap reference".

[0004] Such a circuit usually uses bipolar transistors so as to make full use of the characteristic of the bipolar transistors to have a current voltage law exponentially linked, in turn correlated with the energetic gap of the starting semiconductor.

[0005] In fact the way of working of the bandgap circuits provides for comparing the current flowing in a bipolar with that flowing in other "n" bipolars connected in parallel. Each one of "n + 1" bipolars is connected as diode, that is it has the base and collector electrodes short circuited.

[0006] In the reference bandgap circuits, implemented by CMOS technology with p type substrate, or implemented in technologies according to which masks or specific steps are not provided to realize bipolar transistors, pnp type vertical transistors are used.

[0007] For a n type substrate the dual principle is valid.

[0008] The pnp transistor is implemented making opportunely full use of some steps and necessary structures for the realization of complementary MOSFET transistors, that is the availability of an usual P+ implant, adapted for making the source and drain junction of the MOSFET transistors, and of a N well, adapted for making the channel of the MOS transistor with p channel and the p substrate itself, makes easily available the possibility to obtain said pnp vertical bipolar transistor.

[0009] In the process of implementation of these pnp type vertical bipolar transistors all the projecting laws relating to the distances and minimum sizes, relating to the active areas in the N well and to the P+ active areas placed in the substrate around the N well should be respected.

[0010] By implementing a structure with this standard CMOS technology a remarkable waste of area is obtained and, therefore, there is a lower integration of the devices.

[0011] Moreover an adequate electric coupling among the devices making the circuit is not obtainable.

[0012] In view of the state of the art described, it is an object of the present invention to make a multiemitter bipolar transistor for bandgap reference circuits able to avoid to the problems of the prior art.

[0013] According to the present invention, such object is achieved by a transistor comprising a substrate region of a first type of conductivity in a semiconductor material layer of the same type of conductivity, at least a first contact region of said first type of conductivity inside said substrate region and adjacent to a first terminal of said transistor, a well of second type of conductivity placed inside said substrate region, characterized in that said well of second type of conductivity comprises at least a second contact region of a second type of conductivity adjacent to a region of a second terminal of said transistor, adjacent to a region of a second terminal of said transistor, and a plurality of third contact regions of said first type of conductivity adjacent to a plurality of regions of a third terminal of said transistor interposed each other by opportune insulating shapes.

[0014] Thanks to the present invention is possible to realize a remarkable saving of silicon area.

[0015] Moreover it is possible to have a better coupling of the electric characteristics of the device.

[0016] Moreover it is possible to have a simplification of the interconnections among the several devices of the circuit.

[0017] Moreover it is possible to have an optical shield of the multiemitter bipolar devices constituting the bandgap reference circuit.

[0018] In particularly this last advantage allows a better stability of the voltage reference in devices with an Ultra Violet (UV) erasing package and, in general, for the steps of Electrical Wafer Sort (EWS), that is for the testing steps on wafer of every single chip even if it is not make in the dark.

[0019] The features and the advantages of the present invention will be made evident by the following detailed description of an embodiment thereof which is illustrated as not limiting example in the annexed drawings, wherein:

- the Figure 1 shows a reference bandgap circuit according to the prior art;
- the Figure 2 shows in particular a device of Figure 1;
- the Figure 3 shows a top plan view of a pnp bipolar transistor according to the prior art;
- the Figure 4 shows the device of Figure 3 along the section line IV - IV;
- the Figure 5 shows an embodiment of a matrix structure of the reference circuit according to the prior art;
- the Figure 6 shows a top plan view of a pnp bipolar transistor according to the present invention;
- the Figure 7 shows the device of Figure 6 along the section line VI - VI;
- the Figure 8 shows an embodiment of a matrix structure of the reference circuit according to the present invention.

[0020] In Figure 1 a reference bandgap circuit accord-

ing to the prior art is shown, wherein a reference supply line Vbgap and a couple of pnp bipolar transistor Q1 and Q2 that are connected as diode, that is having the respective base Q1b and Q2b and collector Q1c and Q2c electrodes short circuited, are noted.

[0021] The way of working provides for comparing, by means of a differential amplifier 1, connected at a side to a supply voltage Vcc and at the other side to ground, the voltage drops Vbe1 and Vb2 caused by the currents I1 and I2 that flow on the respective emitter branches of the transistors Q1 and Q2.

[0022] Moreover such a circuit must cause said currents I1 and I2 to be constant by means of a feedback system.

[0023] The currents that flow in the two branches must be one the exact multiple of the other, particularly $I2 = n * I1$.

[0024] To obtain this, it is well known to a skilled person to realize a bipolar transistor Q2 repeating "n" times the bipolar transistor Q1, as shown in Figure 1.

[0025] In fact Q2 is made as a copy of "n" transistors Q1, all transistors being connected in parallel, as shown in Figure 2.

[0026] Moreover, as it is well known, the vertical bipolar transistors Q1 and Q2 are made on a silicon wafer making proper full use of some steps, masks and necessary structures for the implementing of complementary MOSFETs, that is CMOS (not shown in Figure), inside the bandgap reference circuit.

[0027] In Figure 3 a top plan view of a pnp bipolar transistor according to the prior art is shown.

[0028] In a technological process of CMOS type, the availability of a P+ type typical implant 2, for the realization of the source and drain junctions of the MOSFET transistors, and of N type well 3, wherein the conductive channel of said p type MOSFET transistors is made and of a substrate 4 of the CMOS device, allows to realize a pnp type vertical bipolar transistor, without any dedicated process steps.

[0029] In fact the P+ type implant 2 represents the emitter and the collector electrode of the pnp vertical transistor, while the N type well 3 represents the base electrode of said pnp vertical transistor.

[0030] In Figure 4 a view of the device of Figure 3 along the section line IV - IV is shown and the sections of the N+ type implant ring 5 in the base region and the P+ type implants 6 and 7 in the collector and emitter region of the vertical bipolar transistor, adapted to contact respectively the base, the collector and the emitter, are noted.

[0031] The P+ type diffusion 7 of the emitter can be projected in function of the particular needs which the transistor has to respect according the known technology.

[0032] The building of a pnp vertical transistor must take into account the geometrical size of the bipolar transistor itself, because this behaves as vertical bipolar transistor only when the distance between the emitter and collector electrodes in the longitudinal direction is bigger than the thickness of the base region, otherwise the resulting bipolar transistor behaves as lateral bipolar transistor.

[0033] When a bandgap circuit on a layout is realized, in order to have a good reproducibility of the currents, a matrix structure 8 is realized, as shown in Figure 5.

[0034] Such a matrix structure 8 represents, in the specific embodiment, a matrix having five columns by five rows, in the cross-points of which there are some transistors placed but not used.

[0035] At every cross-point of the structure 8 there is, therefore, the representation of a pnp type bipolar transistor Q1, repeated n times. In fact in the center of every cross there is the emitter terminal 31, and moving through the board of the device, the base terminal 32 and the collector terminal 33 is found.

[0036] The other transistors are placed around it and eventually some other transistors are not connected and not used. This is to obviate the defects of symmetry of the structure and to reproduce the currents as similarly as possible.

[0037] In Figure 6 a top plan view of a pnp bipolar transistor made by a CMOS technology according to the present invention is shown.

[0038] As shown in such a Figure, the inventive solution provides for only one N type well 11, adapted to contain the "n + 1" P+ type implants 10.

[0039] The N type well 11 represents the base electrode, while the "n + 1" implants represent the pnp bipolar emitters.

[0040] In Figure 7 the device of Figure 6 along the section line VI - VI is shown, wherein a P type substrate 14, making the collector, that results connectable by means of a P+ type ring 13 that rounds all the inventive structure, and the N type well 11, making the base, connected by means of N+ type ring 12, are noted. The N type well 11 contains the "n + 1" emitters 10, made by the P+ type implants.

[0041] What is represented in such a Figure, therefore, it is a pnp type bipolar transistor, having the P type substrate 14 with a P+ type contact region 13 adjacent to its collector terminal C, and the N type well 11 with N+ type contact regions 12 adjacent to its base terminal B and with P+ type contact regions adjacent to their emitter terminals E1, ..., E3.

[0042] Suitable structures 20, such as oxides or junction wells, to isolate the emitters E1, ..., E3 with respect to each other and the well 12 are provided.

[0043] It is to be noted that this structure is possible because the traditional bandgap circuit provides that the base and collector short circuited to the ground.

[0044] In Figure 8 an embodiment of a matrix structure of the reference circuit according to the present invention is shown.

[0045] In such a Figure a matrix 15 that results to have five columns 18, ..., 22 and five rows 23, ..., 27.

[0046] At every cross an emitter electrode is placed

that is interconnected or floating with respect to the other emitter electrodes.

[0047] From the specific embodiment shown in Figure 8, a matrix 15 results having an interconnection scheme such as that described in the successive table:

	18	19	20	21	22
23	x	e	X	e	x
24	e	e	X	e	e
25	e	x	E	x	e
26	e	e	X	e	e
27	x	e	X	e	x

where "x" indicates a floating emitter, "e" an emitter interconnected with the other emitters and "E" an emitter of the single side.

[0048] The matrix 15 results to be perfectly symmetrical and with better matching characteristics, that is the transistors are much more similar to each other, with respect to the traditional embodiments. This because a structure 16 is repeated more times and it is so as to have structures 17 equal to the structure 16 and connected to each other with the lower number of interconnections.

[0049] In this way the transistor that must be used alone, that is in the single branch of the reference bandgap circuit and is indicated with the symbol "E" in the previous table, is arranged in the center of the matrix 15, so that the matrix 15 itself is realized with the highest number of implementable transistors, so as to increase the system symmetry and therefore the reproducibility of the transistors.

[0050] Making the matrix 15 with "n + 1" emitters near each other, the matching is enhanced both for the smaller occupied area and because it is not necessary to short circuit every base and collector electrode with metal lines.

[0051] Inserting the "n + 1" emitters in the base 11, multiple advantages are obtained such as, for example: a) saving of silicon area, because by inserting the "n + 1" emitters in a N type unique well 11 the only law to be respected is the minimum distance between the active areas of the emitters 10; b) it is not necessary to short circuit the bases and the collectors each other with metal lines, but with the present invention it is sufficient to short circuit only the unique large base and the collector; c) not short circuiting the bases and the collectors allows to contact the n emitters with each other and the central emitter with an operational amplifier (not shown in Figure) with a structure of interconnection wherein intercrosses among the bases and collector do not exist.

[0052] This last advantage gives the possibility to let the higher interconnection level free to be, therefore, used as an optical shield against the light for the whole system of transistors adapted to generate the bandgap voltage, in the case the integrated circuit is mounted onto an UV erasing package, for example, for EPROM memories.

[0053] Moreover the possibility to have this shield allows that the EWS phase on wafer can develop with a biased circuit and not in the dark because the shield guaranties the stability of the bandgap circuit and therefore also of the bandgap voltage.

[0054] In the present embodiment pnp type vertical bipolar transistor are used, but the inventive solution also provides for bandgap reference circuits made by npn type bipolar transistors connected in diode configuration.

[0055] The present invention is destined, therefore, both to standard CMOS processes, EPROM processes, and other specific processes such as, for example, BCD and / or BiCMOS, if in the reference branches a bipolar connected as diode is used.

Claims

1. Transistor comprising a substrate region (14) of a first type (P) of conductivity in a semiconductor material layer of the same type (P) of conductivity, at least a first contact region (13) of said first type (P+) of conductivity inside said substrate region (14) and adjacent to a first terminal (C) of said transistor, a well (11) of second type (N) of conductivity placed inside said substrate region (14), **characterized in that** said well (11) of second type (N) of conductivity comprises at least a second contact region (12) of a second type of conductivity (N+) adjacent to a region of a second terminal (B) of said transistor, and a plurality of third contact regions (10) of said first type of conductivity (P+) adjacent to a plurality of regions of a third terminal (E1, ..., E3) of said transistor interposed each one (10) other (12) by proper insulating shapes (20).

2. Transistor according to claim 1, **characterized in that** said substrate region (14) has a first resistivity value, and that said first (13) and second (12) contact regions have a second value of resistivity lower than said first value of resistivity.

3. Transistor according to claim 1, **characterized in that** said well (11) of said second type of conductivity (N) has a third value of resistivity, and that said third contact regions (10) have a fourth value of resistivity lower than said third value of resistivity.

4. Transistor according to claim 1, **characterized in that** said second type of conductivity (N) is short circuited with said first contact region (13) of said first type of conductivity (P+).

5. Transistor according to claim 1, **characterized in**

that said first contact regions (13) are adjacent to collector terminal regions (C).

6. Transistor according to claim 1, **characterized in that** said second contact regions (10) are adjacent to emitter regions (E1, ..., E3).

7. Transistor according to claim 1, **characterized in that** said third contact regions (12) are adjacent to base terminal regions (B).

8. Transistor according to claim 1, **characterized in that** said first type of conductivity is p type and said second type of conductivity is n type, so as to realize a pnp bipolar transistor.

9. Transistor according to claim 1, **characterized in that** said first type of conductivity is n type and said second type of conductivity is p type, so as to realize a npn bipolar transistor.

10. Transistor according to claim 1, **characterized in that** said first (13) and second (10) contact regions are made by the same implant of dopant atoms.

11. Transistor according to claim 1, **characterized in that** said insulating regions (20) are made by proper insulating means.

5 10 15 20 25 30 35 40 45 50 55

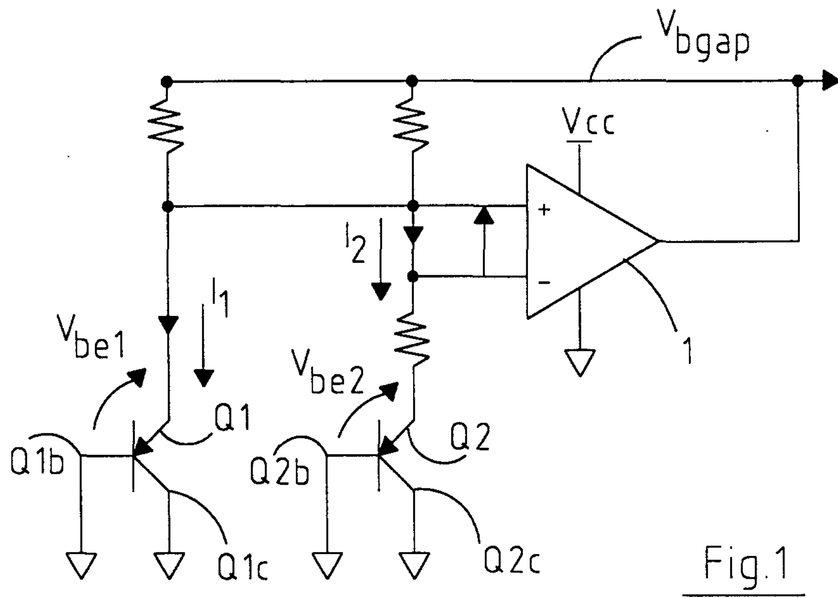


Fig.1

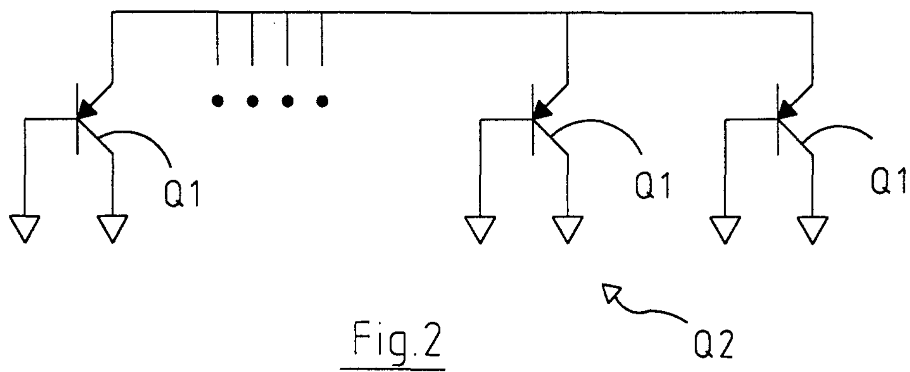


Fig.2

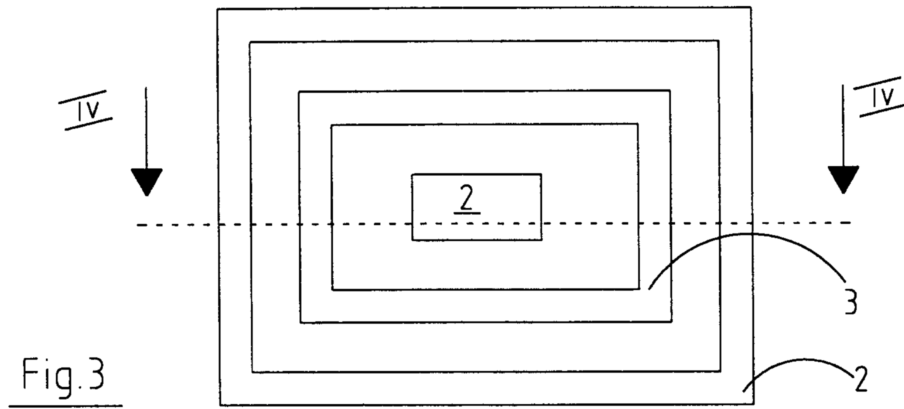


Fig.3

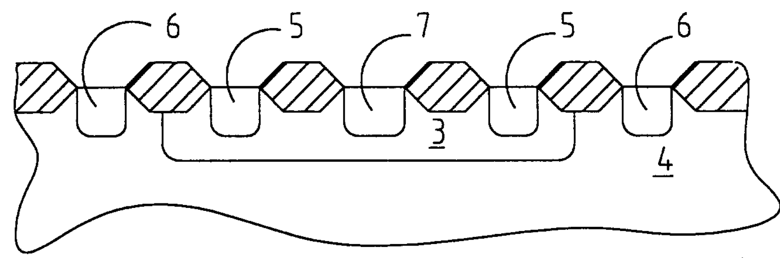


Fig.4

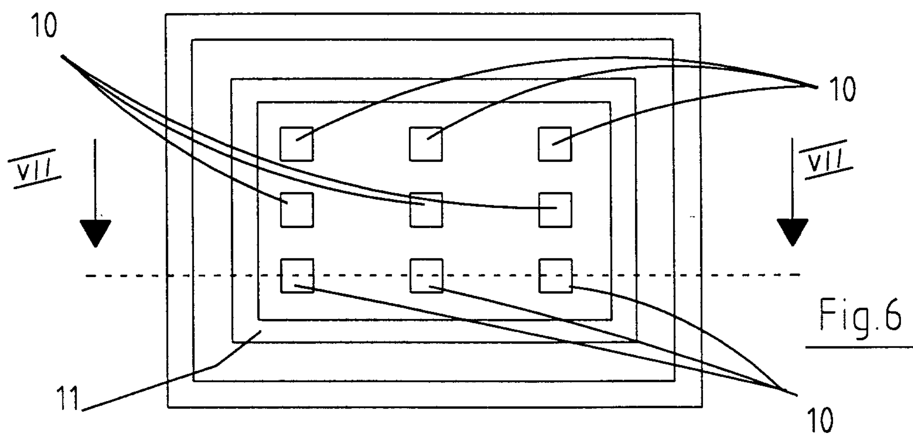


Fig.6

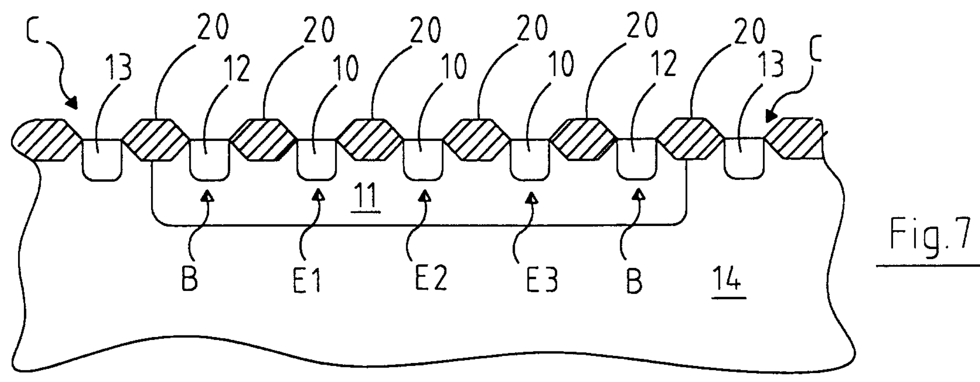


Fig.7

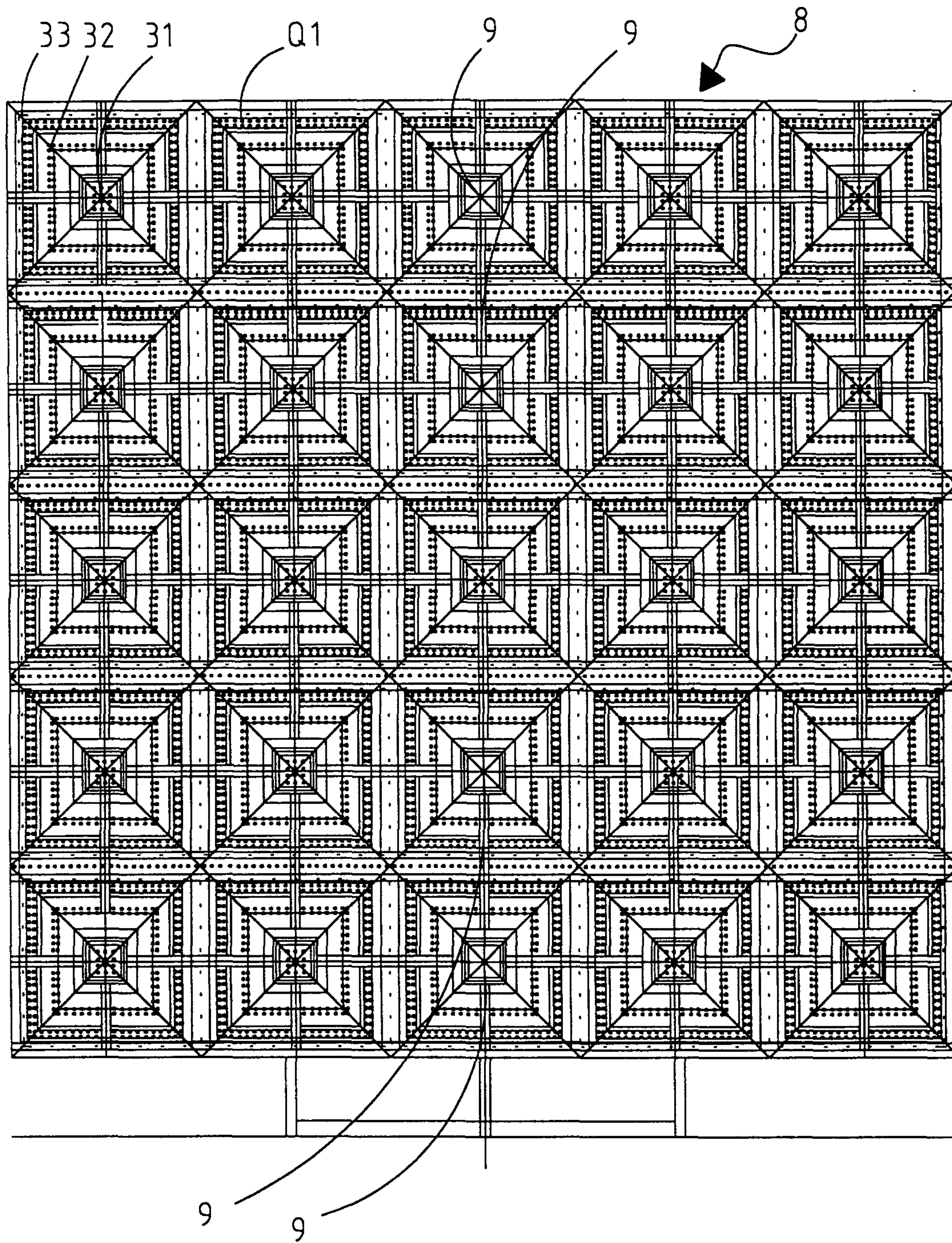


Fig.5

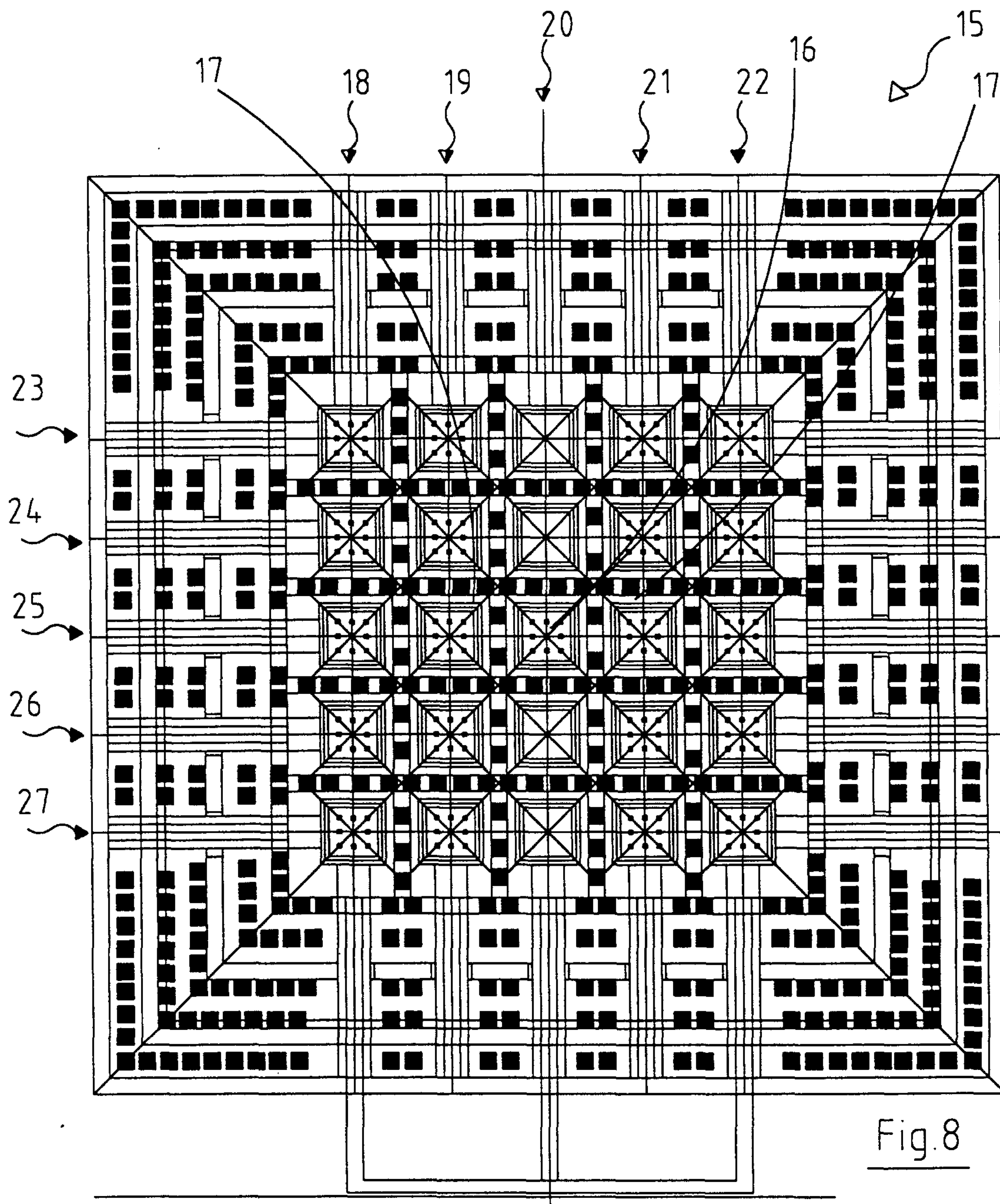


Fig.8

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EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0851

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 439 163 A (TOKYO SHIBAURA ELECTRIC CO) 31 July 1991 (1991-07-31) * the whole document * ---	1-3,5-7, 9-11	H01L29/732 H01L29/08
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 August 2001	Baillet, B

CATEGORY OF CITED DOCUMENTS

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