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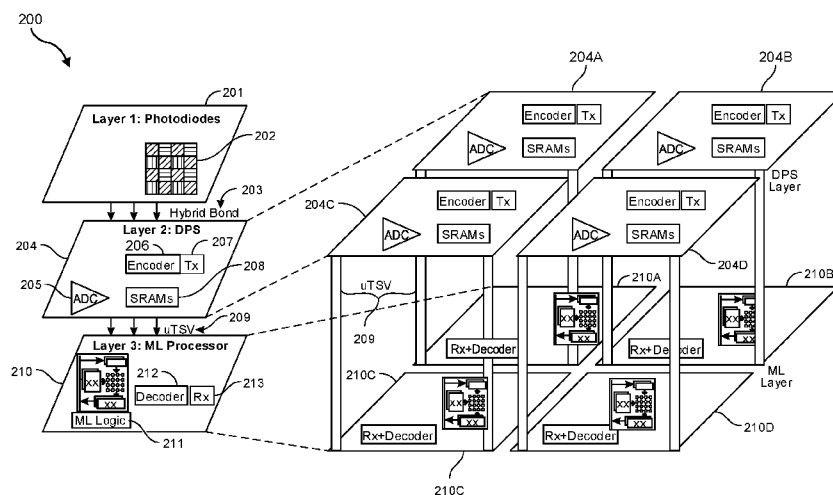


FIG. 2

(57) Abstract: The disclosed system may include a first layer that includes multiple digital pixel sensors configured to detect light. The system may also include a second layer that includes various image processing components configured to process the light detected by the digital pixel sensors. Still further, the system may include a third layer that includes machine learning (ML) hardware processing components. The image processing components of the second layer may be communicatively connected to the ML hardware processing components of the third layer via multiple micro through-silicon vias (uTSVs). Various other methods of manufacturing, apparatuses, and computer-readable media are also disclosed.

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1 IMPROVED ARCHITECTURE FOR COUPLING DIGITAL PIXEL SENSORS AND
2 COMPUTING COMPONENTS

3 **FIELD OF THE DISCLOSURE**

4 **[0001]** The present disclosure is generally directed to digital pixel sensor (DPS)
5 chips that allow for incorporation of machine learning (ML) chips connected via micro
6 through-silicon vias (uTSVs).

7 **BACKGROUND**

8 **[0002]** Traditional on-sensor computing systems such as DPS chipsets typically include
9 three layers: 1) a photodiode layer, 2) a combined analog-to-digital converter (ADC) and
10 memory layer, and 3) a machine learning logic layer that has an ML processor. Within such
11 conventional three-layer systems, image data are transferred from the second layer to the
12 third layer via data transfer interfaces, such as Mobile Industry Processor Interface (MIPI)
13 interfaces. These MIPI interfaces, however, have high area overhead on the second and third
14 layers. Indeed, MIPI interfaces result in large amounts of “keep-out” space on the chips that
15 is virtually unusable. Accordingly, chipset layout and total capacity to hold electrical
16 components is limited in such traditional systems.

17 **[0003]** Moreover, these conventional systems typically consume high amounts of
18 energy when transferring image data. Because the photodiode layer (layer one) is typically
19 fabricated using older and larger technology nodes, as compared with current computing
20 technologies that allow computer processors to be produced at a much smaller scale on much
21 smaller nodes, these traditional systems consume more power when performing processing
22 operations. Moreover, the large area requirements of MIPI transfer interfaces limit the
23 number of transistors and other electronic components that can be fit onto a given third-layer
24 ML processor.

25 **SUMMARY OF THE DISCLOSURE**

26 **[0004]** In accordance with a first aspect of the present disclosure, there is provided a
27 system comprising: a first layer that includes a plurality of digital pixel sensors configured to
28 detect light; a second layer that includes one or more image processing components
29 configured to process the light detected by the digital pixel sensors; and a third layer that
30 includes one or more machine learning (ML) hardware processing components, wherein the
31 image processing components of the second layer are communicatively connected to the ML
32 hardware processing components of the third layer via one or more micro through-silicon vias

1 (uTSVs).

2 [0005] In some embodiments, the image processing components of the second layer
3 comprise at least one of an analog-to-digital converter (ADC), an encoder, a memory, or a
4 transmitter.

5 [0006] In some embodiments, the ML hardware processing components control
6 capture of consecutive image frames.

7 [0007] In some embodiments, the ML hardware processing components are
8 configured to execute one or more smart applications.

9 [0008] In some embodiments, at least one of the one or more smart applications
10 comprises a smart image processing application.

11 [0009] In some embodiments, the ML hardware processing components include a
12 plurality of processing cores.

13 [0010] In some embodiments, one or more of the processing cores are configured to
14 perform local processing on a specified portion of an image captured by the plurality of digital
15 pixel sensors.

16 [0011] In some embodiments, the ML processing cores share information to perform
17 centralized processing that stitches the image captured by the plurality of digital pixel sensors
18 together.

19 [0012] In some embodiments, one or more of the processing cores is configured to
20 recognize one or more objects within a specified region of an image.

21 [0013] In some embodiments, one or more of the processing cores is configured to
22 track the one or more recognized objects across a plurality of subsequent images.

23 [0014] In some embodiments, the one or more recognized objects are tracked across
24 the plurality of subsequent images without neighboring pixel data from other ML processing
25 cores.

26 [0015] In some embodiments, the one or more recognized objects are processed by
27 the same ML processing core until the objects are no longer present in the image.

28 [0016] In some embodiments, the one or more recognized objects are processed by a
29 plurality of ML processing cores upon determining that the objects have moved between
30 images.

31 [0017] In accordance with a second aspect of the present disclosure, there is provided
32 an electronic device comprising: a first layer that includes a plurality of digital pixel sensors

1 configured to detect light; a second layer that includes one or more image processing
2 components configured to process the light detected by the digital pixel sensors; and a third
3 layer that includes one or more machine learning (ML) hardware processing components,
4 wherein the image processing components of the second layer are communicatively
5 connected to the ML hardware processing components of the third layer via one or more
6 uTSVs.

7 **[0018]** In some embodiments, the image processing components of the second layer
8 are configured to combine a plurality of image bits into a combined group of image data bits.

9 **[0019]** In some embodiments, the combined group of image data bits is transferred
10 as a group to the ML hardware processing components of the third layer through the uTSVs.

11 **[0020]** In some embodiments, the combined group of image data bits is transferred
12 as a group to the ML hardware processing components using time-based multiplexing.

13 **[0021]** In some embodiments, at least one of the ML hardware processing
14 components comprises a local memory buffer.

15 **[0022]** In some embodiments, image data stored in the local memory buffer is
16 processed using a systolic array whose parameters are prestored in the local memory buffer.

17 **[0023]** In accordance with a third aspect of the present disclosure, there is provided a
18 method of manufacture comprising: forming a first layer that includes a plurality of digital
19 pixel sensors configured to detect light; forming a second layer adhered to the first layer that
20 includes one or more image processing components configured to process the light detected
21 by the digital pixel sensors; and forming a third layer adhered to the second layer that includes
22 one or more machine learning (ML) hardware processing components, wherein the image
23 processing components of the second layer are communicatively connected to the ML
24 hardware processing components of the third layer via one or more uTSVs.

25 **[0024]** It will be appreciated that any features described herein as being suitable for
26 incorporation into one or more aspects or embodiments of the present disclosure are
27 intended to be generalizable across any and all aspects and embodiments of the present
28 disclosure. Other aspects of the present disclosure can be understood by those skilled in the
29 art in light of the description, the claims, and the drawings of the present disclosure. The
30 foregoing general description and the following detailed description are exemplary and
31 explanatory only and are not restrictive of the claims.

32 **BRIEF DESCRIPTION OF THE DRAWINGS**

1 **[0025]** The accompanying drawings illustrate a number of exemplary embodiments
2 and are a part of the specification. Together with the following description, these drawings
3 demonstrate and explain various principles of the present disclosure.

4 **[0026]** FIG. 1 illustrates an embodiment of an intelligent image sensing and computing
5 platform.

6 **[0027]** FIG. 2 illustrates an embodiment of an intelligent image sensing and computing
7 platform in which various layers are expanded to show greater detail.

8 **[0028]** FIG. 3 illustrates an embodiment of an intelligent image sensing and computing
9 platform in which light data is multiplexed from one layer to another layer.

10 **[0029]** FIG. 4 illustrates a computing layer of an intelligent image sensing and
11 computing platform.

12 **[0030]** FIG. 5 is a flow diagram of an exemplary method for manufacturing an
13 intelligent image sensing and computing platform.

14 **[0031]** FIG. 6 illustrates an embodiment in which multiple cores and smart applications are
15 implemented to processes single images and sequences of images.

16 **[0032]** FIG. 7 illustrates an embodiment in which an image is divided into different
17 sections, each of which is processed by a machine learning processor core.

18 **[0033]** FIG. 8 illustrates an embodiment in which a sequence of images is analyzed by
19 different machine learning processor cores.

20 **[0034]** FIG. 9 is an illustration of exemplary augmented-reality glasses that may be used in
21 connection with embodiments of this disclosure.

22 **[0035]** FIG. 10 is an illustration of an exemplary virtual-reality headset that may be used in
23 connection with embodiments of this disclosure.

24 **[0036]** FIG. 11 is an illustration of exemplary haptic devices that may be used in connection
25 with embodiments of this disclosure.

26 **[0037]** FIG. 12 is an illustration of an exemplary virtual-reality environment according to
27 embodiments of this disclosure.

28 **[0038]** FIG. 13 is an illustration of an exemplary augmented-reality environment according
29 to embodiments of this disclosure.

30 **[0039]** Throughout the drawings, identical reference characters and descriptions indicate
31 similar, but not necessarily identical, elements. While the exemplary embodiments described
32 herein are susceptible to various modifications and alternative forms, specific embodiments

1 have been shown by way of example in the drawings and will be described in detail herein.
2 However, the exemplary embodiments described herein are not intended to be limited to the
3 particular forms disclosed. Rather, the present disclosure covers all modifications,
4 equivalents, and alternatives falling within the scope of the appended claims.

5 DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

6 [0040] Traditional on-sensor computing systems such as DPS chipsets typically include
7 three layers: 1) a photodiode layer, 2) a combined analog-to-digital converter (ADC) and
8 memory layer, and 3) a machine learning logic layer that has an ML processor. Within such
9 conventional three-layer systems, image data are transferred from the second layer to the
10 third layer via data transfer interfaces, such as Mobile Industry Processor Interface (MIPI)
11 interfaces. These MIPI interfaces, however, have high area overhead on the second and third
12 layers. Indeed, MIPI interfaces result in large amounts of “keep-out” space on the chips that
13 is virtually unusable. Accordingly, chipset layout and total capacity to hold electrical
14 components is limited in such traditional systems.

15 [0041] Moreover, these conventional systems typically consume high amounts of
16 energy when transferring image data. Because the photodiode layer (layer one) is typically
17 fabricated using older and larger technology nodes, as compared with current computing
18 technologies that allow computer processors to be produced at a much smaller scale on much
19 smaller nodes, these traditional systems consume more power when performing processing
20 operations. Moreover, the large area requirements of MIPI transfer interfaces limit the
21 number of transistors and other electronic components that can be fit onto a given third-layer
22 ML processor.

23 [0042] In contrast, the embodiments described herein may implement dense micro
24 through-silicon vias to communicate image data from an image sensing layer to a machine
25 learning processing layer. By using uTSVs, the embodiments described herein may transfer
26 image data from a second layer of a DPS to the third layer with high amounts of parallelism.
27 To provide this parallelism, the systems herein may be configured to divide a pixel array on
28 the first layer (e.g., an image sensing, photodiode layer) into multiple smaller blocks or
29 sections. These systems may then be configured to pack the image data of each section
30 together for transfer through uTSVs to a third layer (e.g., a machine learning processing layer).
31 The ML processing layer may, itself, be divided into multiple cores, where each core on the
32 ML layer is equipped with a dedicated uTSV array to receive image data from the sensing layer

1 and process that data in a parallel and distributed manner. By providing parallelism in this
2 manner, the systems herein may process image data much faster and with less power than
3 traditional systems. Moreover, the high amount of bandwidth provided by uTSVs may allow
4 new types of smart machine learning applications to be processed on the ML processing layer.
5 These concepts will be described further below with regard to FIGS. 1-13.

6 **[0043]** Features from any of the embodiments described herein may be used in
7 combination with one another in accordance with the general principles described herein.
8 These and other embodiments, features, and advantages will be more fully understood upon
9 reading the following detailed description in conjunction with the accompanying drawings
10 and claims.

11 **[0044]** FIG. 1 illustrates an embodiment of a system 100 that includes multiple
12 component parts. Each of these component parts may form an intelligent image sensing and
13 computing platform that is more compact, more energy efficient, and provides faster
14 computing power than traditional digital pixel sensor (DPS) imaging systems. The system 100
15 of FIG. 1 may include a first layer 101 that may be referred to herein as an image sensing layer
16 or photodiode layer. The first layer 101 may include multiple different digital pixel sensors
17 102. These digital pixel sensors may be charge-coupled devices (CCDs), active-pixel sensors
18 (complementary metal-oxide-semiconductor (CMOS) sensors), or other similar image sensing
19 devices. These digital pixel sensors 102 may be configured to detect incoming light when
20 exposed to light via an open shutter. The first layer 101 may include substantially any number
21 or type of digital pixel sensors 102. Moreover, these digital pixel sensors 102 may be arranged
22 in substantially any shape or type of layout.

23 **[0045]** The first layer 101 may be connected to a second layer 104 that includes one
24 or more image processing components 105 configured to process the light 103 detected by
25 the digital pixel sensors 102. The image processing components 105 of the second layer 104
26 may include, but are not limited to, analog-to-digital converters (ADCs 106), encoders 107,
27 memory 108 (e.g., random access memory (RAM) or static RAM (SRAM)), transmitters 109 (or
28 transceivers), and other image processing components. In some embodiments, each digital
29 pixel sensor 102 may have its own corresponding ADC on the second layer 104. These ADCs
30 may be configured to convert the detected light 103 (in an analog value) to a digital value that
31 can be stored in memory 108 and/or transmitted to an external data store (e.g., a cloud data
32 store). The encoder 107 may be configured to encode the digital data associated with each of

1 the digital pixels of the first layer 101. The encoding may include converting the digital pixel
2 values to a specified data format or into a specific data structure. The image processing
3 components 105 of the second layer 104 may be connected to the third layer 112 of the
4 system 100 via one or more micro through-silicon vias 110.

5 **[0046]** Micro through-silicon vias (uTSVs) 110 may refer to vertical electrical
6 connections that pass directly through silicon (or other substrate) between layers of an
7 integrated circuit. Micro through-silicon vias 110 may be much smaller than traditional
8 through-silicon vias and may have a much smaller footprint on a processing chip. Indeed, each
9 use of a TSV on a processing chip results in an area on that chip that is a “keep-out zone” or
10 “dead zone” on which other electronic components (e.g., transistors, capacitors, diodes, etc.)
11 or traces may not be placed. Traditional TSVs typically result in large dead zones on processing
12 chips, reducing the processing power and efficiency of those chips. Micro TSVs, however, have
13 much smaller dead zones and, as such, many more can be implemented on a chip such as a
14 machine learning processor.

15 **[0047]** Third layer 112 of the system 100 may include one or more such processing
16 chips in the machine learning (ML) hardware processing components 111. These ML hardware
17 processing components 111 may be communicatively connected to the image processing
18 components 105 of the second layer 104 via one or more uTSVs 110. At least in some
19 embodiments, because uTSVs 110 are used to transfer the digital data produced by the ADCs
20 106 and/or encoders 107, and because many more uTSVs can be used than in traditional
21 scenarios with TSVs, the digital data may be transferred over in parallel and may be processed
22 in parallel using multiple machine learning cores. In some cases, the digital image data from
23 different quadrants of an image may be sent to different ML chips and/or ML cores within
24 those chips. Each of these ML cores may thus, in parallel, process image data as it comes in
25 and may apply machine learning logic to changes between pixels between subsequent image
26 frames. These embodiments will be explained in greater detail below with regard to FIGS. 2-
27 8 and in conjunction with method 500 of FIG. 5.

28 **[0048]** FIG. 2 illustrates a digital pixel sensor system 200 that may be similar to or the
29 same as the system 100 of FIG. 1. The digital pixel sensor system 200 may include three (or
30 more) layers including a first layer 201 that has one or more photodiodes 202. The first layer
31 201 may be bonded to the second layer 204 via a hybrid bond 203 or via some other type of
32 inter-layer bond. The second layer may include ADCs 205, encoders 206, transmitters 207,

1 and memory 208 (e.g., static random-access memory (SRAM)). The second layer 204 may be
2 bonded, at least in some places, via a hybrid bond or other type of bond to the third layer
3 210. The third layer 210 may include one or more machine learning logic processors 211, one
4 or more decoders 212, and one or more receivers 213. Each of the three layers may be made
5 of silicon or some other semiconductor substrate. In some cases, each of the layers may be
6 made of the same material, while in other cases, at least one of the layers may be made of a
7 different material.

8 **[0049]** In some cases, the second layer 204 may be divided into multiple segments,
9 including two, three, four, or more different segments. In the embodiment shown in FIG. 2,
10 the second layer 204 of the digital pixel sensor system 200 is divided into four segments,
11 204A-204D. Each segment 204A-204D may include its own image processing components
12 including its own ADC, its own encoder, its own transmitter, and its own memory (among
13 potentially other components). Similarly, the third layer 210 may also be divided into a
14 corresponding number of segments. Thus, in the embodiment illustrated in FIG. 2, the third
15 layer 210 of system 200 is divided into four different segments, 210A-210D. Each third layer
16 segment 210A-210D may include its own ML logic chip 211, its own decoder 212, and its own
17 receiver 213 (among potentially other components). In some cases, as will be explained
18 below, these ML hardware processing components may be configured to run smart
19 applications that are configured to control the capture of consecutive image frames and
20 execute smart applications (including smart image processing application) to analyze patterns
21 between subsequent images. These smart applications may be capable of handling large
22 amounts of input data, as it is transferred from the photodiodes through the ADCs and to the
23 ML processing chips using the uTSVs 209.

24 **[0050]** The computing environment 300 of FIG. 3 illustrates an embodiment in which
25 data may be transferred between a second layer and a third layer. Such embodiments may
26 be designed to optimize the parameters of uTSVs, including higher density, smaller size, driver
27 circuit control, available communication protocols, etc. Such optimizations may enable tight
28 three-dimensional (3D) integrated circuit (IC) integration of the ML processor on the third
29 layer of the system. FIG. 3 illustrates a diagram of transferring data from a second layer to a
30 third layer of a digital pixel sensor system (e.g., a multi-layer integrated circuit). Leveraging
31 uTSVs for data transfer may incur area overhead on the second and third layers, as each uTSV
32 will take up some area on the second and third layers of the integrated circuit. The

embodiments herein may be configured to determine an optimum number of uTSVs to implement in a given DPS system. In some cases, the optimal number of uTSVs may depend on the processing bandwidth of the machine learning hardware processors on the third layer. Additionally or alternatively, other characteristics may affect the optimal number of uTSVs including image capture frequency, data transmission frequency, encoder output, and other characteristics. Thus, simply adding a large number of uTSVs to the DPS system, and placing the uTSVs as densely as possible between the second and third layers may not be optimal in all situations.

[0051] Accordingly, the embodiments herein may be configured to divide the digital pixel array of the first layer into multiple blocks and then pack the image data of each block together for transfer. For instance, a pixel array 301 may be divided into multiple blocks and fed to an encoder 302. The digital data may then be shared across one or more uTSV channels 303 using time multiplexing or some other type of multiplexing or other transmission method that may speed up the transfer. In some cases, the data may be encoded prior to transfer and, at least in some cases, the data may be compressed prior to transfer using various compression algorithms. On the third layer, the data may be unencoded by decoder 304 (and/or uncompressed, if applicable), resulting in decoded pixel data 305. This decoded pixel data may then be used by the ML processing hardware to identify objects, to track objects, or to perform other types of processing on an image or set of images. In some embodiments, while the third layer is decoding or otherwise processing data, the first and/or second layer may process the next batch of input (e.g., the next image frame). In some examples, processing data concurrently in this fashion may be faster and/or expand the effective quantity of available data storage.

[0052] In some cases, different numbers of uTSVs may be modeled using a specific number of photodiode inputs and a specific number of ML processor outputs. Using such modeling, the optimal number of uTSVs may be identified such that the area taken up by uTSV junctures on the second and third layers is not so high that it impedes the amount of processing that can be performed by the ML chips, but is large enough to provide bandwidth sufficient to transfer the available pixel data from the digital pixel sensors. Such simulation may also take into account any multiplexing, encoding, compression, etc. to arrive at an optimal block granularity that is specific to each DPS device, according to its photodiode detectors, image processing hardware, and ML processing hardware.

1 **[0053]** FIG. 4 illustrates an embodiment of a machine learning hardware processor
2 400 that includes multiple cores 402A-402D. Although four cores are shown, substantially any
3 number of ML processor cores may be included in the ML hardware processor 400. The ML
4 hardware processor may be the same as or different than ML hardware processing
5 components 111 of FIG. 1 or 211 of FIG. 2. In the embodiment shown in FIG. 4, the ML
6 hardware processor 400 includes four global memories 401A-401D that, in some cases, may
7 be used by specific ML cores and, in other cases, may be used by any of the ML cores 402A-
8 402D. Each core may include multiple component parts, as shown in the expanded image of
9 ML core 402B. As illustrated, the expanded version of ML core 402B may include an activation
10 buffer 403 that buffers incoming image data 410 from the uTSV 405. The systolic array 404
11 may facilitate input activations 408 and output activations 409 as part of smart applications
12 that process the incoming image data 410. These activations may interact with the image data
13 410 stored in the activation buffer 403. In some cases, the weight buffer 406 may function as
14 a secondary buffer to the activation buffer, while the controller 407 may control the capture
15 of images. Such control may include specifying image sensor exposure time, image capture
16 frequency, amount and type of data stored, etc. Thus, each of the components of the ML
17 hardware processor 400 may work together to perform local processing on image data,
18 including running machine learning applications that may be used to perform artificial reality
19 or virtual reality functions including location tracking, hand or eye tracking, facial recognition,
20 or other similar functions.

21 **[0054]** In some embodiments, each ML core 402A-402D may be equipped with a
22 dedicated uTSV array to receive data from the sensing layer (e.g., layer one). In some case,
23 each ML core 402A-402D may include multiple uTSV for data transfer. The image data 410
24 may be transferred from the second layer to the third layer in a parallel and distributed
25 manner using the dedicated uTSV array (e.g., using uTSVs 405). As shown in FIG. 4, the ML
26 hardware processor 400 on the third layer may be split into multiple smaller processing arrays
27 to consume the uTSV data with a processing bandwidth that is much higher than that
28 available in conventional systems. Moreover, splitting the ML hardware processor 400 into
29 multiple smaller processing arrays or processing cores may also allow the ML processor to
30 exploit the spatial relationship of the incoming image data to use less power, provide better
31 performance, and use less area on the chip. This combination of low power, high
32 performance, and low chip area use may enable new types of ML applications to be processed

1 using the ML hardware processor 400. At least some of these ML applications are described
2 below with regard to method 500 of FIG. 5 and FIGS. 6-8

3 **[0055]** FIG. 5 illustrates a flow diagram of an exemplary computer-implemented
4 method 500 for manufacturing or producing a digital pixel sensor. The steps shown in FIG. 5
5 may be performed by any suitable computer-executable code and/or computing system. In
6 one example, each of the steps shown in FIG. 5 may represent an algorithm whose structure
7 includes and/or is represented by multiple sub-steps, examples of which will be provided in
8 greater detail below.

9 **[0056]** At step 510 of method 500, the method may include forming a first layer that
10 includes multiple digital pixel sensors configured to detect light. These digital pixel sensors
11 may be CCD's, CMOS sensors, or other types of image sensing hardware. The digital pixel
12 sensors may sense light wavelengths and intensities, and may pass that light data to image
13 processing components on a second layer. At step 520, the manufacturing method may
14 include forming a second layer adhered to the first layer, where the second layer includes one
15 or more image processing components configured to process the light detected by the digital
16 pixel sensors. The image processing components may include ADCs, encoders, transmitters,
17 memory, or other electronic components. These components may be configured to process
18 the incoming light data from the digital pixel sensors and prepare it (e.g., format or encode
19 the light data) for processing by a machine learning processor.

20 **[0057]** Step 530 of method 500 may include forming a third layer adhered to the
21 second layer that includes one or more machine learning (ML) hardware processing
22 components. The image processing components of the second layer may be communicatively
23 connected to the ML hardware processing components of the third layer via one or more
24 uTSVs. In some cases, as shown in FIG. 4, an ML hardware processor may be divided into
25 different parts, each of which may have one or more dedicated uTSVs to pass the encoded
26 data. In some cases, the data for a given image is passed together as a group or block of data.
27 In such cases, for example, the image processing components of the second layer may be
28 configured to concatenate or combine multiple image bits into a combined group of image
29 data bits. This combined group of image data bits may be transferred as a group to the ML
30 hardware processing components of the third layer through the uTSVs (as generally shown in
31 FIG. 3). In some embodiments, the combined group of image data bits may be multiplexed
32 and may be transferred as a group to the ML hardware processing components using, for

1 example, time-based multiplexing. The group of image data bits may be transferred to a single
2 local memory buffer or to multiple local memory buffers on the ML hardware processor. In
3 some cases, image data stored in these local memory buffers may be processed using a
4 systolic array (e.g., 404 of FIG. 4) whose parameters are prestored in the local memory buffer.
5 The systolic array may then use the image data in ML applications or ML data models.

6 **[0058]** The machine learning models described herein may be or may implement
7 substantially any type of machine learning to train a model. At least in some cases, the
8 machine learning module may be an inferential model. As used herein, the term “inferential
9 model” may refer to pure statistical models, pure machine learning models, or any
10 combination of statistical and machine learning models. Such inferential models may include
11 neural networks such as recurrent neural networks. In some embodiments, the recurrent
12 neural network may be a long short-term memory (LSTM) neural network. Such recurrent
13 neural networks are not limited to LSTM neural networks, and may have any other suitable
14 architecture. For example, in some embodiments, the neural network may be a fully recurrent
15 neural network, a gated recurrent neural network, a recursive neural network, a Hopfield
16 neural network, an associative memory neural network, an Elman neural network, a Jordan
17 neural network, an echo state neural network, a second order recurrent neural network,
18 and/or any other suitable type of recurrent neural network. In other embodiments, neural
19 networks that are not recurrent neural networks may be used. For example, deep neural
20 networks, convolutional neural networks, and/or feedforward neural networks, may be used.
21 In some implementations, the inferential model may be an unsupervised machine learning
22 model, e.g., where previous data (on which the inferential model was previously trained) is
23 not required. In other cases, the ML models may implement feedback loops to learn and
24 improve over time.

25 **[0059]** As shown in computing environment 600 of FIG. 6, the ML hardware
26 processing components 603 (e.g., ML processing cores 604 of an ML hardware processor) may
27 be configured to perform local processing on a specified portion of an image captured by
28 digital pixel sensors (e.g., on layer one). The ML hardware processing components 603 may
29 include one or more ML processing chips, each of which may include one or more ML
30 processing cores 604. These ML processing cores 604 may receive single images 601 or
31 sequences of images 602 from the digital pixel sensors (e.g., 102 of FIG. 1). The ML hardware
32 processing components 603 may be configured to run smart applications 605, one or more of

1 which may be image processing applications 606. These applications may access the single
2 images 601 or sequences of images 602 and apply some type of ML processing to provide, as
3 an output, one or more processed images 607. In some cases, the ML processing cores 604
4 may share information to perform centralized processing that stitches together the image(s)
5 captured by the digital pixel sensors.

6 **[0060]** In some cases, for example, as shown in embodiment 700 of FIG. 7, an image
7 710 may be divided into different sections. In this example, the image 701 has been divided
8 into four different sections (710A-710D), although substantially any number of sections may
9 be used. The layer two (e.g., 104) image processing components 105 may be configured to
10 divide the image into sections, or the ML image processing applications 606 of the ML
11 hardware processing components 603 on layer three may perform the division of the image
12 into different sections. In FIG. 7, an ML processor 701 has four ML processing cores (e.g., 702-
13 705) and, in this example, each ML processing core receives a corresponding section of the
14 image 710. As such, each ML processing core 702-705 may receive a corresponding portion
15 of an image (or sequence of images). The image processing application 606 may then stitch
16 together the different sections of the image if desired. Alternatively, each ML processing core
17 may perform its own analysis without combining the image sections back together.

18 **[0061]** The ML processor analysis may include a wide variety of tasks, including
19 recognizing objects within images, tracking objects across images, facial recognition, and
20 other tasks. Each ML processing core 702-705 may perform its own individual analysis, or may
21 work in conjunction with one, two, three, or more other ML processing cores to determine,
22 for instance, whether an object has moved between two subsequent image frames. In FIG. 7,
23 for example, ML processing core 704 may receive image section 710C and may identify a
24 person, a portion of a ball, and a portion of a house. ML processing core 705 may recognize a
25 portion of a ball, a different person, and a portion of a house. ML processing cores 702 and
26 703 may similarly identify portions of a house in their corresponding image sections 710A and
27 710B. Each ML processing core may be configured to learn from previous images, and may
28 improve its ability to recognize objects, recognize faces, track objects, etc. Each ML core may
29 implement feedback loops to continually improve at each task performed by a smart
30 application 605.

31 **[0062]** In FIG. 8, three subsequent images 801A, 801B, and 801C may each be divided
32 into four sections. In a manner similar to that shown in FIG. 7, each section may be sent to

1 and analyzed by an ML processing core. In FIG. 8, the ML processing cores may each
2 separately identify objects and track the movement of those objects. For example, ML
3 processing cores 702 and 703 of FIG. 7 may identify portions of a house 802. This house 802
4 does not move between image frames. However, ML processing cores 704 and 705 may
5 identify persons 803 and 805 and a ball 804. These ML processing cores may be configured to
6 track the recognized people and ball across multiple subsequent images. Thus, as the persons
7 803 and 805 move between images 801A-801C, the ML processing cores 704 and 705 may
8 recognize that movement and may track these persons, as well as the ball 804, across the
9 different images.

10 **[0063]** In some cases, the ML processing cores may be configured to track the
11 recognized objects across the subsequent images 801A-801C without neighboring pixel data
12 from other ML processing cores. Thus, for instance, ML processing core 704 may individually
13 recognize and track objects 803 and 804, while ML processing core 705 may individually
14 recognize and track objects 804 and 805 without accessing pixel data from other image
15 sections or from other ML processing cores. In this example, because no changes occur in
16 block 801A & 802, the processing on these image blocks may be skipped, and the
17 corresponding processing cores may be powered down to save energy. Accordingly, each ML
18 processing core may operate individually, and may track the movement of recognized objects
19 until those objects are no longer present in the image. This individual processing may be fed
20 by individual data feeds through dedicated uTSVs at each ML processing core. Each dedicated
21 uTSV may handle the image data for one or more sections of an image. By dividing up an
22 image and then processing each section in parallel on different ML processing cores, the
23 embodiments herein may process images much faster than traditional systems. Moreover,
24 using global memory (e.g., 401A-401D of FIG. 4), ML processing cores may access image data
25 for other image sections, and may, at least in some cases, operate with other ML processing
26 cores to perform a function, including tracking an image across frames. Thus, in the example
27 of FIG. 8, ML processing cores 704 and 705 may work together to track objects 803-805, since
28 those sections of the images are where the movement is occurring. If other objects were
29 moving in other sections, those ML processing cores could, in the same manner, work
30 together to perform a given function.

31 **[0064]** This framework may be implemented for many different functions, including
32 facial recognition, location tracking, or other functions. Moreover, it will be understood that

1 images may be divided into many different sections in different scenarios. For instance, if an
2 ML processor had eight processing cores, images may be divided into eight sections and
3 correspondingly transmitted through eight uTSVs to the eight ML cores, respectively. Still
4 further, some ML cores may have higher processing capacity and may have two, three, or
5 more dedicated uTSVs for data transfer, while other systems may implement a 1:1 ration
6 between uTSVs and ML processing cores. The embodiments described herein may determine
7 the optimal number of uTSVs for each system, to where the uTSV for each ML processing core
8 provides a high enough bandwidth to keep the core fully utilized, but to where there aren't
9 so many uTSVs that processor core space on the ML hardware processor is taken up by uTSV
10 attachment points. This balance includes tradeoffs that may be assessed and determined for
11 each specific digital pixel sensor system.

12 **[0065]** Accordingly, a system may be provided that may increase digital pixel sensor
13 output by implementing uTSVs for different ML processing cores. These uTSVs may provide a
14 sufficiently high bandwidth stream to keep the ML processing cores fully utilized, while taking
15 up a minimal amount of space on the second and third layers of the digital pixel sensor
16 system. Moreover, the ML processing cores may be implemented alone or in conjunction with
17 each other to execute smart applications including machine learning-based image processing
18 applications.

19 **[0066] Example Embodiments**

20 **[0067]** Example 1: A system may include a first layer that includes a plurality of digital
21 pixel sensors configured to detect light, a second layer that includes one or more image
22 processing components configured to process the light detected by the digital pixel sensors,
23 and a third layer that includes one or more machine learning (ML) hardware processing
24 components, where the image processing components of the second layer are
25 communicatively connected to the ML hardware processing components of the third layer via
26 one or more micro through-silicon vias (uTSVs).

27 **[0068]** Example 2: The system of Example 1, wherein the image processing
28 components of the second layer comprise at least one of an analog-to-digital converter (ADC),
29 an encoder, a memory, or a transmitter.

30 **[0069]** Example 3: The system of any of Examples 1 and 2, wherein the ML
31 hardware processing components control capture of consecutive image frames.

32 **[0070]** Example 4: The system of any of Examples 1-3, wherein the ML hardware

1 processing components are configured to execute one or more smart applications.

2 [0071] Example 5: The system of any of Examples 1-4, wherein at least one of the one
3 or more smart applications comprises a smart image processing application.

4 [0072] Example 6: The system of any of Examples 1-5, wherein the ML hardware
5 processing components include a plurality of processing cores.

6 [0073] Example 7: The system of any of Examples 1-6, wherein one or more of the
7 processing cores are configured to perform local processing on a specified portion of an image
8 captured by the plurality of digital pixel sensors.

9 [0074] Example 8: The system of any of Examples 1-7, wherein the ML processing
10 cores share information to perform centralized processing that stitches the image captured
11 by the plurality of digital pixel sensors together.

12 [0075] Example 9: The system of any of Examples 1-8, wherein one or more of the
13 processing cores is configured to recognize one or more objects within a specified region of
14 an image.

15 [0076] Example 10: The system of any of Examples 1-9, wherein one or more of the
16 processing cores is configured to track the one or more recognized objects across a plurality
17 of subsequent images.

18 [0077] Example 11: The system of any of Examples 1-10, wherein the one or more
19 recognized objects are tracked across the plurality of subsequent images without neighboring
20 pixel data from other ML processing cores.

21 [0078] Example 12: The system of any of Examples 1-11, wherein the one or more
22 recognized objects are processed by the same ML processing core until the objects are no
23 longer present in the image.

24 [0079] Example 13: The system of any of Examples 1-12, wherein the one or more
25 recognized objects are processed by a plurality of ML processing cores upon determining that
26 the objects have moved between images.

27 [0080] Example 14: An electronic device may include a first layer that includes a
28 plurality of digital pixel sensors configured to detect light, a second layer that includes one or
29 more image processing components configured to process the light detected by the digital
30 pixel sensors, and a third layer that includes one or more machine learning (ML) hardware
31 processing components, wherein the image processing components of the second layer are
32 communicatively connected to the ML hardware processing components of the third layer via

1 one or more uTSVs.

2 [0081] Example 15: The electronic device of Example 14, wherein the image
3 processing components of the second layer are configured to combine a plurality of image
4 bits into a combined group of image data bits.

5 [0082] Example 16: The electronic device of any of Examples 14 and 15, wherein the
6 combined group of image data bits is transferred as a group to the ML hardware processing
7 components of the third layer through the uTSVs.

8 [0083] Example 17: The electronic device of any of Examples 14-16, wherein the
9 combined group of image data bits is transferred as a group to the ML hardware processing
10 components using time-based multiplexing.

11 [0084] Example 18: The electronic device of any of Examples 14-17, wherein at least
12 one of the ML hardware processing components comprises a local memory buffer.

13 [0085] Example 19: The electronic device of any of Examples 14-18, wherein image
14 data stored in the local memory buffer is processed using a systolic array whose parameters
15 are prestored in the local memory buffer.

16 [0086] Example 20: A method of manufacture may include forming a first layer that
17 includes a plurality of digital pixel sensors configured to detect light, forming a second layer
18 adhered to the first layer that includes one or more image processing components configured
19 to process the light detected by the digital pixel sensors, and forming a third layer adhered to
20 the second layer that includes one or more machine learning (ML) hardware processing
21 components, wherein the image processing components of the second layer are
22 communicatively connected to the ML hardware processing components of the third layer via
23 one or more uTSVs.

24 [0087] The digital pixel sensor systems described herein may be used in a variety of
25 different computing environments, including artificial reality environments. Artificial-reality
26 systems may be implemented in a variety of different form factors and configurations. Some
27 artificial-reality systems may be designed to work without near-eye displays (NEDs). Other
28 artificial-reality systems may include an NED that also provides visibility into the real world
29 (such as, e.g., augmented-reality system 900 in FIG. 9) or that visually immerses a user in an
30 artificial reality (such as, e.g., virtual-reality system 1000 in FIG. 10). While some artificial-
31 reality devices may be self-contained systems, other artificial-reality devices may
32 communicate and/or coordinate with external devices to provide an artificial-reality

1 experience to a user. Examples of such external devices include handheld controllers, mobile
2 devices, desktop computers, devices worn by a user, devices worn by one or more other
3 users, and/or any other suitable external system.

4 **[0088]** Turning to FIG. 9, augmented-reality system 900 may include an eyewear
5 device 902 with a frame 910 configured to hold a left display device 915(A) and a right display
6 device 915(B) in front of a user's eyes. Display devices 915(A) and 915(B) may act together or
7 independently to present an image or series of images to a user. While augmented-reality
8 system 900 includes two displays, embodiments of this disclosure may be implemented in
9 augmented-reality systems with a single NED or more than two NEDs.

10 **[0089]** In some embodiments, augmented-reality system 900 may include one or
11 more sensors, such as sensor 940. Sensor 940 may generate measurement signals in response
12 to motion of augmented-reality system 900 and may be located on substantially any portion
13 of frame 910. Sensor 940 may represent one or more of a variety of different sensing
14 mechanisms, such as a position sensor, an inertial measurement unit (IMU), a depth camera
15 assembly, a structured light emitter and/or detector, or any combination thereof. In some
16 embodiments, augmented-reality system 900 may or may not include sensor 940 or may
17 include more than one sensor. In embodiments in which sensor 940 includes an IMU, the IMU
18 may generate calibration data based on measurement signals from sensor 940. Examples of
19 sensor 940 may include, without limitation, accelerometers, gyroscopes, magnetometers,
20 other suitable types of sensors that detect motion, sensors used for error correction of the
21 IMU, or some combination thereof.

22 **[0090]** In some examples, augmented-reality system 900 may also include a
23 microphone array with a plurality of acoustic transducers 920(A)-920(J), referred to
24 collectively as acoustic transducers 920. Acoustic transducers 920 may represent transducers
25 that detect air pressure variations induced by sound waves. Each acoustic transducer 920 may
26 be configured to detect sound and convert the detected sound into an electronic format (e.g.,
27 an analog or digital format). The microphone array in FIG. 9 may include, for example, ten
28 acoustic transducers: 920(A) and 920(B), which may be designed to be placed inside a
29 corresponding ear of the user, acoustic transducers 920(C), 920(D), 920(E), 920(F), 920(G),
30 and 920(H), which may be positioned at various locations on frame 910, and/or acoustic
31 transducers 920(I) and 920(J), which may be positioned on a corresponding neckband 905.

32 **[0091]** In some embodiments, one or more of acoustic transducers 920(A)-(J) may be

1 used as output transducers (e.g., speakers). For example, acoustic transducers 920(A) and/or
2 920(B) may be earbuds or any other suitable type of headphone or speaker.

3 **[0092]** The configuration of acoustic transducers 920 of the microphone array may
4 vary. While augmented-reality system 900 is shown in FIG. 9 as having ten acoustic
5 transducers 920, the number of acoustic transducers 920 may be greater or less than ten. In
6 some embodiments, using higher numbers of acoustic transducers 920 may increase the
7 amount of audio information collected and/or the sensitivity and accuracy of the audio
8 information. In contrast, using a lower number of acoustic transducers 920 may decrease the
9 computing power required by an associated controller 950 to process the collected audio
10 information. In addition, the position of each acoustic transducer 920 of the microphone array
11 may vary. For example, the position of an acoustic transducer 920 may include a defined
12 position on the user, a defined coordinate on frame 910, an orientation associated with each
13 acoustic transducer 920, or some combination thereof.

14 **[0093]** Acoustic transducers 920(A) and 920(B) may be positioned on different parts
15 of the user's ear, such as behind the pinna, behind the tragus, and/or within the auricle or
16 fossa. Or, there may be additional acoustic transducers 920 on or surrounding the ear in
17 addition to acoustic transducers 920 inside the ear canal. Having an acoustic transducer 920
18 positioned next to an ear canal of a user may enable the microphone array to collect
19 information on how sounds arrive at the ear canal. By positioning at least two of acoustic
20 transducers 920 on either side of a user's head (e.g., as binaural microphones), augmented-
21 reality device 900 may simulate binaural hearing and capture a 3D stereo sound field around
22 about a user's head. In some embodiments, acoustic transducers 920(A) and 920(B) may be
23 connected to augmented-reality system 900 via a wired connection 930, and in other
24 embodiments acoustic transducers 920(A) and 920(B) may be connected to augmented-
25 reality system 900 via a wireless connection (e.g., a Bluetooth connection). In still other
26 embodiments, acoustic transducers 920(A) and 920(B) may not be used at all in conjunction
27 with augmented-reality system 900.

28 **[0094]** Acoustic transducers 920 on frame 910 may be positioned in a variety of
29 different ways, including along the length of the temples, across the bridge, above or below
30 display devices 915(A) and 915(B), or some combination thereof. Acoustic transducers 920
31 may also be oriented such that the microphone array is able to detect sounds in a wide range
32 of directions surrounding the user wearing the augmented-reality system 900. In some

1 embodiments, an optimization process may be performed during manufacturing of
2 augmented-reality system 900 to determine relative positioning of each acoustic transducer
3 920 in the microphone array.

4 **[0095]** In some examples, augmented-reality system 900 may include or be connected
5 to an external device (e.g., a paired device), such as neckband 905. Neckband 905 generally
6 represents any type or form of paired device. Thus, the following discussion of neckband 905
7 may also apply to various other paired devices, such as charging cases, smart watches, smart
8 phones, wrist bands, other wearable devices, hand-held controllers, tablet computers, laptop
9 computers, other external compute devices, etc.

10 **[0096]** As shown, neckband 905 may be coupled to eyewear device 902 via one or
11 more connectors. The connectors may be wired or wireless and may include electrical and/or
12 non-electrical (e.g., structural) components. In some cases, eyewear device 902 and neckband
13 905 may operate independently without any wired or wireless connection between them.
14 While FIG. 9 illustrates the components of eyewear device 902 and neckband 905 in example
15 locations on eyewear device 902 and neckband 905, the components may be located
16 elsewhere and/or distributed differently on eyewear device 902 and/or neckband 905. In
17 some embodiments, the components of eyewear device 902 and neckband 905 may be
18 located on one or more additional peripheral devices paired with eyewear device 902,
19 neckband 905, or some combination thereof.

20 **[0097]** Pairing external devices, such as neckband 905, with augmented-reality
21 eyewear devices may enable the eyewear devices to achieve the form factor of a pair of
22 glasses while still providing sufficient battery and computation power for expanded
23 capabilities. Some or all of the battery power, computational resources, and/or additional
24 features of augmented-reality system 900 may be provided by a paired device or shared
25 between a paired device and an eyewear device, thus reducing the weight, heat profile, and
26 form factor of the eyewear device overall while still retaining desired functionality. For
27 example, neckband 905 may allow components that would otherwise be included on an
28 eyewear device to be included in neckband 905 since users may tolerate a heavier weight
29 load on their shoulders than they would tolerate on their heads. Neckband 905 may also have
30 a larger surface area over which to diffuse and disperse heat to the ambient environment.
31 Thus, neckband 905 may allow for greater battery and computation capacity than might
32 otherwise have been possible on a stand-alone eyewear device. Since weight carried in

neckband 905 may be less invasive to a user than weight carried in eyewear device 902, a user may tolerate wearing a lighter eyewear device and carrying or wearing the paired device for greater lengths of time than a user would tolerate wearing a heavy standalone eyewear device, thereby enabling users to more fully incorporate artificial-reality environments into their day-to-day activities.

[0098] Neckband 905 may be communicatively coupled with eyewear device 902 and/or to other devices. These other devices may provide certain functions (e.g., tracking, localizing, depth mapping, processing, storage, etc.) to augmented-reality system 900. In the embodiment of FIG. 9, neckband 905 may include two acoustic transducers (e.g., 920(I) and 920(J)) that are part of the microphone array (or potentially form their own microphone subarray). Neckband 905 may also include a controller 925 and a power source 935.

[0099] Acoustic transducers 920(I) and 920(J) of neckband 905 may be configured to detect sound and convert the detected sound into an electronic format (analog or digital). In the embodiment of FIG. 9, acoustic transducers 920(I) and 920(J) may be positioned on neckband 905, thereby increasing the distance between the neckband acoustic transducers 920(I) and 920(J) and other acoustic transducers 920 positioned on eyewear device 902. In some cases, increasing the distance between acoustic transducers 920 of the microphone array may improve the accuracy of beamforming performed via the microphone array. For example, if a sound is detected by acoustic transducers 920(C) and 920(D) and the distance between acoustic transducers 920(C) and 920(D) is greater than, e.g., the distance between acoustic transducers 920(D) and 920(E), the determined source location of the detected sound may be more accurate than if the sound had been detected by acoustic transducers 920(D) and 920(E).

[0100] Controller 925 of neckband 905 may process information generated by the sensors on neckband 905 and/or augmented-reality system 900. For example, controller 925 may process information from the microphone array that describes sounds detected by the microphone array. For each detected sound, controller 925 may perform a direction-of-arrival (DOA) estimation to estimate a direction from which the detected sound arrived at the microphone array. As the microphone array detects sounds, controller 925 may populate an audio data set with the information. In embodiments in which augmented-reality system 900 includes an inertial measurement unit, controller 925 may compute all inertial and spatial calculations from the IMU located on eyewear device 902. A connector may convey

1 information between augmented-reality system 900 and neckband 905 and between
2 augmented-reality system 900 and controller 925. The information may be in the form of
3 optical data, electrical data, wireless data, or any other transmittable data form. Moving the
4 processing of information generated by augmented-reality system 900 to neckband 905 may
5 reduce weight and heat in eyewear device 902, making it more comfortable to the user.

6 **[0101]** Power source 935 in neckband 905 may provide power to eyewear device 902
7 and/or to neckband 905. Power source 935 may include, without limitation, lithium ion
8 batteries, lithium-polymer batteries, primary lithium batteries, alkaline batteries, or any other
9 form of power storage. In some cases, power source 935 may be a wired power source.
10 Including power source 935 on neckband 905 instead of on eyewear device 902 may help
11 better distribute the weight and heat generated by power source 935.

12 **[0102]** As noted, some artificial-reality systems may, instead of blending an artificial
13 reality with actual reality, substantially replace one or more of a user's sensory perceptions
14 of the real world with a virtual experience. One example of this type of system is a head-worn
15 display system, such as virtual-reality system 1000 in FIG. 10, that mostly or completely covers
16 a user's field of view. Virtual-reality system 1000 may include a front rigid body 1002 and a
17 band 1004 shaped to fit around a user's head. Virtual-reality system 1000 may also include
18 output audio transducers 1006(A) and 1006(B). Furthermore, while not shown in FIG. 10,
19 front rigid body 1002 may include one or more electronic elements, including one or more
20 electronic displays, one or more inertial measurement units (IMUs), one or more tracking
21 emitters or detectors, and/or any other suitable device or system for creating an artificial-
22 reality experience.

23 **[0103]** Artificial-reality systems may include a variety of types of visual feedback
24 mechanisms. For example, display devices in augmented-reality system 900 and/or virtual-
25 reality system 1000 may include one or more liquid crystal displays (LCDs), light emitting diode
26 (LED) displays, organic LED (OLED) displays, digital light project (DLP) micro-displays, liquid
27 crystal on silicon (LCoS) micro-displays, and/or any other suitable type of display screen.
28 These artificial-reality systems may include a single display screen for both eyes or may
29 provide a display screen for each eye, which may allow for additional flexibility for varifocal
30 adjustments or for correcting a user's refractive error. Some of these artificial-reality systems
31 may also include optical subsystems having one or more lenses (e.g., conventional concave
32 or convex lenses, Fresnel lenses, adjustable liquid lenses, etc.) through which a user may view

1 a display screen. These optical subsystems may serve a variety of purposes, including to
2 collimate (e.g., make an object appear at a greater distance than its physical distance), to
3 magnify (e.g., make an object appear larger than its actual size), and/or to relay (to, e.g., the
4 viewer's eyes) light. These optical subsystems may be used in a non-pupil-forming
5 architecture (such as a single lens configuration that directly collimates light but results in so-
6 called pincushion distortion) and/or a pupil-forming architecture (such as a multi-lens
7 configuration that produces so-called barrel distortion to nullify pincushion distortion).

8 **[0104]** In addition to or instead of using display screens, some of the artificial-reality
9 systems described herein may include one or more projection systems. For example, display
10 devices in augmented-reality system 900 and/or virtual-reality system 1000 may include
11 micro-LED projectors that project light (using, e.g., a waveguide) into display devices, such as
12 clear combiner lenses that allow ambient light to pass through. The display devices may
13 refract the projected light toward a user's pupil and may enable a user to simultaneously view
14 both artificial-reality content and the real world. The display devices may accomplish this
15 using any of a variety of different optical components, including waveguide components (e.g.,
16 holographic, planar, diffractive, polarized, and/or reflective waveguide elements), light-
17 manipulation surfaces and elements (such as diffractive, reflective, and refractive elements
18 and gratings), coupling elements, etc. Artificial-reality systems may also be configured with
19 any other suitable type or form of image projection system, such as retinal projectors used in
20 virtual retina displays.

21 **[0105]** The artificial-reality systems described herein may also include various types
22 of computer vision components and subsystems. For example, augmented-reality system 900
23 and/or virtual-reality system 1000 may include one or more optical sensors, such as two-
24 dimensional (2D) or 3D cameras, structured light transmitters and detectors, time-of-flight
25 depth sensors, single-beam or sweeping laser rangefinders, 3D LiDAR sensors, and/or any
26 other suitable type or form of optical sensor. An artificial-reality system may process data
27 from one or more of these sensors to identify a location of a user, to map the real world, to
28 provide a user with context about real-world surroundings, and/or to perform a variety of
29 other functions.

30 **[0106]** The artificial-reality systems described herein may also include one or more
31 input and/or output audio transducers. Output audio transducers may include voice coil
32 speakers, ribbon speakers, electrostatic speakers, piezoelectric speakers, bone conduction

1 transducers, cartilage conduction transducers, tragus-vibration transducers, and/or any other
2 suitable type or form of audio transducer. Similarly, input audio transducers may include
3 condenser microphones, dynamic microphones, ribbon microphones, and/or any other type
4 or form of input transducer. In some embodiments, a single transducer may be used for both
5 audio input and audio output.

6 **[0107]** In some embodiments, the artificial-reality systems described herein may also
7 include tactile (i.e., haptic) feedback systems, which may be incorporated into headwear,
8 gloves, body suits, handheld controllers, environmental devices (e.g., chairs, floormats, etc.),
9 and/or any other type of device or system. Haptic feedback systems may provide various
10 types of cutaneous feedback, including vibration, force, traction, texture, and/or
11 temperature. Haptic feedback systems may also provide various types of kinesthetic
12 feedback, such as motion and compliance. Haptic feedback may be implemented using
13 motors, piezoelectric actuators, fluidic systems, and/or a variety of other types of feedback
14 mechanisms. Haptic feedback systems may be implemented independent of other
15 artificial-reality devices, within other artificial-reality devices, and/or in conjunction with
16 other artificial-reality devices.

17 **[0108]** By providing haptic sensations, audible content, and/or visual content,
18 artificial-reality systems may create an entire virtual experience or enhance a user's real-
19 world experience in a variety of contexts and environments. For instance, artificial-reality
20 systems may assist or extend a user's perception, memory, or cognition within a particular
21 environment. Some systems may enhance a user's interactions with other people in the real
22 world or may enable more immersive interactions with other people in a virtual world.
23 Artificial-reality systems may also be used for educational purposes (e.g., for teaching or
24 training in schools, hospitals, government organizations, military organizations, business
25 enterprises, etc.), entertainment purposes (e.g., for playing video games, listening to music,
26 watching video content, etc.), and/or for accessibility purposes (e.g., as hearing aids, visual
27 aids, etc.). The embodiments disclosed herein may enable or enhance a user's artificial-reality
28 experience in one or more of these contexts and environments and/or in other contexts and
29 environments.

30 **[0109]** As noted, augmented-reality systems 900 and 1000 may be used with a variety
31 of other types of devices to provide a more compelling artificial-reality experience. These
32 devices may be haptic interfaces with transducers that provide haptic feedback and/or that

1 collect haptic information about a user's interaction with an environment. The artificial-reality
2 systems disclosed herein may include various types of haptic interfaces that detect or convey
3 various types of haptic information, including tactile feedback (e.g., feedback that a user
4 detects via nerves in the skin, which may also be referred to as cutaneous feedback) and/or
5 kinesthetic feedback (e.g., feedback that a user detects via receptors located in muscles,
6 joints, and/or tendons).

7 **[0110]** Haptic feedback may be provided by interfaces positioned within a user's
8 environment (e.g., chairs, tables, floors, etc.) and/or interfaces on articles that may be worn
9 or carried by a user (e.g., gloves, wristbands, etc.). As an example, FIG. 11 illustrates a
10 vibrotactile system 1100 in the form of a wearable glove (haptic device 1110) and wristband
11 (haptic device 1120). Haptic device 1110 and haptic device 1120 are shown as examples of
12 wearable devices that include a flexible, wearable textile material 1130 that is shaped and
13 configured for positioning against a user's hand and wrist, respectively. This disclosure also
14 includes vibrotactile systems that may be shaped and configured for positioning against other
15 human body parts, such as a finger, an arm, a head, a torso, a foot, or a leg. By way of example
16 and not limitation, vibrotactile systems according to various embodiments of the present
17 disclosure may also be in the form of a glove, a headband, an armband, a sleeve, a head
18 covering, a sock, a shirt, or pants, among other possibilities. In some examples, the term
19 "textile" may include any flexible, wearable material, including woven fabric, non-woven
20 fabric, leather, cloth, a flexible polymer material, composite materials, etc.

21 **[0111]** One or more vibrotactile devices 1140 may be positioned at least partially
22 within one or more corresponding pockets formed in textile material 1130 of vibrotactile
23 system 1100. Vibrotactile devices 1140 may be positioned in locations to provide a vibrating
24 sensation (e.g., haptic feedback) to a user of vibrotactile system 1100. For example,
25 vibrotactile devices 1140 may be positioned against the user's finger(s), thumb, or wrist, as
26 shown in FIG. 11. Vibrotactile devices 1140 may, in some examples, be sufficiently flexible to
27 conform to or bend with the user's corresponding body part(s).

28 **[0112]** A power source 1150 (e.g., a battery) for applying a voltage to the vibrotactile
29 devices 1140 for activation thereof may be electrically coupled to vibrotactile devices 1140,
30 such as via conductive wiring 1152. In some examples, each of vibrotactile devices 1140 may
31 be independently electrically coupled to power source 1150 for individual activation. In some
32 embodiments, a processor 1160 may be operatively coupled to power source 1150 and

1 configured (e.g., programmed) to control activation of vibrotactile devices 1140.

2 [0113] Vibrotactile system 1100 may be implemented in a variety of ways. In some
3 examples, vibrotactile system 1100 may be a standalone system with integral subsystems and
4 components for operation independent of other devices and systems. As another example,
5 vibrotactile system 1100 may be configured for interaction with another device or system
6 1170. For example, vibrotactile system 1100 may, in some examples, include a
7 communications interface 1180 for receiving and/or sending signals to the other device or
8 system 1170. The other device or system 1170 may be a mobile device, a gaming console, an
9 artificial-reality (e.g., virtual-reality, augmented-reality, mixed-reality) device, a personal
10 computer, a tablet computer, a network device (e.g., a modem, a router, etc.), a handheld
11 controller, etc. Communications interface 1180 may enable communications between
12 vibrotactile system 1100 and the other device or system 1170 via a wireless (e.g., Wi-Fi,
13 Bluetooth, cellular, radio, etc.) link or a wired link. If present, communications interface 1180
14 may be in communication with processor 1160, such as to provide a signal to processor 1160
15 to activate or deactivate one or more of the vibrotactile devices 1140.

16 [0114] Vibrotactile system 1100 may optionally include other subsystems and
17 components, such as touch-sensitive pads 1190, pressure sensors, motion sensors, position
18 sensors, lighting elements, and/or user interface elements (e.g., an on/off button, a vibration
19 control element, etc.). During use, vibrotactile devices 1140 may be configured to be
20 activated for a variety of different reasons, such as in response to the user's interaction with
21 user interface elements, a signal from the motion or position sensors, a signal from the touch-
22 sensitive pads 1190, a signal from the pressure sensors, a signal from the other device or
23 system 1170, etc.

24 [0115] Although power source 1150, processor 1160, and communications
25 interface 1180 are illustrated in FIG. 11 as being positioned in haptic device 1120, the present
26 disclosure is not so limited. For example, one or more of power source 1150, processor 1160,
27 or communications interface 1180 may be positioned within haptic device 1110 or within
28 another wearable textile.

29 [0116] Haptic wearables, such as those shown in and described in connection with
30 FIG. 11, may be implemented in a variety of types of artificial-reality systems and
31 environments. FIG. 12 shows an example artificial-reality environment 1200 including one
32 head-mounted virtual-reality display and two haptic devices (i.e., gloves), and in other

embodiments any number and/or combination of these components and other components may be included in an artificial-reality system. For example, in some embodiments there may be multiple head-mounted displays each having an associated haptic device, with each head-mounted display and each haptic device communicating with the same console, portable computing device, or other computing system.

[0117] Head-mounted display 1202 generally represents any type or form of virtual-reality system, such as virtual-reality system 1000 in FIG. 10. Haptic device 1204 generally represents any type or form of wearable device, worn by a user of an artificial-reality system, that provides haptic feedback to the user to give the user the perception that he or she is physically engaging with a virtual object. In some embodiments, haptic device 1204 may provide haptic feedback by applying vibration, motion, and/or force to the user. For example, haptic device 1204 may limit or augment a user's movement. To give a specific example, haptic device 1204 may limit a user's hand from moving forward so that the user has the perception that his or her hand has come in physical contact with a virtual wall. In this specific example, one or more actuators within the haptic device may achieve the physical-movement restriction by pumping fluid into an inflatable bladder of the haptic device. In some examples, a user may also use haptic device 1204 to send action requests to a console. Examples of action requests include, without limitation, requests to start an application and/or end the application and/or requests to perform a particular action within the application.

[0118] While haptic interfaces may be used with virtual-reality systems, as shown in FIG. 12, haptic interfaces may also be used with augmented-reality systems, as shown in FIG. 13. FIG. 13 is a perspective view of a user 1310 interacting with an augmented-reality system 1300. In this example, user 1310 may wear a pair of augmented-reality glasses 1320 that may have one or more displays 1322 and that are paired with a haptic device 1330. In this example, haptic device 1330 may be a wristband that includes a plurality of band elements 1332 and a tensioning mechanism 1334 that connects band elements 1332 to one another.

[0119] One or more of band elements 1332 may include any type or form of actuator suitable for providing haptic feedback. For example, one or more of band elements 1332 may be configured to provide one or more of various types of cutaneous feedback, including vibration, force, traction, texture, and/or temperature. To provide such feedback, band elements 1332 may include one or more of various types of actuators. In one example, each of band elements 1332 may include a vibrotactor (e.g., a vibrotactile actuator) configured to

1 vibrate in unison or independently to provide one or more of various types of haptic
2 sensations to a user. Alternatively, only a single band element or a subset of band elements
3 may include vibrotactors.

4 **[0120]** Haptic devices 1110, 1120, 1204, and 1330 may include any suitable number
5 and/or type of haptic transducer, sensor, and/or feedback mechanism. For example, haptic
6 devices 1110, 1120, 1204, and 1330 may include one or more mechanical transducers,
7 piezoelectric transducers, and/or fluidic transducers. Haptic devices 1110, 1120, 1204, and
8 1330 may also include various combinations of different types and forms of transducers that
9 work together or independently to enhance a user's artificial-reality experience. In one
10 example, each of band elements 1332 of haptic device 1330 may include a vibrotactor (e.g.,
11 a vibrotactile actuator) configured to vibrate in unison or independently to provide one or
12 more of various types of haptic sensations to a user.

13 **[0121]** As detailed above, the computing devices and systems described and/or
14 illustrated herein broadly represent any type or form of computing device or system capable
15 of executing computer-readable instructions, such as those contained within the modules
16 described herein. In their most basic configuration, these computing device(s) may each
17 include at least one memory device and at least one physical processor.

18 **[0122]** In some examples, the term "memory device" generally refers to any type or
19 form of volatile or non-volatile storage device or medium capable of storing data and/or
20 computer-readable instructions. In one example, a memory device may store, load, and/or
21 maintain one or more of the modules described herein. Examples of memory devices include,
22 without limitation, Random Access Memory (RAM), Read Only Memory (ROM), flash memory,
23 Hard Disk Drives (HDDs), Solid-State Drives (SSDs), optical disk drives, caches, variations or
24 combinations of one or more of the same, or any other suitable storage memory.

25 **[0123]** In some examples, the term "physical processor" generally refers to any type
26 or form of hardware-implemented processing unit capable of interpreting and/or executing
27 computer-readable instructions. In one example, a physical processor may access and/or
28 modify one or more modules stored in the above-described memory device. Examples of
29 physical processors include, without limitation, microprocessors, microcontrollers, Central
30 Processing Units (CPUs), Field-Programmable Gate Arrays (FPGAs) that implement softcore
31 processors, Application-Specific Integrated Circuits (ASICs), portions of one or more of the
32 same, variations or combinations of one or more of the same, or any other suitable physical

1 processor.

2 [0124] Although illustrated as separate elements, the modules described and/or
3 illustrated herein may represent portions of a single module or application. In addition, in
4 certain embodiments one or more of these modules may represent one or more software
5 applications or programs that, when executed by a computing device, may cause the
6 computing device to perform one or more tasks. For example, one or more of the modules
7 described and/or illustrated herein may represent modules stored and configured to run on
8 one or more of the computing devices or systems described and/or illustrated herein. One or
9 more of these modules may also represent all or portions of one or more special-purpose
10 computers configured to perform one or more tasks.

11 [0125] In addition, one or more of the modules described herein may transform data,
12 physical devices, and/or representations of physical devices from one form to another. For
13 example, one or more of the modules recited herein may receive data to be transformed,
14 transform the data, output a result of the transformation to form a first layer, use the result
15 of the transformation to form second and third layers, and store the result of the
16 transformation to manufacture a multi-layered electronic device. Additionally or
17 alternatively, one or more of the modules recited herein may transform a processor, volatile
18 memory, non-volatile memory, and/or any other portion of a physical computing device from
19 one form to another by executing on the computing device, storing data on the computing
20 device, and/or otherwise interacting with the computing device.

21 [0126] In some embodiments, the term “computer-readable medium” generally
22 refers to any form of device, carrier, or medium capable of storing or carrying computer-
23 readable instructions. Examples of computer-readable media include, without limitation,
24 transmission-type media, such as carrier waves, and non-transitory-type media, such as
25 magnetic-storage media (e.g., hard disk drives, tape drives, and floppy disks), optical-storage
26 media (e.g., Compact Disks (CDs), Digital Video Disks (DVDs), and BLU-RAY disks), electronic-
27 storage media (e.g., solid-state drives and flash media), and other distribution systems.

28 [0127] The process parameters and sequence of the steps described and/or
29 illustrated herein are given by way of example only and can be varied as desired. For example,
30 while the steps illustrated and/or described herein may be shown or discussed in a particular
31 order, these steps do not necessarily need to be performed in the order illustrated or
32 discussed. The various exemplary methods described and/or illustrated herein may also omit

1 one or more of the steps described or illustrated herein or include additional steps in addition
2 to those disclosed.

3 **[0128]** The preceding description has been provided to enable others skilled in the art
4 to best utilize various aspects of the exemplary embodiments disclosed herein. This
5 exemplary description is not intended to be exhaustive or to be limited to any precise form
6 disclosed. Many modifications and variations are possible without departing from the scope
7 of the present disclosure. The embodiments disclosed herein should be considered in all
8 respects illustrative and not restrictive. Reference should be made to the appended claims
9 and their equivalents in determining the scope of the present disclosure.

10 **[0129]** Unless otherwise noted, the terms “connected to” and “coupled to” (and their
11 derivatives), as used in the specification and claims, are to be construed as permitting both
12 direct and indirect (i.e., via other elements or components) connection. In addition, the terms
13 “a” or “an,” as used in the specification and claims, are to be construed as meaning “at least
14 one of.” Finally, for ease of use, the terms “including” and “having” (and their derivatives), as
15 used in the specification and claims, are interchangeable with and have the same meaning as
16 the word “comprising.”

17

1 CLAIMS:

- 2 1. A system comprising:
3 a first layer that includes a plurality of digital pixel sensors configured to detect light;
4 a second layer that includes one or more image processing components configured to
5 process the light detected by the digital pixel sensors; and
6 a third layer that includes one or more machine learning (ML) hardware processing
7 components, wherein the image processing components of the second layer are
8 communicatively connected to the ML hardware processing components of the third layer via
9 one or more micro through-silicon vias (uTSVs).
- 10 2. The system of claim 1, wherein the image processing components of the
11 second layer comprise at least one of an analog-to-digital converter (ADC), an encoder, a
12 memory, or a transmitter.
- 13 3. The system of claim 1 or claim 2, wherein the ML hardware processing
14 components control capture of consecutive image frames.
- 15 4. The system of any preceding claim, wherein the ML hardware processing
16 components are configured to execute one or more smart applications; and preferably
17 wherein at least one of the one or more smart applications comprises a smart image
18 processing application.
- 19 5. The system of any preceding claim, wherein the ML hardware processing
20 components include a plurality of processing cores.
- 21 6. The system of claim 5, wherein one or more of the processing cores are
22 configured to perform local processing on a specified portion of an image captured by the
23 plurality of digital pixel sensors.
- 24 7. The system of claim 6, wherein the ML processing cores share information to
25 perform centralized processing that stitches the image captured by the plurality of digital pixel
26 sensors together.
- 27 8. The system of claim 5, wherein one or more of the processing cores is
28 configured to recognize one or more objects within a specified region of an image; and
29 preferably wherein one or more of the processing cores is configured to track the one or more
30 recognized objects across a plurality of subsequent images.
- 31 9. The system of claim 8, wherein the one or more recognized objects are tracked
32 across the plurality of subsequent images without neighboring pixel data from other ML

1 processing cores.

2 10. The system of claim 8 or claim 9, wherein the one or more recognized objects
3 are processed by the same ML processing core until the objects are no longer present in the
4 image.

5 11. The system of any of claims 8 to 10, wherein the one or more recognized
6 objects are processed by a plurality of ML processing cores upon determining that the objects
7 have moved between images.

8 12. An electronic device comprising:

9 a first layer that includes a plurality of digital pixel sensors configured to detect light;

10 a second layer that includes one or more image processing components configured to
11 process the light detected by the digital pixel sensors; and

12 a third layer that includes one or more machine learning (ML) hardware processing
13 components, wherein the image processing components of the second layer are
14 communicatively connected to the ML hardware processing components of the third layer via
15 one or more uTSVs.

16 13. The electronic device of claim 12, wherein the image processing components
17 of the second layer are configured to combine a plurality of image bits into a combined group
18 of image data bits; and preferably wherein the combined group of image data bits is
19 transferred as a group to the ML hardware processing components of the third layer through
20 the uTSVs; or preferably wherein the combined group of image data bits is transferred as a
21 group to the ML hardware processing components using time-based multiplexing.

22 14. The electronic device of claim 12 or claim 13, wherein at least one of the ML
23 hardware processing components comprises a local memory buffer; and preferably wherein
24 image data stored in the local memory buffer is processed using a systolic array whose
25 parameters are prestored in the local memory buffer.

26 15. A method of manufacture comprising:

27 forming a first layer that includes a plurality of digital pixel sensors configured to
28 detect light;

29 forming a second layer adhered to the first layer that includes one or more image
30 processing components configured to process the light detected by the digital pixel sensors;
31 and

32 forming a third layer adhered to the second layer that includes one or more machine

1 learning (ML) hardware processing components, wherein the image processing components
2 of the second layer are communicatively connected to the ML hardware processing
3 components of the third layer via one or more uTSVs.
4

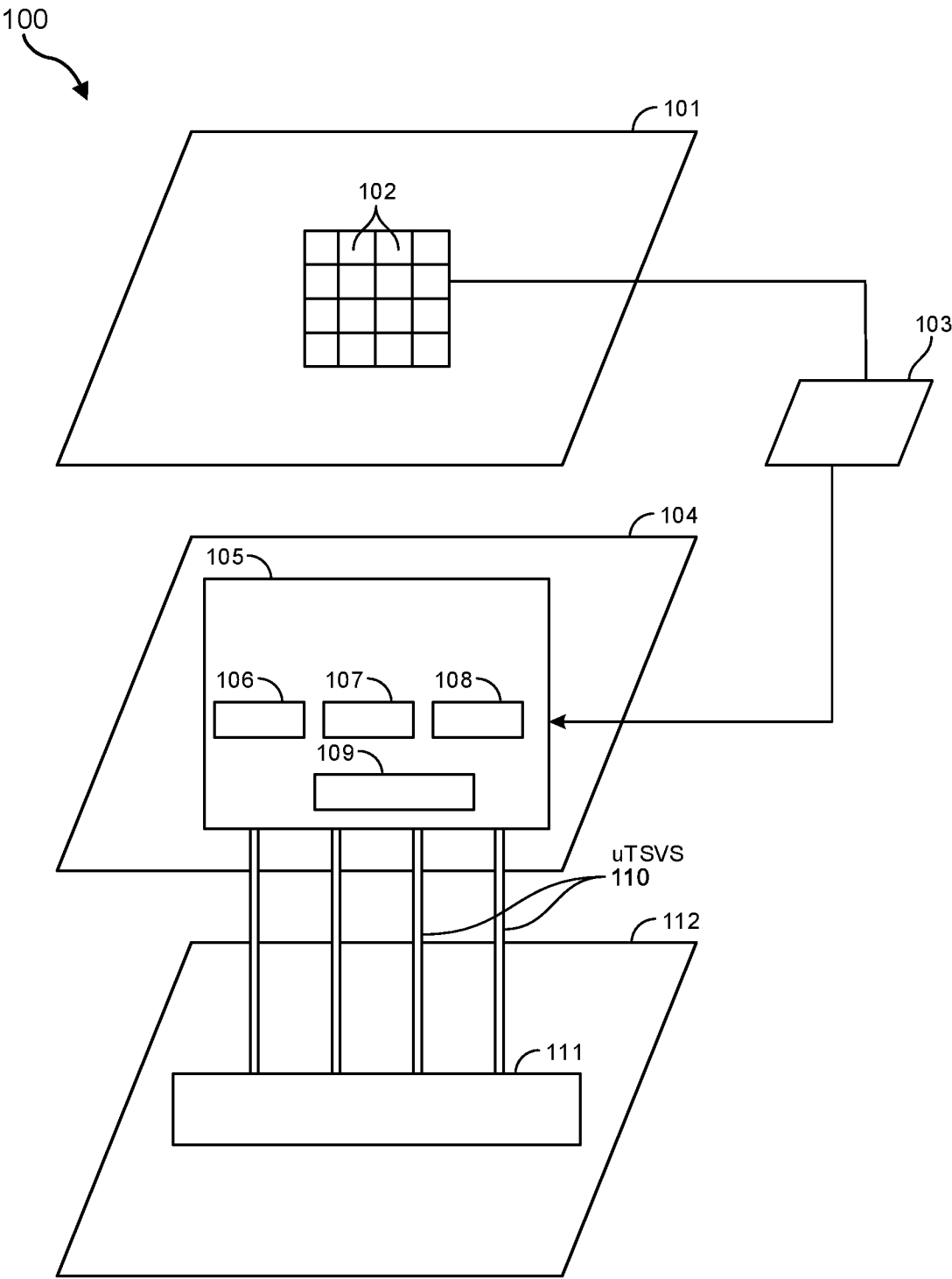


FIG. 1

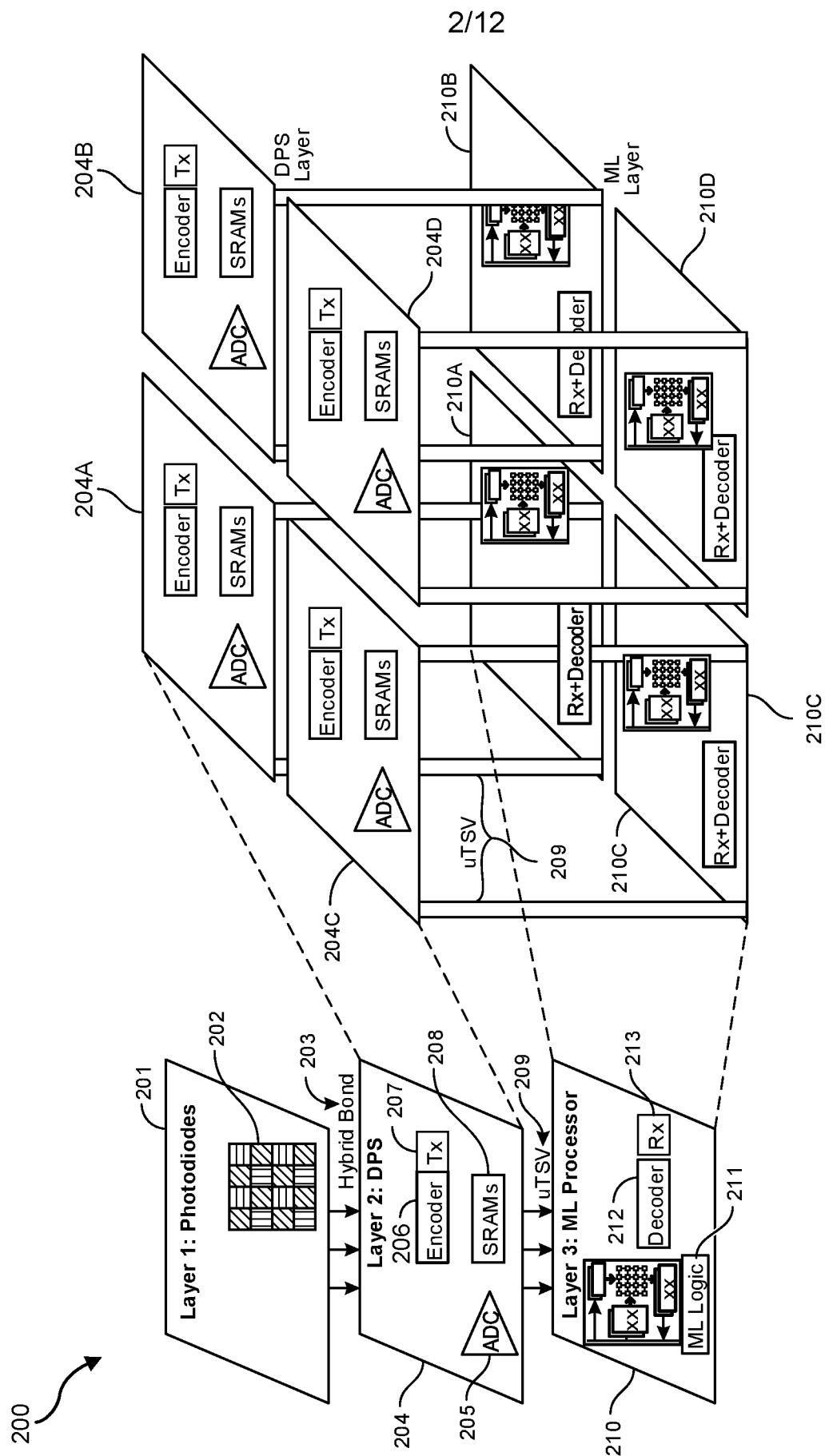


FIG. 2

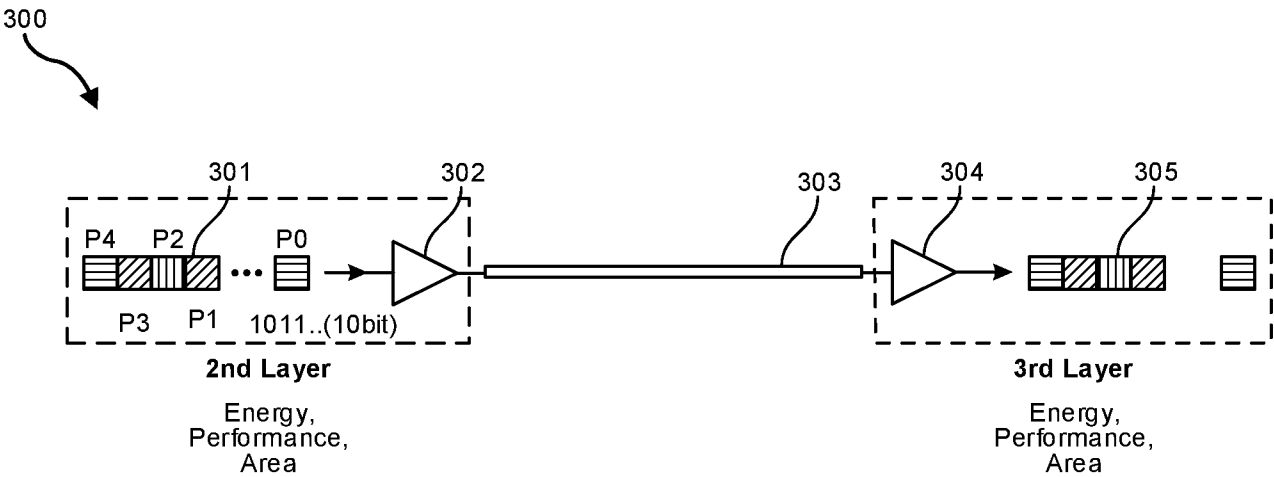


FIG. 3

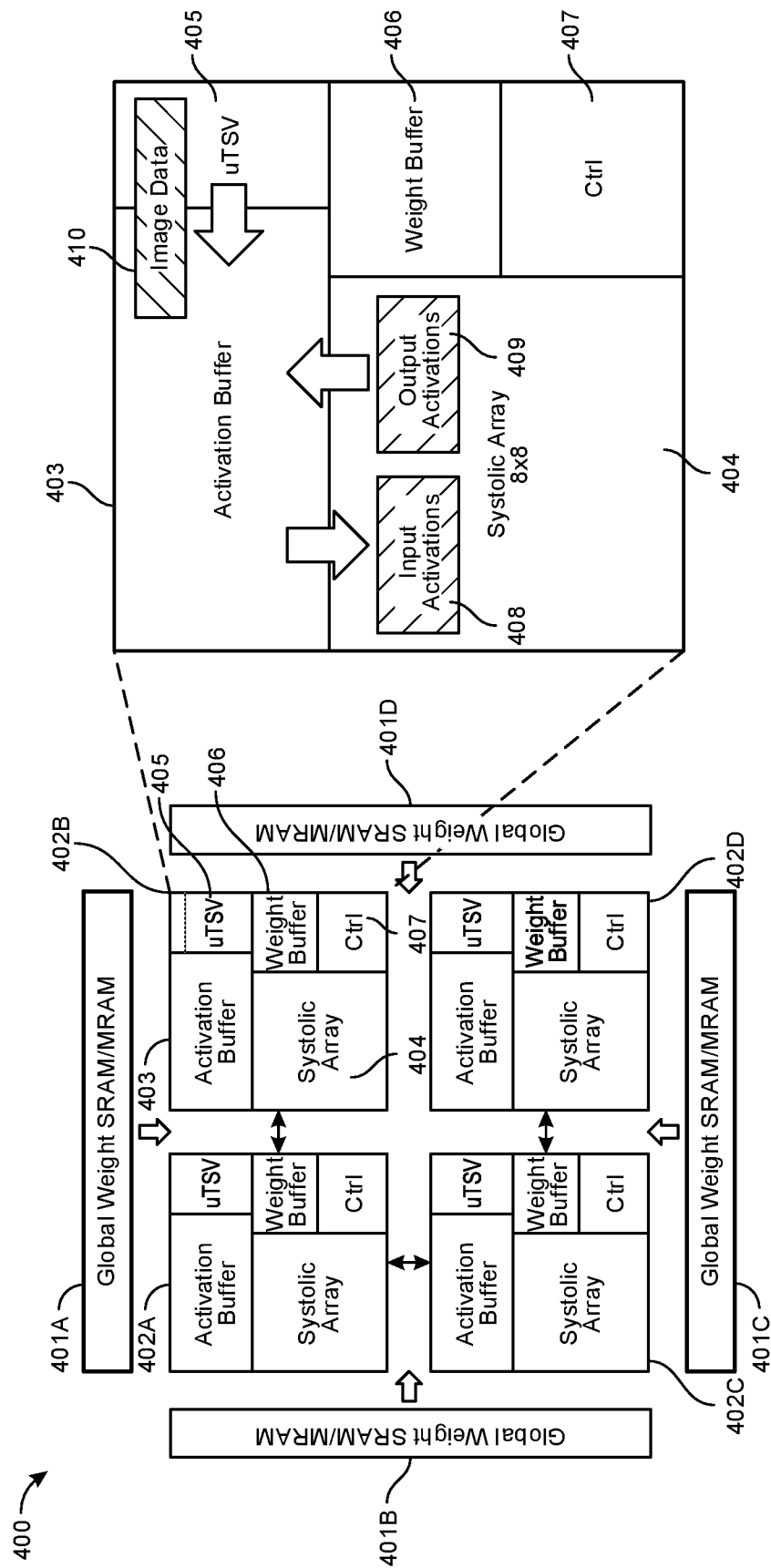


FIG. 4

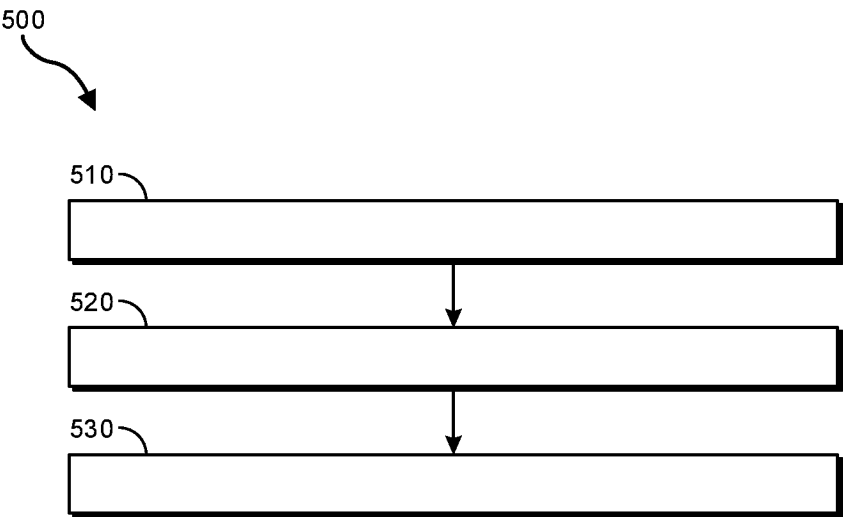


FIG. 5

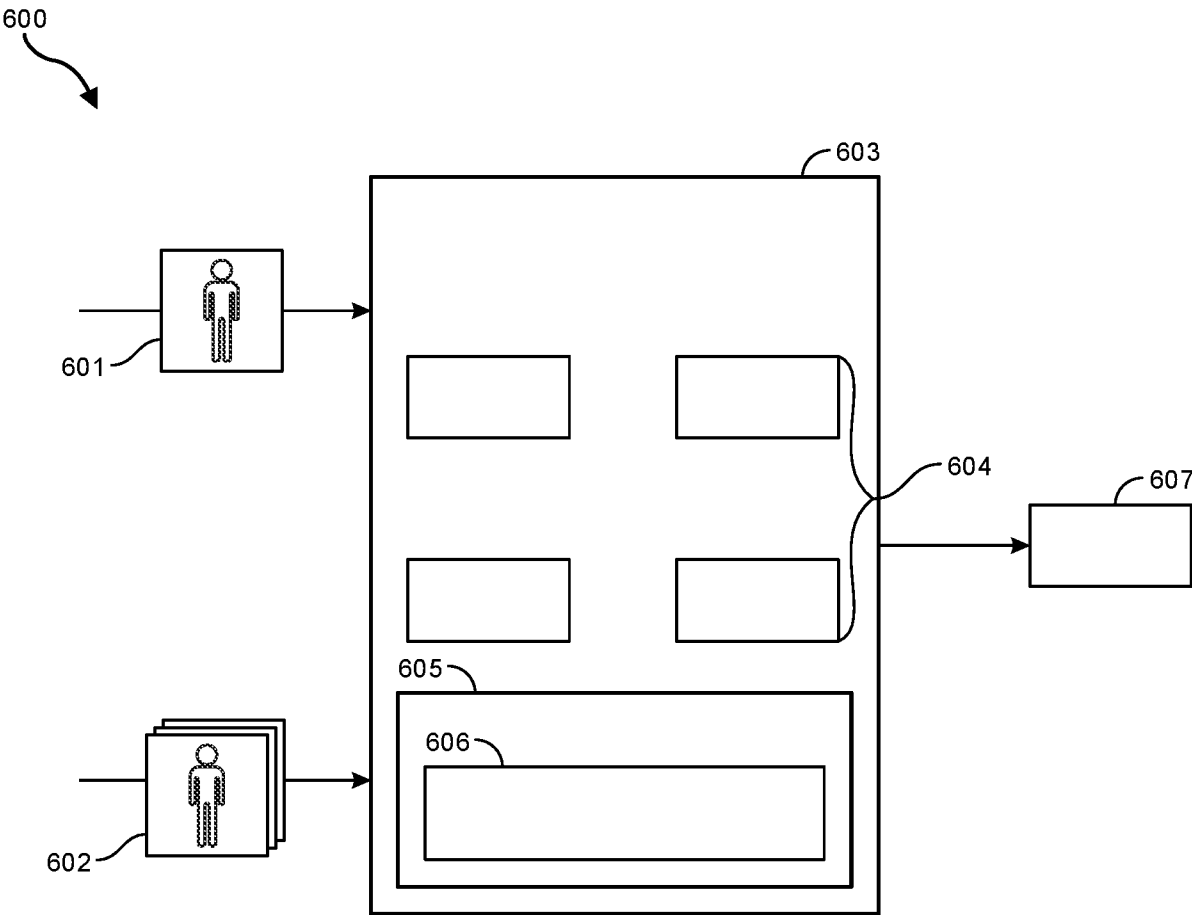


FIG. 6

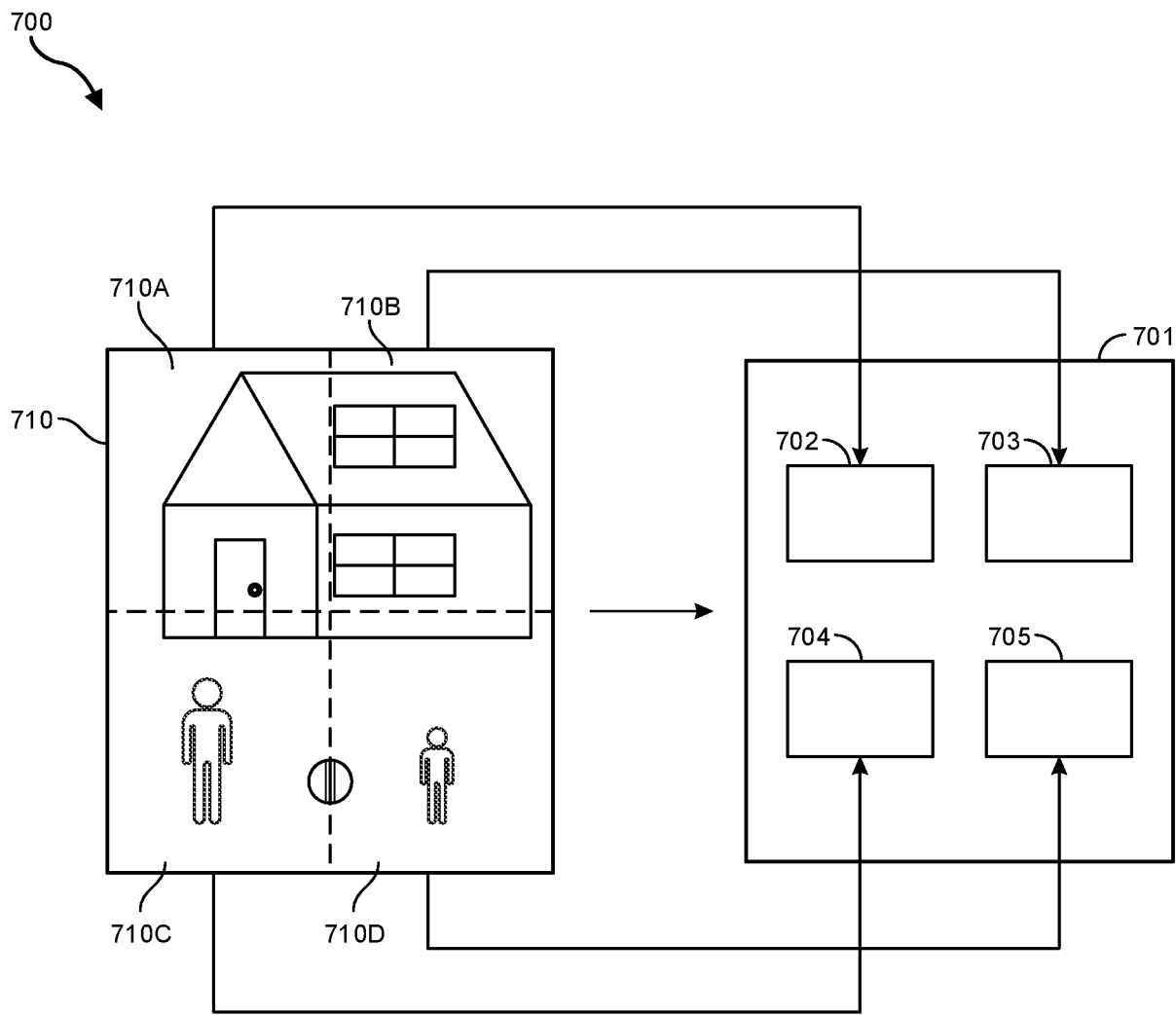


FIG. 7

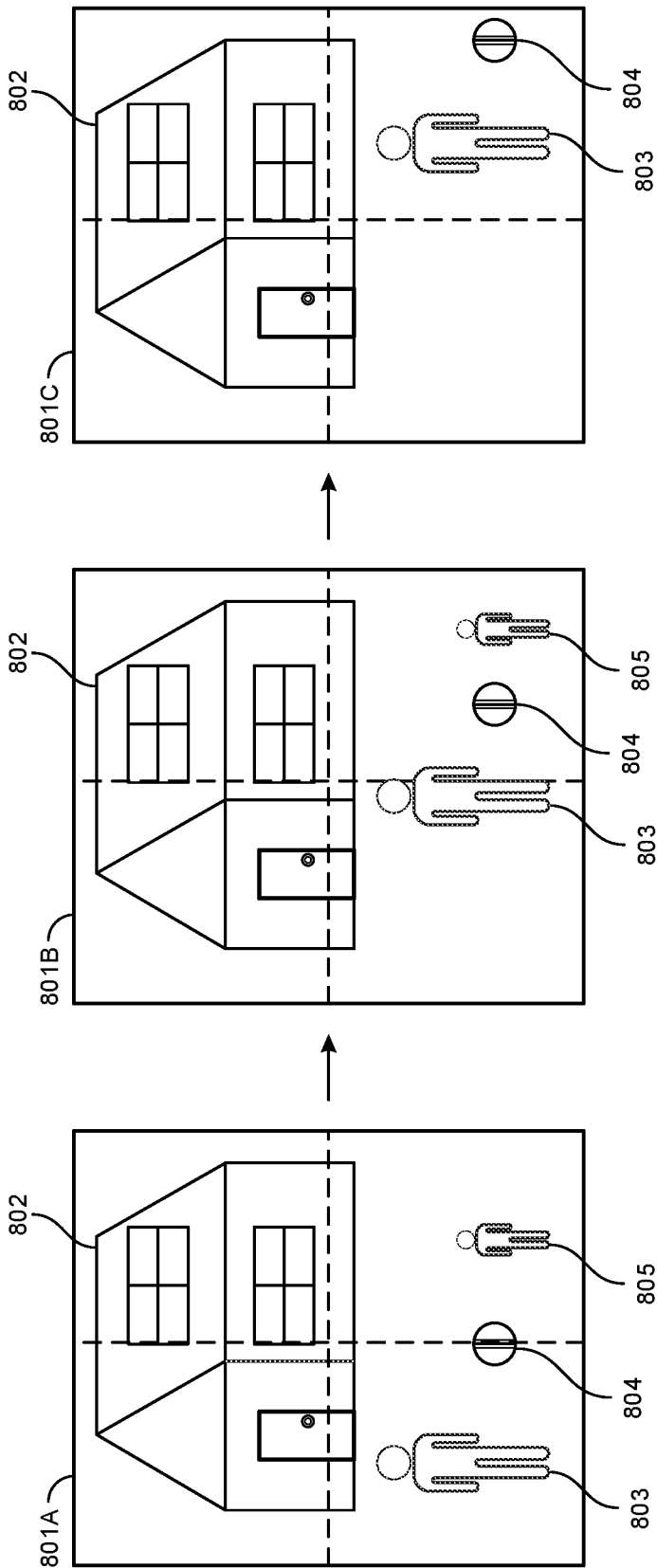


FIG. 8

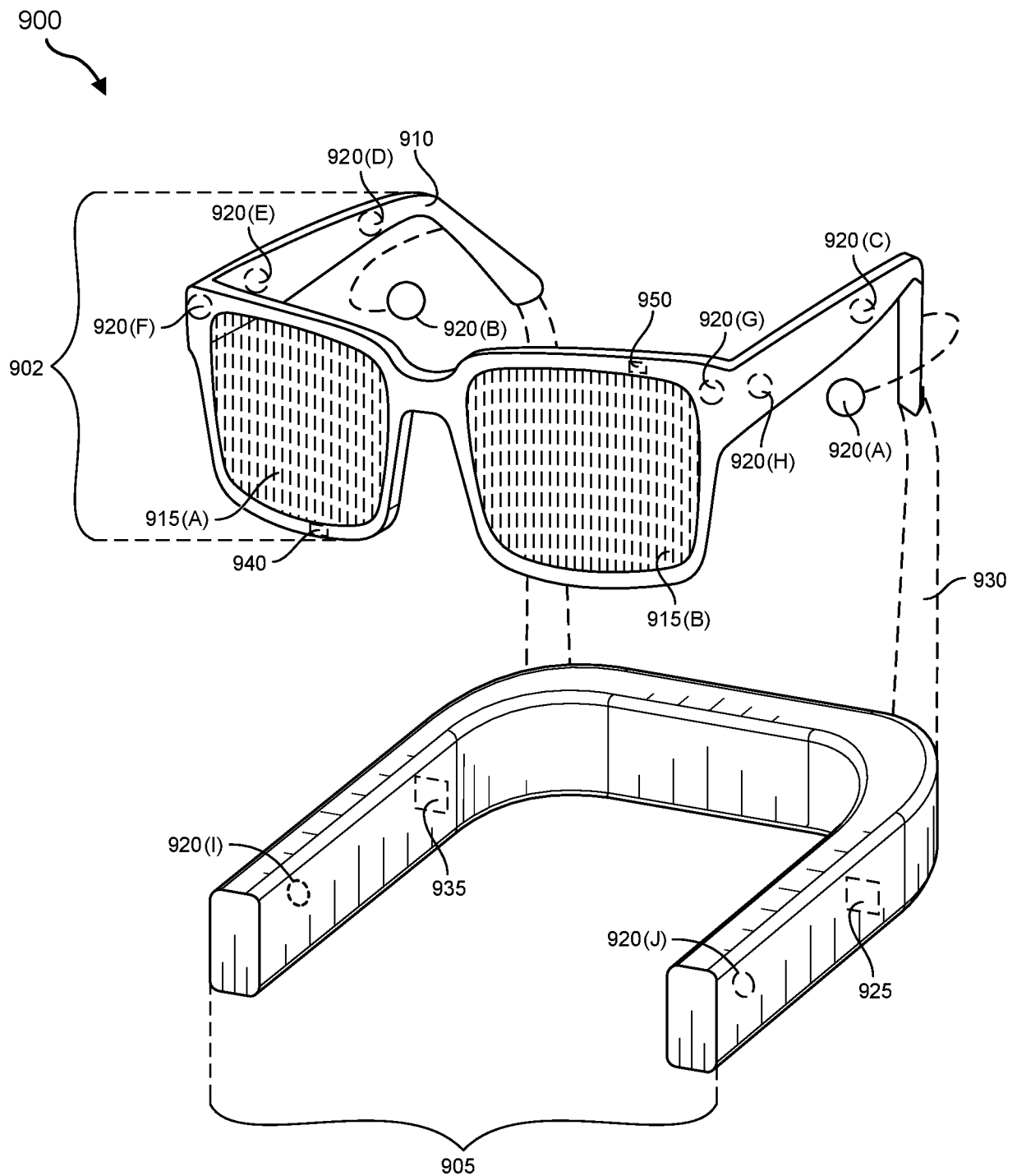


FIG. 9

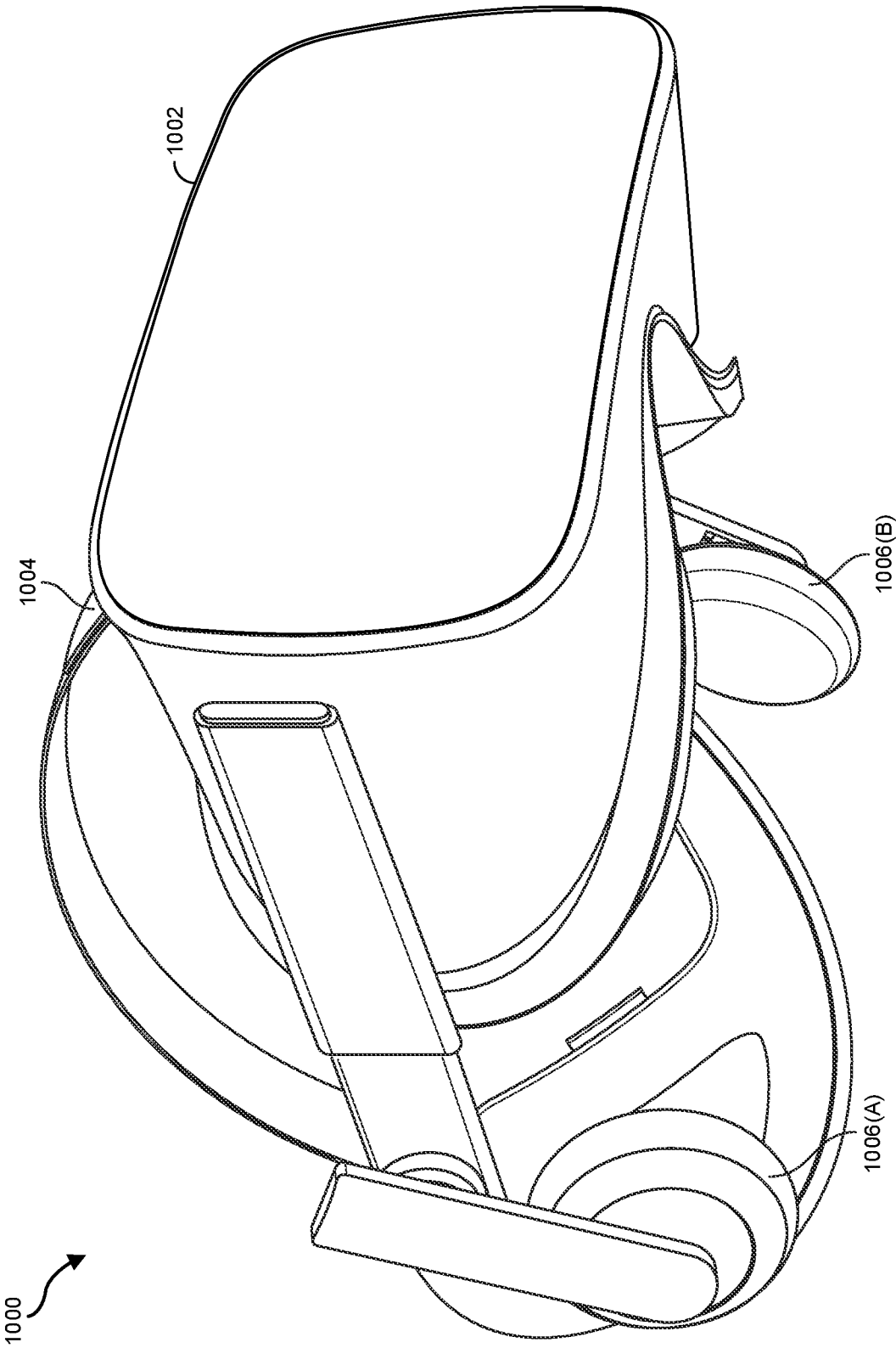


FIG. 10

10/12

1100

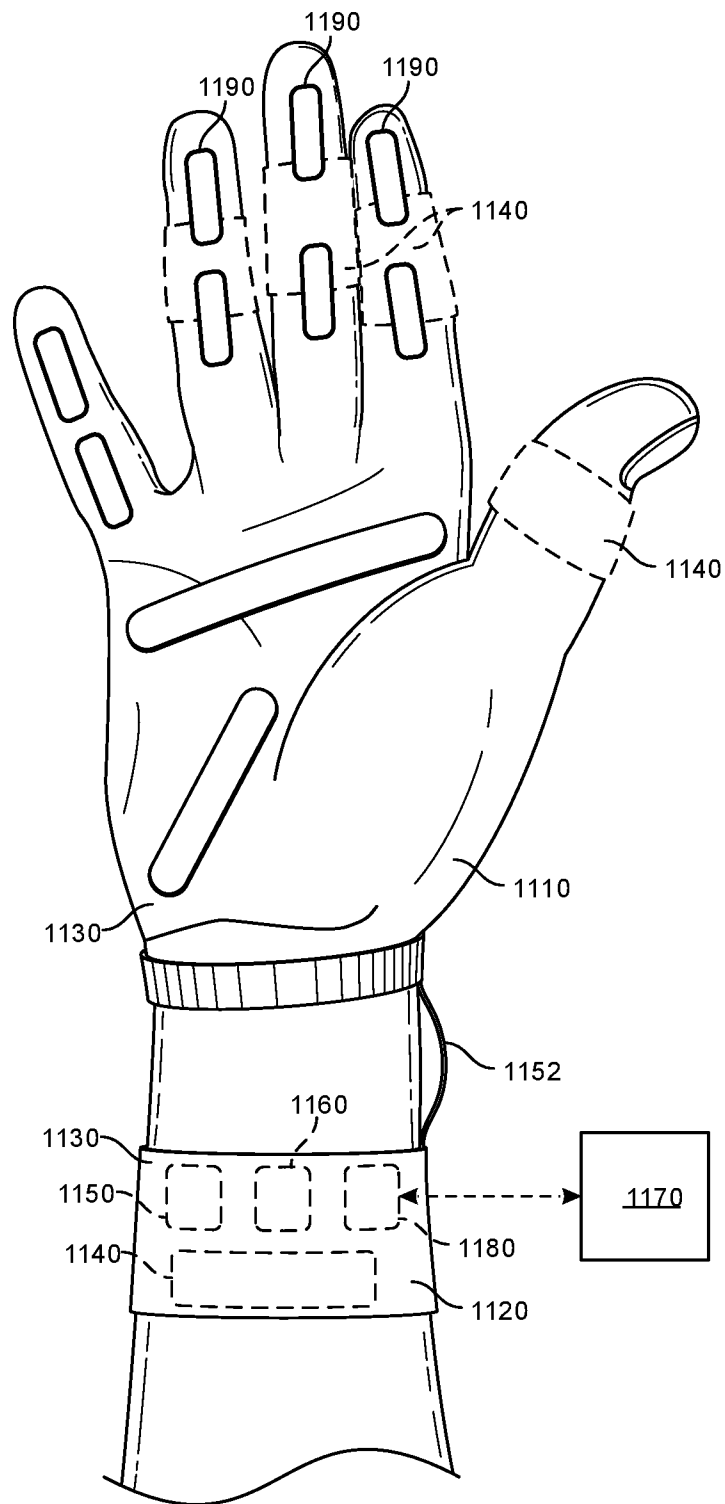


FIG. 11

11/12

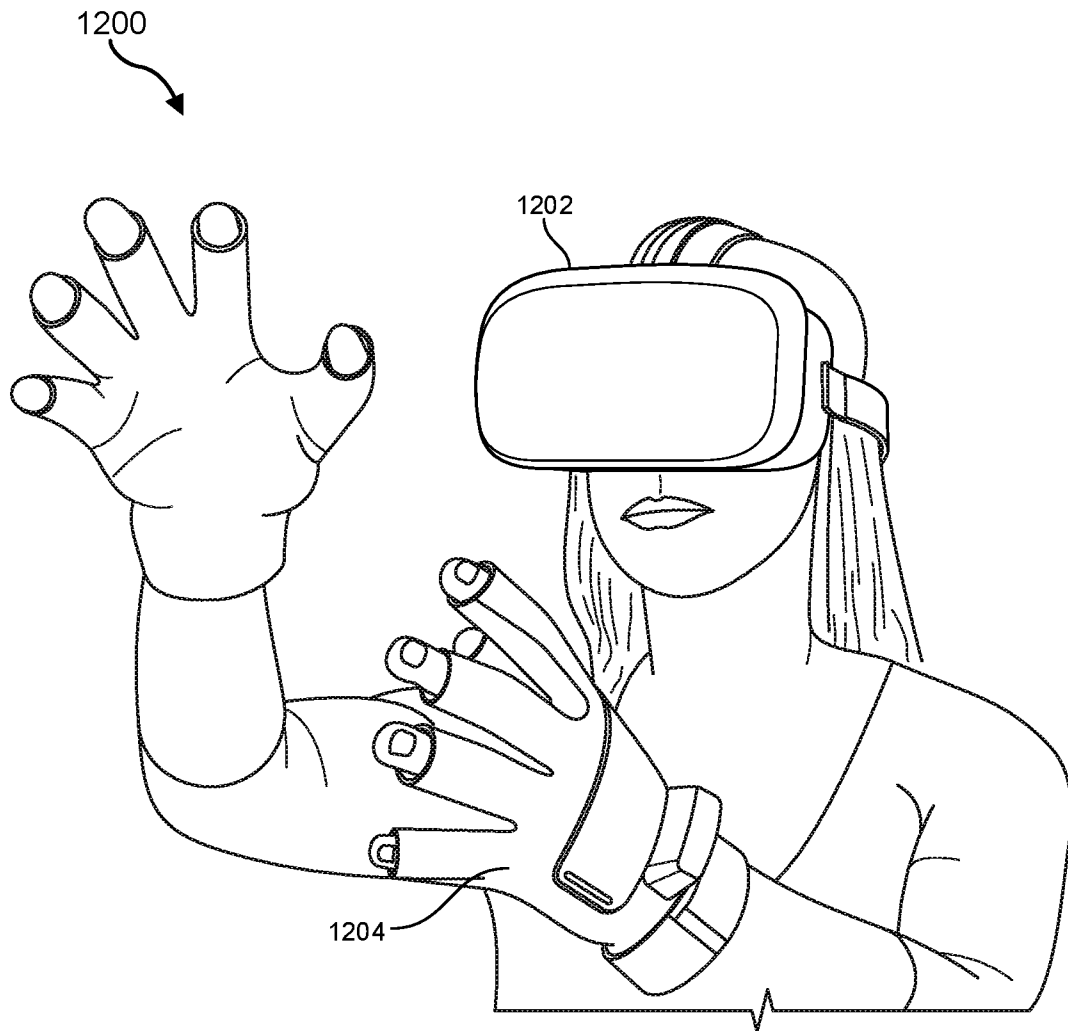
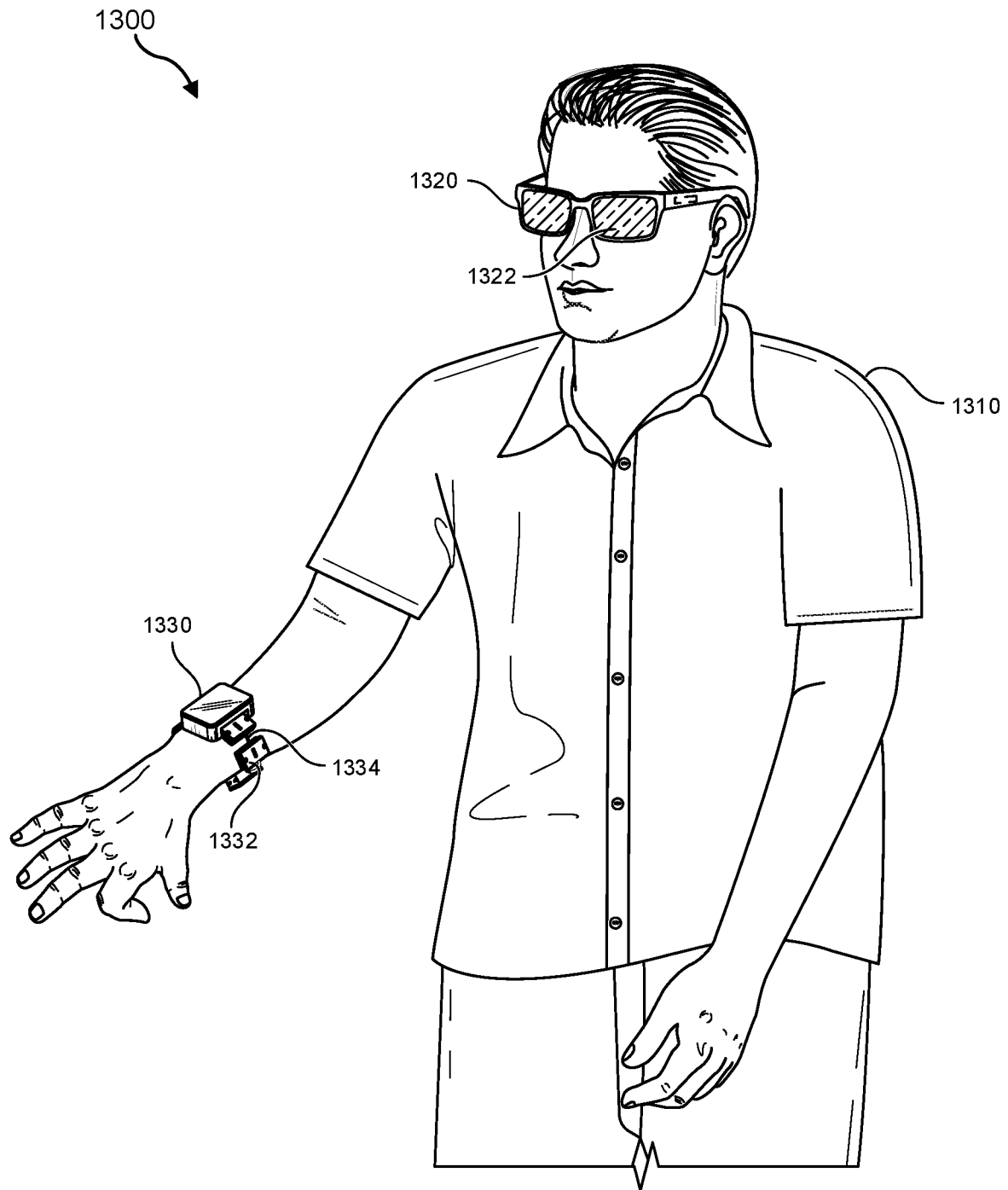


FIG. 12

12/12

**FIG. 13**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2022/038650

A. CLASSIFICATION OF SUBJECT MATTER INV. H04N5/369 G06T19/00 G06N20/00 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H04N G06T G06N		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2019/035154 A1 (LIU XINQIAO [US]) 31 January 2019 (2019-01-31) abstract paragraphs [0004], [0016], [0036], [0038], [0052] figure 3 ----- -/--	1-4, 12, 14, 15 5-11, 13
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
22 September 2022		30/09/2022
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Lauri, Lauro

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2022/038650

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No

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