

[54] APPARATUS FOR OBTAINING A SUBSTANTIALLY CONTINUOUSLY SCALED ANALOGUE REPRESENTING THE AVERAGE VALUE OF A SEQUENCE OF BINARY WORDS

[76] Inventors: Stephen Raymond Hodge; David Thompson Argent, both of Easthouses Rd., Newton Grange, Midlothian, Scotland

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Primary Examiner—Gareth D. Shaw
Attorney—Albin Browdy et al.

[57] ABSTRACT

Apparatus for obtaining a substantially continuously scaled analogue representing the average value of a sequence of binary words, comprising an accumulator for storing the sequence, a digital to analogue converter, a multiplexer to supply the accumulator sum to the converter, a counter for registering the number of words supplied to the accumulator and logic circuit means driven by the counter and adapted to set the multiplexer in position for the supply to the converter of the quotient of the accumulator word sum and the number of words counted by the counter and to afford at the converter a reference voltage proportional to the quotient, the converter by multiplying the voltage reference and quotient providing the output which is an average word.

2 Claims, 2 Drawing Figures

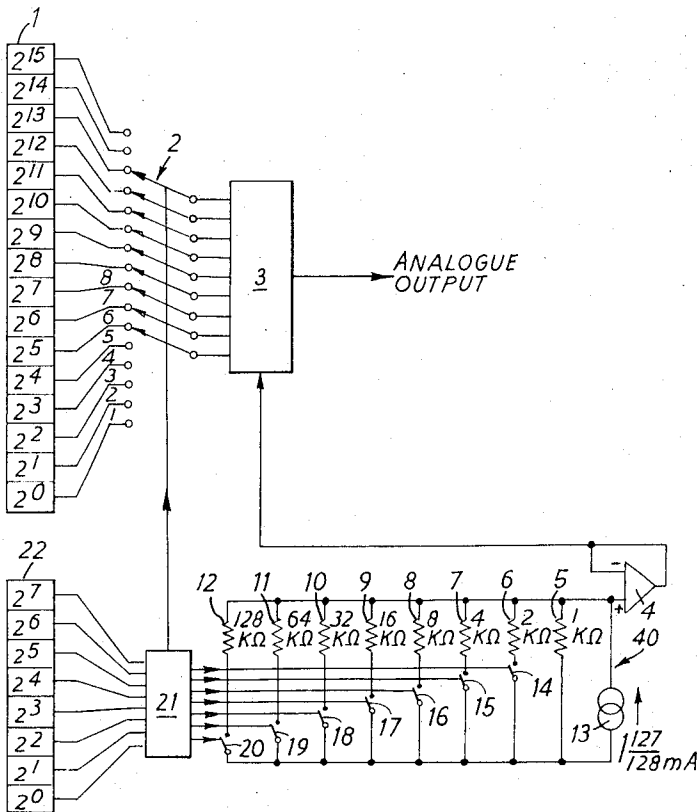
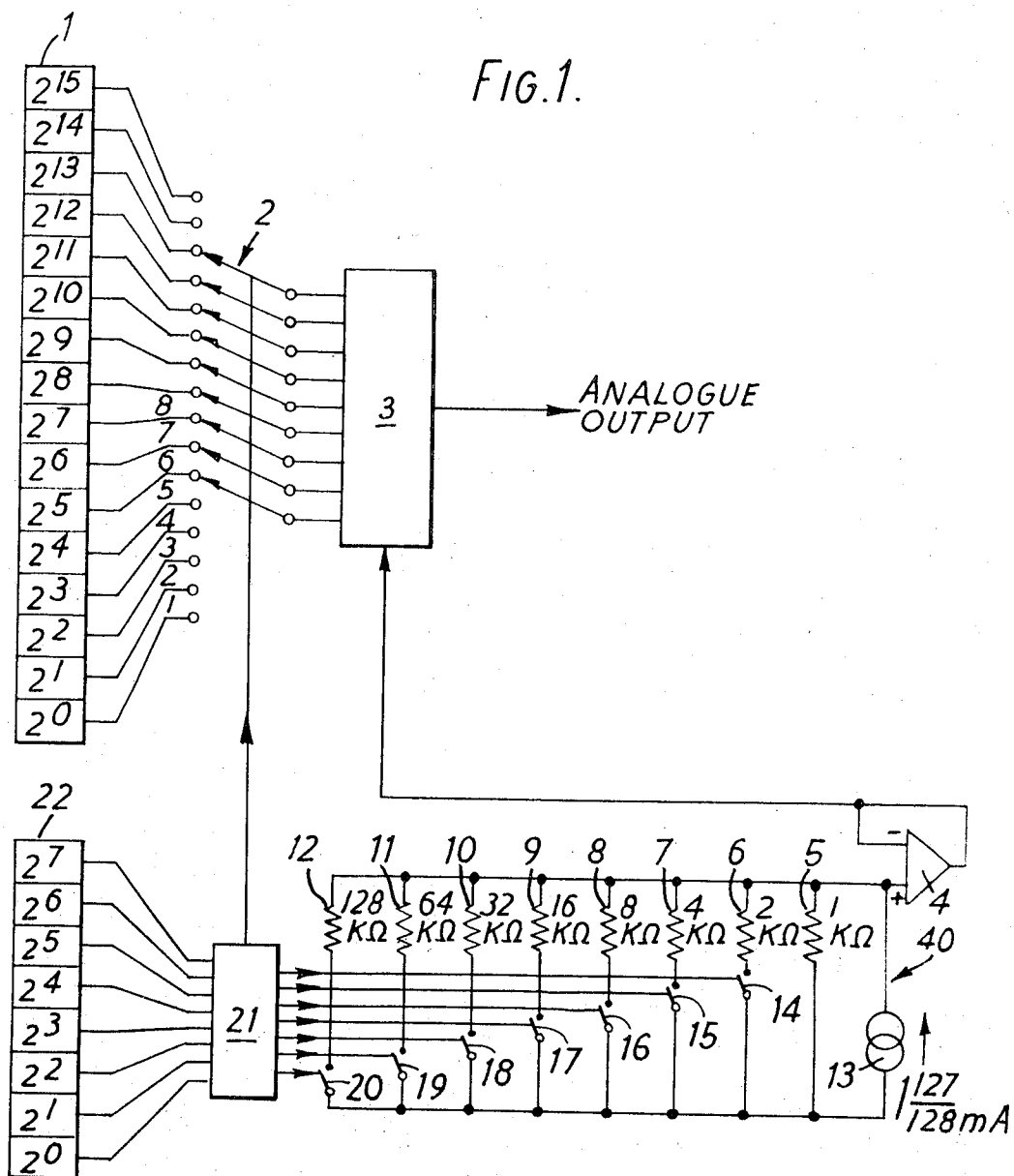


FIG. 1.



SHEET 2 OF 2
FIG. 2.

SCAN COUNT	MULTI- PLEXER POS'N	BINARY DIV'N	SWITCHES OPEN								R _{TOT}	V _{REF}	NET DIV'N
			14	15	16	17	18	19	20				
1	1	1								128/255 KΩ	1.00 VOLTS	1.00	
2	2	2								128/255 "	1.00 "	2.00	
3	3	4	⊗							128/191 "	1.34 "	2.99	
4										128/255 "	1.00 "	4.00	
5	4	8	⊗	⊗						128/159 "	1.60 "	4.99	
6			⊗							128/191 "	1.34 "	5.99	
7				⊗						128/223 "	1.14 "	7.00	
8										128/255 "	1.00 "	8.00	
9	5	16	⊗	⊗	⊗					128/143 "	1.78 "	8.97	
10			⊗	⊗						128/159 "	1.60 "	9.98	
11			⊗		⊗					128/179 "	1.46 "	10.98	
12			⊗							128/191 "	1.34 "	11.99	
13				⊗	⊗					128/207 "	1.23 "	12.99	
14				⊗						128/223 "	1.14 "	13.99	
15					⊗					128/239 "	1.06 "	15.00	
16										128/255 "	1.00 "	16.00	
17	6	32	⊗	⊗	⊗	⊗				128/135 "	1.89 "	16.94	
18			⊗	⊗	⊗					128/143 "	1.78 "	17.93	
19			⊗	⊗		⊗				128/151 "	1.69 "	18.96	
20			⊗	⊗						128/159 "	1.60 "	19.96	
21			⊗		⊗	⊗				128/167 "	1.53 "	20.96	
22			⊗		⊗					128/175 "	1.46 "	21.96	
23			⊗			⊗				128/183 "	1.40 "	22.97	
24			⊗							128/191 "	1.34 "	23.98	
25				⊗	⊗	⊗				128/199 "	1.28 "	24.98	
26				⊗	⊗					128/207 "	1.23 "	25.98	
27				⊗		⊗				128/215 "	1.18 "	26.98	
28				⊗						128/223 "	1.14 "	27.98	
29					⊗	⊗				128/231 "	1.10 "	28.99	
30					⊗					128/239 "	1.06 "	29.99	
31						⊗				128/247 "	1.03 "	30.99	
32										128/255 "	1.00 "	32.00	
33	7	64	⊗	⊗	⊗	⊗	⊗			128/131 "	1.95 "	31.89	
34			⊗	⊗	⊗	⊗				128/135 "	1.89 "	33.88	
35			⊗	⊗	⊗		⊗			128/139 "	1.84 "	34.88	
36			⊗	⊗	⊗					128/143 "	1.78 "	35.87	
37			⊗	⊗		⊗	⊗			128/147 "	1.74 "	36.88	
38			⊗	⊗		⊗				128/151 "	1.69 "	37.88	
39			⊗	⊗			⊗			128/165 "	1.65 "	38.90	
40			⊗	⊗						128/159 "	1.60 "	39.92	

APPARATUS FOR OBTAINING A SUBSTANTIALLY CONTINUOUSLY SCALED ANALOGUE REPRESENTING THE AVERAGE VALUE OF A SEQUENCE OF BINARY WORDS

This invention relates to apparatus for obtaining a substantially continuously scaled analogue representing the average value of a sequence of binary words.

The present invention consists in apparatus for obtaining a substantially continuously scaled analogue representing the average value of a sequence of binary words, comprising an accumulator for storing the sum of a sequence of words supplied thereto in binary form, a digital to analogue converter, multiplexer means for supplying the accumulator word sum to the converter, the multiplexer means being settable in a number, n , of positions in each of which it is arranged for the supply to the converter of the quotient of the accumulator word sum to a predetermined significant bit and 2^n , a counter for registering the number of words supplied to the accumulator and having a capacity of registering up to 2^n words, and logic circuit means driven by the counter and adapted to set the multiplexer in position for the supply to the converter of the quotient of the accumulator word sum to said predetermined significant bit and 2^n and to afford at the converter a reference voltage proportional to the quotient of 2^n and the number of words counted by the counter, the converter by multiplying the voltage reference and multiplexer input thereto providing an output which is the average word.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

FIG. 1 is a circuit diagram largely in block form of an apparatus in accordance with the invention; and

FIG. 2 is a table summarising the operation of the circuit of FIG. 1 at each of 40 successive counts.

Referring first to FIG. 1, the apparatus consists of a 16-bit accumulator 1 for storing the sum of a sequence of words supplied thereto in binary form. Nine consecutive bits of the accumulator are indexed at any one time by a nine $\times$ nine way multiplexer 2, the output of which is fed into a digital to analogue converter 3. The converter 3 is of known form per se and is fed, in addition to the output from the multiplexer, with a reference voltage which is generated in a voltage follower 4 from a Norton circuit 40 involving a constant current source 13, in parallel with which are each of resistors 5-12, the values of which from resistor 5-12 increase in binary sequence resistor 5 being 1 K Ω and resistor 12, 128 K Ω . Resistors 6-12 are switched across the source 13 by respective switches 14-20. The switches 14-20 and the multiplexer switches are controlled by logic circuit means 21 in the form of a combinational network which is driven from an eight-bit scan counter 22, which counts the number of words supplied to the accumulator.

The logic circuit means 21 consist of two distinct sections, a first section providing the control logic driving the nine by eight way multiplexer 2 and a second section providing the control logic for operating the switches 14 to 20 of the Norton circuit 40. The first section comprises combinational logic consisting mainly of groups of exclusive -OR and NOR functions the output of which is switched from logic level 0 to logic level 1 whenever one and only one of the scan counter elements is at logic level 1 which occurs when the count of the counter 22 is at 1, 2, 4, 8, 16, 32, 64,

128 or 256. The switch from 1 to 0 of the output of the combinational logic serves as the clock input to a three-bit binary counter consisting of three flip-flops, a fourth flip-flop being provided and being 'set' when the scan counter increments from 1 to 2 and remaining 'set' for the rest of the count. The four-bit number thus obtained is used as a binary address to the multiplexer 2 to switch the latter and thus determine the selection of the word from the accumulator 1.

The second section of logic consists of combinational logic of the same general composition as that of the first section, i.e., mainly groups of exclusive -OR and NOR functions, which examines the logic levels of the elements, which are flip-flops, of the counter 22 to produce therefrom the necessary switching functions for the switches 14 to 20.

It will be seen that the logic circuit means 21 set the multiplexer in any one of n positions where n has the maximum value of nine and that the multiplexer accordingly supplies to the digital to analogue converter 3 the quotient of the word sum in the accumulator to the ninth most significant bit and 2^n .

The voltage reference input from the voltage follower 4 to the converter is proportional to the quotient of 2^n and the number of words inserted into the accumulator, n having the value of the setting of the multiplexer at the particular total of words inserted into the accumulator.

The table of FIG. 2 illustrates the operation of the switches 14-20 for the first forty words introduced into the accumulator. To explain the table fully, one typical example is worked as follows: at the seventeenth word, switches 14-17 are open and switches 18-20 are closed. Thus the parallel resistance (R_{TOT}) across the source 13 equals 128/135 chms which, multiplied by the current from the source of 1 and 127/128 milliamperes gives a reference voltage (V_{REF}) of 1.89 volts. As the multiplexer is in position No. 6 when the seventeenth word is introduced, the multiplexer serves to divide the word total in the accumulator by 2^5 , i.e., 32. As the reference voltage is multiplying the multiplexer input to the converter, the nett division effected by the converter is $32/1.89$ equals 16.94, which is closely approximate to 17.

It will be apparent therefore that each time a new binary number of up to eight digits is put into the accumulator, the counter 22 clocks up one count and so registers the total number of words in the accumulator. The logic 21, driven by the counter 22, causes the voltage follower to produce a reference voltage of a value between 1.00 and 1.992 volts and further causes appropriate setting of the multiplexer. As the digital to analogue converter multiplies the two inputs thereto, it provides an output which is almost exactly proportional to the content of the accumulator divided by the number of words accumulated therein.

Whilst the apparatus has been described in relation to a sixteen-bit accumulator and a counter which counts up to 256 words, the apparatus can be adapted to different sized accumulators and counters which will count other numbers of words. The theoretical accuracy is always within one bit of the counter 22.

The invention thus provides a novel combination of means for obtaining an analogue voltage or current which is approximately proportional to the quotient of two binary numbers of which the dividend has more digits than the divisor. The invention also provides

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novel means of ensuring that the analogue equivalent of the average of a sequence of numbers entered into an accumulator is always generated with approximately the correct scaling factor.

We claim:

1. Apparatus for obtaining a substantially continuously scaled analogue signal representing the average value of a sequence of binary words, comprising an accumulator for storing the sum of a sequence of words supplied thereto in binary form, a digital to analogue converter, multiplexer means for supplying the accumulator word sum to the converter, the multiplexer means being settable in a number, n , of positions in each of which it is arranged for the supply to the converter of the quotient of the accumulator word sum to a predetermined significant bit and 2^n , a counter for

4

registering the number of words supplied to the accumulator and having a capacity of registering up to 2^n words, and logic circuit means driven by the counter and adapted to set the multiplexer in position for the supply to the converter of the quotient of the accumulator word sum to said predetermined significant bit and 2^n and to afford at the converter a reference voltage proportional to the quotient of 2^n and the number of words counted by the counter, the converter by multiplying the voltage reference and multiplexer input thereto providing an output which is the average word.

2. Apparatus as claimed in claim 1, further including a Norton circuit, wherein the logic circuit operates said Norton circuit to afford at the converter the reference voltage.

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