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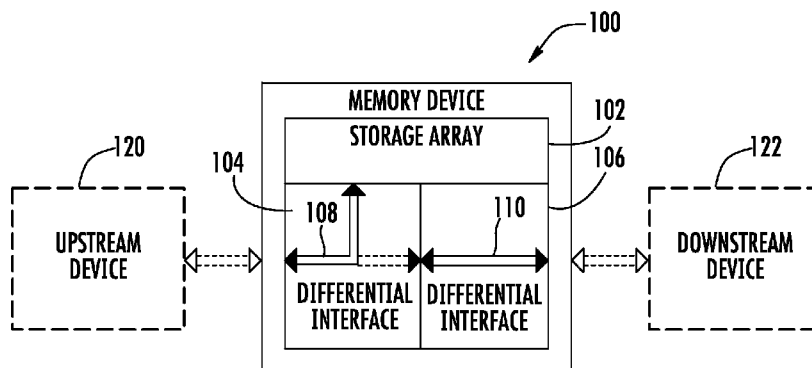


FIG. 1A

(57) Abstract: A memory device includes a storage array, a first differential interface coupled to the storage array and including a first bidirectional signal channel to facilitate communication with an upstream device, and a second differential interface coupled to the first differential interface and including a second bidirectional signal channel to facilitate communication with a downstream device.

COMMUNICATION INTERFACE FOR MEMORY DEVICE

BACKGROUND

[0001] The memory industry developed the Double Data Rate (DDR) physical communication interface for Dynamic Random-Access Memory (DRAM) and memory modules in 2002. The DDR interface has evolved from an original bit rate of 226 Mb/s to the current DDR4 bit rate of 2.13 Gb/s, and is projected to achieve a bit rate of 3.2 Gb/s by 2019. The DDR4 interface includes a parallel data bus. The DDR4 interface also uses single-ended signaling. The DDR4 interface is also designed to support only DRAM memory, and has tightly intertwined physical and protocol layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Figure 1A is a block diagram of an example memory device having a communication interface.

[0003] Figure 1B is a block diagram of the memory device of Figure 1A having two bidirectional signal channels in each differential interface.

[0004] Figure 1C is a block diagram of the memory device of Figure 1A having four bidirectional signal channels in each differential interface.

[0005] Figure 2A is a block diagram of the memory device of Figure 1C having a switching device between the two differential interfaces, wherein the memory device is selected by the switch.

[0006] Figure 2B is a block diagram of the memory device of Figure 2A, wherein the memory device is not selected by the switch.

[0007] Figure 3 is a block diagram of the memory device of Figure 1C having a switching device with a pass-through design with respect to the two interfaces.

[0008] Figure 4 is a block diagram of an example memory module including the memory device of Figure 1A.

[0009] Figure 5 is a block diagram of the memory module of Figure 4 having two memory ranks interconnected using a differential bus.

[00010] Figure 6 is a block diagram of a memory apparatus having two memory modules interconnected by a differential bus.

DETAILED DESCRIPTION OF EXAMPLES

[00011] Examples of communication interfaces for memory devices are disclosed herein. Although DDR4 may be projected to achieve a bit rate of 3.2 Gb/s by 2019, some DDR interfaces may not meet future performance requirements, including percentage of annual bit rate and bandwidth growth, average bandwidth efficiency per pin, power consumption, ability to support multiple Dual In-line Memory Modules (DIMMs) per channel at the highest data rates, and the ability to support memory technologies other than DRAM. For example, in 2012 there was a 25% bandwidth increase from DDR3-1333 to DDR3-1600. In 2019, the annual bandwidth increase may be approximately 9% from DDR4-2933 to DDR4-3200. A new, more scalable and efficient memory interface is needed to meet the rapidly expanding needs of computer systems.

[00012] In particular, the maximum bandwidth of the DDR4 parallel bus provides an inefficient bandwidth per pin at both the central processing unit (CPU) and DIMM connector. For example, by 2019 the DDR4-3200 parallel data bus may support a maximum bandwidth of 25.6 Gb/s. For a CPU having 259 pins dedicated to the DDR4 interface, this bandwidth may provide an average of only about 0.8 Gb/s/pin at the CPU. For a DDR4 DIMM connector having 288 pins, this bandwidth may provide an average of only about 0.7 Gb/s at the DIMM connector. Also, the single-ended signaling used by the

DDR 4 interface may account for as much as 50% of DIMM power consumption. A more power-efficient interface would be desirable. Furthermore, the limited number of connectors in the DDR4 multi-drop bus may result in lower system memory capacity. For example, the DDR4 interface runs at lower data rate when multiple DIMMs are connected to the bus and may require registers and data buffers for high capacity memory modules. The buffer may allow larger capacity DIMMs with higher data rates on the existing DDR4 single ended, multi-drop bus, but adds 2.5 W of power and 3 ns of latency. Due to signal integrity constraints at higher data rates, the number of DDR DIMM connectors per channel that can support the maximum data rate for an installed DIMM will decrease from 3 connectors in DDR4-2133 to one connector in DDR-3200. There is need for a new interface to maintain memory expansion. Even further, because the DDR4 interface was designed to support only DRAM memory, it has tightly intertwined physical and protocol layers and is not easily adapted to support emerging memory technologies such as memristors, Phase Change Memory (PCM), Spin Transfer Torque (STT), resistive bridge RAM, resistive memory (RRAM), etc.

[00013] The examples of communication interfaces for memory devices disclosed herein may provide more scalable and efficient memory interface. In particular, the examples of communication interfaces for memory devices disclosed herein may include a data bus utilizing differential signaling. Use of differential signaling may provide greater and more sustained year-to-year increases in bandwidth and throughput, as well as more efficient bandwidth per pin and improved power efficiency. The examples of communication interfaces for memory devices disclosed herein may also include a daisy chain point-to-point interface in order to allow for memory expansion without sacrificing bandwidth or requiring registers or data buffers for higher capacity data modules. The examples of communication interfaces for memory devices disclosed herein may also separate the physical and protocol layers

to allow support for multiple memory technologies using the same physical interface.

[00014] Figure 1 is a block diagram of an example memory device 100 having a communication interface. Memory device 100 may be, for example, a memory chip or other integrated circuit that may be used in or by an electronic computing device to store data, program instructions, etc. The term “memory device” as used herein refers to storage devices used to store data on the premise that the same data will be read from them multiple times, as opposed to dedicated “buffering devices” which are devices used to temporarily store data while it is being moved from one place to another in order to, for example, compensate for a difference in rate of flow of data, or time of occurrence of events, when transferring data from one device to another. Memory device 100 may be provided as integrated circuits (ICs) or chips bonded and mounted into plastic packages with metal pins for connection to control signals and buses. In some examples, memory device 100 may be assembled into multi-chip plug-in modules (DIMMs, etc.), stacked or non-stacked DRAM modules, etc.

[00015] Memory device 100 may include a storage array 102. Storage array 102 may be, for example, a DRAM storage array (as shown in Figure 1B) having an array of charge storage cells consisting of one capacitor and transistor per data bit, with the charge capacitor being periodically refreshed to compensate for transistor leakage. In some examples, storage array 102 may be a memristor-based storage array (as shown in Figure 1C) capable of storing data when power is removed. While the examples of memory device 100 herein may be described primarily in the context of DRAM-based or memristor-based storage arrays, it will be appreciated that other types of storage arrays are contemplated as well.

[00016] Memory device 100 may also include a communication interface. For example, as shown in Figure 1A, memory device 100 may

include an interface 104 and an interface 106. Interface 104 and interface 106 may employ differential signaling. The term “differential” as used herein refers to a method for electrically transmitting information using two complementary signals, wherein the electrical signal includes a differential pair of signals transmitted using two transmission lines. Differential signaling may be used as opposed to “single-ended” signaling, wherein one transmission line carries a varying voltage that represents the signal, while another is connected to a reference voltage, such as ground. For a given supply voltage, differential signaling may provide twice the noise immunity of single-ended signaling. Accordingly, differential signaling may facilitate lower supply voltages for memory device 100 in order to save power and reduce emitted electromagnetic radiation. In some examples, interface 104 and interface 106 may be formed and/or structurally integrated within memory device 100. In some examples, interface 104 and 106 may be included in the logic of a through-silicon-via (TSV) connection.

[00017] Interface 104 and interface 106 may allow memory device 100 to be electrically coupled and/or to be in electrical communication with and/or via devices upstream and/or downstream of memory device 100. For example, interface 104 may be electrically coupled to storage array 102 and/or interface 106 to permit transmission of data among an upstream device 120, a downstream device 122, and memory device 100. Upstream device 120 may be, for example, a memory controller, another memory device 100, a memory module, such as a DIMM, etc. Similarly, downstream device 122 may be, for example, another memory device 100, a memory module, such as a DIMM, etc. Other types of upstream devices 120 and downstream devices 122 are contemplated as well.

[00018] In particular, interface 104 and interface 106 may facilitate point-to-point connectivity among upstream device 120, downstream device 122, and memory device 100. The term “point-to-point” as used herein refers to a connection topology that facilitates communication between only two devices.

Point-to-point connectivity may be used as opposed to a “multidrop” bus, in which all devices are connected to the same bus, each device listens for requests it is intended to receive, and through an arbitration process determines which device sends information at any point. Using point-to-point connectivity may facilitate higher data rates when multiple memory devices 100 are connected together.

[00019] In some examples, interface 104 may be a primary interface to facilitate connection to and/or communication with and/or via upstream device 120, and interface 106 may be a secondary interface to facilitate connection to and/or communication with downstream device 122. For example, as shown in Figure 1B, interface 104 may facilitate electrical coupling of memory device 100 with an upstream memory controller, and interface 106 may facilitate electrical coupling of memory device 100 with a downstream memory device 100. In this example, interface 104 and interface 106 may facilitate point-to point electrical connectivity and communications between, for example, upstream device 120 and memory device 100, between upstream device 120 and downstream device 122, etc.

[00020] In some examples, interface 104 and interface 106 may facilitate daisy chain connections. The term “daisy chain” as used herein refers to an electrical connection scheme in which multiple devices may be interconnected in series to a controlling device by connecting each component to another similar component, rather than always directly connecting each device to the controlling device. In a daisy chain connection, only the first device in the chain directly connects to the controlling device and only device communicates with the controlling device at a given time. For example, as shown in Figure 1B, interface 104 and interface 106 may facilitate a daisy chain connection in which memory device 100 is connected to the memory controller via interface 104, and another memory device is connected to memory device 100 via interface 106. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory

device 100, with downstream device 122, etc. Similarly, in the example shown in Figure 1C, interface 104 may facilitate a daisy chain connection of memory device 100 with an upstream memory device, which may be another memory device 100, and interface 106 may facilitate a daisy chain connection of memory device 100 with a downstream device 122, which may be yet another memory device 100. When upstream device 120 is connected to, for example, an upstream memory controller, point-to-point connections may be established between the memory controller and each memory device 100 connected in the daisy chain. In this way, the use of daisy chain connectivity may facilitate memory expansion without diminishing the maximum system bandwidth.

[00021] In some examples, interface 104 and interface 106 facilitate direct electrical coupling of memory device 100 with upstream device 120 and/or downstream device 122. Such coupling is “direct” in the sense that a buffer is not positioned or required to be positioned between memory device 100 and upstream device 120 or downstream device 122, such as to isolate memory device 100 from upstream device 120 or downstream device 122 and maintain maximum data rates when high capacity, high speed memory devices are used. In particular, providing differential interfaces 104 and 106 directly on memory device 100 as shown in Figures 1A, 1B, and 1C may eliminate the need for the buffer, without handicapping the speed or capacity of memory device 100. This may in turn reduce system power requirements and latencies associated with the use of buffers.

[00022] Interface 104 and interface 106 may each include any suitable number of differential signal channels to facilitate connection to and/or communication with and/or via upstream device 120 and/or downstream device 122. For example, as shown in Figure 1A, interface 104 may include a differential signal channel 108, and interface 106 may include a differential signal channel 110. Similarly, Figure 1B illustrates an example in which interface 104 includes two differential signal channels (channel 108a and

channel 108b), and in which interface 106 also includes two differential signal channels (channel 110a and channel 110b). Figure 1C illustrates an example in which interface 104 includes four differential signal channels (channels 108a, 108b, 108c, and 108d), and in which interface 106 also includes four differential signal channels (channels 110a, 110b, 110c, and 110d).

[00023] As shown in Figures 1A, 1B, and 1C, each of signal channels 108 and signal channel 110 may be bidirectional signal channels. The term “bidirectional signal channel” as used herein refers to a single signal channel (e.g., a differential signal pair) that facilitates communications both to and from upstream device 120 and downstream device 122 using the same signal channel as opposed to using dedicated independent transmit and receive channels. Bidirectional communications may be facilitated by the use of, for example, a synchronous protocol, a split transaction protocol, or other techniques. Such bidirectional communications may include, for example, transmitting commands, row address, column address, and other data to memory device 100 or to downstream device 122 from upstream device 120, transmitting status and other data from memory device 100 or downstream device 122 to upstream device 120, etc. In some examples, memory device 100 may support a burst length of 8 bits, while in other examples, other burst lengths, such as 32 bits or 64 bits, may be used. In some examples, 16B/18B transmission encoding may be used to ensure data integrity. In some examples, row access strobe (RAS) and column access strobe (CAS) generator functionality may be integrated into memory device 100, while in other examples, RAS and CAS functionality may be provided by upstream device 120 (e.g., a memory controller).

[00024] As will be appreciated, the use of bidirectional signal channels may reduce the number of pins needed to connect memory device 100 with upstream device 120 and/or downstream device 122. For example, the use of four bidirectional differential signal channels in each of interface 104 and interface 106 of memory device 100 (as shown in Figure 1C) may enable the

use of 68 total pins, as compared to a total of 78 pins on a current DDR4 DRAM chip. In this example, interface 104 and interface 106 may together include 16 pins corresponding to the four bidirectional differential signal channels in each interface, 10 pins dedicated to differential grounds, 12 pins for sideband and test functionality, 12 power pins, and 18 ground pins.

[00025] In order to facilitate point-to-point daisy chain connectivity, in some examples, memory device 100 may include a switching device to selectively couple bidirectional signal channels 108 in interface 104 to either storage array 102 or to bidirectional signal channels 110 in interface 106. For example, Figures 2A and 2B are block diagrams of a memory device 200 similar to memory device 100 shown in and described with reference to Figure 1C. Those components of memory device 200 that correspond to memory device 100 as shown in Figure 1C are numbered similarly. As shown in Figures 2A and 2B, a switching device 130 may be positioned between interface 104 and 106 to selectively couple bidirectional signal channels 108a, 108b, 108c, and 108d in interface 104 to either storage array 102 (e.g., for a point-to-point connection between upstream device 120 and memory device 200 as shown in Figure 2A) or to bidirectional signal channels 110a, 110b, 110c, and 110d in interface 106 (e.g., for a point-to-point daisy chain connection between upstream device 120 and downstream device 122 via memory device 200 as shown in Figure 2B). As shown in Figure 2A, a device select signal (e.g., from an upstream memory controller) may be applied to switching device 130 in order to select memory device 200 for a point-to-point connection. As shown in Figure 2B, the device select signal may be used to de-select memory device 200 in order to, for example, initiate a point-to-point daisy chain connection between an upstream device 120 and a downstream device 122.

[00026] Figure 3 is a block diagram of a memory device 300 similar to memory device 100 shown in Figure 1C. Those components of memory device 300 that correspond to memory device 100 as shown in Figure 1C are

numbered similarly. As shown in Figure 3, memory device 300 may utilize a pass-through design in order to integrate a switching device 130 with respect to storage array 102, interface 104, and interface 106. A device select signal may be applied to select or de-select memory device 300 for a point-to-point connection with an upstream device 120.

[00027] Figure 4 is a block diagram of an example memory module 400 including memory device 100 of Figure 1A. Those components of memory device 400 that correspond to memory device 100 as shown in Figure 1C are numbered similarly. Memory module 400 may be, for example, a DIMM module, although it will be understood that other types of memory modules are contemplated as well. As shown in Figure 4, memory module 400 may include memory devices 100a ... 100n, where n is any suitable number of memory devices. For example, a memory module 400 may include a single memory rank having 8, 9, or 18 memory devices 100. Each memory device 100 may include an interface 104 and an interface 106. For example, as shown in Figure 4, memory devices 100a ... 100n may include respective interfaces 104a ... 104n. Each interface 104 and 106 may include a suitable number of differential signal channels 108 and 110. For example, as shown in Figure 4, each of interfaces 104a ... 104n may include a respective differential signal channel 108a ... 108n to facilitate connection to and/or communication with an upstream device 120, and each of interfaces 106a ... 106n may include a respective differential signal channel 110a ... 110n to facilitate connection to and/or communication with a downstream device 122. Each differential signal channel 108 and 110 may be a bidirectional signal channel.

[00028] As shown in Figure 4, interfaces 104a ... 104n from each of memory devices 100a ... 100n may be ganged to form a differential bus 140. Similarly, interfaces 106a ... 106n from each of memory devices 100a ... 100n may be ganged to form a differential bus 142. Differential bus 140 may facilitate communication with an upstream device 120, and differential bus

142 may facilitate communication with a downstream device. In particular, differential bus 140 and differential bus 142 may facilitate point-to-point daisy chain connections and/or communications with or via memory module 400 similar to those described above with reference to Figures 1A, 1B, and 1C. For example, upstream device 120 may be a memory controller, while downstream device 122 may be another memory module, such as a DIMM module, etc. As shown in Figure 4, differential bus 140 and differential bus 142 may facilitate a daisy chain connection in which memory module 400 is connected to the memory controller via differential bus 140, and another memory module is connected to memory module 400 via differential bus 142. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory module 400, with downstream device 122, etc.

[00029] As will be appreciated, the use of bidirectional differential signal channels in interfaces 104 and 106 may significantly reduce the number of pins required in each memory module 400. For example, a DIMM memory module 400 having 18 memory devices 100, with each memory device 100 including an interface 104 and an interface 106, and each interface 104 including two respective bidirectional differential signal channels 108, and each interface 106 including two respective bidirectional differential signal channels 110, may include a total of 266 pins as compared to a total of 288 pins on a current DDR4 DIMM module. In this example, differential bus 140 and differential bus 142 may each include 72 pins corresponding to the bidirectional differential signal channels in each interface, 37 pins dedicated to differential grounds, and 12 pins for sideband and test functionality for a total of 121 pins per interface, with an additional 6 power pins, and 18 ground pins. In some examples, differential bus 140 and differential bus 142 facilitate direct electrical coupling of memory module 400 with upstream device 120 and/or downstream device 122. Such coupling is “direct” in the sense that a buffer is not positioned or required to be positioned between memory module 400 and upstream device 120 or downstream device 122, such as to isolate memory

module 400 from upstream device 120 or downstream device 122 and maintain maximum data rates when high capacity, high speed memory devices are used.

[00030] As will also be appreciated, the number of pins that may be required by an upstream memory controller to support an interface with memory module 400 may be reduced as well. For example, continuing with the above example where each differential interface 104 may include 72 pins corresponding to the bidirectional differential signal channels in the interface and 37 pins dedicated to differential grounds, the memory controller may require a total of 130 pins, including an additional 6 sideband pins, 6 power pins, and 9 ground pins. A typical DDR4 controller interface may require 259 pins including address, data, power, ground and sideband signals. Accordingly, a memory controller may provide interfaces for two memory modules 400 using approximately the same number of pins required for a current DDR4 DIMM module. Running each interface at 6.4 Gb/s (twice the bit rate of DDR4-3200) may result in doubling the DDR4 bandwidth for approximately the same number of pins.

[00031] Figure 5 is a block diagram of a memory module 500 having two memory ranks interconnected using a differential bus. Memory module 500 is similar to memory module 400, and those components of memory device 500 that correspond to memory device 400 as shown in Figure 4 are numbered similarly. Memory module 500 may differ from memory module 400 in that memory module 500 includes memory ranks 150a and 150b. Memory module 500 may be, for example, a dual package DIMM module, although it will be understood that other types of memory modules are contemplated as well. As shown in Figure 5, each memory rank 150 of memory module 500 may include memory devices 100a ... 100n, where n is any suitable number of memory devices. For example, each memory rank 150 may have 8, 9, or 18 memory devices 100. Each memory device 100 may include an interface 104 and an interface 106. For example, as shown in

Figure 5, memory devices 100a ... 100n may include respective interfaces 104a ... 104n. Each interface 104 and 106 may include a suitable number of differential signal channels 108 and 110. For example, as shown in Figure 5, each of interfaces 104a ... 104n may include a respective differential signal channel 108a ... 108n to facilitate connection to and/or communication with an upstream device 120, and each of interfaces 106a ... 106n may include a respective differential signal channel 110a ... 110n to facilitate connection to and/or communication with a downstream device 122. Each differential signal channel 108 and 110 may be a bidirectional signal channel.

[00032] As shown in Figure 5, for each of memory ranks 150a and 150b, interfaces 104a ... 104n from each of memory devices 100a ... 100n may be ganged to form a differential bus 140. Similarly, interfaces 106a ... 106n from each of memory devices 100a ... 100n may be ganged to form a differential bus 142. Differential bus 140 may facilitate communication with an upstream device 120, and differential bus 142 may facilitate communication with a downstream device. Differential bus 140 and differential bus 142 may facilitate point-to-point daisy chain connections and/or communications with or via memory module 500 similar to those described above with reference to Figures 1A, 1B, 1C, and 4. For example, with respect to memory rank 150a, upstream device 120 may be a memory controller, and memory rank 150b may be a downstream device. With respect to memory rank 150b, memory rank 150 may be an upstream device, and downstream device 122 may be a memory rank of another memory module 500.

[00033] As shown in Figure 5, differential bus 140 and differential bus 142 of memory rank 150a may facilitate a daisy chain connection in which memory module 500 is connected to the memory controller via differential bus 140, and memory rank 150b is connected to memory rank 150a via differential bus 142. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory rank 150a, with memory rank 150b, etc. Differential bus 140 and differential bus 142 of memory rank

150b may facilitate a daisy chain connection in which memory rank 150a is connected to memory rank 150b via differential bus 140, and memory rank 150b is connected to another memory module 500 by differential bus 142. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory rank 150a, with memory rank 150b, with downstream device 122, etc.

[00034] Figure 6 is a block diagram of a memory apparatus 600 having two memory modules 400a and 400b interconnected by a differential bus. Those components of memory apparatus 600 that correspond to memory device 400 as shown in Figure 4 are numbered similarly. Each memory module 400 may be, for example, a single package DIMM module. While each memory module 400 may be illustrated as a single package memory module having a single memory rank 150, it will be appreciated that dual package memory modules, such as that shown and described with respect to Figure 5, are contemplated as well. As shown in Figure 6, each memory module of memory apparatus 600 may include memory devices 100a ... 100n, where n is any suitable number of memory devices. For example, each memory module 400 may have 8, 9, or 18 memory devices 100. Each memory device 100 may include an interface 104 and an interface 106. For example, as shown in Figure 6, memory devices 100a ... 100n may include respective interfaces 104a ... 104n. Each interface 104 and 106 may include a suitable number of differential signal channels 108 and 110. For example, as shown in Figure 6, each of interfaces 104a ... 104n may include a respective differential signal channel 108a ... 108n to facilitate connection to and/or communication with an upstream device 120, and each of interfaces 106a ... 106n may include a respective differential signal channel 110a ... 110n to facilitate connection to and/or communication with a downstream device 122. Each differential signal channel 108 and 110 may be a bidirectional signal channel.

[00035] As shown in Figure 6, for each of memory modules 400a and 400b, interfaces 104a ...104n from each of memory devices 100a ... 100n may be ganged to form a differential bus 140. Similarly, interfaces 106a ...106n from each of memory devices 100a ... 100n may be ganged to form a differential bus 142. Differential bus 140 may facilitate communication with an upstream device 120, and differential bus 142 may facilitate communication with a downstream device. Differential bus 140 and differential bus 142 may facilitate point-to-point daisy chain connections and/or communications with or via memory module 400 similar to those described above with reference to Figures 1A, 1B, 1C, and 4. For example, with respect to memory module 400a, upstream device 120 may be a memory controller, and memory module 400b may be a downstream device. With respect to memory module 400b, memory module 400a may be an upstream device, and downstream device 122 may be a memory rank of another memory module 400. As shown in Figure 6, differential bus 140 and differential bus 142 of memory module 400a may facilitate a daisy chain connection in which memory module 400a is connected to the memory controller via differential bus 140, and memory module 400b is connected to memory module 400a via differential bus 142. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory module 400a, with memory module 400b, etc. Differential bus 140 and differential bus 142 of memory module 400b may facilitate a daisy chain connection in which memory module 400a is connected to memory module 400b via differential bus 140, and memory module 400b is connected to another memory module 400 by differential bus 142. Using the daisy chain connection, the memory controller may establish a point-to-point connection with memory module 400a, with memory module 400b, with downstream device 122, etc.

[00036] Although the present disclosure has been described with reference to example implementations, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the claimed subject matter. For example, although different

example implementations may have been described as including features providing one or more benefits, it is contemplated that the described features may be interchanged with one another or alternatively be combined with one another in the described example implementations or in other alternative implementations. Because the technology of the present disclosure is relatively complex, not all changes in the technology are foreseeable. The present disclosure described with reference to the example implementations and set forth in the following claims is manifestly intended to be as broad as possible. For example, unless specifically otherwise noted, the claims reciting a single particular element also encompass a plurality of such particular elements.

WHAT IS CLAIMED IS:

- 1 1. A memory device, comprising:
2 a storage array;
3 a first differential interface coupled to the storage array and
4 including a first bidirectional signal channel to facilitate communication with an
5 upstream device; and
6 a second differential interface coupled to the first differential
7 interface and including a second bidirectional signal channel to facilitate
8 communication with a downstream device.
- 1 2. The memory device of claim 1, wherein the memory device is a first
2 memory device, wherein the upstream device is a memory controller and the
3 downstream device is a second memory device.
- 1 3. The memory device of claim 1, wherein the storage array is a
2 dynamic random access memory array.
- 1 4. The memory device of claim 1, wherein the first and second
2 differential interfaces facilitate point-to-point daisy chain connections to the
3 upstream device and the downstream device via first and second differential
4 buses.
- 1 5. The memory device of claim 1, wherein the first and second
2 bidirectional signal channels facilitate communication with an upstream device
3 using one of a synchronous protocol and a split transaction protocol.
- 1 6. The memory device of claim 1, further comprising a switching
2 device to selectively couple the first bidirectional signal channel to one of the
3 storage array and the second bidirectional signal channel.

1 7. A memory module, comprising:
2 first and second memory devices, each of the first and second
3 memory devices including
4 a respective storage array;
5 a respective first differential interface coupled to the
6 respective storage array and including a respective first bidirectional signal
7 channel; and
8 a respective second differential interface coupled to the
9 respective first differential interface and including a respective second
10 bidirectional signal channel; and
11 wherein the first differential interfaces form a first differential bus to
12 facilitate communication with an upstream device, and wherein the second
13 differential interfaces form a second differential bus to facilitate communication
14 with a downstream device.

1 8. The memory module of claim 7, wherein the first and second
2 memory devices form a first memory rank, and further comprising a second
3 memory rank coupled to the first memory rank via the second differential bus.

1 9. The memory module of claim 7, wherein the upstream device is a
2 memory controller and the downstream device is a second memory module.

1 10. The memory module of claim 7, wherein the memory module is a
2 dual in-line memory module.

1 11. The memory module of claim 7, wherein the first and second
2 differential buses facilitate point-to-point daisy chain connections to the upstream
3 device and the downstream device.

1 12. A memory apparatus, comprising:

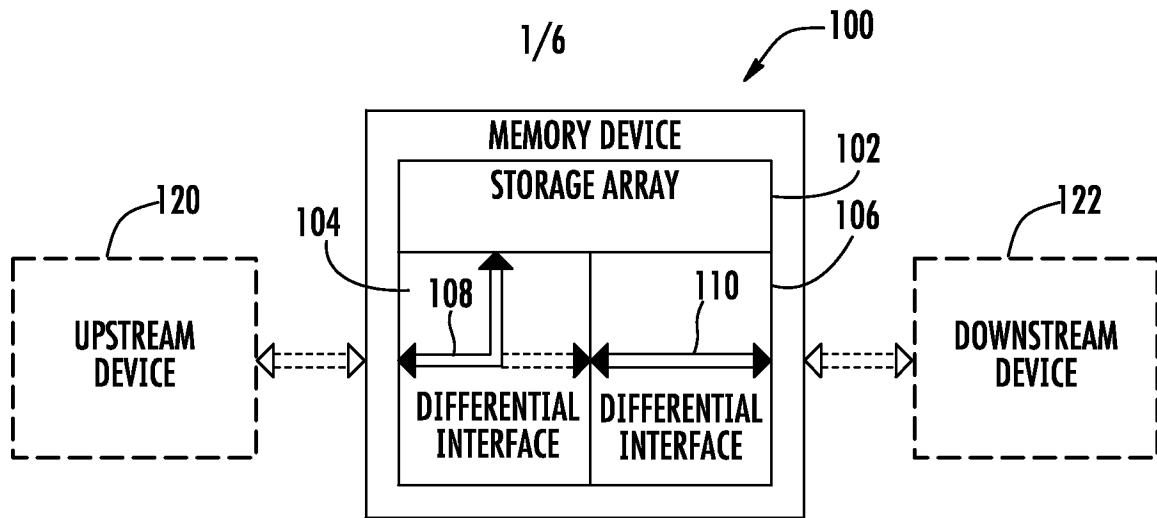
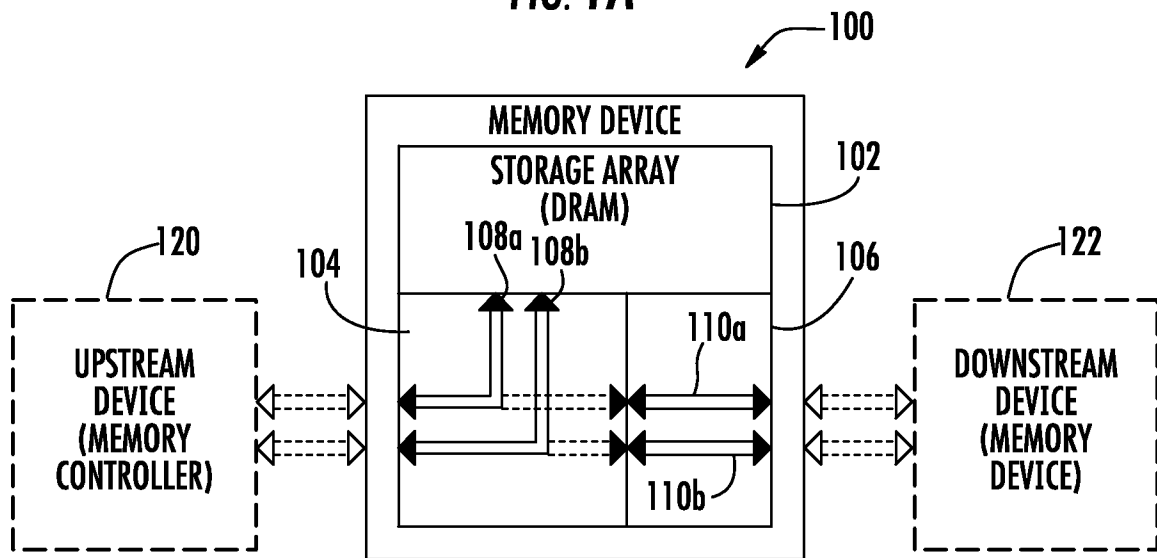
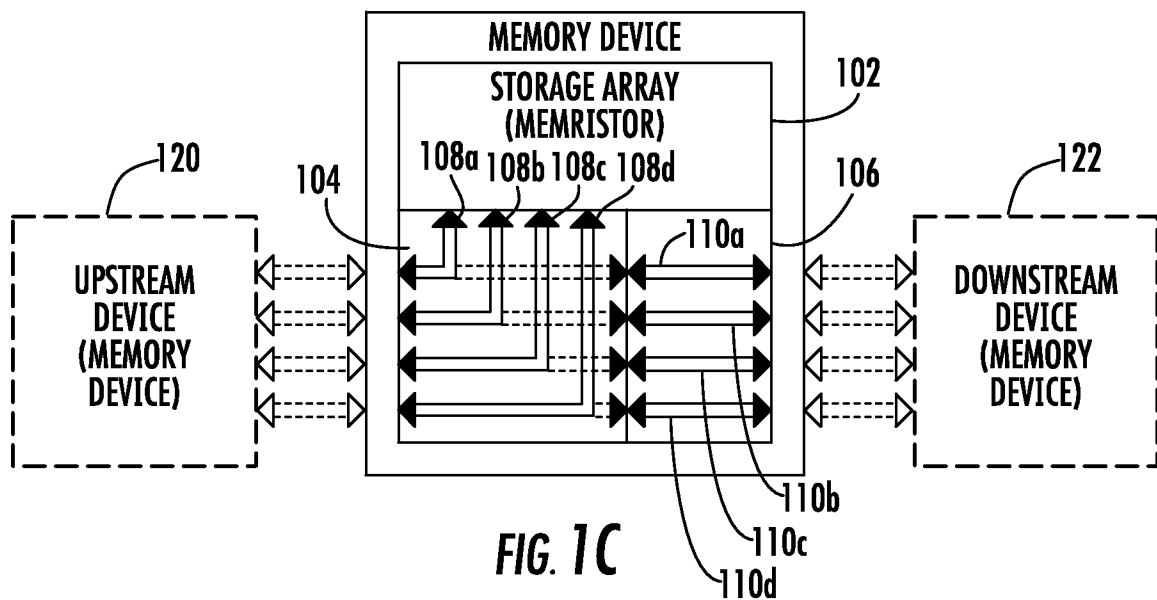
2 first and second memory modules, wherein each of the first and
3 second memory modules includes a respective memory rank having respective
4 memory devices, and wherein each respective memory device includes
5 a respective storage array;
6 a respective first differential interface coupled to the
7 respective storage array and including a respective first bidirectional signal
8 channel to facilitate communication with an upstream device; and
9 a respective second differential interface coupled to the
10 respective first differential interface and including a respective second
11 bidirectional signal channel to facilitate communication with a downstream
12 device; and
13 wherein the second differential interface of the memory rank of the
14 first module is coupled to the first differential interface of the memory rank of the
15 second module.

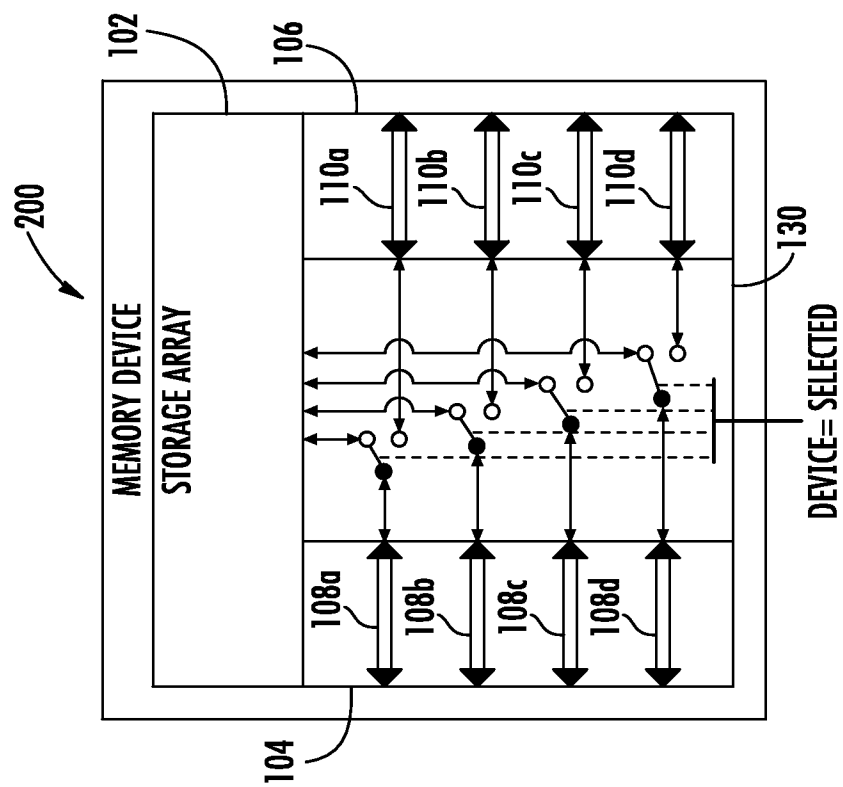
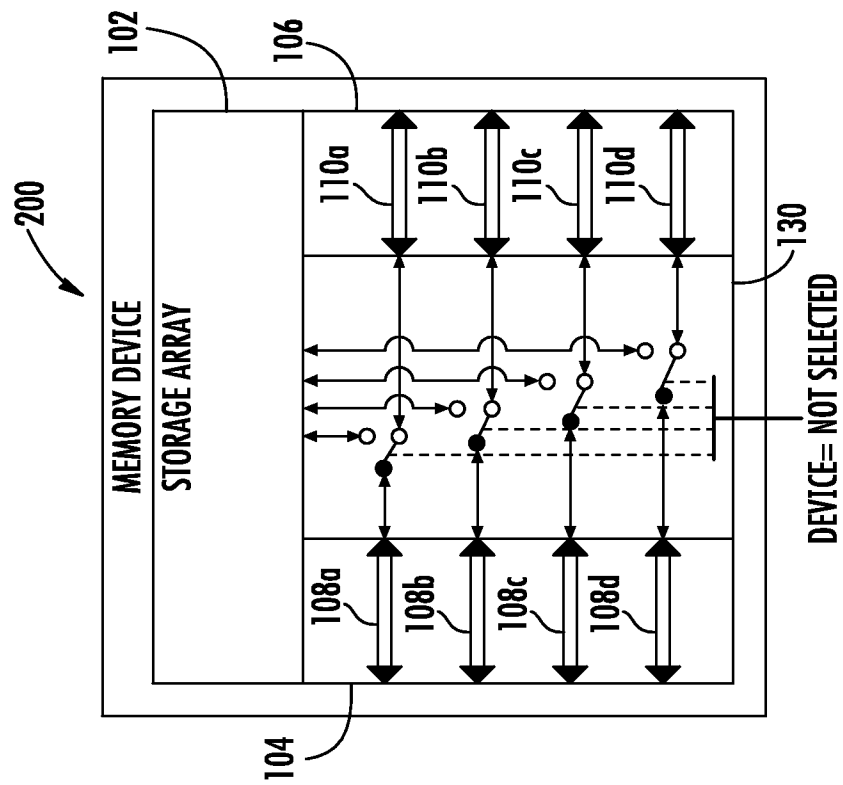
1 13. The memory apparatus of claim 12, further comprising a memory
2 controller, wherein the memory controller is coupled to the first differential
3 interface of the memory rank of the first memory module.

1 14. The memory apparatus of claim 12, wherein the first and second
2 differential buses facilitate point-to-point daisy chain connections to the upstream
3 and downstream devices.

1 15. The memory apparatus of claim 12, the storage arrays are dynamic
2 random access memory arrays, and wherein the memory modules are dual in-
3 line memory modules.

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**FIG. 1A****FIG. 1B****FIG. 1C**



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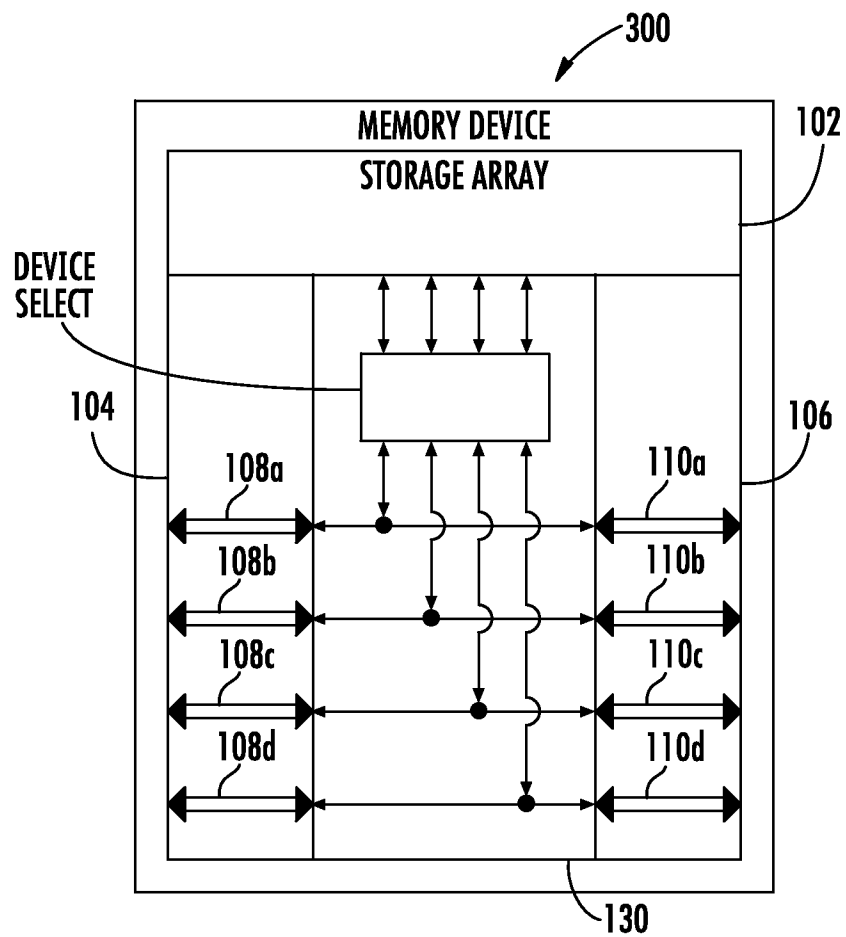


FIG. 3

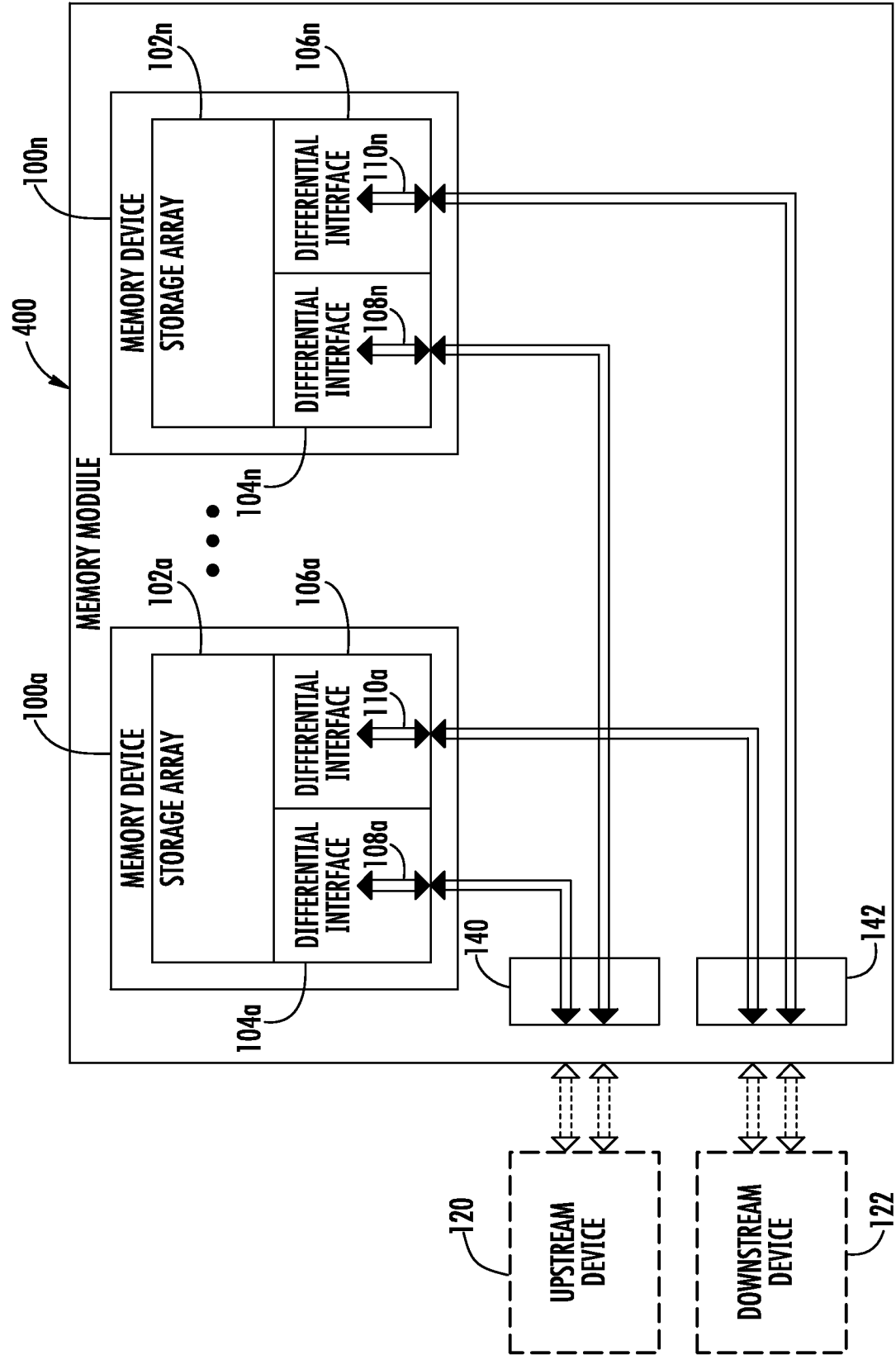


FIG. 4

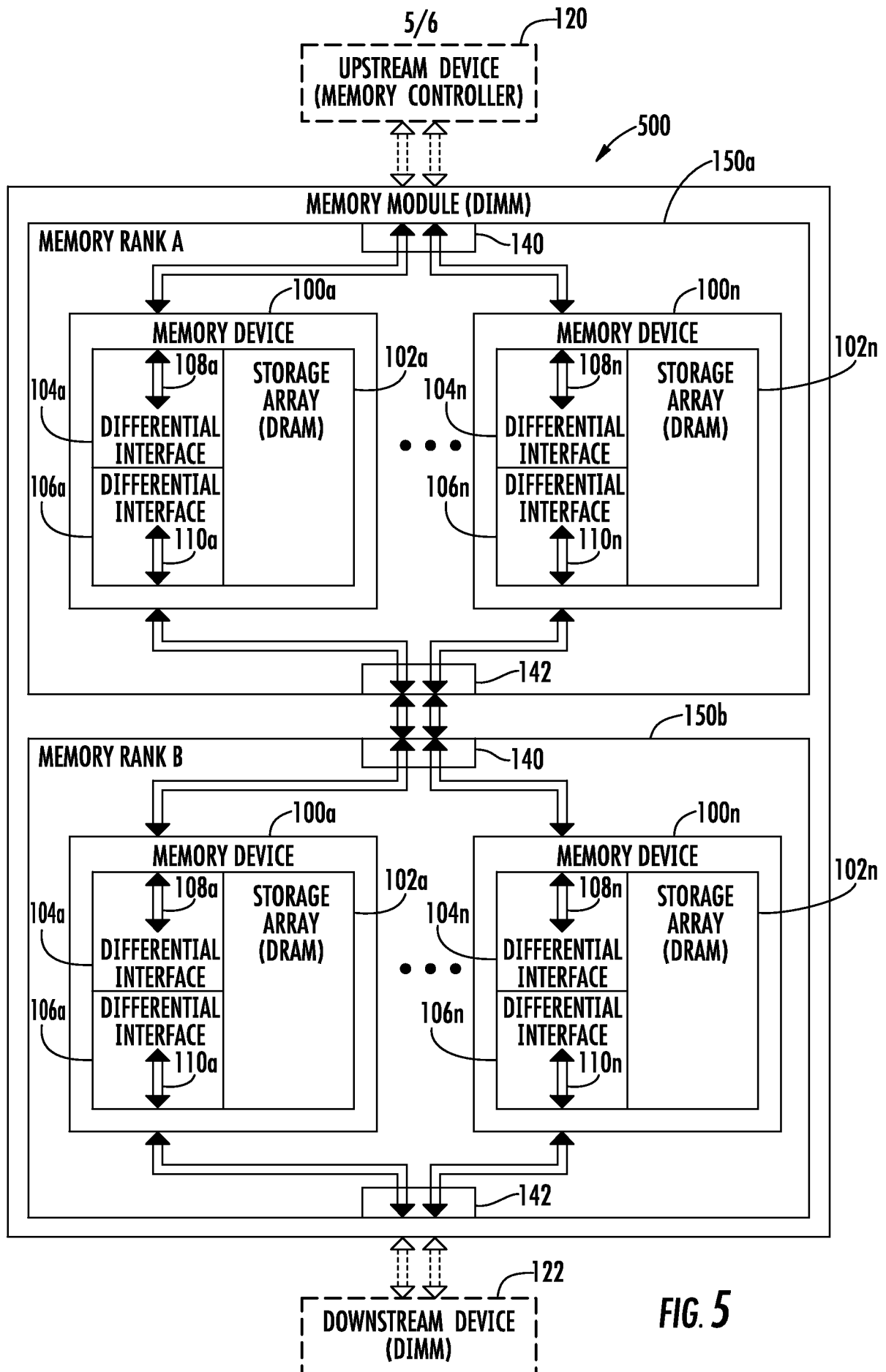


FIG. 5

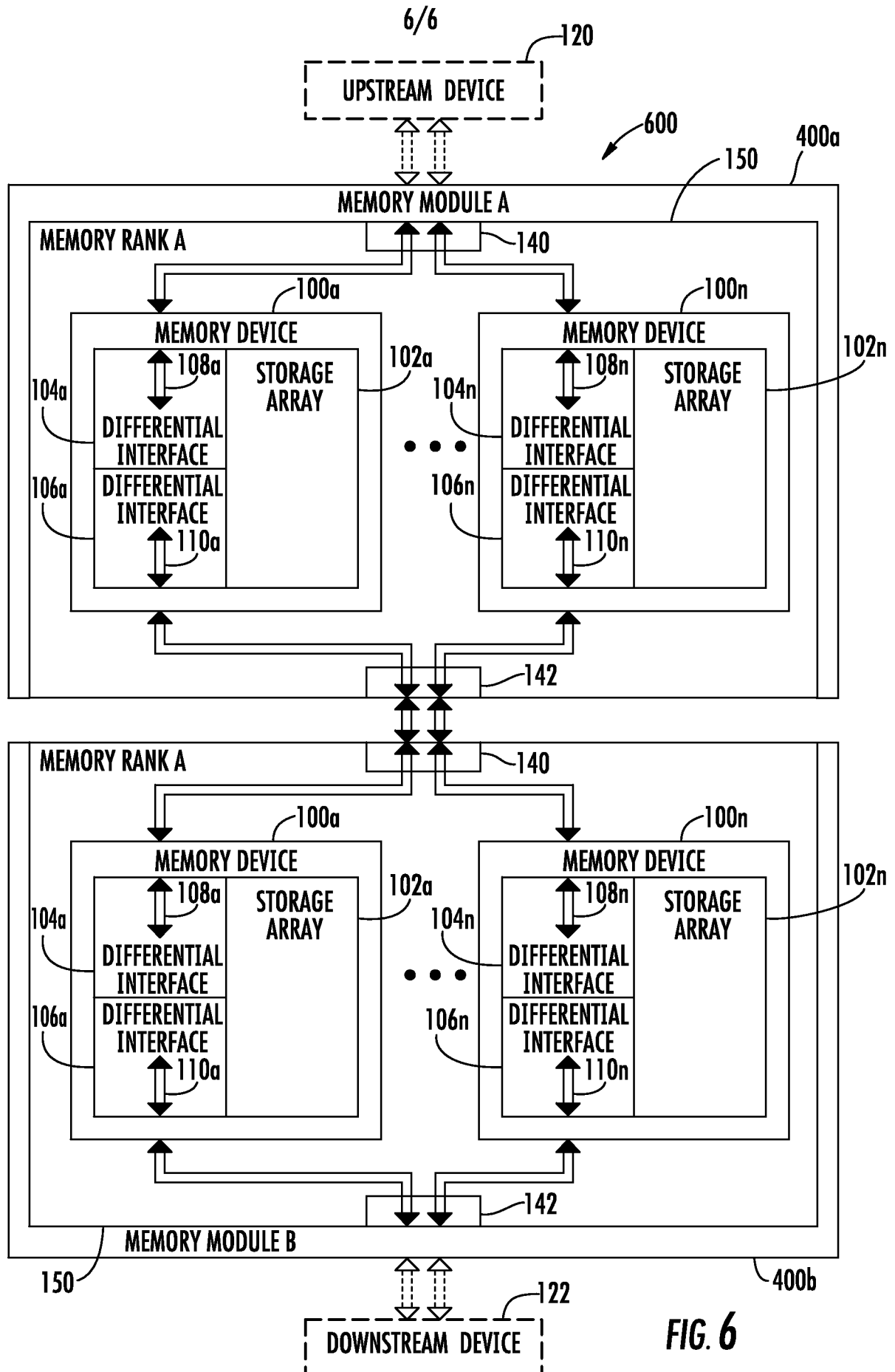


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/028256**A. CLASSIFICATION OF SUBJECT MATTER****G06F 12/06(2006.01)i, G06F 12/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 12/06; G06F 13/40; G06F 3/00; G06F 13/16; H04L 12/56; G06F 12/08

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: memory device, storage array, bidirectional signal, upstream, downstream, communication, DRAM, protocol, point-to-point

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0252164 A1 (KEVIN P. GRUNDY et al.) 13 October 2011 See paragraphs [0035]-[0038], [0041], [0084], [0089], [0126]; claim 1; and figures 3, 17, 23.	1-15
A	US 2007-0189313 A1 (GERALD KEITH BARTLEY et al.) 16 August 2007 See paragraphs [0060]-[0061]; and figure 8.	1-15
A	US 2013-0124763 A1 (ANALOG DEVICES, INC.) 16 May 2013 See paragraph [0101]; and figure 7.	1-15
A	US 2008-0313374 A1 (KEVIN C. GOWER et al.) 18 December 2008 See paragraph [0046]; and figure 15.	1-15
A	EP 1628225 A2 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 22 February 2006 See paragraphs [0029]-[0030]; and figure 9.	1-15



Further documents are listed in the continuation of Box C.



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Date of the actual completion of the international search

22 February 2016 (22.02.2016)

Date of mailing of the international search report

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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