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(54) **Title:** NOVEL SELF-ALIGNED QUADRUPLE PATTERNING PROCESS FOR FIN PITCH BELOW 20NM

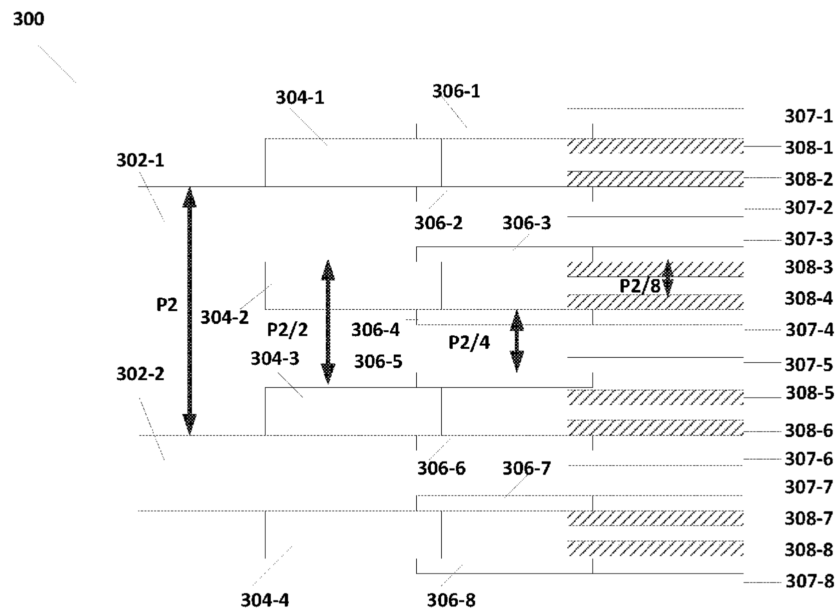
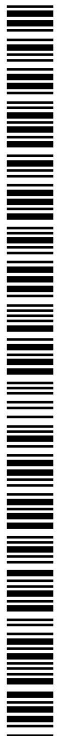


Figure 3

(57) **Abstract:** A method of producing a FinFET device with fin pitch of less than 20 nm is presented. In accordance with some embodiments, fins are deposited on sidewall spacers, which themselves are deposited on mandrels. The mandrels can be formed by lithographic processes while the fins and sidewall spacers formed by deposition technologies.



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— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
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NOVEL SELF-ALIGNED QUADRUPLE PATTERNING PROCESS FOR FIN PITCH BELOW 20nm

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Application No. 15/271,043 filed September 20, 2016, the content of which is incorporated herein by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] This application relates to production of FinFET structures with pitch below twenty (20) nanometers (nm).

BACKGROUND

[0003] Fin-type field-effect transistors (FinFETs) are increasingly being used to effectively scale integrated circuits. FinFETs, which have a vertical fin structure that function as channels, occupy less horizontal space on the semiconductor substrate and can be formed in logic areas and in memory areas through general semiconductor patterning processes.

[0004] However, the continued pressure to further scale integrated circuits has generated a demand for processes for forming smaller and smaller fin structures. The limits of optical resolution in current lithographic processes do not allow for the formation of structures having features small enough for further scaling of integrated circuits. As the demand for feature sizes of these devices continues to get smaller, there is a need to develop new processes for achieving the target sizes.

SUMMARY

[0005] In accordance with some embodiments, a method of forming fins of a two-fin FinFET device includes forming mandrels with a lithographic etch process; forming sidewall spacers on the mandrels; and forming fins on the sidewall spacers, wherein the two-fin FinFET device is formed on each of the sidewall spacers.

[0006] A method of forming a multi-fin device, can include forming one or more mandrels with a first pitch and a first width; forming sidewall spacers on each side of the one or more

mandrels, the sidewall spacers each having a second width; and forming fins on sides of the sidewall spacers, wherein the fins have a pitch of less than 20nm.

[0007] These and other embodiments are more fully discussed below with respect to the following figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1A shows a planar view of a multi-fin FinFET device.

[0009] Figure 1B shows a cross-sectional view of a multi-fin FinFET device.

[0010] Figure 2 illustrates an example process for producing a FinFET device.

[0011] Figure 3 illustrates another example process for producing a FinFET device.

[0012] Figure 4 illustrates an example process according to some embodiments of the present invention for producing a FinFET device.

[0013] Figure 5 illustrates another example process according to some embodiments of the present invention for producing a FinFET device.

[0014] Embodiments of the present disclosure and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

[0015] In the following description, specific details are set forth describing some embodiments. It will be apparent, however, to one skilled in the art that some embodiments may be practiced without some or all of these specific details. The specific embodiments disclosed herein are meant to be illustrative but not limiting. One skilled in the art may realize other elements that, although not specifically described here, are within the scope and the spirit of this disclosure.

[0016] This description and the accompanying drawings that illustrate inventive aspects and embodiments should not be taken as limiting--the claims define the protected invention. Various changes may be made without departing from the spirit and scope of this description and the

claims. In some instances, well-known structures and techniques have not been shown or described in detail in order not to obscure the disclosure.

[0017] Figures 1A and 1B illustrate a FinFET structure 100. As shown in the planar view of Figure 1A, FinFET structure 100 includes one or more parallel fins 104-1 through 104-N formed on a substrate 102. A gate structure 106 is deposited over fins 104-1 through 104-N. Modern structures may include two or more fins 104 that are uniformly separated by a pitch P. The FinFET devices can be nMOS or pMOS devices, depending on the formation of fins 104-1 through 104-N. Figure 1B illustrates a cross-sectional view of structure 100 illustrated in Figure 1A. The pitch P is defined by the space between two fins and the width of the fin, as shown in Figure 1A.

[0018] Although FinFET structure 100 illustrated in Figures 1A and 1B have increased the device density immensely, increasing the device density further leads to a need for small feature sizes and smaller pitches for the FinFET structures that are used. However, the technology has exceeded the limits of current lithographic technologies to produce FinFET structures with higher pitches. In particular, scaling the fin pitch to below 20 nm is desirable to scale logic cell height and thus overall chip sizes.

[0019] Modern lithography is wavelength limited in the production of devices with small features. Currently, 193nm lithography is limited to feature sizes of about 80nm. In other words, 193 nm lithographic processes can produce features with a minimum pitch, defined by the minimum feature width plus the minimum feature spacing, of about 80 nm using a single lithographic exposure and etch process. In order to obtain smaller pitch sizes, multiple patterning lithography (MPL) has been developed. Two forms of MPL have been attempted, one using repeated lithographic processes (litho-etch-litho-etch or LELE) techniques and another based on self-aligned spacer processing. In the production of fins for FinFET structures, the self-aligned spacer processing is favored. However, attaining smaller than 20nm pitches has proven difficult due to the process limitations.

[0020] Self-aligned spacer processing is often referred to as self-aligned double processing (SADP). In SADP, a group of mandrels are formed lithographically by patterning and etching a mandrel material. Sidewall spacers can then be formed on the sidewalls of the mandrels. The

formation of sidewall spacers can be accomplished by depositing material over the mandrel material, removing the deposited material on the horizontal surfaces, and removing the mandrel material leaving the sidewall spacers. Deposition of sidewall spacers can result in spacer widths that are much smaller than those available with lithographic formation of the mandrels. The sidewall spacers and mandrels can then be polished to expose the mandrels and the spacers used as an etch mask for removal of the remaining mandrel materials.

[0021] Consequently, the SADP process involves forming a spacer as a film layer on the sidewall of the pre-patterned mandrels, removing the spacer layer from the horizontal surfaces, and removing the originally patterned mandrel material leaving the spacers themselves. Since there are two side-wall spacers for every mandrel, the line density has now doubled. Consequently, SADP is applicable for defining narrow gates at half the original lighographic pitch. This spacer approach can, theoretically, be repeated to successively half the pitch between spacers. For example, a second SADP procedure, referred to as a self-aligned quadruple patterning (SAQP), can result in a pitch of a quarter that of the pitch of the originally formed mandrels.

[0022] Figure 2 illustrates a SAQP process 200. As illustrated in Figure 2, mandrels 202-1 through 202-4 are deposited with a pitch of P1. Figure 2 illustrates mandrels 202-1 through 202-4, however any number of mandrels 202 may be formed. As discussed above, mandrels 202 are patterned and etched using a lithographic process.

[0023] Sidewall spacers 204-1 through 204-8 are then formed on mandrels 202-1 through 202-4 in an SADP process by deposition of sidewall materials on mandrels 202, removal of the sidewall materials on the horizontal surfaces, and etching to remove mandrels 202. As illustrated in Figure 2, sidewall spacers 204-1 and 204-2 are formed on opposite sides of mandrel 202-1; sidewall spacers 204-3 and 204-4 are formed on opposite sides of mandrel 202-2; sidewall spacers 204-5 and 204-6 are formed on opposite sides of mandrel 202-3; and sidewall spacers 204-7 and 204-8 are formed on opposite sides of mandrel 202-4.

[0024] In a second SADP process on sidewall spacers 204, sidewall spacers 206-1 through 206-8 and fins 208-1 through 208-8 are formed on the sidewalls of sidewall spacers 204. As illustrated in Figure 2, sidewall spacer 206-1 and fin 208-1 are formed on opposite sides of

sidewall spacer 204-1; fin 208-2 and sidewall spacer 206-2 are formed on opposite sides of sidewall spacer 204-2; sidewall spacer 206-3 and fin 208-3 are formed on opposite sides of sidewall spacer 204-3; fin 208-4 and sidewall spacer 206-4 are formed on opposite sides of sidewall spacer 204-4; sidewall spacer 206-4 and fin 208-5 are formed on opposite sides of sidewall spacer 204-5; fin 208-6 and sidewall spacer 206-6 are formed on opposite sides of sidewall spacer 204-6; sidewall spacer 206-7 and fin 208-7 are formed on opposite sides of sidewall spacer 204-7; and fin 208-8 and sidewall spacer 206-8 are formed on opposite sides of sidewall spacer 204-8. Spacers 204-1 through 204-8 as well as spacers 206-1 through 206-8 are then removed, leaving fins 208-1 through 208-8. As such, fins 208-1 and 208-2 form part of a two-fin FinFET device; fins 208-3 and 208-4 form part of a two-fin FinFET device; fins 208-5 and 208-6 form part of a two-fin FinFET device; and fins 208-7 and 208-8 form part of a two-fin FinFET device. As is illustrated in Figure 2, only one fin 208 is formed on each of sidewall spacers 206.

[0025] As is further illustrated in Figure 2, at each successive SADP process, the pitch between deposited devices is halved. Consequently, if the pitch between mandrels 202 is P1, the pitch between spacers 204 is P1/2, and the final pitch between fins 208 that are in a single device is P1/4. Further, the pitch between devices is P1. Using the limitations of the 193 nm lithographic process, then P1 is 80 nm and the pitch between fins is 20nm. Consequently, a SAQP as illustrated in Figure 2 cannot produce a pitch size that is less than 20nm between fins.

[0026] Figure 3 illustrates a self-aligned octuplet process (SAOP), which can achieve a less than 20 nm pitch with the 193nm lithographic process. The SAOP is performed by three successive SADP processes, resulting in a pitch that is 1/8 that of the pitch between the mandrels. As illustrated in Figure 3, a lithographic process is used to pattern mandrels 302-1 and 302-2. Mandrels 302 are deposited with a pitch of P2. As is illustrated in Figure 3, in a first SADP process sidewall spacers 304 are then deposited on mandrels 302. Consequently, sidewall spacers 304-1 and 304-2 are formed on opposite sides of mandrel 302-1 and sidewall spacers 304-3 and 3-4-4 are formed on the opposite sides of mandrel 302-2. Mandrels 302 are then removed, leaving sidewall spacers 304. As illustrated in Figure 3, sidewall spacers 304 have a pitch of P2/2. In a second SADP process, sidewall spacers 306 are formed on sidewall spacers 304 and sidewall spacers 304 removed. As shown in Figure 3, sidewall spacers 306-1 and 306-2

are formed on opposite sides of sidewall spacer 304-1; sidewall spacers 306-3 and 306-4 are formed on opposite sides of sidewall spacer 304-2; sidewall spacers 306-5 and 306-6 are formed on opposite sides of sidewall spacers 304-3; and sidewall spacers 306-7 and 306-8 are formed on opposite sides of sidewall spacers 304-4. The pitch between sidewall spacers 306 is now P2/4.

[0027] In yet a third SADP process, sidewall spacers 307 and fins 308 are formed on sidewall spacers 306, after which both spacers 307 and spacers 306 are removed leaving fins 308. As shown in Figure 3, sidewall spacer 307-1 and fin 308-1 are formed on opposite sides of sidewall spacer 306-1; fin 308-2 and sidewall spacer 307-2 are formed on opposite sides of sidewall spacer 306-2; sidewall spacer 307-3 and fin 308-3 are formed on opposite sides of sidewall spacer 306-3; fin 308-4 and sidewall spacer 307-4 are formed on opposite sides of sidewall spacer 306-4; sidewall spacer 307-5 and fin 308-5 are formed on opposite sides of sidewall spacer 306-5; fin 308-6 and sidewall spacer 307-6 are formed on opposite sides of sidewall spacer 306-6; sidewall spacer 307-7 and fin 308-7 are formed on opposite sides of sidewall spacer 306-7; and fin 308-8 and sidewall spacer 307-8 are formed on opposite sides of sidewall spacer 306-8. The resulting pitch between fins 308 and sidewall spacers 307 is, then, P2/8. Again, only one fin 308 is formed on each of sidewall spacers 306.

[0028] If P2 is, for example, 128nm, then P2/2 is 64nm; P2/4 is 32nm; and P2/8 is 16nm. Consequently, a pitch of 16nm is achievable, with a device separation (after the removal of dummy fins or sidewall spacers 307 of 32nm, using the SAOP process. However, the third SADP process required to achieve requires too many process steps, increasing costs and complicating the process, and is difficult to achieve within the constraints of materials depositions processes.

[0029] Figure 4 illustrates an example of a SAQP process according to some embodiments of the present invention for achieving a two-fin device with a pitch of less than 20 nm. As shown in Figure 4, mandrels 402 are deposited in a lithographic process. Mandrels 402-1 and 402-2 are illustrated in Figure 4. Mandrels 402-1 and 402-2 are deposited with a pitch P3 and width W1. Sidewall spacers 404 are deposited on the sidewalls of mandrels 402. Consequently, sidewall spacers 404-1 and 404-2 are formed on opposite sides of mandrel 402-1 and sidewall spacers 404-3 and 404-4 are formed on opposite sides of mandrel 402-2. However, instead of arranging

the width W2 of sidewall spacers 404 such that a pitch between sidewall spacers 404 is P3/2, the width W2 of sidewall spacers 404 is arranged to affect the final pitch of fins 406.

[0030] As illustrated in Figure 4, fins 406 are formed on the sidewalls of side-wall spacers 404. As illustrated, fins 406-1 and 406-2 are formed on opposite sides of sidewall spacer 404-1; fins 406-3 and 406-4 are formed on opposite sides of sidewall spacer 404-2; fins 406-5 and 506-6 are formed on opposite sides of sidewall spacer 404-3; and fins 406-7 and 406-8 are formed on opposite sides of sidewall spacer 404-4. In some embodiment, the width W2 of sidewall spacers 404 and the width W3 of fins 406 are the same.

[0031] As is further illustrated in Figure 4, mandrels 402 may be formed with a pitch of P3. Fins 406 in each device have a pitch of P and devices have a pitch separation of D. As an example, the pitch P can be made 16nm if the width W2 of sidewall spacers 404 and W2 of fins 406 sum to 16 nm. As an example, if W2 and W3 are both 8 nm, which is an achievable dimension for deposition of sidewall materials using a 7nm process technology, then the pitch P is 16 nm. The pitch of sidewall spacers 404 PS can be arranged to be P3/2 by varying the widthW1 of mandrels 402 and the width of spacers W2. The separation D between the resulting two-fin devices is given by the sum of W1 and W2. However, the spacing between mandrels 402 may not result in an even distance between each of sidewall spacers 404.

[0032] Consequently, as illustrated in Figure 4, fins with small pitch, pitch less than 20nm, are formed in a process that includes formation of mandrels 402 with a width of W1 and pitch of P3 with a lithographic etch process. Sidewall spacers 404 are formed by deposition of material on the sides of mandrels 402, and mandrel material is removed to leave sidewall spacers 404. Sidewall spacers 404 each have a width W2 and sidewall spacers have a pitch of PS. Fins 406 are then formed on the sidewall of spacers 404, with each spacer 404 providing for a single two-fin device formation. As a result, once spacers 404 are removed, none of the fins 406 deposited on the sidewall are removed (i.e. there is no dummy spacer removal). In some embodiments, the mandrel pitch P3 can be used to separate NMOS from PMOS FinFET devices.

[0033] The example embodiment of the present invention illustrated in Figure 4 can produce fin pitches of less than 20nm primarily because the fin pitch is dependent only on the ability to deposit sidewall spacers 404 and fins 406 within a particular width. In the 7nm technologies,

those deposition widths can be as low as 7 nm, and 8nm widths or above are available. Separation between devices, D, remains dependent on the process limitations involved in forming mandrels 402.

[0034] Figure 5 illustrates an example of a process according to some embodiments of the present invention for producing a multi-fin FinFET device where the number of fins is greater than two. Although, due to the limitations of the process technologies, fin pitches of less than 20nm may not be easily achieved, the process illustrated in Figure 5 can be used to produce multi-fin devices where the fin-pitch can be larger than 20nm.

[0035] As shown in Figure 5, mandrels 502 are formed with a lithographic and etch process. Mandrels 502 (mandrels 502-1 through 502-4 are illustrated) have a pitch of P4 and a width of W1, within the limits of resolution of the lithographic process. As is further shown, sidewall spacers 504 are formed on mandrels 502. In particular, sidewall spacers 504-1 and 504-3 are formed on opposite sides of mandrel 502-1; sidewall spacers 504-3 and 504-4 are formed on opposite sides of mandrel 502-2; sidewall spacers 504-5 and 504-6 are formed on opposite sides of mandrel 502-3; and 504-7 and 504-8 are formed on opposite sides of mandrel 502-4.

[0036] As is further illustrated, fins 506 and sacrificial sidewall spacers 507 are formed on sidewall spacers 504. Figure 5 illustrates production of a 3-fin device, however, a four-fin device can also be produced using sidewalls 504 on a single mandrel 502. A device with more than four fins can be produced using sidewalls 504 from adjacent mandrels 502.

[0037] In the example 3-fin device illustrated in Figure 5, fins for each device may span adjacent mandrels 502. As illustrated in Figure 5, fins 506-1 and 506-2 are formed on opposite sides of sidewall spacer 504-1. Sacrificial spacers 507-1 and 507-2 formed on opposite sides of sidewall spacer 504-2 during the formation of fins 506 and removed. Fins 506-3 and 506-4 are formed on opposite sides of sidewall spacer 504-3 and fin 506-5, which forms the third fin of a device that includes fins 506-3, 506, and 506-5, is formed on a first side of sidewall spacer 504-4. Sacrificial spacer 507-3 is formed on a second side of sidewall spacer 504-4. As is further illustrated in Figure 5, sacrificial sidewall spacer 507-4 and fin 506-6 are formed on opposite sides of sidewall spacer 504-5; fins 506-7 and 506-8 are formed on opposite sides of sidewall spacer 504-6; sacrificial sidewall spacers 507-5 and 507-6 are formed on opposite sides of

sidewall spacer 504-7; and fins 506-9 and 506-10 are formed on opposite sides of sidewall spacer 504-8.

[0038] Consequently, as illustrated in Figure 5, provided that a larger fin-pitch can be tolerated, devices with more than two fins can be formed according to some embodiments of the present invention. As illustrated in Figure 5, the spacing between fins 506 is determined by width W2 of sidewall spacer 504. Consequently, the fin pitch, which is shown as P4/4 as an example in Figure 5, is given by the sum of the width W2 of sidewall spacer 504 and the width W3 of sidewall spacer w3. The width of mandrel 502, W1, can be adjusted to produce an overall pitch of P4/4 for the multi-fin device. In some embodiments, the width of spacers 504, W2, and the width of fins 506, W3, are the same.

[0039] In the preceding specification, various embodiments have been described with reference to the accompanying drawings. It will, however, be evident that various modifications and changes may be made thereto, and additional embodiments may be implemented, without departing from the broader scope of the invention as set for in the claims that follow. The specification and drawings are accordingly to be regarded in an illustrative rather than restrictive sense.

CLAIMS

What is claimed is:

1. A method of forming fins of a two-fin FinFET device, comprising:
forming mandrels with a lithographic etch process;
forming sidewall spacers on the mandrels; and
forming fins on the sidewall spacers,
wherein the two-fin FinFET device is formed on each of the sidewall spacers.

2. The method of claim 1, wherein a pitch of the two-fin FinFET device is less than 20nm.

3. The method of claim 1, wherein separation between a pair of the two-fin FinFET devices is determined by a width of the mandrel.

4. The method of claim 1, wherein a distance between mandrels can separate nMOS FinFET devices from pMOS FinFET devices.

5. The method of claim 1, wherein a pitch of the two-fin FinFET device is determined by a sidewall spacer width and a fin width.

6. The method of claim 1, further including removing the mandrels and the sidewall spacers.

7. A method of forming a multi-fin device, comprising:
forming one or more mandrels with a first pitch and a first width;
forming sidewall spacers on each side of the one or more mandrels, the sidewall spacers each having a second width; and
forming fins on sides of the sidewall spacers, wherein the fins have a pitch of less than 20nm.

8. The method of claim 7, wherein the mandrels are formed with a lithographic exposure and etch process.

9. The method of claim 7, wherein the sidewall spacers and the fins are deposited with materials deposition technology.

10. The method of claim 9, wherein the materials deposition technology is a 7nm technology.

11. The method of claim 7, further including removing the mandrels and the sidewall spacers to leave the fins.

12. The method of claim 7, wherein the multi-fin device is a two-fin device, the two fin device formed on one of the sidewall spacers.

13. The method of claim 12, wherein adjacent two-fin devices are separated according to the width of the mandrel.

14. The method of claim 7, wherein the multi-fin device includes more than two fins formed on adjacent sidewall spacers.

15. A multi-fin device, comprising:

a plurality of fins formed by deposition on sidewall spacers, the sidewall spacers having been separated by mandrels,

wherein a pitch of the plurality of fins is less than 20nm.

16. The multi-fin device of claim 15, wherein the plurality of fins includes two fins formed on opposite sides of one sidewall spacer.

17. The multi-fin device of claim 16, wherein the two-fins are separated from another two-fin device.

18. The multi-fin device of claim 15, wherein the plurality of fins includes more than two fins formed on sides of adjacent sidewall spacers.

19. The multi-fin device of claim 15, wherein the sidewall spacers are removed.

20. A multi-fin device, comprising:

means for providing a plurality of fins with a pitch of less than 20 nm.

21. The multi-fin device of claim 20, wherein the means for providing a plurality of fins includes

means for depositing mandrels; and

means for depositing sidewall spacers on the mandrels.

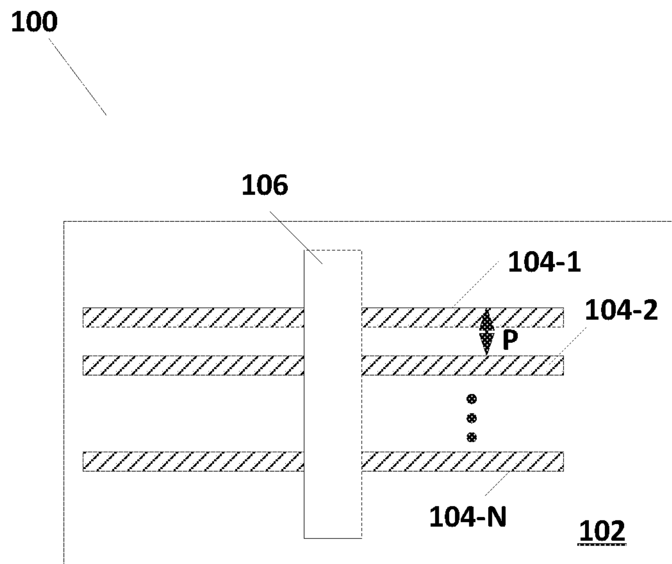


Figure 1A

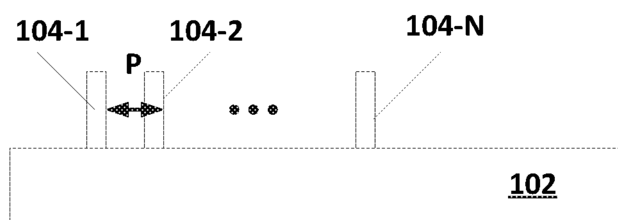


Figure 1B

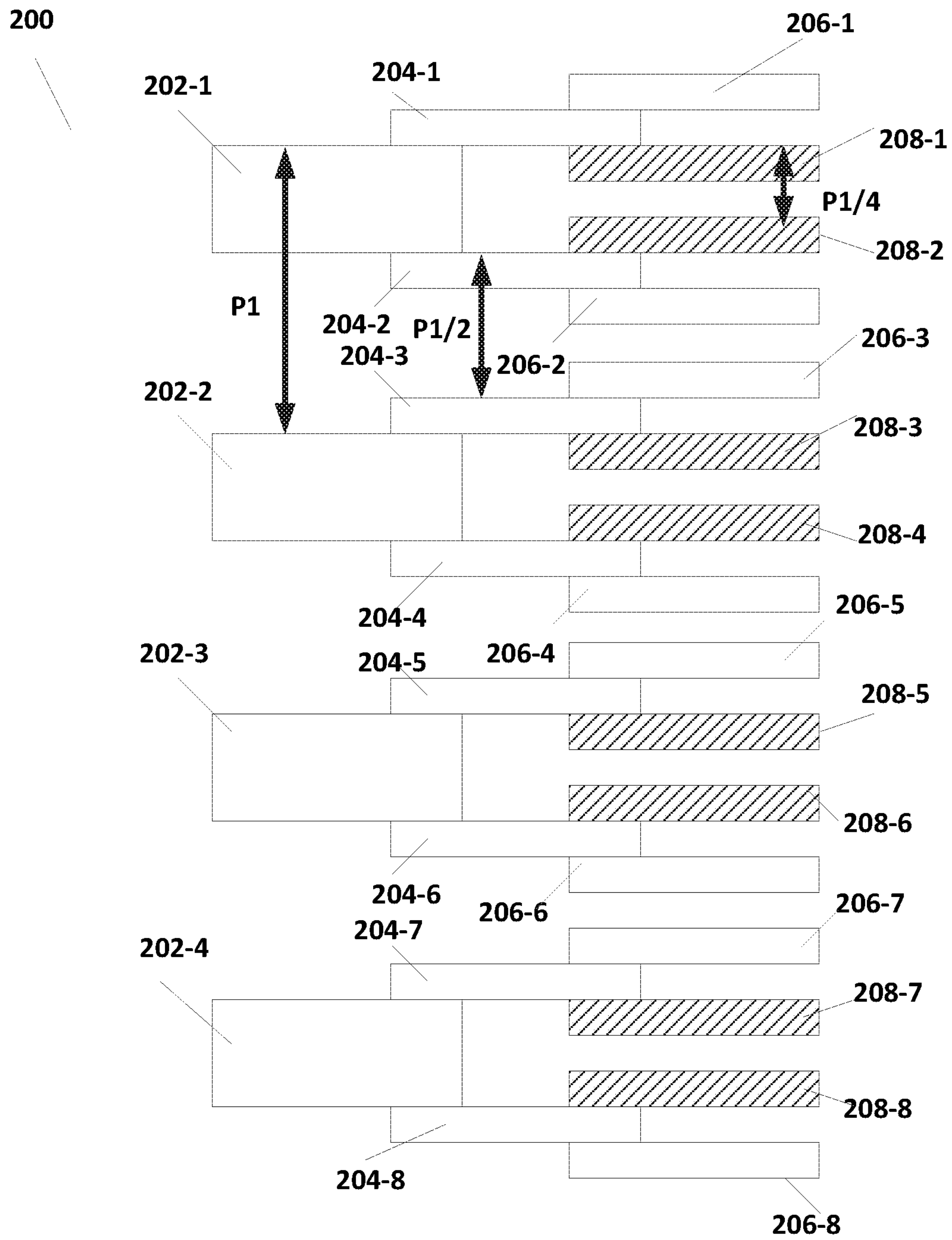


Figure 2

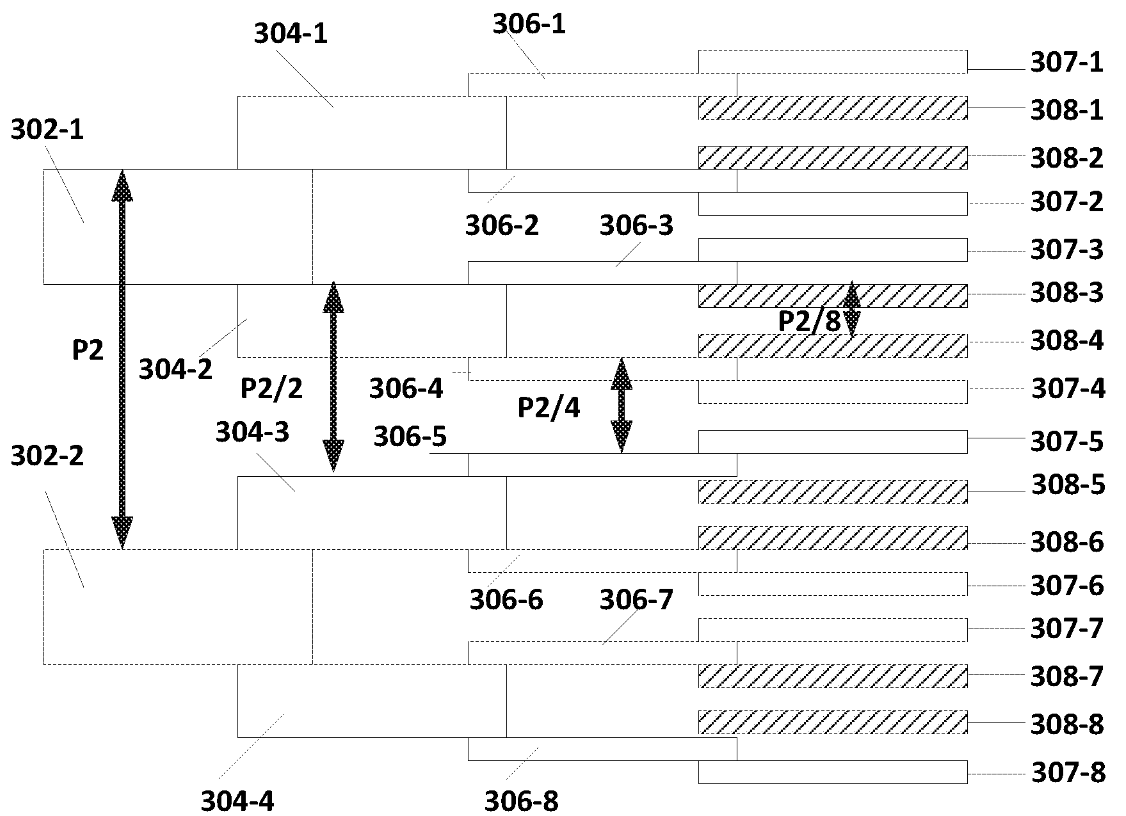


Figure 3

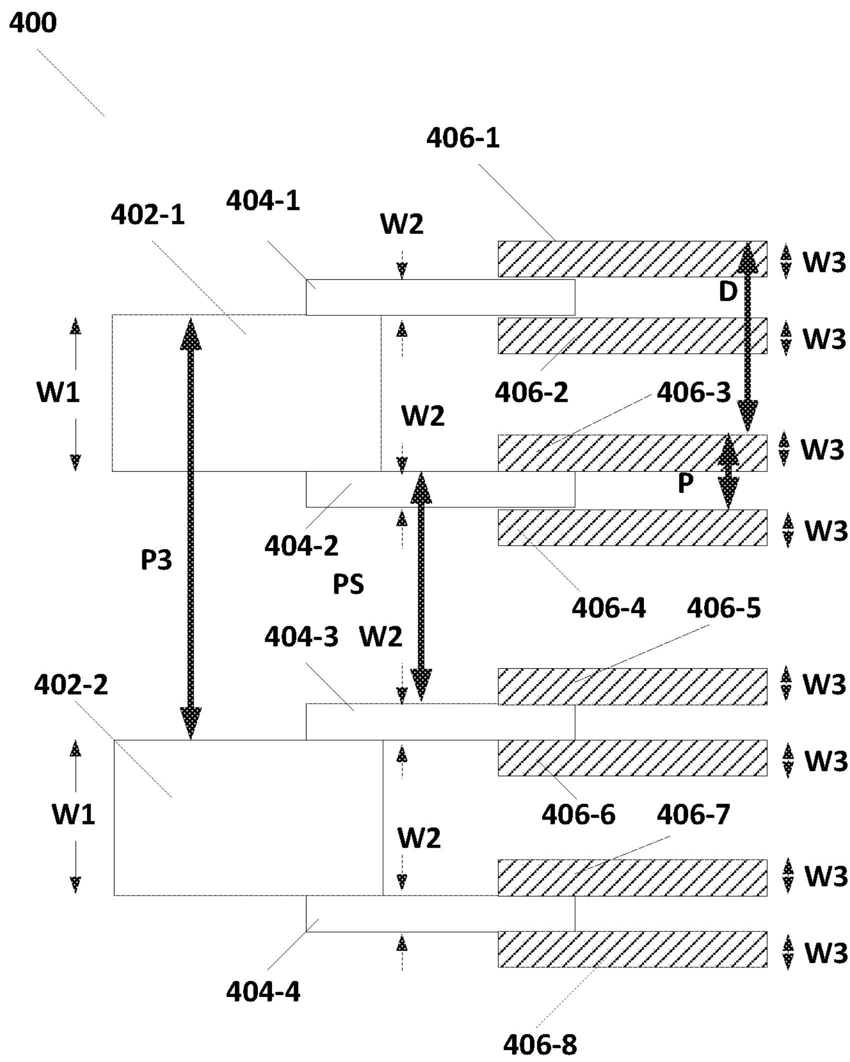
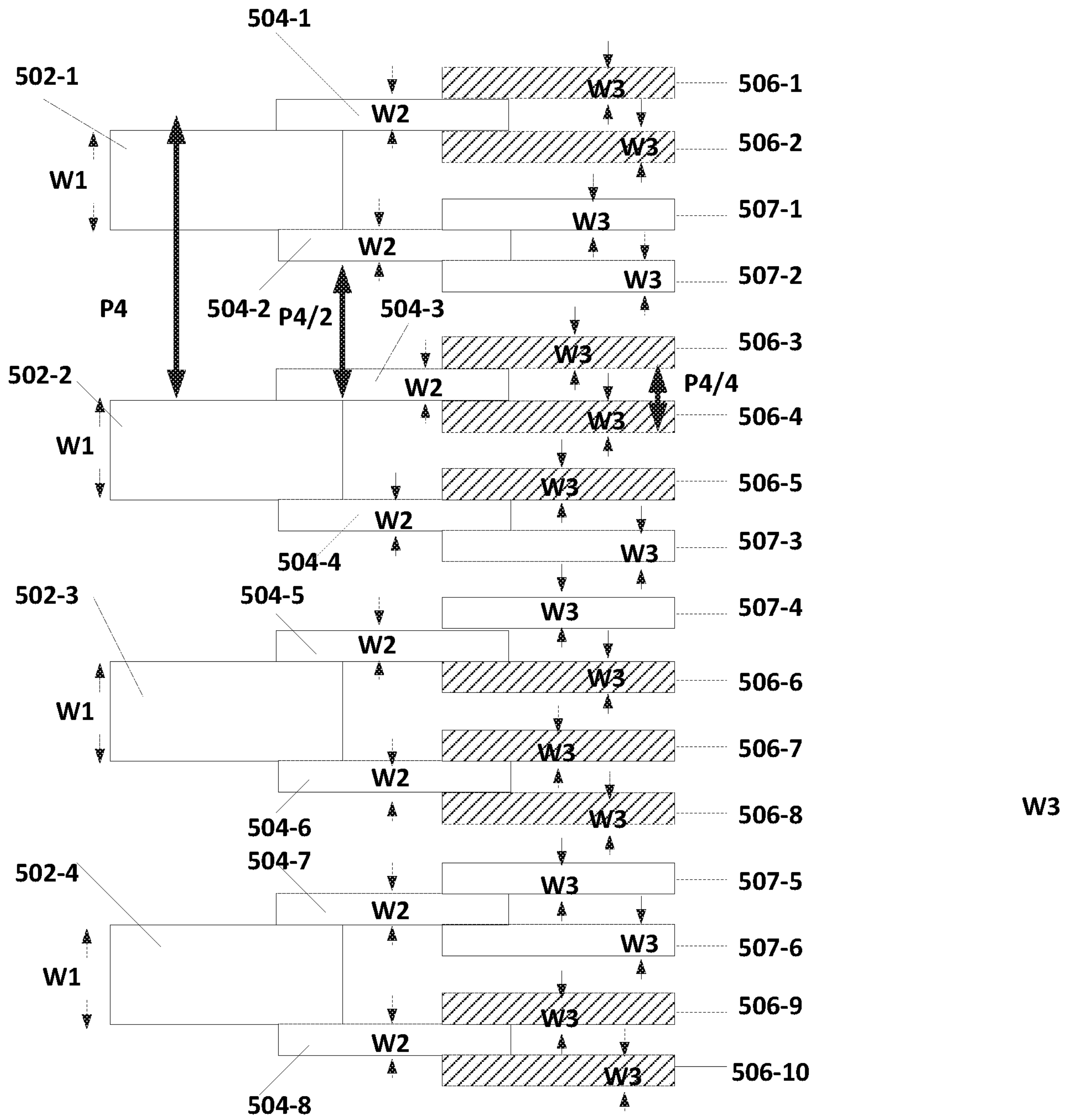


Figure 4

500



W3

Figure 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/045966

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/66 H01L21/308 H01L21/84
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/181164 A1 (CHENG KANGGUO [US] ET AL) 23 June 2016 (2016-06-23) paragraph [0005] - paragraph [0043]; figures 1-17	1-21
A	US 2014/231913 A1 (LEOBANDUNG EFFENDI [US]) 21 August 2014 (2014-08-21) paragraph [0002] - paragraph [0043]; figures 1-7	1-21
A	US 9 123 659 B1 (FU SSU-I [TW] ET AL) 1 September 2015 (2015-09-01) column 1 - column 10; figures 1-30	1-21
A	US 2013/196508 A1 (LICAUSI NICHOLAS V [US]) 1 August 2013 (2013-08-01) paragraph [0013] - paragraph [0040]; figures 1-4	1-21

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
18 October 2017	26/10/2017

Name and mailing address of the ISA/	Authorized officer
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