(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 September 2010 (02.09.2010)

PCT

(10) International Publication Number
WO 2010/097191 A1

(51) International Patent Classification:
H01L 21/60 (2006.01) *H01L 23/485* (2006.01)

(21) International Application Number:
PCT/EP2010/001092

(22) International Filing Date:
22 February 2010 (22.02.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10 2009 010 885.8
27 February 2009 (27.02.2009) DE

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: A METALLIZATION SYSTEM OF A SEMICONDUCTOR DEVICE INCLUDING METAL PILLARS HAVING A REDUCED DIAMETER AT THE BOTTOM

(57) Abstract: In a metallization system of a complex semiconductor device, metal pillars (271) such as copper pillars may be formed in a nail-like configuration in order to reduce the maximum mechanical stress acting on the metallization system while providing a required contact surface for connecting to the package substrate. The nail-like configuration may be obtained on the basis of appropriately configured resist masks.

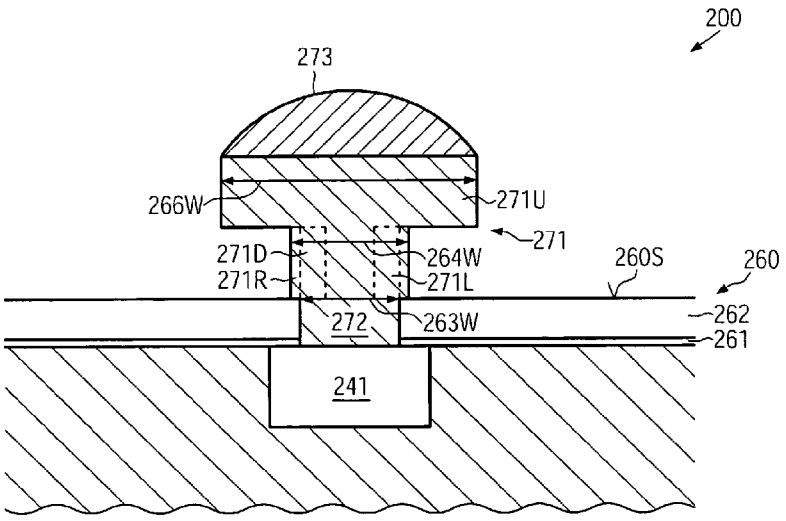

FIG. 2e

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A METALLIZATION SYSTEM OF A SEMICONDUCTOR DEVICE INCLUDING METAL PILLARS HAVING A REDUCED DIAMETER AT THE BOTTOM

FIELD OF THE PRESENT DISCLOSURE

Generally, the present disclosure relates to integrated circuits having metallization systems including metal pillars and more particularly to the techniques for reducing chip-package interactions caused by thermal mismatch between the chip and the package.

DESCRIPTION OF THE PRIOR ART

Semiconductor devices are typically formed on substantially disc-shaped substrates made of any appropriate material. The majority of semiconductor devices including highly complex electronic circuits is currently and, in the foreseeable future, will be manufactured on the basis of silicon, thereby rendering silicon substrates and silicon containing substrates, such as SOI (silicon on insulator) substrates, viable base materials for forming semiconductor devices, such as microprocessors, SRAMs, ASICs (application specific ICs), systems on chip (SoC), and the like. The individual integrated circuits are arranged in an array on the wafer, wherein most of the manufacturing steps, which may involve several hundred and more individual process steps in sophisticated integrated circuits, are performed simultaneously for all chip areas on the substrate, except for photolithography processes, metrology processes and packaging of the individual devices after dicing the substrate. Thus, economical constraints drive semiconductor manufacturers to steadily increase the substrate dimensions, thereby also increasing the area available for producing actual semiconductor devices and thus increasing production yield.

In addition to increasing the substrate area, it is also important to optimize the utilization of the substrate area for a given substrate size so as to actually use as much substrate area as possible for semiconductor devices and/or test structures that may be used for process control. In the attempt to maximize the useful surface area for a given substrate size, the feature sizes of circuit elements are steadily scaled down. Due to this ongoing demand for shrinking the feature sizes of highly

sophisticated semiconductor devices copper in combination with a low-K dielectric material has become a frequently used alternative in the formation of so-called interconnect structures comprising metal line layers and intermediate via layers that include metal lines as intra-layer connections and vias as inter-layer connections, which commonly connect individual circuit elements to provide for the required functionality of the integrated circuit. Typically, a plurality of metal line layers and via layers stacked on top of each other is necessary to realize the connections between all internal circuit elements and I/O (input/output), power and ground pads of the circuit design under consideration.

For extremely scaled integrated circuits the signal propagation delay is no longer limited by the circuit elements, such as field effect transistors, and the like, but is limited, owing to the increased density of circuit elements requiring an even more increased number of electrical connections, by the close proximity of the metal lines, since the line-to-line capacitance is increased in combination with a reduced conductivity of the lines due to a reduced cross sectional area. For this reason, traditional dielectrics such as silicon dioxide (k>4) and silicon nitride (k>7) are replaced by dielectric materials having a lower permittivity, which are therefore also referred to as low-k dielectrics having a relative permittivity of 3 or less. However, the density and mechanical stability or strength of the low-k materials may be significantly less compared to the well-approved dielectrics silicon dioxide and silicon nitride. As a consequence, during the formation of the metallization system and any subsequent manufacturing processes of integrated circuits production yield may depend on the mechanical characteristics of sensitive dielectric materials, such as low-k dielectric layers, and their adhesion to other materials.

In addition to the problems of reduced mechanical stabilities of advanced dielectric materials having a dielectric constant of 3.0 and significantly less, device reliability may be affected by these materials during operation of sophisticated semiconductor devices due to an interaction between the chip and the package caused by a thermal mismatch of the corresponding thermal expansion of the different materials. For instance, in the fabrication of complex integrated circuits increasingly a contact technology may be used in connecting the package carrier to the chip, which is known as flip chip packaging technique. Contrary to the well-established wire

bonding techniques in which appropriate contact pads may be positioned at the periphery of the very last metal layer of the chip that may be connected to corresponding terminals of the package by a wire, in the flip chip technology a respective bump structure may be formed on the last metallization layer, for instance comprised of a solder material which may be brought into contact with respective contact pads of the package. Thus, after reflowing the bump material a reliable electrical and mechanical connection may be established between the last metallization layer and the contact pads of the package carrier. In this manner a very large number of electrical connections may be provided across the entire chip area of the last metallization layer with reduced contact resistance and parasitic capacitance, thereby providing the IO (input/output) capabilities, which may be required for complex integrated circuits, such as CPUs, storage memories and the like. During the corresponding process sequence for connecting the bump structure with a package carrier a certain degree of pressure and/or heat may be applied to the composite device so as to establish a reliable connection between each of the bumps formed on the chip and the bumps or pads that may be provided on the package substrate. The thermally or mechanically induced stress may, however, also act on the lower lying metallization layers, which may typically include low-k dielectrics or even ultra low-k (ULK) dielectric materials, thereby significantly increasing the probability of creating defects by delamination of these sensitive materials due to reduced mechanical stability and adhesion to other materials.

Moreover, during operation of the finished semiconductor device attached to a corresponding package substrate also significant mechanical stress may occur due to a significant mismatch in the thermal expansion behaviour of the silicon-based semiconductor chip and the package substrate, since in volume production of sophisticated integrated circuits, economic constraints typically require the usage of specified substrate materials for the package, such as organic materials, which typically may exhibit a different thermal conductivity and a different coefficient of thermal expansion compared to the silicon chip.

In recent developments, the thermal and electrical performance of a "bump structure" is increased by providing copper pillars instead of or in addition to solder

bumps or balls, thereby reducing the required floor space for individual contact elements and also enhancing thermal and electrical conductivity due to the superior characteristics of copper compared to typically used solder material. These copper pillars may, however, contribute to an even more severe interaction between the package and the metallization system of the chip, since typically the copper pillars are significantly less deformable compared to the bump structures, which may be advantageous in view of electrical and thermal behaviour which, however, may result in even increased mechanical stress components in a locally very restricted manner, as will be described in more detail with reference to Figs 1a and 1b.

Fig 1a schematically illustrates a cross-sectional view of an integrated circuit 150 comprising a semiconductor die or chip 100 connected to a package substrate 180 that is substantially comprised of an organic material, such as appropriate polymer materials and the like, wherein the connection between the chip 100 and the package substrate 180 may be accomplished by means of a pillar structure 170. The semiconductor chip 100 may typically comprise a substrate 101, for instance a silicon substrate or an SOI substrate, depending on the overall configuration of the circuit layout and the performance of the integrated circuit 150. Moreover, a silicon-based semiconductor layer 102 may typically be provided "above" the substrate 101, wherein the semiconductor layer 102 may comprise a very large number of circuit elements, such as transistors, capacitors, resistors and the like, as are required for the desired functional behaviour of the integrated circuit 150. As previously discussed, the ongoing shrinkage of critical dimensions of circuit elements may result in critical dimensions of transistors in the order of magnitude of 50 nm and significantly less in presently available sophisticated semiconductor devices produced by volume production techniques. The semiconductor chip 100 comprises a metallization system 110, which in advanced devices includes a plurality of metallization layers, ie. of device levels, in which metal lines and vias are embedded in an appropriate dielectric material. As discussed above at least a portion of the corresponding dielectric materials used in the various metallization layers is usually comprised of materials of reduced mechanical stability in order to reduce the parasitic capacitance of adjacent metal lines.

As previously explained, the pillar structure 170 may be provided as a part of the metallization system 110, wherein the corresponding copper pillars are formed in the very last metallization layer of the system 110. On the other hand, the package substrate 180 comprises appropriately positioned and dimensioned contact pads (not shown) which may be brought into contact with corresponding pillars or any solder material formed thereon, in order to establish respective mechanical and electrical connections upon application of heat and/or mechanical pressure. Furthermore, the package substrate 180 usually comprises appropriate conductive lines in order to connect the upper pillar portions of the pillar structure 170 with corresponding terminals, which then establish an electrical interface to other peripheral components, such as a printed wiring board and the like. For convenience, any such conductive lines are not shown.

During operation of the integrated circuit 150 heat is generated within the semiconductor chip 100, for instance caused by the circuit elements formed in and above the semiconductor layer 102. This waste heat is dissipated, for instance by the metallization system 110 and the pillar structure 170 in a highly efficient manner and/or via the substrate 101, depending on the overall thermal conductivity of the substrate 101. For example, the heat dissipation capability of SOI substrates is significantly less compared to pure silicon substrates due to the reduced thermal conductivity of the buried insulating oxide layer, which separates the semiconductor layer 102 from the remaining substrate material. Thus, a major heat dissipation path is provided by the pillar structure 170 and the package substrate 180. Consequently, a moderately high average temperature is created in the semiconductor chip 100 and also in the package substrate 180 wherein, as previously discussed, a mismatch in the coefficient of thermal expansion between these two components may cause a significant mechanical stress. As is for instance indicated by arrows 103 and 183, the package substrate 180 may have an increased thermal expansion compared to the semiconductor chip 100, wherein a corresponding mismatch therefore results in a significant degree of thermal stress, in particular at the "interface" between the semiconductor chip 100 and the package substrate 180, that is, in particular the pillar structure 170 and the metallization system 110 may experience significant shear forces caused by the thermal mismatch during the operation of the integrated circuit 150. Due to the reduced

mechanical stability and the reduced adhesion of sophisticated dielectric materials, corresponding defects may occur, which may affect the overall reliability of the integrated circuit 150. In particular, the stiffness of the individual pillars of the pillar structure 170 may result in locally high shear forces, which are transferred into the metallization system, however in a locally very restricted area, resulting in delamination defects and the like.

Fig 1b schematically illustrates a portion of the integrated circuit 150 in order to illustrate the situation during the occurrence of a significant thermal mismatch between the package substrate 180 and the semiconductor chip 100. As illustrated, a portion of the metallization system 110 may be illustrated in which a last metallization layer 140 may comprise a dielectric material 142, in which is embedded a contact pad 141, which may comprise copper material in sophisticated applications. Furthermore a passivation layer 160, which may also be referred to as a final passivation layer, is provided on the last metallization layer 140 and exposes a portion of the contact pad 141. Moreover, a metal pillar 171, such as a copper pillar, may extend from the final passivation layer 160 to the package substrate 180, ie. a corresponding contact pad 181 formed therein. Moreover, typically a solder material 173 may be formed on the metal pillar 171 and may connect to the contact pad 181. Moreover, as illustrated by the dashed lines, usually the opening formed in the final passivation layer 160 may be less than a width 171w of the metal pillar 171 thereby forming a contact region 172 that connects the metal pillar 171 with the contact pad 141. Consequently, during operation the shear forces 183, 103 may result in a certain torque, in particular generated at corresponding portions 165, at which the bottom of the metal pillar 171 is in contact with the final passivation layer 160. Consequently, in this area a maximum mechanical stress may be exerted in a locally selective manner to the metallization system 110, thereby forcing corresponding defects that may primarily originate from the areas 165.

Consequently, although advanced contact regimes between a chip and a package substrate based on copper pillars may provide for significant advantages with respect to heat dissipation capabilities and electrical conductivity at a reduced required floor space, thereby allowing to enhance density of contact elements

and/or dummy elements for heat dissipation, the increased mechanical stress created in the metallization system 110 may not be compatible with the reliability requirements of sophisticated semiconductor devices. For this reason, frequently the height of the copper pillars is reduced which, however, may be associated with a corresponding reduction of the spacing between the package substrate and the chip, which in turn may cause a non-reliable filling in of any underfill material. Thus, corresponding voids in the underfill material may also contribute to a high degree of non-reliability, for instance caused by non-uniformities in heat conductivity and the like. In other conventional approaches, the metallization systems may be formed on the basis of less sensitive low-k dielectric materials or ultra low-k materials in order to enhance the mechanical stability of the metallization system, which however is associated with a significant reduction in electrical performance due to increased parasitic capacitances, resulting in an increased signal propagation delay.

In view of the situation described above, the present disclosure relates to methods and semiconductor devices in which a pillar structure may be provided while avoiding, or at least reducing, the effects of one or more of the problems identified above.

SUMMARY OF THE DISCLOSURE

Generally, the present disclosure relates to semiconductor devices and manufacturing techniques in which the negative effect of mechanical stress transferred to the metallization system via a pillar structure may be reduced by reducing the maximum forces at the point wherein the metal pillar is in contact with the final passivation layer, while nevertheless maintaining the required contact area at the top of the metal pillar. To this end, in some illustrative aspects disclosed herein, the lateral dimension of the metal pillar at the top thereof may be selected so as to comply with requirements in view of connecting to a package substrate, while on the other hand the lateral dimension of the metal pillar at the bottom thereof, ie. at a height corresponding to the surface of the final passivation layer, may significantly be reduced, thereby also reducing the "point-like" stress

transferred into the metallization system. Consequently, the metal pillar may be provided in nail-like configuration, which may be accomplished by appropriately modifying the process of metal deposition, however without significantly contributing to overall process complexity.

One illustrative semiconductor device disclosed herein comprises a metallization system formed above a substrate and comprising a final passivation layer. Moreover, the semiconductor device comprises a metal pillar extending from the final passivation layer, wherein the metal pillar is in contact with a contact pad formed in the metallization system. Furthermore, the metal pillar has a first lateral dimension at the final passivation layer and has a second lateral dimension at the top surface thereof, wherein the first lateral dimension is less than the second lateral dimension.

One illustrative method disclosed herein comprises forming a first deposition mask above a final passivation layer of a metallization system of a semiconductor device, wherein the first deposition mask has a first opening with a first width. Additionally, the method comprises forming a second deposition mask above the first deposition mask, wherein the second deposition mask has a second opening aligned to the first opening with a second width that is greater than the first width. Finally, the method comprises forming a metal pillar using the first and second deposition masks.

A still further illustrative method disclosed herein relates to forming a semiconductor device. The method comprises forming a final passivation layer above a plurality of metallization layers and forming an opening in the final passivation layer so as to expose a portion of a contact pad. Additionally, the method comprises forming a metal pillar so as to extend from the final passivation layer, wherein the metal pillar has a first lateral dimension at the top surface of the final passivation layer and has a second lateral dimension at a top surface thereof, wherein the first lateral dimension is less than the second lateral dimension by at least 30 percent relative to the second lateral dimension.

BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the present disclosure are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs 1a and 1b schematically illustrate cross-sectional views of an integrated circuit including semiconductor chip and a package substrate connected by a pillar structure having a conventional configuration, thereby creating a high mechanical stress; and

Figs 2a – 2e schematically illustrate cross-sectional views of a semiconductor device including a sophisticated metallization system and a pillar structure with metal pillars having a "nail-like" configuration for reducing the maximum stress component at the metallization system while nevertheless providing for the required connectivity to a package substrate according to illustrative embodiments.

DETAILED DESCRIPTION

While the present disclosure is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present disclosure to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

Generally, the present disclosure provides semiconductor devices and techniques in which sophisticated metallization systems including metal pillars may efficiently be used without unduly increasing the local stress load for the metallization system, thereby providing the possibility of using highly sophisticated dielectric materials, which may have a reduced mechanical stability compared to conventional dielectrics, as previously explained. The local stress load or forces may efficiently

be reduced for given requirements with respect to providing a contact surface area for connecting to a package substrate by reducing the torque forces acting on the final passivation layer, which may be accomplished by appropriately reducing the lateral dimension or width or diameter of the metal pillar at an area which is in contact with the final passivation layer, while providing a desired greater width at least at a top surface of the metal pillar. Consequently, the existing torque forces at the interface between the metal pillar and the dielectric material of the final passivation layer may be reduced, thereby also reducing the local load of any underlying materials, such as sensitive low-k dielectric materials, thereby enhancing overall stability during the manufacturing process for connecting the semiconductor chip with the package substrate and also during operation of the integrated circuit, as discussed above. In some illustrative embodiments disclosed herein, the reduced lateral dimension or width of the metal pillar may be selected such that this lateral dimension also substantially corresponds to the lateral dimension of a connection area connecting the metal pillar with a contact pad of the last metallization layer, while in other cases the connection area may be formed on the basis of a desired diameter followed by a lower portion of the metal pillar having greater width, however significantly reduced compared to conventional pillar structures, followed by an upper portion of the metal pillar having the required greater lateral dimension in order to comply with requirements in view of connectivity and the like.

With reference to Figs 2a – 2e further illustrative embodiments will now be described in more detail, wherein also reference may be made to Figs 1a and 1b, if appropriate.

Fig 2a schematically illustrates a cross-sectional view of a semiconductor device 200 in an advanced manufacturing stage. As illustrated, the semiconductor device 200 may comprise a substrate 201, such as a silicon substrate, an SOI substrate and the like, as is required in view of the overall configuration of the device 200. Furthermore, a device level or a semiconductor layer 202 may be formed above the substrate 201 and may comprise a large number of circuit elements, such as transistors, capacitors, resistors and the like, which may be formed on the basis of appropriate design rules corresponding to the device 200. For instance, critical

dimensions of circuit elements in the device level 202 may be approximately 50 nm and less, thereby also requiring a sophisticated metallization system. It should be appreciated that although the techniques disclosed herein are highly advantageous in the context of complex semiconductor devices, a corresponding regime for forming a pillar structure may also be advantageously applied to less critical semiconductor devices in which the circuit elements may have critical dimensions of 50 nm and more. Moreover, the semiconductor device 200 may comprise a metallization system 210, which typically includes a plurality of metallization layers 220, ..., 240, at least some of which, in some illustrative embodiments, comprise sensitive dielectric materials, as previously discussed. Moreover, a last metallization layer 240 may have formed therein a metal region in the form of a contact pad 241, which may be comprised of any appropriate material, such as copper, aluminum, copper/aluminum and the like. It should be appreciated that in sophisticated metallization systems the metal lines and vias may be provided on the basis of a copper material due to the superior characteristics in view of thermal and electrical conductivity, as is also previously discussed. It should be noted, however, that also metallization systems including other materials, such as aluminum, silver and the like, possibly in combination with other metals, may also be contemplated herein. Moreover, the contact pad 241 may comprise any appropriate barrier material, if required, in order to reliably confine a corresponding metal such as copper when a direct contact of the metal with a surrounding dielectric material 242 may be considered inappropriate.

Furthermore, a final passivation layer 260 may be formed above the last metallization layer 240 and may comprise two or more sub layers 261, 262, as is required in view of the overall characteristics with respect to passivation, mechanical integrity and the like. For example, the first sub layer 261 may be comprised of silicon dioxide, silicon nitride and the like, while the second sub layer 262 may represent a passivating material, such as polyamide and the like. In the manufacturing stage shown an opening 263 may be formed in the final passivation layer 260 so as to extend to the contact pad 241, wherein a corresponding lateral dimension of the opening 263, as well as a thickness of the final passivation layer 260 may be selected in accordance with well-established process strategies so that the corresponding characteristics of the final passivation layer 260 and of the

opening 263 may be compatible with conventional strategies for forming a pillar above the final passivation layer 260. In other cases, the width of the opening may be selected less compared to conventional design strategies, if desired. Furthermore, a first deposition mask 264 may be provided so as to define the position and the lateral size of a first portion of a metal pillar to be formed on the basis of the mask 264. To this end, the deposition mask 264 may comprise an opening 264a having an appropriately selected lateral dimension or width 264w, which may be significantly less compared to a conventional metal pillar for otherwise identical device requirements. For instance, a corresponding conventional lateral dimension is indicted by the dashed line 264c. For example, the conventional width 264c may substantially correspond to a desired cross-sectional area required for connecting to a package substrate, as previously explained. For instance, if a contact surface area with a diameter of approximately 100 – 30 µm may be required, ie. the conventional width 264c would be selected to approximately 100 – 30 µm, the width 264w of the opening 264a may be selected to approximately 70 percent or less, such as 50 percent or less, relative to the lateral dimension of the required dimension at the contact surface of a metal pillar still to be formed. Moreover, a thickness 264t of the deposition mask 264 may be selected so as to correspond to a desired height of the portion of the metal pillar having the reduced lateral dimension. For example, the thickness 264t may correspond to approximately half of the final height of the metal pillar still to be formed, while in other cases a further reduced thickness may be selected, if desired.

The semiconductor device 200 as shown in Fig 2a may be formed on the basis of the following process strategy. First, circuit elements in the device level 202 as well as the metallization system 210 including the metallization layers 220, 230 and 240 may be formed on the basis of any appropriate process strategy wherein, if desired, a high degree of compatibility with desired technology standards and process techniques may be maintained. Thereafter, the final passivation layer 260 may be formed, for instance by depositing corresponding dielectric materials, such as the sub layers 261 and 262 and subsequently patterning the same by well-established lithography techniques. For example, the polyimide material 262 may be provided in the form of a photo sensitive material and may be patterned by a corresponding development process, followed by the etching of the layer 261. In

other cases, a corresponding resist mask may be provided so as to etch through the final passivation layer 260 in order to expose a portion of the contact pad 241. If required, any appropriate barrier material 265 may be deposited, in order to confine a corresponding reactive metal, such as copper, if a direct contact with material of the passivation layer 260 may be considered inappropriate. Moreover, the layer 265 may be advantageous in view of enhanced adhesion of a metal to be formed in the opening 263 and on exposed portions of a top surface 260s and sidewalls 260w of the final passivation layer 260. For this purpose, any appropriate materials, such as chromium, copper, tantalum, tantalum nitride and the like, or combinations of various materials, may be used. Thereafter, the deposition mask 264 may be provided, for instance in the form of a resist material wherein the thickness thereof may be selected so as to obtain the desired target thickness 264t. In some illustrative embodiments, after providing the mask material a planarization process may be performed so as to obtain the desired target thickness 264t. Thereafter, the opening 264a may be patterned by using an appropriate lithography mask in order to obtain the reduced width 264w.

Fig 2b schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, a second deposition mask 266 may be formed above the deposition mask 264 and may have formed therein an opening 266a that is aligned to the openings 264a and 263 and which may define the lateral position and the size and shape of a portion of a metal pillar still to be formed on the basis of the openings 264a, 266a. Consequently, the width 266w, as well as the overall shape of the opening 266a, may be selected so as to comply with the requirements for a metal pillar for connecting to a package substrate, as is also previously discussed with respect to the integrated circuit 150 in Figs 1a and 1b. Consequently, the width 266w may in some illustrative embodiments be in the range of 100 – 30 μm or even less, if highly sophisticated applications are considered. Due to the significantly increased dimensions 266w compared to the dimension 264w the metal pillar to be formed on the basis of the openings 266a, 264a may have a "nail-like" configuration in order to reduce the local torque forces exerted to the final passivation layer 260. Furthermore, the deposition mask 266 may be provided with any appropriate thickness so as to accommodate a thickness of an upper portion of the metal pillars still to be formed, possibly in combination

with additional materials, such as a solder material and the like, if required. The deposition mask may be provided in the form of resist material, which may be patterned by using well-established lithography techniques, ie. by providing a positive resist or negative resist, depending on the process strategy, and removing an exposed portion or a non-exposed portion of the resist materials. Thereafter, if required, a wet chemical cleaning process may be performed so as to prepare the exposed surface of the contact pad 241, possibly in combination with a corresponding barrier material (not shown), for instance the barrier material 265 as explained with reference to Fig 2a.

Fig 2c schematically illustrates the semiconductor device 200 when exposed to a deposition ambient 205, during which an appropriate metal material may be filled into the openings 266a, 264a so as to form a metal pillar 271. It should be appreciated that in the embodiments shown in Figs 2a – 2c, also a connection element 272 may be formed within the opening 263 during the deposition process 205 so that a connection element 272 and the metal pillar 271, comprising a lower portion 271l with dimensions defined by the opening 264a and an upper portion 271u having dimensions as defined by the opening 266a, may be formed on the basis of the same material. In other cases, the connection portion 272 may be formed separately from the metal pillar 271, if considered appropriate. For example, a specific material may be deposited by electrochemical deposition techniques on the basis of the final passivation layer 260 and the opening 263 and thereafter the first and second deposition masks 264 and 266 may be formed in order to provide the metal pillar 271 with the desired configuration and on the basis of a specific metal material.

The deposition process 205 may comprise any appropriate electrochemical deposition technique, such as electroless plating, electroplating and the like, wherein in some illustrative embodiments an electroless plating technique may be used without requiring a corresponding current distribution layer, which may have to be patterned after completing the metal pillar 271. For this purpose, a plurality of well-established deposition recipes are available. In some illustrative embodiments additional cap materials may be formed on a top surface 271s if required, for instance in view of enhancing performance during a corresponding process for

directly connecting to a contact pad of a package substrate in a later manufacturing stage and the like.

Fig 2d schematically illustrates the semiconductor device 200 according to further illustrative embodiments in which a further material 273, for instance in the form of a solder material, such as a lead-free solder material, may be deposited during a deposition process 206, such as an electrochemical deposition process, for which well-established deposition recipes are available. For this purpose, a thickness of the deposition mask 266 may appropriately be selected so as to accommodate the metal pillar 271, ie. the upper portion 271u thereof, and a desired thickness of the material 273. Thereafter, the deposition masks 266 and 264 may be removed by any appropriate etch techniques, such as plasma stripping and the like, followed by any further etch processes so as to remove portions of current distribution layers, if provided, barrier materials and the like. It should be appreciated that if such materials may have to be removed from the final passivation layer 260, appropriate isotropic etch recipes may be used, so that the shadowing effect of the upper portion 271u may not negatively affect the efficient removal of any such materials.

Fig 2e schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage according to some illustrative embodiments. As illustrated, the device 200 may comprise the metal pillar 271, including the upper portion 271u and the lower portion 271l with the respective lateral dimensions 266w and 264w that may be selected as is specified above. Moreover, in the embodiment shown, the additional material 273 in the form of a solder material may be formed above the metal pillar 271 and may, in the embodiment shown, have an enhanced shape obtained upon reflowing the previously deposited solder material. In other embodiments, the metal pillar 271 may be provided without an additional solder material as illustrated in Fig 2c, or the reflowing of the solder material 273 if provided may be omitted, as shown in Fig 2d. As illustrated, in some embodiments the reduced lateral dimension 264w may be selected so that at least a portion of the metal pillar 271 may "rest" above the final passivation layer 260, as indicated by the portion 271r. In this case, due to the overall reduced width 264w, the corresponding mechanical forces acting on the surface of the final passivation layer 260 may be reduced, as previously explained. Consequently, a corresponding local

mechanical stress acting on any materials positioned below the final passivation layer 260 may also be reduced, thereby reducing the probability of creating defects, such as delamination, cracks and the like. In other illustrative embodiments, the dimension 264w may be selected so as to substantially correspond to a lateral dimension 263w of the connection element 272, thereby also reducing the resulting locally occurring forces acting on the final passivation layer 260. In still other illustrative embodiments, the lateral dimension 264w may be selected less than the dimension 263w, as indicated by 271d, thereby substantially completely avoiding an interaction of the metal pillar 271 with the surface 260s of the passivation layer 260. It should be appreciated that a corresponding variation of the lateral width 264w may be accomplished by appropriately selecting the width of the opening 264a of the deposition mask 264 (cf. Fig 2b).

As a result, the present disclosure provides semiconductor devices and manufacturing techniques in which the local forces at an interface between the surface of a passivation material and a metal pillar may be reduced by reducing the lateral dimension of a lower portion of the metal pillar, while maintaining a desired surface area for connecting to a package substrate at an upper portion thereof. Consequently, any desired material having an increased stiffness compared to conventional solder materials may be used, such as copper, copper alloys, nickel and the like, while also providing the possibility of using sophisticated dielectric materials in the metallization system without compromising the overall connectivity of the metal pillar structure.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the principles disclosed herein. It is to be understood that the forms shown and described herein are to be taken as the presently preferred embodiments.

CLAIMS

1. A semiconductor device comprising:

a metallization system formed above a substrate, said metallization system comprising a final passivation layer; and

a metal pillar extending from said final passivation layer, said metal pillar being in contact with a contact pad formed in said metallization system and having a first lateral dimension at said final passivation layer and having a second lateral dimension at a top surface thereof, said first lateral dimension being less than said second lateral dimension.

2. The semiconductor device of claim 1, further comprising an opening in said final passivation layer, wherein said opening is filled with a contact metal connecting said metal pillar with said contact pad.

3. The semiconductor device of claim 2, wherein a lateral dimension of said opening is substantially equal to said first lateral dimension.

4. The semiconductor device of claim 2, wherein said lateral dimension of said opening is less than said first lateral dimension.

5. The semiconductor device of claim 2, wherein said contact metal and said metal pillar are comprised of the same metal containing material.

6. The semiconductor device of claim 1, further comprising a solder material formed above said top surface of said metal pillar.

7. The semiconductor device of claim 6, wherein said solder material is provided as a reflown solder material.

8. The semiconductor device of claim 1, wherein said metal pillar comprises copper.

9. The semiconductor device of claim 1, wherein said second lateral dimension of said metal pillar is approximately 30 µm to 100 µm.

10. The semiconductor device of claim 1, wherein a value of said first lateral dimension is approximately 50 percent or less relative to said second lateral dimension.

11. A method comprising:

forming a first deposition mask above a final passivation layer of metallization system of a semiconductor device, said first deposition mask having a first opening with a first width;

forming a second deposition mask above said first deposition mask, said second deposition mask having a second opening aligned to said first opening, said second opening having a second width that is greater than said first width; and

forming a metal pillar using said first and second deposition masks.

12. The method of claim 11, wherein forming said first and second deposition masks comprises forming a first resist mask and forming a second resist mask on said first resist mask.

13. The method of claim 11, further comprising forming an opening in said final passivation layer, wherein said opening of the final passivation layer has a width that is less than said second width.

14. The method of claim 13, wherein said width of the opening of said final passivation layer is less than said first width.

15. The method of claim 11, further comprising forming a solder material above a top surface of said metal pillar.

16. The method of claim 15, further comprising reflowing said solder material prior to connecting said semiconductor device to a package substrate.

17. The method of claim 11, wherein said second width is approximately 100µm or less.

18. A method of forming a semiconductor device, the method comprising:

forming a final passivation layer above a plurality of metallization layers;

forming an opening in said final passivation layer so as to expose a portion of a contact pad; and

forming a metal pillar so as to extend from said final passivation layer, said metal pillar having a first lateral dimension at a top surface of said final passivation layer, said metal pillar further having a second lateral dimension at a top surface thereof, said first lateral dimension being less than said second lateral dimension by at least 30 percent relative to said second lateral dimension.

19. The method of claim 18, wherein said first lateral dimension is less by at least 50 percent.

20. The method of claim 18, wherein forming said metal pillar comprises forming a first deposition mask above said final passivation layer and forming a second deposition mask above said first deposition mask, wherein said first deposition mask has a first opening aligned to said opening of the final passivaiton layer and said second deposition mask has a second opening aligned to said first opening.

21. The method of claim 20, wherein said first and second deposition masks are provided as resist masks.

22. The method of claim 20, wherein a metal material is filled in said first and second openings and said opening of said final passivation layer in a common deposition process so as to form said metal pillar and a connection element connecting said metal pillar with said contact pad.

23. The method of claim 18, wherein said metal pillar is formed of a copper containing material.

24. The method of claim 18, further comprising forming a solder material above said top surface of the metal pillar.

25. The method of claim 24, wherein said solder material and said metal pillar are formed on the basis of a common deposition mask.

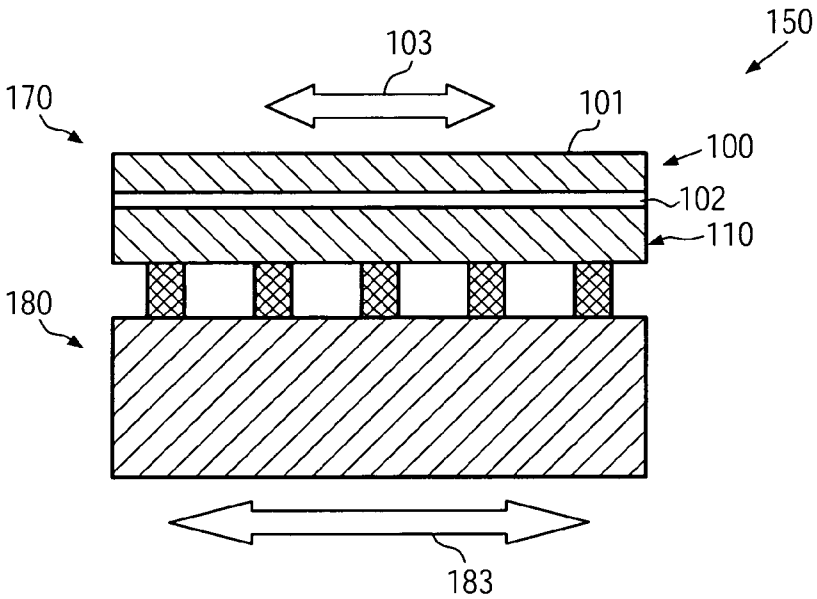

FIG. 1
(prior art)

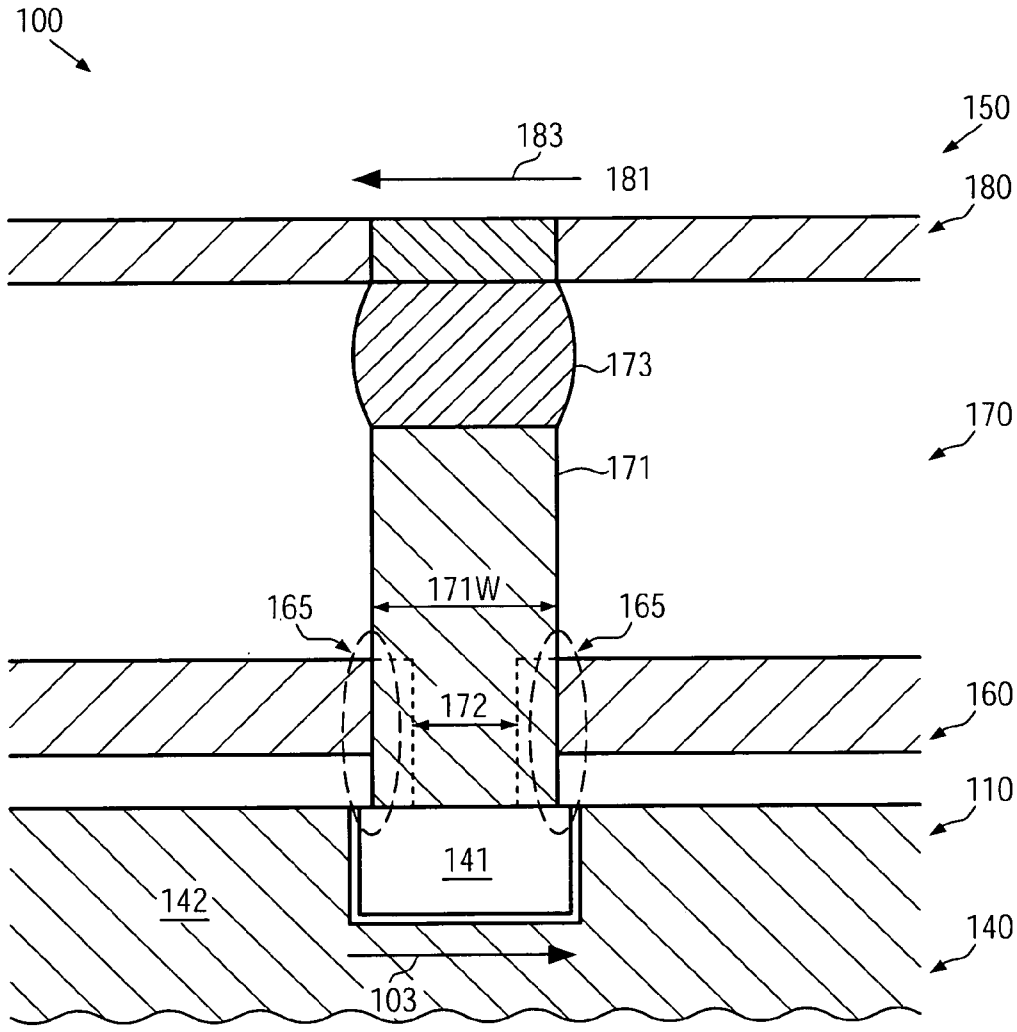

FIG. 1b
(prior art)

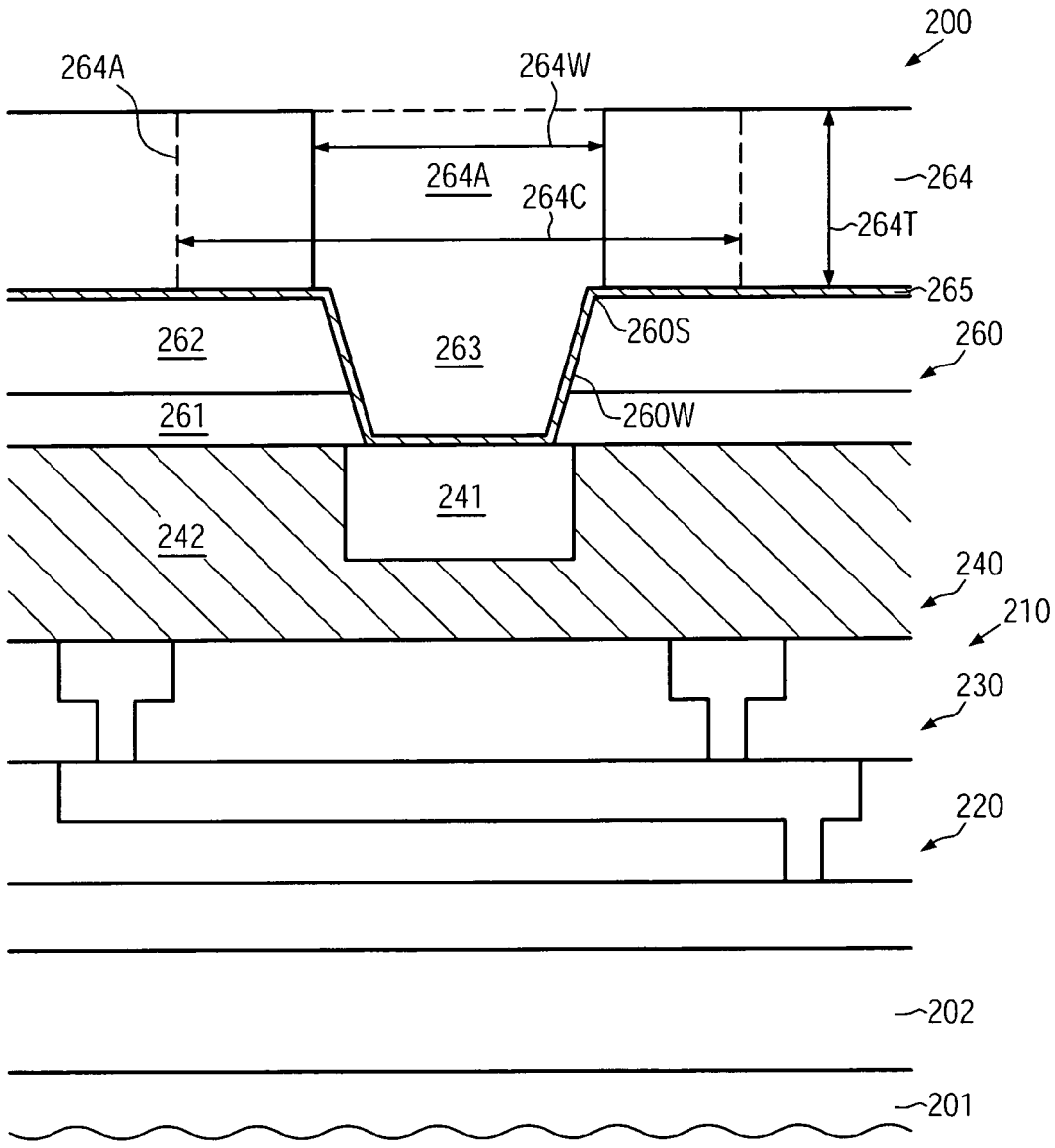
200
264A
264W
264A
264C
264
264T
265
262
263
260S
260
261
260W
241
242
240
210
230
220
202
201

FIG. 2a

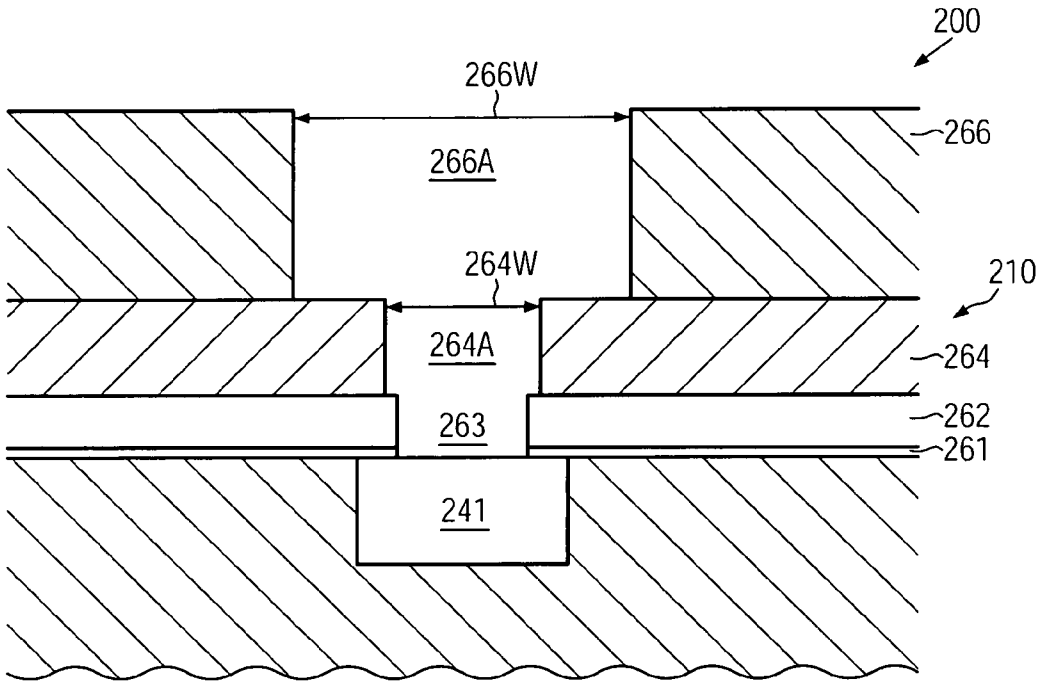
200
266W
266
266A
264W
210
264A
264
263
262
261
241

FIG. 2b

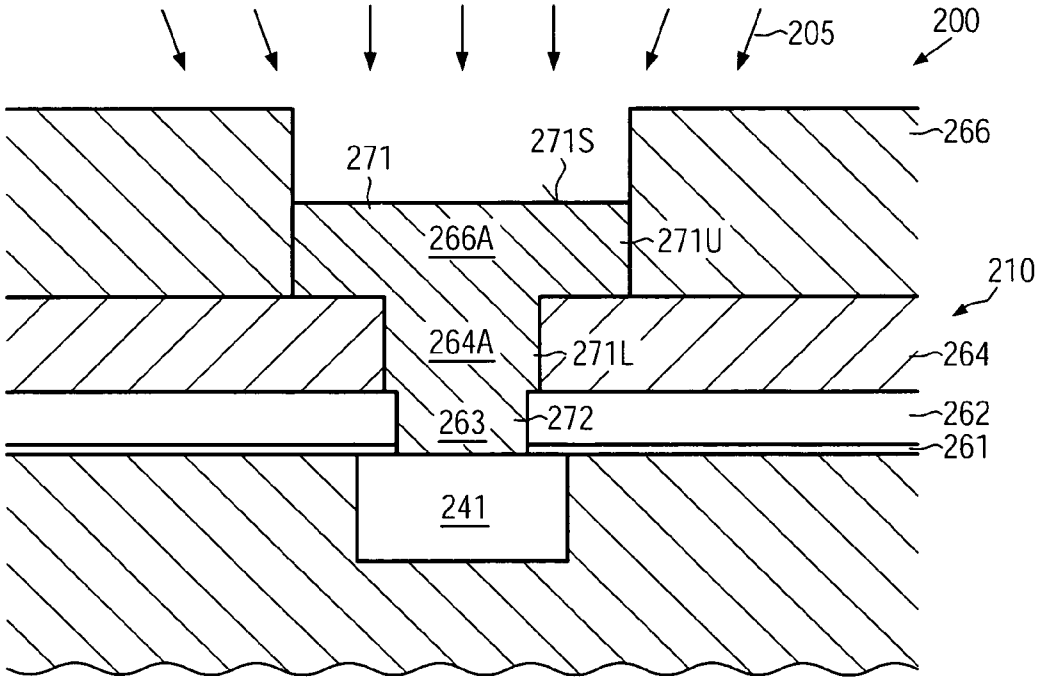
205
200
266
271
271S
266A
271U
210
264A
271L
264
263
272
262
261
241

FIG. 2c

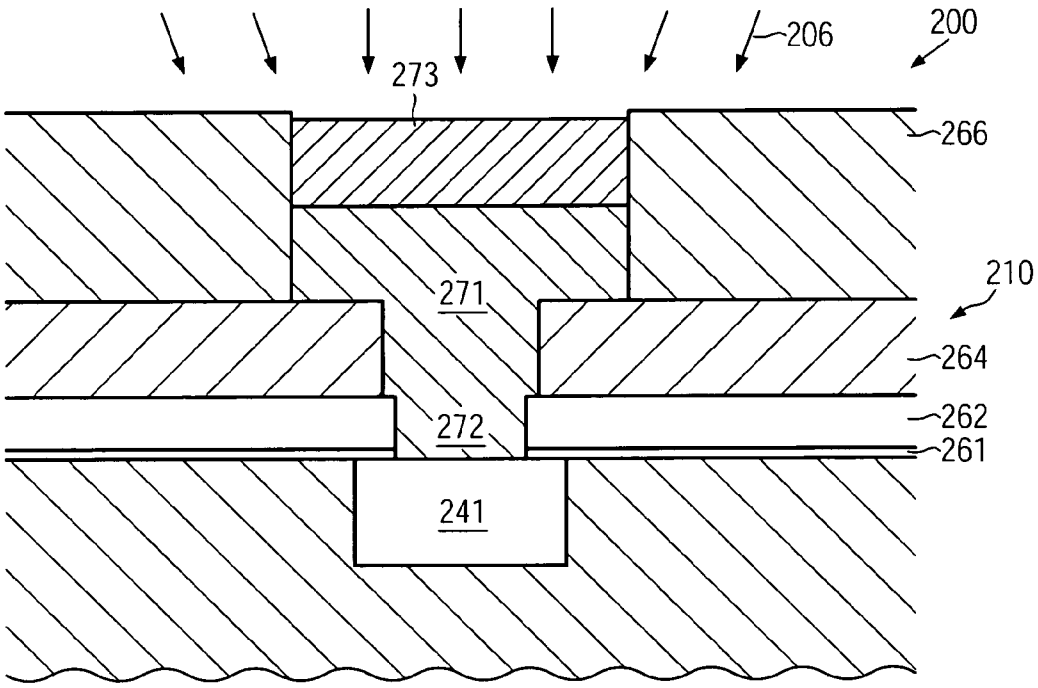
206
200
273
266
271
210
264
272
262
261
241

FIG. 2d

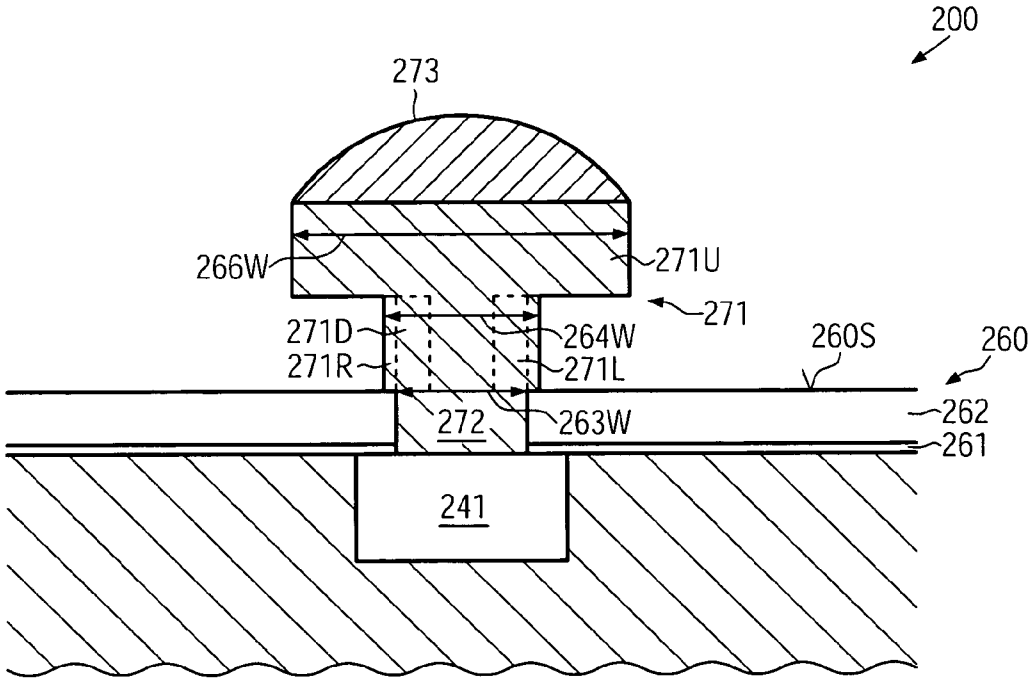
200
273
266W
271U
271
271D
264W
260S
260
271R
271L
272
263W
262
261
241

FIG. 2e

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/001092

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60 H01L23/485
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2006/088992 A1 (HUANG MIN-LUNG [TW] ET AL) 27 April 2006 (2006-04-27) figures 6-14 paragraphs [0022] - [0026]	1-21,23, 24 22,25
X	US 2004/082161 A1 (HO KWUN-YAO [TW] ET AL) 29 April 2004 (2004-04-29) figures 2A-2D, 7 paragraphs [0033] - [0036], [0039], [0044]	1-25
X	US 2005/253264 A1 (AIBA YOSHITAKA [JP] ET AL) 17 November 2005 (2005-11-17) figure 7 paragraphs [0115] - [0138]	1-8

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 April 2010	06/05/2010

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/001092

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006088992 A1	27-04-2006	TW 242253 B	21-10-2005
US 2004082161 A1	29-04-2004	TW 244129 B	21-11-2005
US 2005253264 A1	17-11-2005	CN 1697148 A	16-11-2005
		CN 101136344 A	05-03-2008
		JP 4119866 B2	16-07-2008
		JP 2005327816 A	24-11-2005
		KR 20050108308 A	16-11-2005
		TW 238477 B	21-08-2005
		US 2007249093 A1	25-10-2007