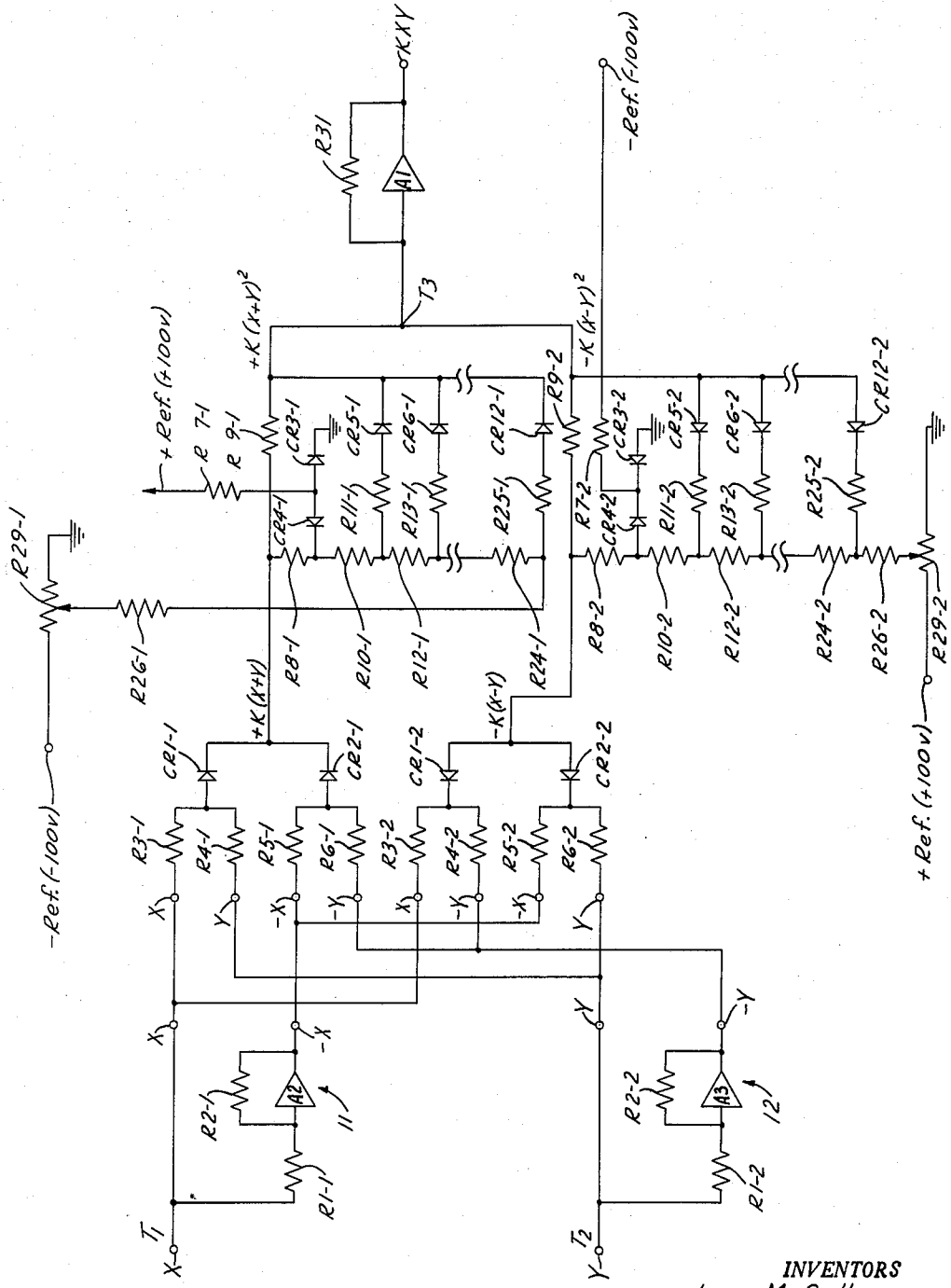
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QUARTER SQUARE ANALOG MULTIPLIER

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QUARTER SQUARE ANALOG MULTIPLIER

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This invention relates to analog multipliers and more particularly to quarter square analog multipliers.

In quarter square analog multipliers heretofore available, four squaring networks are required to obtain a quarter square multiplier. There is a need for a new and improved quarter square multiplier which requires fewer squaring networks and other components.

In general, it is an object of the present invention to provide a quarter square analog multiplier which has fewer components and which is less expensive.

Another object of the invention is to provide a multiplier of the above character in which only inputs of $+x$, $+y$ are required to realize the product kxy at the output of the multiplier.

Another object of the invention is to provide a multiplier of the above character which requires a maximum of three amplifiers.

Another object of the invention is to provide a quarter square analog multiplier of the above character which has improved characteristics.

Additional objects and features of the invention will appear from the following description in which the preferred embodiment is set forth in detail in conjunction with the accompanying drawings.

Referring to the drawings:

The sole figure is a circuit diagram, partially in block form, of a quarter square analog multiplier incorporating our invention.

As shown in the figure, our quarter square analog multiplier has two input terminals T1 and T2 to which are applied the signals x and y. Either of these signals may be of either polarity, that is, x may be a positive or a negative voltage, and y may be a positive or a negative voltage. For purposes of convenience, it has been assumed that both x and y are positive as indicated in the figure. However, in any event, both the opposites of x and y must be made available. Therefore, an inverter 11 is connected to the terminal T1 and supplies $-x$ and inverter 12 is connected to the terminal T2 and supplies $-y$. The inverter 11 consists of an operational amplifier A2 with a feedback resistor R2–1. An input resistor R1–1 is connected to the operational amplifier A2. The feedback resistor is sized such that the output from the operational amplifier A2 has the same magnitude but is opposite in polarity to the input voltage. The inverter 12 is constructed in a similar manner and consists of an operational amplifier A3, feedback resistor R1–2 and an input resistor R2–2.

By examining the circuit diagram, it can be seen that terminals are provided which are identified as x, y, $-x$, $-y$, x, $-y$, $-x$ and y. The terminals marked x receive their voltage directly from the x input terminal T1 and the terminals marked y receive their voltage directly from the y input terminal T2. The terminals marked $-x$ and $-y$ receive their voltages from the inverters 11 and 12 as hereinbefore described. These terminals are connected into resistive summing networks as shown.

Each of the summing networks consists of a pair of matched resistors which are connected to a diode. Thus, diode CR–1 conducts only when the sum of $x+y$ is positive. As pointed out above, either x or y can be positive or negative. It is only when the positive voltage summed by the resistors R3–1 and R4–1 is positive that the diode

CR1—1 conducts. If CR1—1 is conducting, CR2–1 will not be conducting because it is supplied with the opposites of the voltages being supplied to the resistors R3–1 and R4–1 connected to the diode CR1—1. Similarly, either diode CR1–2 or CR2—2 may be conducting depending upon the voltages supplied. Both of these diodes only conduct when a negative voltage is presented to the diodes and only one will be conducting at a time.

The outputs from the diodes in the summing networks are connected to a pair of squaring networks consisting of a plurality of diodes and resistors as hereinafter described. The network which is connected to the diodes CR1—1 and CR2–1 can be termed the x squaring network, whereas the network connected to the diodes CR1–2 and CR2—2 can be termed the y squaring network. The outputs of the squaring networks are combined and supplied to an operational amplifier A1.

Means is provided on each of the x and y squaring networks to provide a zero output when the input is zero. For this condition, there should be zero current flowing into the amplifier A1 for a zero voltage to appear at its output. The zero current flow at the input of amplifier A1 for zero signal output is obtained by providing paths to ground for currents from the reference supplies. These paths to ground consist of diodes CR4–1 and CR3–1 for the x network and diodes CR4–2 and CR3–2 for the y network. Diodes CR4–1 through CR12–1 and CR4–2 through CR12–2 are back biased when the input signal is zero and thus do not conduct current from the reference voltage supplies to amplifier A1.

For the diodes in this multiplier, it has been found that it is preferable to utilize diodes of a silicon type. As is well known to those skilled in the art, such diodes have a voltage drop. This voltage drop created difficulty in obtaining zero output for zero input because of the voltages across diodes CR4–1 and CR4–2. However, this voltage drop was cancelled by providing diodes CR3–1 and CR3—2 in the x and y networks respectively. This diode in each of the networks has across it a voltage having magnitude and which is opposite in polarity to the voltage drop in the associated diode CR4–1 or CR4–2 to provide a net voltage between associated resistors, resistors R8–1 and R10–1 or R8–2 and R10–2, which is equal to zero. The currents producing voltage drops across diodes CR3–1 and CR3–2 are obtained from the plus and minus references to which the diodes are connected through dropping resistors R7–1 and R7–2, respectively. Diodes CR3–1 and CR3–2 conduct at all times.

From the foregoing, it can be seen that the diodes CR3 and CR4 of each of the networks serve to clamp the input of the amplifier A1 to ground. This serves to eliminate the possibility of an output signal from the multiplier when input is zero. The resistors R7–1 and R7–2 ensure that exactly the proper amount of current will pass through the diodes CR3–1 and CR3–2, respectively, to obtain the proper voltage drop across the diodes and to thereby cancel the voltage drop which occurs across the diodes CR4–1 and CR4–2, respectively.

The bias which is applied to the various diodes in each of the x and y networks is determined by the reference voltages and the resistors R29–1 and R29–2, respectively, and may be called the x gain adjust and y gain adjust, respectively. These controls permit adjustment of k, the scale factor of the output kxy; e.g. $k=.01$.

Now let it be assumed that there is a positive output from either the diode CR1–1 or CR2–1 which represents $k(x+y)$. This positive voltage is supplied to the output amplifier A1 through the resistor R9–1. At a predetermined voltage as, for example, 10 volts, the diode CR4–1 stops conducting because the current from the $x+y$ source

exceeds that from the negative reference supplied through R29–1. As soon as CR4–1 stops conducting, there is less attenuation of the input signal because R8 is not grounded through the conducting diodes CR3 and CR4. Current then flows through the resistor R9–1 to provide a change in the slope of the output of the amplifier A1. When the $k(x+y)$ voltage reaches another predetermined voltage such as 20 volts, the diode CR5–1 begins conducting. Prior to this time, the diode CR5–1 was held cutoff because of the current coming from the negative reference supply. At 20 volts, the current arriving from the $k(x+y)$ signal source equals the current coming from the negative reference source to start the diode CR5–1 conducting. It should be pointed out that all the diodes CR5–1 through CR12–1 are biased or held cutoff by the negative reference until the $k(x+y)$ input voltage reaches the required level to overcome the bias. The current from the negative reference source flows to ground because of the zero source impedance of the signal source and the zero source impedance at the amplifier junction T–3 for the amplifier A1. It is for this reason that these source impedances should be as near zero as possible.

As soon as CR5–1 begins conducting, there is another current path for the input signal to reach the junction of the amplifier A1 and, therefore, the transfer characteristic of the amplifier A1 takes on a steeper slope. This same procedure continues as the $k(x+y)$ voltage increases to provide additional current paths to the junction T3 of the amplifier A1. Thus, as each diode starts conducting, the transfer characteristic of the amplifier takes on a still steeper slope. To obtain this steeper slope, it is necessary to increase the gain or transfer characteristic of the amplifier. However, the gain of the amplifier is not actually increased. It is merely the relationship between the input and the feedback resistance R31 which changes the transfer characteristic or the gain of the amplifier. However, in this embodiment, the feedback resistance R31 is constant. The diode network connected to the input of the amplifier A1, in effect, varies the input resistance to the amplifier to thereby increase the gain of the amplifier as the $k(x+y)$ signal is increased.

As is well known to those skilled in the art, it is desirable that the output of the amplifier A1 approach the square law which is actually one-half of the parabola. The parabolic curve is approximated by dividing it into a predetermined number of straight line segments as, for example, ten segments, which are approximated in each of the squaring networks.

In the circuit diagram, certain of the components have been indicated as being omitted. Thus, resistors 14–1, 16–1, 18–1, 20–1 and 22–1 and resistors R15–1, 17–1, 19–1, 21–1, 23–1 and diodes CR7–1 through CR11–1 have been omitted. Corresponding resistors and diodes for the y network have also been omitted. These squaring networks provide ten straight line segments which approximate the square law.

It was found that it was desirable that the reference source impedance for our multiplier be zero or close to it. However, it has been found that if the source impedance is not quite zero, the accuracy of our multiplier is not adversely effected because of the use of the voltage divider consisting of the resistor R29–1 and the other resistors in the network which effectively shunt the resistive impedance of the reference voltage supply. The resistor R29–1 for the x network and resistor R29–2 for the y network are normally the only resistors which are adjustable and are utilized to determine the scale factor of the multiplier.

The y squaring network operates in the manner similar to the x squaring network and for that reason, it will not be described in detail.

By way of example, one embodiment of our quarter square analog multiplier had the following components.

All Diodes	1N463
Resistors:	K Ohms
R3–1	50
R3–2	50
R3–3	50
R3–4	50
R3–5	50
R3–6	50
R3–7	50
R3–8	50
R7–1	100
R7–2	100
R8–1	8.04
R8–2	8.04
R9–1	766
R9–2	766
R10–1	32.9
R10–2	32.9
R11–1	825
R11–2	825
R12–1	23.6
R12–2	23.6
R13–1	732
R13–2	732
R14–1	18.9
R14–2	18.9
R15–1	509
R15–2	509
R16–1	14.6
R16–2	14.6
R17–1	412
R17–2	412
R18–1	10.7
R18–2	10.7
R19–1	277
R19–2	277
R20–1	8.25
R20–2	8.25
R21–1	160
R21–2	160
R22–1	5.83
R22–2	5.83
R23–1	70.1
R23–2	70.1
R24–1	3.77
R24–2	3.77
R25–1	14.2
R25–2	14.2
R26–1	182
R26–2	182
R27–1	3.3
R27–2	3.3
R28–1	11.8
R28–2	11.8
R29–1	5
R29–2	5
R30–1	51.1
R30–2	51.1

From the foregoing, it can be seen that we have provided a new and improved quarter square analog multiplier in which the sums of $x+y$ and $x-y$ are obtained within the multiplier itself by the use of precision resistors so that they can be multiplied by means of square law networks provided in the multiplier. Thus, it can be seen that the x network produces a function which is a square of the sum of the two input voltages, whereas the y network produces a negative of the square of the difference of the two input voltages. Both the x and y networks do the same thing. A sign reversal is obtained by inverting the diodes in one network as is readily apparent from the circuit diagram.

It is apparent from the foregoing that we have provided a new and improved quarter square analog multiplier in which x and y are the only inputs required and in which

only three amplifiers are required for multiplication. In addition, only two squaring networks are required. Thus, the multiplier is simplified while still obtaining relatively great accuracy.

We claim:

1. In a quarter square analog multiplier, first and second terminals for receiving an input voltage on each terminal, first and second inverting means connected to each terminal for inverting the polarity of the voltage applied to the terminal, first and second passive summing means connected to each of the terminals and to the output of the inverting means connected to each terminal for producing the sum and the difference of the two signals, first and second symmetrical biased diode squaring networks connected to said first and second summing means for squaring the sum of the two signals and for squaring the difference of the two signals, and means and means combining the outputs of the squaring networks.

2. A multiplier as in claim 1 wherein the two input signals and their inversions are available within the circuitry.

3. In a quarter square analog multiplier, a pair of input terminals having input voltages identified as x and y applied to the input terminals, inverting means including an operational amplifier connected to each of the terminals for supplying a voltage of equal magnitude but opposite polarity of the voltage connected to the input terminal, passive summing means connected to the input terminals and to the output of the inverting means connected to each terminal to provide $k(x+y)$ and $k(x-y)$, a pair of squaring networks connected to the outputs summing networks and producing $k(x+y)^2$ and $-k(x-y)^2$, and means combining the outputs of the squaring networks to provide kxy.

4. A multiplier as in claim 3 wherein said summing means consists solely of pairs of resistors connected in parallel and a diode connected to each pair of resistors.

5. A multiplier as in claim 3 wherein each of the squaring networks consists of a plurality of diodes connected in parallel, means including a first reference source for maintaining the diodes cut off below predetermined voltages so that each diode conducts at a different predetermined voltage, an additional diode connected to the parallel connected diodes, and means including a second reference source for biasing the additional diode in a direction opposite to the direction in which the other diodes are biased.

6. A multiplier as in claim 5 together with diode means connected to the additional diode for cancelling out the voltage drop occurring in the additional diode so that the output of the multiplier is zero when the input is zero.

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