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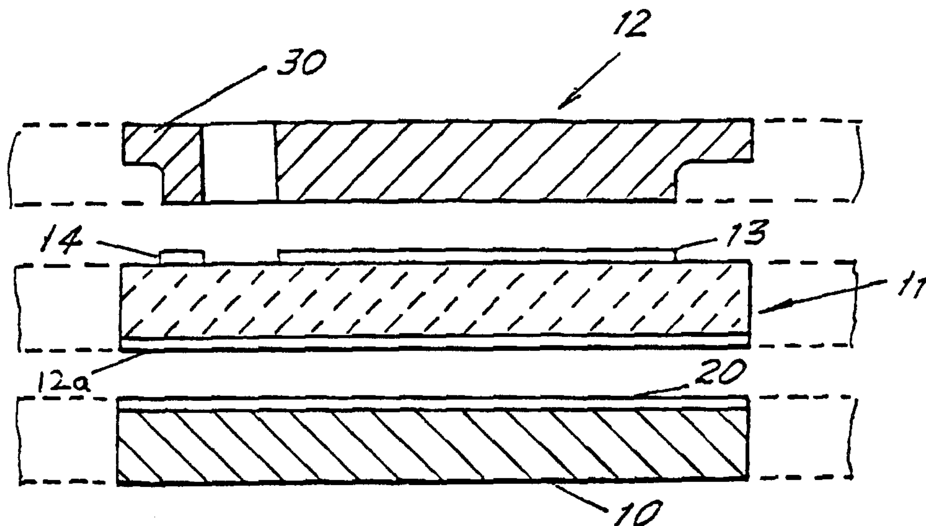
Published
With international search report.

(54) Title: CHIP SCALE PACKAGE



(57) Abstract

A process for forming a true chip scale package comprising the sandwiching of a silicon wafer (11) with a large number of identical die therein between top and bottom metal contact plates (12a, 13, 20) of the same size as the wafer. The sandwich is secured together as by soldering, and the die and contact plates are singulated in the form of a final chip scale package. The edge of each chip may have an insulation band formed thereon. Slots (34) may be formed in the top contact to define, with the edge saw cuts, a separate contact area on each top contact.

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TITLE: CHIP SCALE PACKAGE

BACKGROUND OF THE INVENTION

This invention relates to semiconductor device packages and the method of making such packages and more specifically relates to a chip-scale package and method of its manufacture.

5 Semiconductor device packages are well known for housing and protecting semiconductor die and for providing output connections to the die electrodes. Commonly, the semiconductor die are diced from a large parent wafer in which the die diffusions and metallizing are made in conventional wafer processing equipment. Such die may be diodes, field effect transistors, thyristors 10 and the like. The die are fragile and the die surfaces must be protected from external environment. Further, convenient leads must be connected to the die electrodes for connection of the die in electrical circuits.

Commonly, such die are singulated from the wafer, as by sawing, and the bottom of the die is mounted on and connected to a portion of a lead 15 frame which has identical sections to receive respective die. The top electrodes of the die are then commonly wire bonded to other portions of the lead frame, and a molded insulation housing is then formed over each lead frame section enclosing the die, and permitting lead portions of the lead frame to penetrate through the molded housing to be available for external connection.

20 It is desirable in many applications that packaged semiconductor devices be as small as possible to enable the mounting of many such devices on a support surface, such as a printed circuit board or an IMS (insulation-metal-substrate) support surface. Devices housed in the conventional manner occupy a much larger area than the area of the die which is housed. It would be very 25 desirable to provide a semiconductor package which offers the same purposes of the conventional housing (of protecting the die and providing convenient external connection to the die electrodes), but which will occupy less surface area on a support surface.

BRIEF SUMMARY OF THE INVENTION

30 This invention provides a novel semiconductor die package of "chip-scale". That is, the package of the present invention occupies very little more area than the actual area of the die. Thus, the invention reduces the package

area (or "footprint") to close to the irreducible area of the die itself. The invention also provides a novel process for forming such chip-scale packages.

In accordance with the present invention semiconductor die are first processed in conventional wafer form. The completed semiconductor wafer is then bonded to a bottom contact wafer which is preferably made of a metal having thermal expansion characteristics similar to those of silicon, and, typically may be of molybdenum or tungsten. In this bonding process, the die bottom will have a bottom electrode of any suitable metal and is preferably overcoated with silver. Similarly, the base contact plate or wafer preferably has a metallized (silver) surface. Thus, the bottom surface of the silicon wafer and top surface of the base contact can be connected by diffusion bonding, soldering, eutectic bonding or the like.

The top contact wafer is similarly of a material having thermal expansion characteristics matched to that of silicon and its bottom surface can be metallized with silver, matching the metallized top surface of the electrode, or electrodes, on the die wafer surface.

The top contact is further processed so that the contact sections for each die location are pre-cut to define separate contact portions when the devices are singulated. The separated cuts are filled in with a suitable plastic such as an epoxy or polyamide. A bottom groove in the top contact is filled with a plastic filler also encloses respective device areas and defines a thinned area.

The top metal wafer and base metal wafer are then bonded to the silicon die wafer in a common bonding or soldering operation, with the top electrode contacts aligning with and contacting the contact areas of the respective die.

The bonded assembly is then saw-cut to singulate each die (in the conventional die streets) with its respective top and base contacts covering the full top and bottom die area. The die junctions are well protected and wire bond or pressure connections can be easily made to the top and bottom contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is an exploded view of the top and bottom contacts and silicon die in wafer form.

Figure 2 is a bottom view of the top contact of Figure 1 to show the pattern of machined cuts in the wafer for use with a MOSgated wafer die having source and gate electrodes on its top surface.

Figure 3 shows the wafers of Figures 1 and 2 brought together for bonding.

Figure 4 is an exploded view of one of the bonded die of Figures 1 and 3 after singulation.

Figure 5 is an exploded view of a die made in accordance with the invention, but having a different top electrode pattern.

5 Figures 6 and 7 show the die of Figure 5 in its assembled condition.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to Figure 1, there is shown one die section taken from an assembly of three wafers 10, 11 and 12. The wafers will have a much
10 larger extent than that shown, and typically can contain hundreds or even thousands of die identical to that detailed in Figure 1.

The die wafer 11 is a silicon wafer which has been conventionally processed to define a power MOSFET which may be that shown in U.S. patent 5,008,725. Thus, each of the die in the wafer 11 will have a bottom aluminum
15 drain electrode 12a, a top source electrode 13 and a gate electrode 14. Each die will be separated from other die in wafer 11 by "streets" which provide a small area for saw cutting the die apart. Other devices could be used such as diode die, thyristor die and the like.

Wafer 10 in Figure 1 is a base contact wafer and is preferably of a
20 metal having expansion characteristics matched to those of silicon and may be molybdenum or tungsten or the like. The top surface of wafer 10 may have a silver metallized surface layer 20. The bottom surface of aluminum contact 12a may also be metallized with silver. Metals other than silver can be used.

Wafer 12 in Figures 1 and 2 is also of an expansion metal such as
25 molybdenum, but has a surface configuration which matches the top electrodes of the die in wafer 11. Thus, the gate contact portions 30 of wafer 12 are fully isolated from the source contact portions 31 (after the die are singulated). As best shown in Figure 2, a series of intersecting grooves 32 are formed in the bottom of wafer 12 and define saw cut regions 33 (Figure 3) for singulating the die. Thru-
30 cut slots 34, shown shaded in Figure 2 separate the gate contacts 30 from the source contacts 31 after singulation. Note that thru-cut slots 34 and shallower slots 32 are preferably back-filled with plastic (epoxy or polyamide) as shown in Figure 3.

The bottom surface of wafer 12 will then have gate contact
35 portions and source contact sections aligned with gate pad or electrode 14 and source electrode 13 respectively. These bottom surface portions may also be metallized with silver or the like.

Figure 3 shows the assembly process of the three wafers 10, 11 and 12 of Figure 1 in which the wafers 11 and 12 are carefully aligned with one another to match up the respective source and gate electrodes. Thereafter, wafers 10, 11 and 12 are simultaneously bonded together as by soldering, diffusion bonding, eutectic bonding or any other desired bonding process.

The bonded wafers are then diced to singulate the die, as by sawing through the centers of grooves 32. In some cases, after sawing, the exposed edges of die 11 may need extra protection by a small insulation coating. Figure 4 shows a singulated die in exploded form.

It will be apparent that the present invention is applicable to numerous types of device, including diodes, thyristors and FETs of all varieties. Suitable adjustments will be made in the contact wafers, depending on the shape of the electrodes in the die wafer. Thus, Figure 5 shows a MOSFET die 40 with a different surface pattern in which a gate pad 41 has gate fingers 42 extending therefrom and insulated from a source electrode surface 43, as in U.S. Patent 5,130,767. In this case, the upper source expansion contact 50 will have suitable undercuts (not shown) which avoid contact with gate pad 41 and its extending fingers 42. The top expansion contact wafer will then have separated gate portion 51 and source portion 50 which are otherwise the same as those of the embodiment of Figures 1 to 4. Figure 7 shows a protective insulation filter 60 surrounding the edge of die 40 and insulating gate electrode 51 from source electrode 50.

While the upper and lower contact plates are shown as uniformly metallic, it should be noted that any conductive composition can be used either soldered or otherwise adhered to the die surfaces or otherwise deposited thereon.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention not be limited by the specific disclosure herein.

WHAT IS CLAIMED IS:

1. The process of manufacturing a semiconductor device package; said process comprising:

the formation of a plurality of adjacently located identical die with identical junction patterns in a single wafer of semiconductor material, said
5 adjacent die having separated by streets in said wafer;

forming a top solderable metal and a bottom solderable metal on each of said die within said wafer;

conductively affixing one surface of each of a first and second metal contact disk over the full upper and full lower surfaces respectively of said
10 wafer and in contact with said top and bottom solderable contacts respectively;

and thereafter slicing vertically through said first and second metal contact disks and said wafer in said streets of said wafer, thereby to separate said plurality of die and their respective top and bottom contacts from one another.

2. The process of claim 1 wherein said wafer is formed of monocrystalline silicon and said first and second contacts are formed of a metal having thermal expansion characteristics which are matched to those of silicon.

3. The process of claim 1 wherein said first and second contacts are formed of a metal having thermal expansion characteristics similar to that of molybdenum.

4. The process of claim 1 wherein said wafer and first and second contacts are separated by a saw cut process.

5. The process of claim 3 wherein said wafer and first and second contacts are separated by a saw cut process.

6 The process of claim 1 which further includes the application of an insulation filler around the edge of each of said die.

7. The process of claim 5 which further included the application of an insulation filler around the edge of each of said die.

8. The process of claim 1 wherein said first metal contact has a plurality of short slots therein which extends between two of the trenches around each of said die, whereby, when said die are singulated, the first metal contact of said die is separated into at least two segments by said slot.

9. The process of claim 8 wherein said plurality of short slots are filled with an insulation compound.

10. The process of claim 2 therein said first metal contact has a plurality of short slots wherein which extends between two of the trenches around each of said die, whereby, when said die are singulated, the first metal contact of said die is separated into at least two segments by said slot.

11. The process of claim 3 wherein said first metal contact has a plurality of short slots therein which extends between two of the trenches around each of said die, whereby, when said die are singulated, the first metal contact of said die is separated into at least two segments by said slot.

12. The process of claim 6 wherein said first metal contact has a plurality of short slots therein which extends between two of the trenches around each of said die, whereby, when said die are singulated, the first metal contact of said die is separated into at least two segments by said slot.

13. A chip scale package comprising, in combination, a thin semiconductor die of generally rectangular area; first and second solderable contact metals on the top and bottom surfaces of said die; first and second contact plates conductively connected in surface to surface contact with said first and
5 second contact metals respectively; said first and second contact plates having the same exterior outline as said semiconductor die.

14. The package of claim 1, which further includes an insulation coating formed on the edge of and around the periphery of said die.

15. The package of claim 13 which further includes a slot in said top contact plate to divide said top contact plate into first and second insulated top electrodes.

16. The device of claim 15 wherein said slot is filled with insulation material.

17. The package of claim 14 which further includes a slot in said top contact plate to divide said top contact plate into first and second insulated top electrodes.

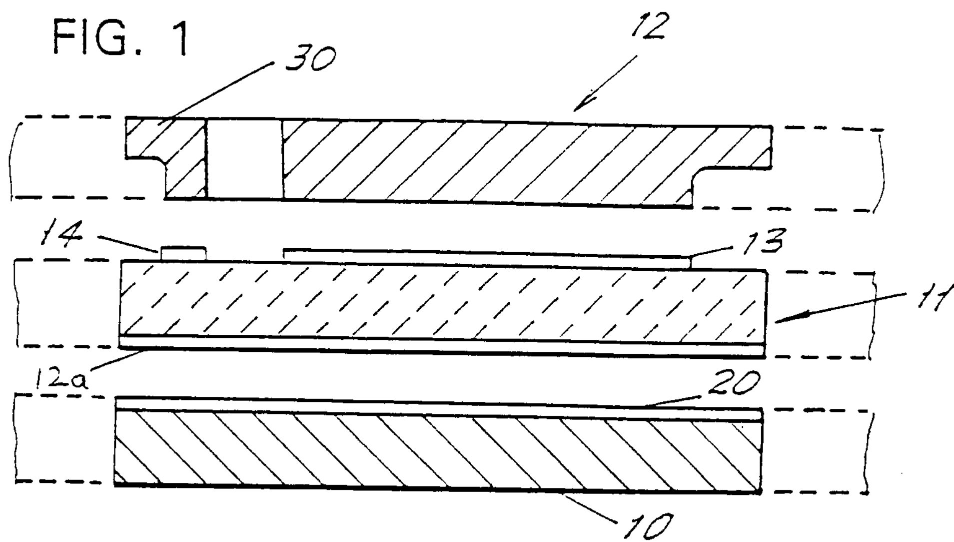


FIG. 1
12
30
14
13
11
12a
20
10

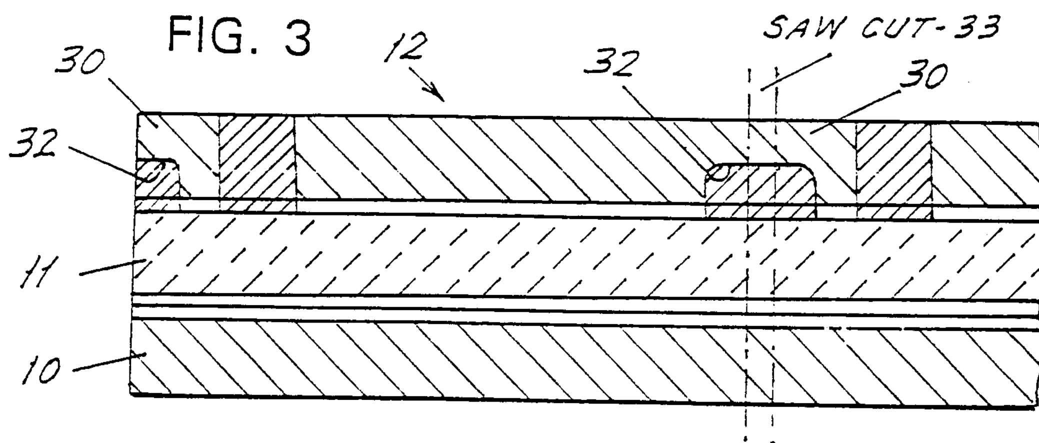


FIG. 3
12
30
32
SAW CUT-33
32
30
11
10

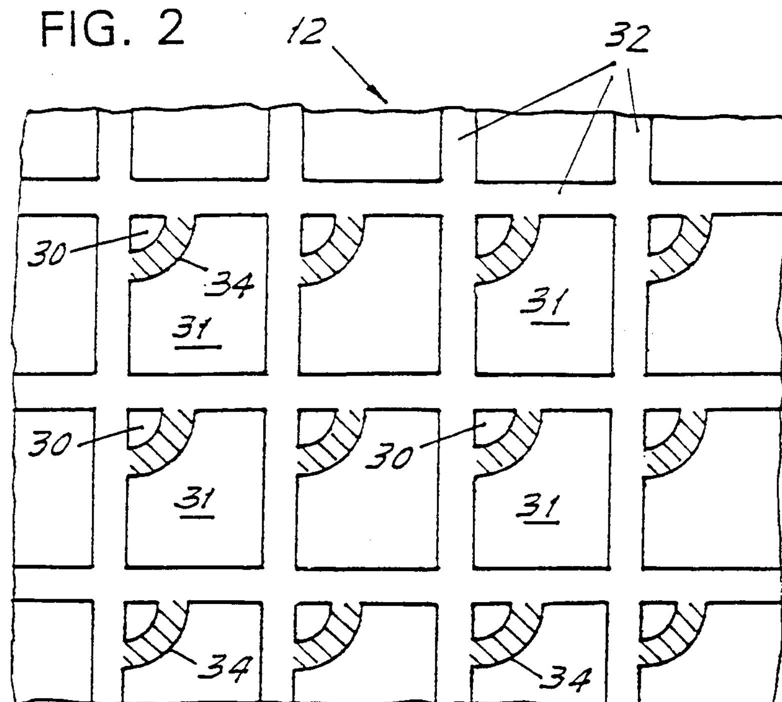
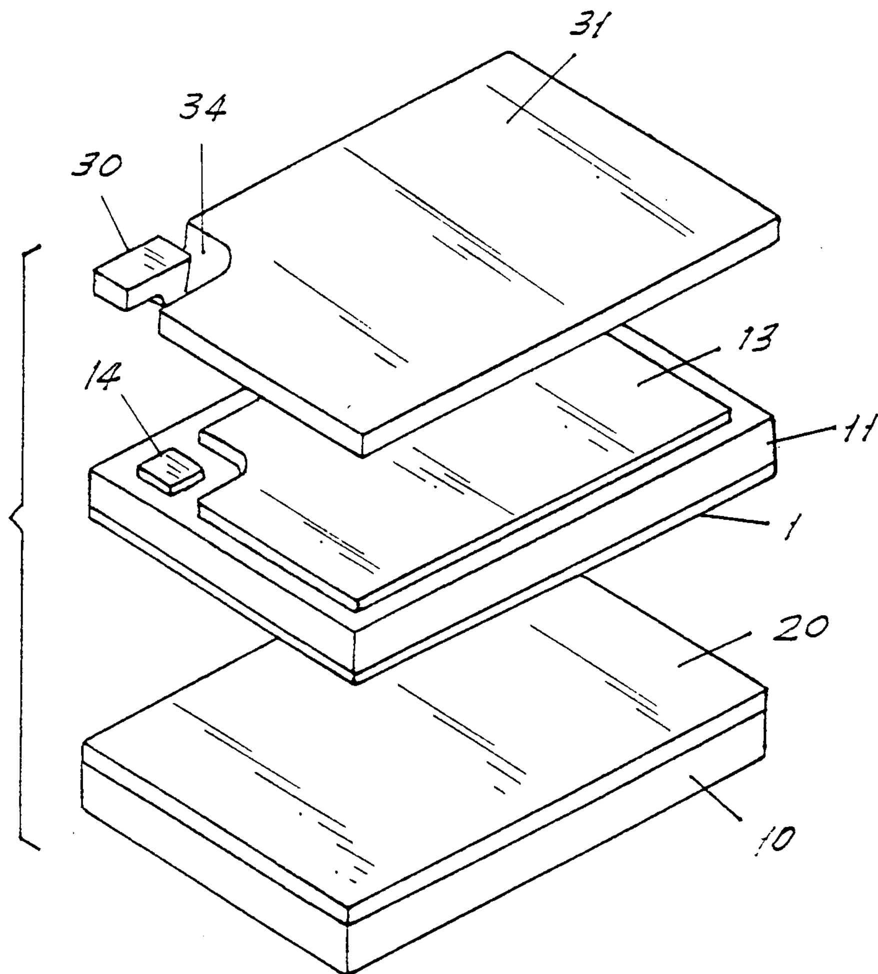


FIG. 2
12
32
30
34
31
31
30
31
30
31
34
34

FIG. 4



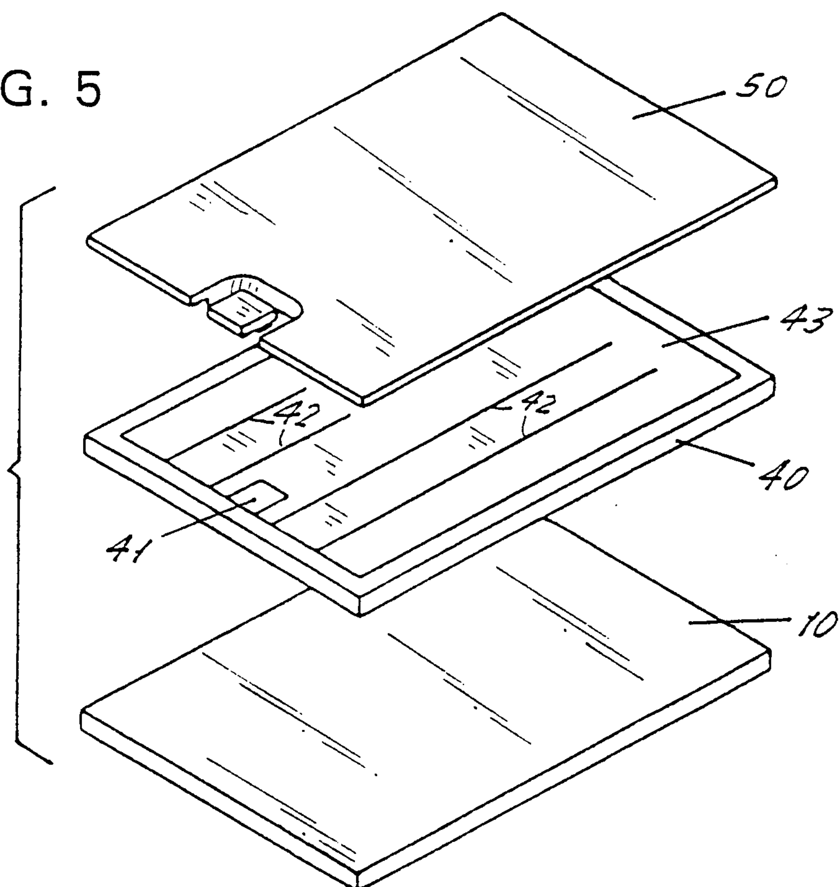


FIG. 5

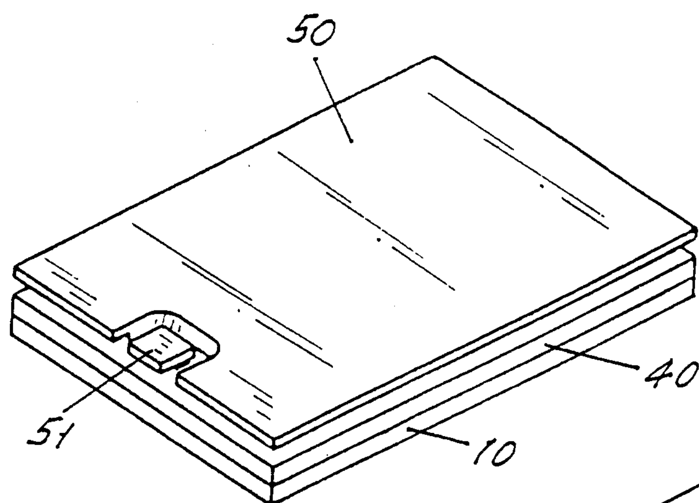


FIG. 6

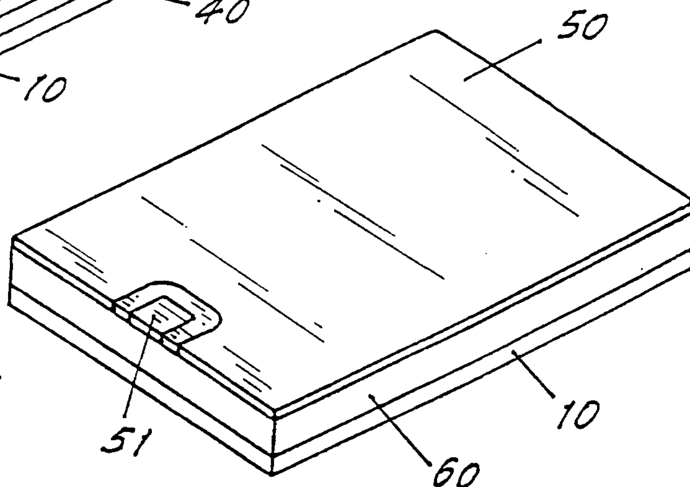


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/10785

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/76, 21/60, 21/44, 23/02
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/620-628, 678, 723, 730, 686, 685, 700, 701, 758; 438/113, 114, 33, 68, 458, 460

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS EAST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y --- A	US 4,962,062 A (UCHIYAMA et al.) 09 October 1990 (09.10.1990), figures 1(A)-1(D).	13-17 ------ 1-12
Y,P --- A,P	US 6,087,719 A (TSUNASHIMA) 11 July 2000 (11.07.2000), figures 1, 4K, 5G, 6.	13-17 ------ 1-12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 JULY 2000	15 AUG 2000

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	ALEXANDER WILLIAMS
Facsimile No. (703) 305-3230	Telephone No. (703) 308-4863

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/10785

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/10785

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

257/620-628, 678, 723, 730, 686, 685, 700, 701, 758; 438/113, 114, 33, 68, 458, 460

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I, claim(s) 1-12, drawn to a chip scale package.
Group II, claim(s) 13-17, drawn to process of making a chip scale package.

The inventions listed as Groups II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: instead of the wafer contacts being separated by a saw cut process, it can be performed by a mechnical means of cutting.