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(71) Applicant: MICROCHIP TECHNOLOGY INCORPORATED [US/US]; 2355 West Chandler Blvd., Chandler, Arizona 85224-6199 (US).

(72) Inventors: QUIQUEMPOIX, Vincent; 428 Rue de la Tuiliere, 01220 Divonne les Bains (FR). VAUCHER, Fabien; Vulliette 29g, 1000 Lausanne (CH).

(74) Agent: SLAYDEN, Bruce W., II; Slayden Grubert Beard PLLC, 401 Congress Ave., Suite 1650, Austin, Texas 78701 (US).

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(54) Title: SWITCHED-CAPACITANCE DAC USING BOOTSTRAPPED SWITCHES

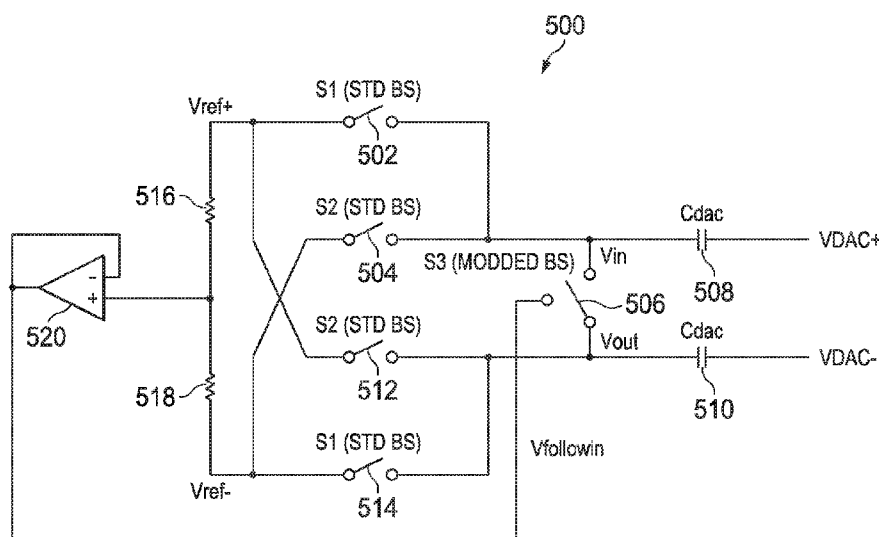


FIG. 5

(57) **Abstract:** A charge transfer digital-to-analog converter includes a differential reference voltage, a pair of capacitors, and switches including a shunting switch. The switches are configured to be switched in successive phases to generate a charge transfer through the capacitors to generate an output corresponding to a digital input. The specific switches activated and deactivated in each phase are selected according to the digital input. Each capacitor of the pair of capacitors is connected to a respective pin for the output. The shunting switch is configured to short the pair of capacitors to create a zero-differential charge on a first side of the capacitors. The shunting switch is implemented with a bootstrap circuit to maintain a constant common mode voltage of the first side of the capacitors while the shunting switch is activated.



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SWITCHED-CAPACITANCE DAC USING BOOTSTRAPPED SWITCHES

PRIORITY

5 The present application claims priority to U.S. Provisional Patent Application No. 62/564,770, filed September 28, 2017, the contents of which are hereby incorporated in their entirety.

FIELD OF THE INVENTION

10 The present disclosure relates to digital-to-analog conversion and, more particularly, to a five-level switched-capacitance digital-to-analog converter (DAC) using bootstrapped switches.

BACKGROUND

15 Analog-to-digital converters (ADC) are in widespread use today in electronics for consumers, industrial applications, etc. Typically, analog-to-digital converters include circuitry for receiving an analog input signal and outputting a digital value proportional to the analog input signal. This digital output value is typically in the form of either a parallel word or a serial digital bit string. There are many types of analog-to-digital conversion schemes such as voltage-to-frequency conversion, charge redistribution, delta modulation, as well as others. Typically, each of these conversion schemes has its advantages and disadvantages.

20 One type of analog-to-digital converter that has seen increasing use is the switched capacitor-based sigma-delta converter. Such converters may utilize several charge-transfer DACs in feedback.

SUMMARY

25 Embodiments of the present disclosure include a charge transfer DAC which may include a differential reference voltage, a pair of capacitors, and switches including a shorting switch. The switches may be configured to be switched in successive phases to generate a charge transfer through the capacitors to generate an output corresponding to a digital input, wherein the specific switches activated and deactivated in each phase are selected according to the digital input. Each capacitor of the pair of capacitors may be connected to a respective

30 pin for the output. The shorting switch may be configured to short the pair of capacitors to create a zero-differential charge on a first side of the capacitors. The shorting switch may be implemented with a bootstrap circuit to maintain a constant common mode voltage of the first

side of the capacitors while the shorting switch is activated. In combination with any of the above embodiments, the DAC may further include a voltage follower circuit configured to provide input into the shorting switch. In combination with any of the above embodiments, the voltage follower circuit may be configured to receive as an input a midpoint voltage of the differential reference voltage. In combination with any of the above embodiments, the voltage follower circuit may be configured to generate a follow voltage that matches the common mode voltage of the pair of capacitors. In combination with any of the above embodiments, the voltage follower circuit is configured to provide sufficient current to bias a transistor of the shorting switch. In combination with any of the above embodiments, the voltage follower circuit may be a wire connecting the shorting switch with a midpoint of a voltage divider for the differential reference voltage. In combination with any of the above embodiments, during a startup phase, a midpoint voltage of the differential reference voltage may be applied to each of the pair of capacitors to define the common mode voltage. In combination with any of the above embodiments, during a startup phase, differential nodes of the differential reference voltage may be applied to the pair of capacitors to define the common mode voltage. In combination with any of the above embodiments, the shorting switch may include a transistor configured to control a connection between an input pin and an output pin, the input pin and the output pin connected to respective ones of the pair of capacitors. In combination with any of the above embodiments, the input pin and the output pin may be isolated from the bootstrap circuit. In combination with any of the above embodiments, the bootstrap circuit may be configured to control a gate of the transistor to control the connection between the input pin and the output pin. In combination with any of the above embodiments, the DAC may further include a voltage follower circuit configured to provide input into the shorting switch. In combination with any of the above embodiments, the shorting switch may include a transistor configured to control a connection between respective ones of the pair of capacitors. In combination with any of the above embodiments, the input from the voltage follower circuit into the shorting switch may be configured to be input into the bootstrap circuit and to be isolated from the output. In combination with any of the above embodiments, the shorting switch may include a transistor configured to control a connection between an input pin and an output pin, the input pin and the output pin connected to respective ones of the pair of capacitors. In combination with any of the above

embodiments, the ADC may include reset switches connecting a midpoint of the differential reference voltage and the input pin and the output pin, wherein the reset switches are configured to be engaged to equalize voltages of the input pin and the output pin to the midpoint of the differential reference voltage during a reset phase. In combination with any
5 of the above embodiments, the shorting switch may be configured to maintain symmetry of differential inputs on the first side of the capacitors. In combination with any of the above embodiments, the symmetry may be defined by a same impedance seen at each first side of the capacitors so that a differential charge remains constant during switching of the capacitors when the shorting switch is enabled.

10 Embodiments of the present disclosure may include an ADC including any of the above embodiments of a DAC in a feedback configuration. The DAC may be configured to provide a feedback to an analog loop filter, the filter configured to accept an analog voltage input and output to a quantizer. The quantizer may be configured to output a bitstream and output to the DAC.

15 Embodiments of the present disclosure may include an apparatus, integrated circuit, chip, microcontroller, system on a chip (SoC), system, or device including any of the embodiments of a DAC described above.

Embodiments of the present disclosure may include methods performed by any of the DACs, ADCs, apparatuses, integrated circuits, chips, microcontrollers, SoCs, systems, or
20 devices of the above embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is an illustration of an n-level DAC implemented within an ADC, according to embodiments of the present disclosure.

FIGURE 2 is an illustration of an example 5-level, single capacitor pair DAC

25 FIGURE 3 is an illustration of an example bootstrap switch, according to embodiments of the present disclosure.

FIGURE 4 is an illustration of an example bootstrap circuit configured to avoid leakage paths on voltage inputs, according to embodiments of the present disclosure.

FIGURE 5 is an illustration of an example DAC using a modified bootstrap circuit,
30 according to embodiments of the present disclosure.

FIGURE 6 is an illustration of further details of an example DAC using a modified

bootstrap circuit and additional reset switches, according to embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 is an illustration of an n-level DAC 112 implemented within an ADC 100, according to embodiments of the present disclosure. Although DAC 112 is shown as-
5 used in ADC 100, DAC 112 may be used in any suitable application. DAC 112 may be a multi-bit DAC, include any suitable number of levels greater than two (number of bits greater than one). In one embodiment, the DAC resolution may be 5-level. DAC 112 may be implemented as a charge transfer DAC.

10 In one embodiment, DAC 112 may be implemented using bootstrapped switches. DAC 112, through its use of bootstrapped switches, may be configured to improve settling times and charge injection effects. Embodiments of the present disclosure may use bootstrapped switches, rather than CMOS switches. As a result, linearity, input voltage range, temperature range, and distortion may be improved. This may occur because the input charge
15 injection is no longer a function of the input voltage, and because the gate voltage of such bootstrapped switches is always maximized and do not vary with the input voltage. DAC 112 using bootstrap switches may lead to a lower ADC distortion due to constant gate-to-source voltage (VGS) on the DAC switches which makes charge injection effects resulting as an offset error on the ADC output and not as a distortion error.

20 In ADC 100, an analog input voltage 102 may be received to be converted to a digital value represented by output bitstream 104. Implementation of ADC 100 may include representation in an analog domain 106 and a digital domain 108. ADC 100 may be implemented using a switched capacitor-based sigma-delta converter. ADC 100 may be implemented as a charge-based converter. ADC 100 may include an analog loop filter 110,
25 a quantizer 114, and DAC 112. Analog loop filter 110 and quantizer 114 may be implemented by any suitable combination of analog or digital circuitry, application specific integrated circuits, field-programmable gate arrays, or combination thereof. DAC 112 may be implemented according to the teachings of the present disclosure.

Analog input voltage 102 may be input as signal U and fed to analog loop filter 110.
30 The output signal Y of analog loop filter 110 may be forwarded to quantizer 114 which may be configured to provide the output digital bitstream V representing a digital value of analog

input voltage 102. V may be a multi-bit bitstream. V may be connected to the input of DAC 112. The output of DAC 112, analog output V' (which may be the analog conversion of V through DAC) may be fed back to analog loop filter 110.

As discussed above, DAC 112 may be preferably implemented with a multi-level DAC. A multi-level DAC may be chosen rather than a 2-level (or single-bit) DAC as such a choice may increase converter resolution, induce less quantization noise, induce a better stability of the modulator and therefore a better dynamic range and less sensitivity to idle tones as well as better distortion behavior. A multiple-level implementation of quantizer 114 may be possible as such an implementation does not require as much accuracy as DAC 112. Since the output of DAC 112 resides at the input of ADC 100, the inaccuracies of DAC 112 are directly transmitted to the input signal and may be difficult to compensate since analog loop filter 110 cannot filter and decorrelate DAC output and analog input signals during its process. A five level, inherently linear DAC can be built with only one pair of capacitors and five switches. This is shown, for example, in U.S. Patent 7,102,558 B2.

Switching within DAC 112 may be controlled by any suitable logic, digital circuitry, analog circuitry, or any combination thereof. Control signals to switches in DAC 112 may be set according to a generation rate for the conversion.

FIGURE 2 is an illustration of an example 5-level, single capacitor pair DAC 200. DAC 200 may partially implement DAC 112.

DAC 200 may include a single pair of capacitors 208, 210. Capacitors 208, 210 may each have a capacitance of C_{dac} . DAC 200 may include input voltages V_{ref+} and V_{ref-} , and output voltages V_{DAC+} and V_{DAC-} . DAC 200 may include switches 202, 204, 206, 212, 214. Switches 202, 204, 206, 212, 214 may operate in two phases. The first phase may be denoted P1, and the second phase may be denoted P2. P1 and P2 may be non-overlapping phases. P1 and P2 may be used in a sigma-delta converter to sample and transfer charges within the modulator. Switches 202, 214 may be operated in the same manner with a common control logic signal referred to as S1. Switches 204, 212 may be operated in the same manner with a common control logic signal, referred to as S2. Switch 206 may be operated by a control logic signal referred to as S3. The specific switches that are to be activated or kept open in a given phase may depend upon the intended input of the DAC. In a given phase, only one set of switches (S1, S2, or S3) are enabled at the same time, as the other two switches

may be off. In each phase, the selected switch may be based on the bitstream to be transmitted.

Table 216 illustrates example operation of DAC 200. In sigma delta converters, capacitive charge transfer DACs such as DAC 200 may be used to realize the feedback of the modulator if the modulator is made of switched capacitors. Five different levels, corresponding to $+2/+1/0/-1/-2$ times C_{dac} times the voltage differential ($V_{ref+} - V_{ref-}$) as the differential charge that is transferred, may be asserted in two phases. In each of the two phases, there may be one sample taken and one charge transfer performed in the signal delta modulator. The table illustrates voltage levels of input to the DAC. The charge transferred in phase one for such an input is shown, as well as the charge transferred in phase two for such an input. The resulting DAC output is also shown. If there is no mismatch between the capacitor pair, then there may be inherently linear DAC performance over the 5-levels of charge transferred.

However, if switches 202, 204, 206, 212, 214 are implemented in CMOS, as standard CMOS pass-gate switches (parallel combination of NMOS and PMOS), the bandwidth of the DAC may be degraded at low temperatures and at V_{ref} common-mode voltage ($(V_{ref+} + V_{ref-})/2$ close to $V_{DD}/2$). Slow process corners create dynamic issues such as distortion. Charge injection may not be linear when switches are turned off since V_{GS} is not constant for each switch. Additionally, the input common mode may need to be defined properly if switch 206 (representing S_3) is on at first sampling. Therefore, a constant V_{GS} for the switches and proper handling of the input common mode at first sampling may be required to maintain performance over a large common-mode range and large temperature range.

FIGURE 3 is an illustration of an example bootstrap switch 300, according to embodiments of the present disclosure. Switch 300 may be used to implement switches 202, 204, 212, 214. In one embodiment, a further modification of switch 300 may be used to implement switch 206, discussed below within the context of FIGURE 4 and FIGURE 5.

Use of bootstrapped switches may avoid distortion. In switch 300, switch SW may be a main switch performing the operation of switch 300. Switch SW may be implemented by, for example, an NMOS transistor. Switch 300 may include switches M1, M2, M3, M4, and M5. Switch 300 may include a bootstrap capacitor C_{boot} .

Switch SW may be controlled by a logic signal from a remainder of the bootstrapped

circuit. Operation of switch 300 may be controlled through a control signal, which may be “SWon”. The converse of SWon may be “SWoff”. When switch 300 is to be enabled, SWon may be a logical one and SWoff may be a logical zero. When switch 300 is to be disabled, SWon may be a logical zero and SWoff may be a logical one.

5 Switches M1, M4, and M5 may be controlled by SWoff. Switches M2 and M3 may be controlled by SWon. Switch M1 may be connected to ground and to a first plate or side of Cboot. Switch M3 may be connected to Vin (which is connected to a first plate of Cdac 208 in FIGURE 2, in turn connected to Vdac+ on its second plate). Switch M4 may be connected to a supply voltage, VDD, and to a second plate of Cboot. Switch M5, SW, and
10 switch M2 may be connected to a common node, whose voltage may be denoted as Vboot. Switch M2 may also be connected to the second plate of Cboot. Switch M5 may also be connected to ground. SW may connect Vin and Vout (which is connected to a first plate of Cdac 210 in FIGURE 2, in turn connected to Vdac- on its second plate).

The bootstrap portions of switch 300 may be configured to provide a gate voltage for
15 SW that is dependent upon Vin such that the VGS is constant and maximized. When this goal is attained, the on-resistance of the switch is minimized and not dependent upon input voltage. In FIGURE 3, bootstrapping may be performed in two phases. The phases may be non-overlapping. A first phase may include SWon being a logic zero or low and SWoff being a logic one or high. A second phase may include SWoff being a logic zero or low and SWon
20 being a logic one or high. Vboot is shown as going from ground to ($\alpha \cdot VDD + Vin$).

In the first phase, SWoff is logic high, meaning that SW is itself off. The Cboot may be precharged during this phase to a maximum VDD voltage. This precharge may be performed by the switching action of M1 and M4. During the precharge phase, the main switch, SW, is kept off through switch M5 driving the gate of SW to ground.

25 In the second phase, SWon is logic high, meaning that SW is itself on. Activation of M2 and M3 results in connection of Cboot to both Vin and the gate of SW. This may cause the gate voltage, Vboot, to be ($VDD + Vin$) since the charge of Cboot remains basically unchanged from the first phase. In this case, the VGS of SW is constant, maximal, and equal to VDD.

30 In implementations, the charge of Cboot may not be perfectly maintained between the on and off phases. As a result, Cboot may be subject to losses due to parasitic capacitances

of switches attached to Cboot. The efficiency of the charging Cboot may be given as α and may be within a range of zero to one, wherein one represents perfect efficiency. The factor α may be made close to one if the Cboot capacitance value is much larger than the parasitic capacitances of the switches. The charge transfer may be impacted by such parasitics such that a gate voltage, Vboot, for SW may be $(\alpha \cdot V_{DD} + V_{in})$. The bootstrapping technique may avoid VGS variation and make charge injection constant and not vary with Vin. Since VGS is maximized, the on-resistance (Ron) of the switch is then minimized, and bandwidth is maximized. The charge injection can be further minimized by reducing the width of the main switch which will, in this case, reduce the bandwidth linearly by increasing Ron linearly.

Accordingly, in one embodiment, one or more of switches 202, 204, 206, 212, 214 may be implemented with a bootstrapped technique shown in FIGURE 3, wherein Vin of the voltage of the switch can be either Vref+ or Vref-.

However, using such an implementation for the switch 206 may induce additional undesired effects rendering it inefficient. Switch M3 may render switch 206 asymmetrical, if implemented according to FIGURE 3, as the parasitic capacitances on Vin and Vout are not equal as in a standard CMOS switch implementation of switch 206. M3, as a voltage follower, may induce additional charge injection and may induce an additional leakage current path on the voltage Vin. Therefore, in one embodiment modifications of this bootstrap switch implementation may be made to recover symmetry and avoid any leakage path on the Vin voltage and avoid any additional charge injection. In a further embodiment, switch 206, the main switch to short the surfaces of capacitors 208, 210 together, may be implemented with a modified kind of bootstrap circuit as shown in FIGURE 4.

FIGURE 4 is an illustration of an example bootstrap circuit 400 configured to avoid leakage paths on voltage inputs, according to embodiments of the present disclosure. Circuit 400 may modify circuit 300 as shown in the figure and described below. Circuit 400 may be symmetrical and avoid effects of switch M3 connected to Vin as shown in FIGURE 3.

M3 might not be directly connected to Vin, but rather to another voltage, Vfollowin. Vfollowin may be another input to circuit 400. Voltage Vin may be unmodified by M3. In FIGURE 4, Vboot voltage may be equal to $(\alpha \cdot V_{DD} + V_{followin})$ during the on phase of SW. If Vfollowin is equal to Vin, then the same Vboot voltage can be created with the operations of the switches.

FIGURE 5 is an illustration of an example DAC 500 using a modified bootstrap circuit, according to embodiments of the present disclosure. DAC 500 may further implement DAC 200 and DAC 112, DAC 500 may include one or more bootstrap switches to implement, for example, switch 506.

5 Switch 506 may also be referenced as S3 and may be implemented by the modified bootstrap switch 400 of FIGURE 4. Switch 506 may correspond to S3 of FIGURE 2. Switches 502, 514 may also be referenced as S1 and switched together, corresponding to S1 of FIGURE 2. Switches 502, 514 may be implemented by the bootstrap switch 300 of FIGURE 3. Switches 504, 512 may also be referenced as S2 and switched together,
10 corresponding to S2 of FIGURE 2. Switches 502, 514 may be implemented by the bootstrap switch 300 of FIGURE 3. DAC 500 may include a pair of capacitors 508, 510 each with a value of C_{dac} , each output to V_{dac+} and V_{dac-} . DAC 500 may receive inputs V_{ref+} and V_{ref-} . Switch 506 may receive a $V_{followin}$ input from an output of a voltage follower 520.

In one embodiment, DAC 500 may include a voltage follower 520. Voltage follower
15 520 may be a unity gain buffer. Voltage follower 520 may be configured to transfer its input to its output unchanged. Voltage follower 520 may be denoted as a voltage “follower” in that its output voltage follows its input voltage. While voltage follower 520 may provide a voltage gain of, ideally, one, it may provide a current boost. Voltage follower 520 may be configured to prevent portions of DAC 500 from receiving its output from loading portions of DAC 500
20 connected to its input. Voltage follower 520 may be implemented with an op-amp and a feedback loop from its output to its input.

In one embodiment, voltage follower 520 may have as its other input (as compared to the feedback loop) a voltage from a midpoint of a voltage divider. The midpoint voltage may be given as $V_{CMVref} = ((V_{ref+}) + (V_{ref-}) / 2)$. The voltage divider may include resistors
25 516, 518 connected as in series together. Resistors 516, 518 may have matched impedances. The voltage divider may be connected between V_{ref+} and V_{ref-} . In various embodiments, other implementations of providing a divided voltage to voltage follower 520 may be used.

For switch 506, voltage connected to capacitor 508 may be a first input, or V_{in} . Voltage connected to capacitor 510 may be a second input, or V_{out} . In one embodiment,
30 voltage follower 520 may be configured to output a voltage denoted as V_{follow_in} , representing the followed voltage. In another embodiment, V_{follow_in} may be an additional,

third input to switch 506. In yet another embodiment, switch 506 may be implemented with a modified bootstrap circuit. $V_{\text{follow_in}}$ may be used as an input to the bootstrap circuit of switch 506. For example, $V_{\text{follow_in}}$ may be used as an input of the M3 switch in FIGURE 4 to the bootstrap circuit of switch 506.

5 In one embodiment, voltage follower 520 may be configured to provide sufficient current to bias $V_{\text{follow_in}}$ in switch 506. $V_{\text{follow_in}}$ may be at the same voltage as the common mode voltage of $V_{\text{ref+}}$ and $V_{\text{ref-}}$ for capacitors 508, 510. In another embodiment, voltage follower 520 may be replaced by a simple wire connected to the resistive divider generating the midpoint voltage. This configuration is preferred for size and power
10 consumption optimization but can impact bandwidth if the midpoint voltage settling time is large compared to the P1 or P2 phases of the sigma-delta modulator.

Switch 506 may be configured to short capacitors 508, 510 together, as these are connected to V_{in} and V_{out} , respectively. This may create zero differential input voltage. However, the top plates of capacitors 508, 510 may have a high impedance. Accordingly,
15 without the features of the embodiments of the present disclosure, the common mode may drop due to a requirement for input current with the switches on. In contrast, bootstrapped switch 506 may have no current pulled from capacitors 508, 510 but yet the common mode may be maintained when switch 506 is on. Thus, loss of charge on capacitors 508, 510 may be avoided when switch 506 is on while bootstrapping is still used.

20 As per the teachings of this invention, the V_{in} and V_{out} of the shorting switch 506 should be properly defined before input switch 506 is enabled as these voltages are essentially high impedance during a phase where S3 is on. In one embodiment, one can ensure this by having a first phase where S1 or S2 can be enabled and then charging the V_{in} and V_{out} of S3 so that common-mode voltage at the inputs of the capacitors is defined when the capacitors
25 are shorted through S3.

FIGURE 6 is an illustration of further details of an example DAC 600 using a modified bootstrap circuit and additional reset switches, according to embodiments of the present disclosure. DAC 600 may otherwise be implemented according to DAC 500 of FIGURE 5.

30 DAC 600 may include a reset switch 602 and a reset switch 604, each connected between $V_{\text{follow_in}}$ and respective ones of V_{in} and V_{out} . Reset switches 602, 604 may be

implemented as, for example, CMOS switches. Reset switches 602, 604 may be enabled in a first phase (typically the reset phase of the ADC) so that the voltages V_{in} and V_{out} are equal to $V_{followin}$ during this reset phase. Reset switches 602, 604 may be disabled, or open during the rest of the operation. Furthermore, reset switches 602, 604 may be enabled periodically to remove or otherwise address leakage current. In addition, reset switches 602, 604 may be enabled whenever S3 is on. This implementation also properly defines the common-mode $((V_{in}+V_{out})/2)$ of the switch 506 and avoids switching with a floating common-mode if S3 is enabled in the reset phase of the ADC.

Although example embodiments have been described above, other variations and embodiments may be made from this disclosure without departing from the spirit and scope of these embodiments.

CLAIMS

We claim:

- 5 1. An apparatus, comprising:
a charge transfer digital-to-analog converter (DAC), the DAC comprising:
a differential reference voltage;
a pair of capacitors;
a plurality of switches including a shorting switch; and
10 wherein:
the plurality of switches are configured to be switched in successive
phases to generate a charge transfer through the capacitors to generate an
output corresponding to a digital input, wherein the specific switches activated
and deactivated in each phase are selected according to the digital input;
15 each capacitor of the pair of capacitors is connected to a respective pin
for the output;
the shorting switch is configured to short the pair of capacitors to
create a zero-differential charge on a first side of the capacitors; and
the shorting switch is implemented with a bootstrap circuit to maintain
20 a constant common mode voltage of the first side of the capacitors while the shorting switch
is activated.
- 25 2. The apparatus of Claim 1, further comprising a voltage follower circuit
configured to provide input into the shorting switch.
3. The apparatus of Claim 2, wherein the voltage follower circuit is configured to
receive as an input a midpoint voltage of the differential reference voltage.
- 30 4. The apparatus of any of Claims 2-3, wherein the voltage follower circuit is
configured to generate a follow voltage that matches the common mode voltage of the pair of
capacitors.

5. The apparatus of any of Claims 2-4, wherein the voltage follower circuit is configured to provide sufficient current to bias a transistor of the shorting switch.

6. The apparatus of any of Claims 2-5, wherein the voltage follower circuit is a wire connecting the shorting switch with a midpoint of a voltage divider for the differential reference voltage.

7. The apparatus of any of Claims 1-6, wherein during a startup phase, a midpoint voltage of the differential reference voltage is applied to each of the pair of capacitors to define the common mode voltage.

8. The apparatus of any of Claims 1-7, wherein during a startup phase, differential nodes of the differential reference voltage are applied to the pair of capacitors to define the common mode voltage.

15

9. The apparatus of any of Claims 1-8, wherein:
the shorting switch includes a transistor configured to control a connection between an input pin and an output pin, the input pin and the output pin connected to respective ones of the pair of capacitors;

20 the input pin and the output pin are isolated from the bootstrap circuit.

10. The apparatus of Claim 9, wherein the bootstrap circuit is configured to control a gate of the transistor to control the connection between the input pin and the output pin.

25

11. The apparatus of any of Claims 1-10, wherein:
the apparatus further includes a voltage follower circuit configured to provide input into the shorting switch;

the shorting switch includes a transistor configured to control a connection between
30 respective ones of the pair of capacitors; and

the input from the voltage follower circuit into the shorting switch is configured to be

input into the bootstrap circuit and to be isolated from the output.

12. The apparatus of any of Claims 1-11:

wherein the shorting switch includes a transistor configured to control a connection between an input pin and an output pin, the input pin and the output pin connected to respective ones of the pair of capacitors; and

further comprising reset switches connecting a midpoint of the differential reference voltage and the input pin and the output pin, wherein the reset switches are configured to be engaged to equalize voltages of the input pin and the output pin to the midpoint of the differential reference voltage during a reset phase.

13. The apparatus of any of Claims 1-12, wherein the shorting switch is configured to maintain symmetry of differential inputs on the first side of the capacitors.

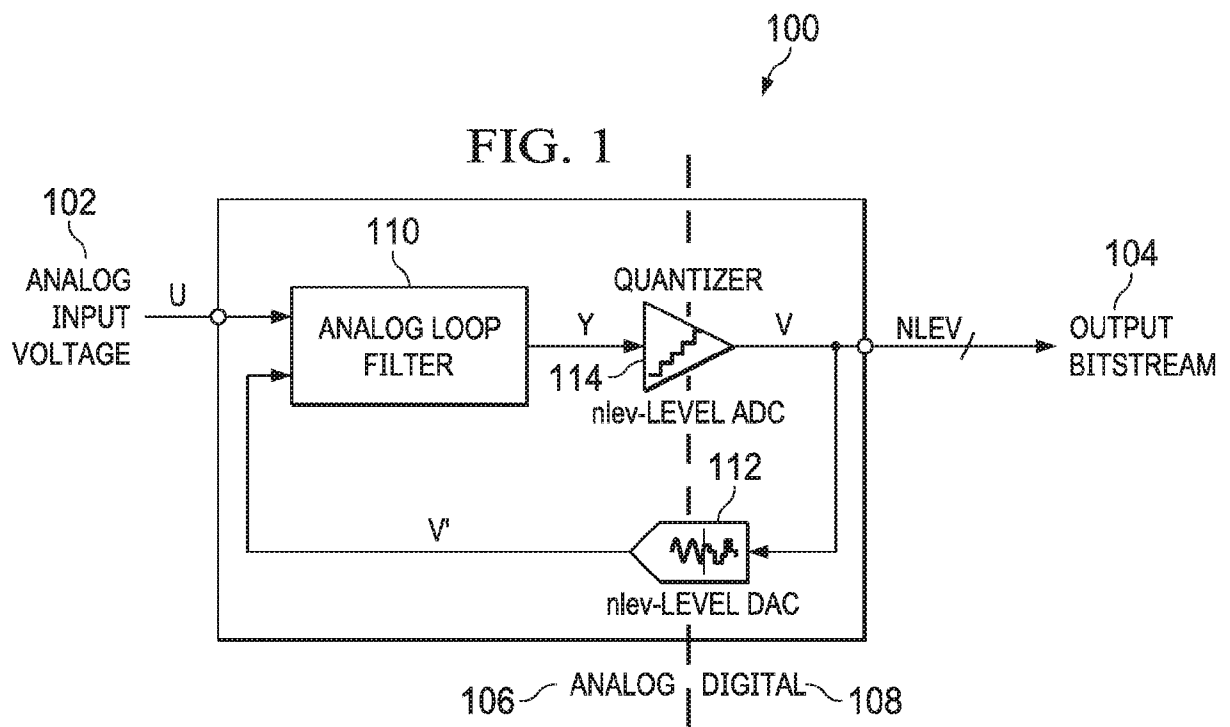
14. The apparatus of Claim 13, wherein the symmetry is defined by a same impedance seen at each first side of the capacitors so that a differential charge remains constant during switching of the capacitors when the shorting switch is enabled.

15. A method, comprising operation of any of the apparatuses of Claims 1-14.

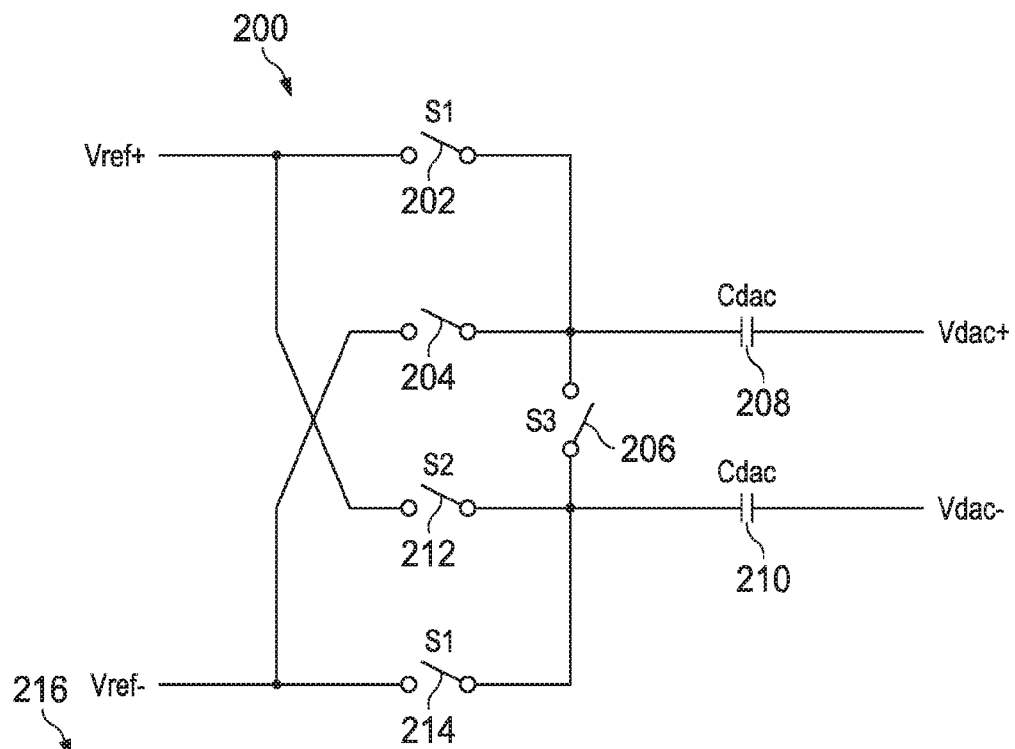
16. An analog to digital converter, comprising any of the apparatuses of Claims 1-

14.

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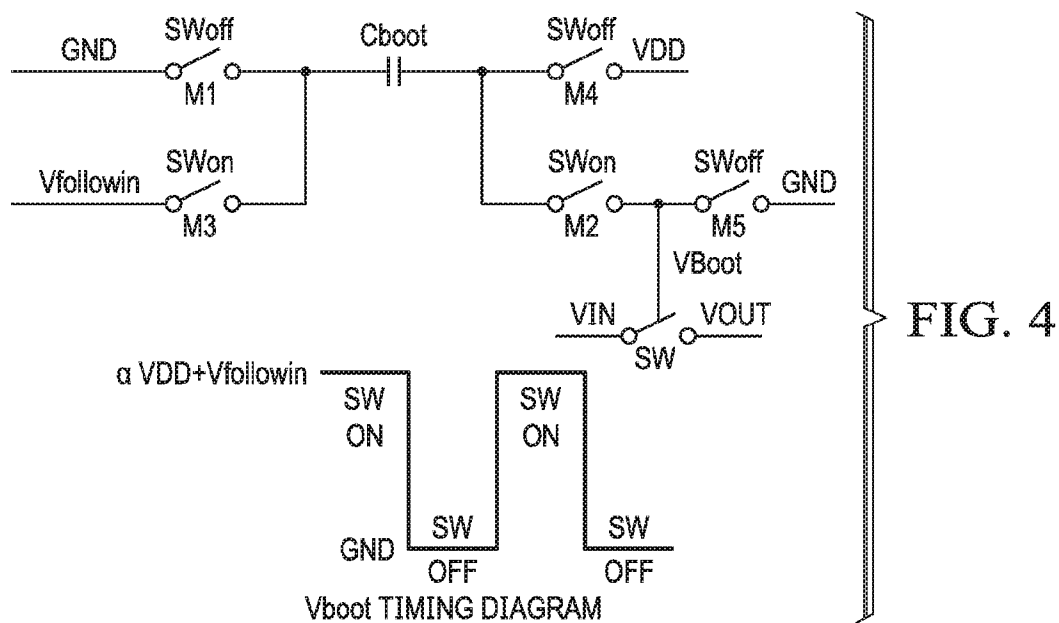
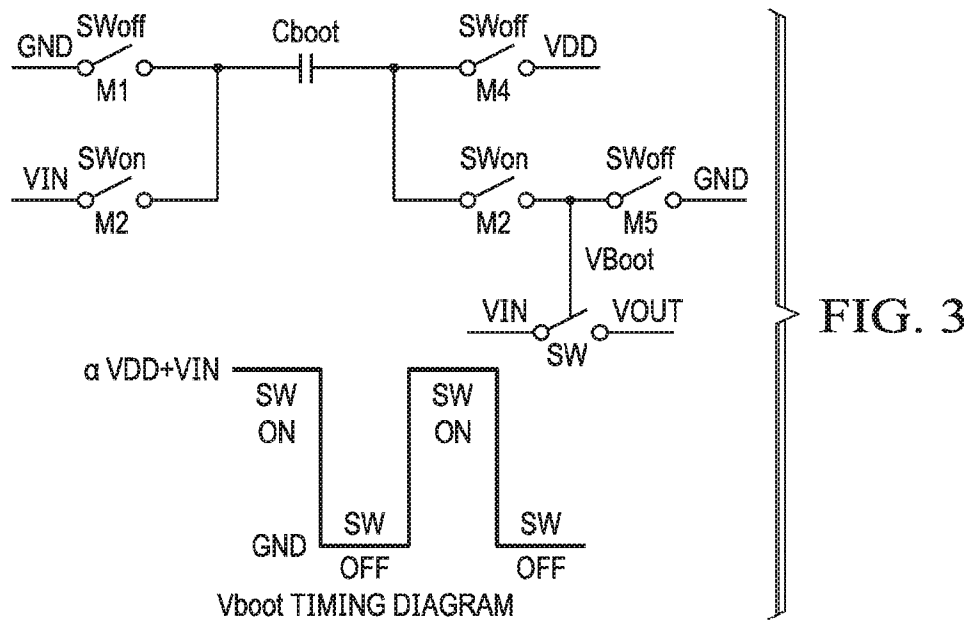
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DAC INPUT	SWITCHES ON IN PHASE 1	SWITCHES ON IN PHASE 2	CHARGE TRANSFER IN PHASE 1	CHARGE TRANSFER IN PHASE 2	DAC OUTPUT (PHASE 2 - PHASE 1)
2	S2	S1	$-C_{dac} \cdot V_{ref}$	$+C_{dac} \cdot V_{ref}$	$+2C_{dac} \cdot V_{ref}$
1	S2	S3	$-C_{dac} \cdot V_{ref}$	0	$+C_{dac} \cdot V_{ref}$
	S3	S1	0	$+C_{dac} \cdot V_{ref}$	
0	S3	S3	0	0	0
	S2	S2	$-C_{dac} \cdot V_{ref}$	$-C_{dac} \cdot V_{ref}$	0
	S1	S1	$+C_{dac} \cdot V_{ref}$	$+C_{dac} \cdot V_{ref}$	0
-1	S3	S2	0	$-C_{dac} \cdot V_{ref}$	$-C_{dac} \cdot V_{ref}$
	S1	S3	$+C_{dac} \cdot V_{ref}$	0	
2	S1	S2	$+C_{dac} \cdot V_{ref}$	$-C_{dac} \cdot V_{ref}$	$-2C_{dac} \cdot V_{ref}$

FIG. 2

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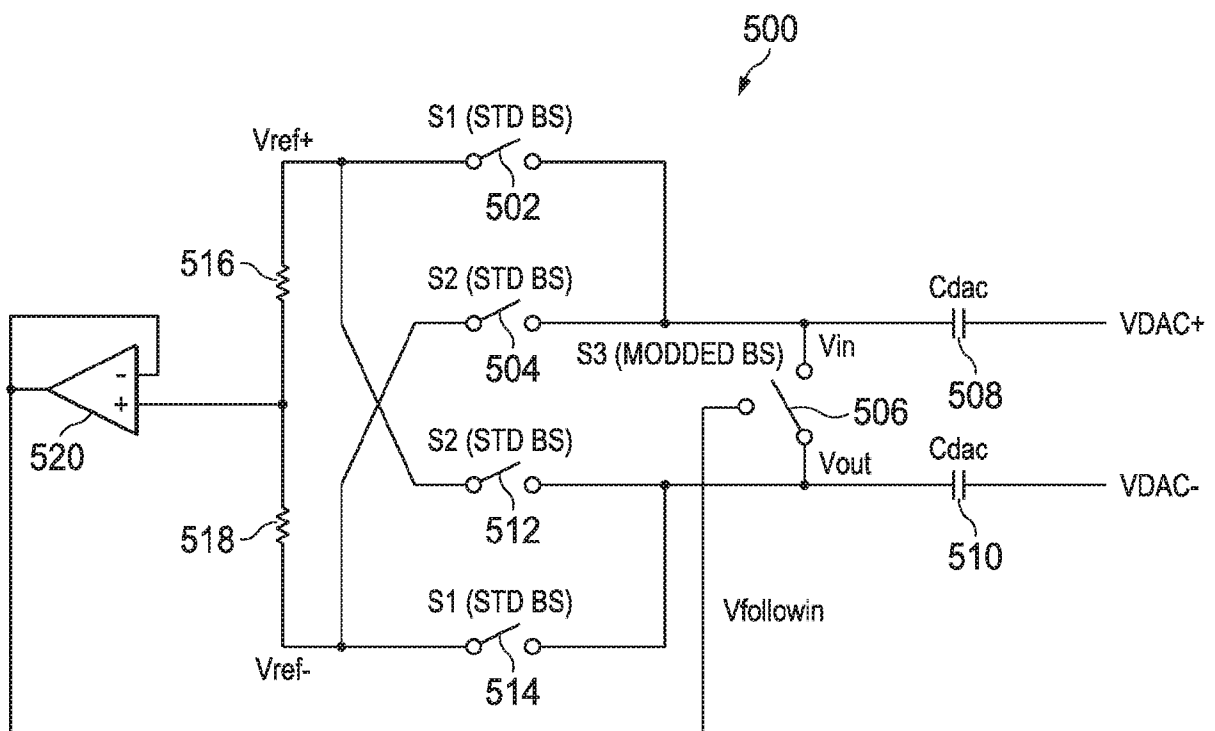


FIG. 5

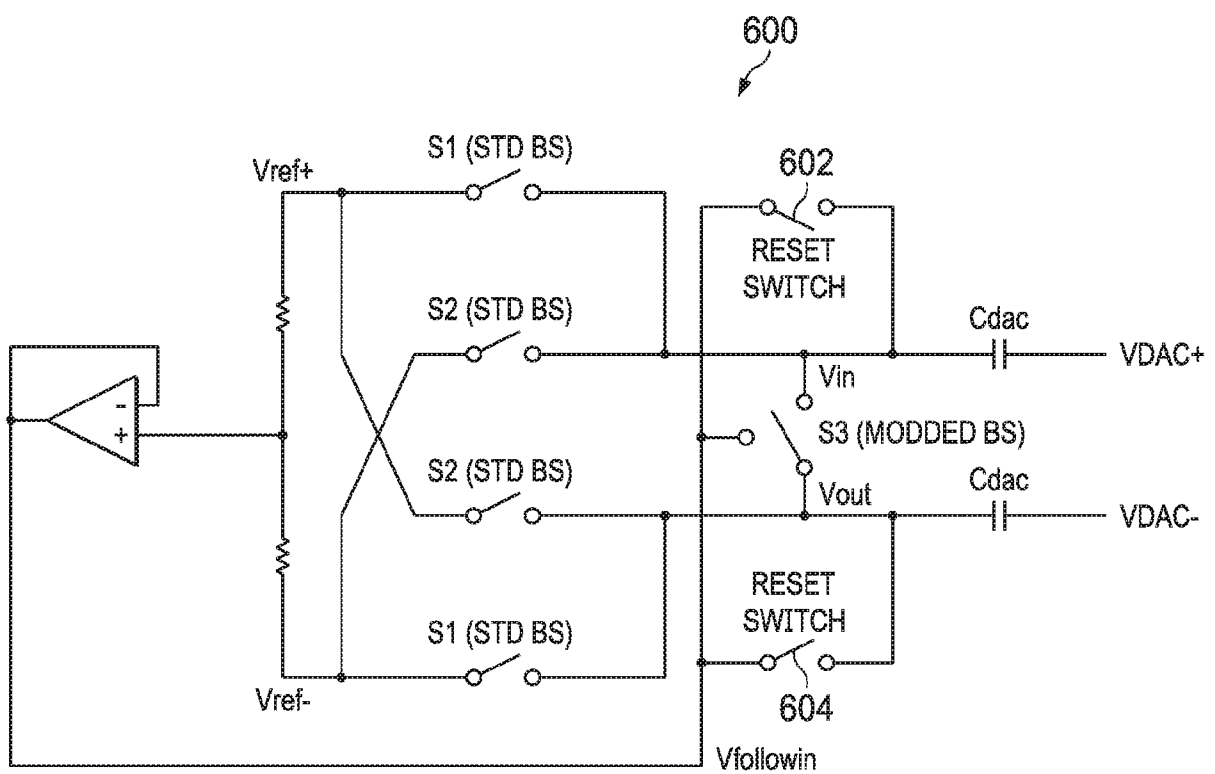


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2018/053007

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03M1/06

ADD. H03M1/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/253354 A1 (QUIQUEMPOIX VINCENT [FR]) 11 September 2014 (2014-09-11) paragraphs [0024], [0031]; figures 1-3 -----	1-16
A	MENG XIN ET AL: "Bootstrapping techniques for floating switches in switched-capacitor circuits", 2013 IEEE 56TH INTERNATIONAL MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS (MWSCAS), IEEE, 3 August 2014 (2014-08-03), pages 398-401, XP032648683, ISSN: 1548-3746, DOI: 10.1109/MWSCAS.2014.6908436 ISBN: 978-1-4799-4134-6 [retrieved on 2014-09-23] Section III; figures 6-9 ----- -/-	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

20 December 2018

Date of mailing of the international search report

07/01/2019

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Jesus, Paulo

INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	TSUNG-SUM LEE ET AL: "Design techniques for low-voltage micropower CMOS switched-capacitor delta-sigma modulator", CIRCUITS AND SYSTEMS, 2004. PROCEEDINGS. THE 2004 IEEE ASIA-PACIFIC CONFERENCE ON TAINAN, TAIWAN DEC. 6-9, 2004, PISCATAWAY, NJ, USA, IEEE, vol. 1, 6 December 2004 (2004-12-06), pages 249-252, XP010783092, DOI: 10.1109/APCCAS.2004.1412740 ISBN: 978-0-7803-8660-0 Section 3.3; figures 1-2	1-16
A	ZHAO ZHOU ET AL: "A gain boosting switch for S/H circuit using clock boosting and symmetrical techniques to decrease the effect of channel charge injection", 2013 INTERNATIONAL CONFERENCE ON COMPUTATIONAL PROBLEM-SOLVING (ICCP), IEEE, 26 October 2013 (2013-10-26), pages 308-311, XP032637853, DOI: 10.1109/ICCPS.2013.6893517 [retrieved on 2014-09-05] Section II; figures 1-10	1-16

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Information on patent family members

International application No

PCT/US2018/053007

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		TW 201442435 A	01-11-2014
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		WO 2014164211 A1	09-10-2014
