United States Patent

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[54] **SINGLE PULSE GENERATING CIRCUIT**
7 Claims, 2 Drawing Figs.

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[50] **Field of Search** 320/1; 317/141,151; 307/246,293,294,141,141.8

[56] **References Cited**
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ABSTRACT: A circuit uses a capacitor store to generate a single pulse in response to the closing of a switch. A first terminal of the capacitor is normally connected to a charging source. The closing of the switch transfers the first terminal from the charging source to a discharge path after a predetermined time delay. The discharge path is completed in response to a control signal so that the capacitor is discharged and a single pulse appears at the second terminal of the capacitor.

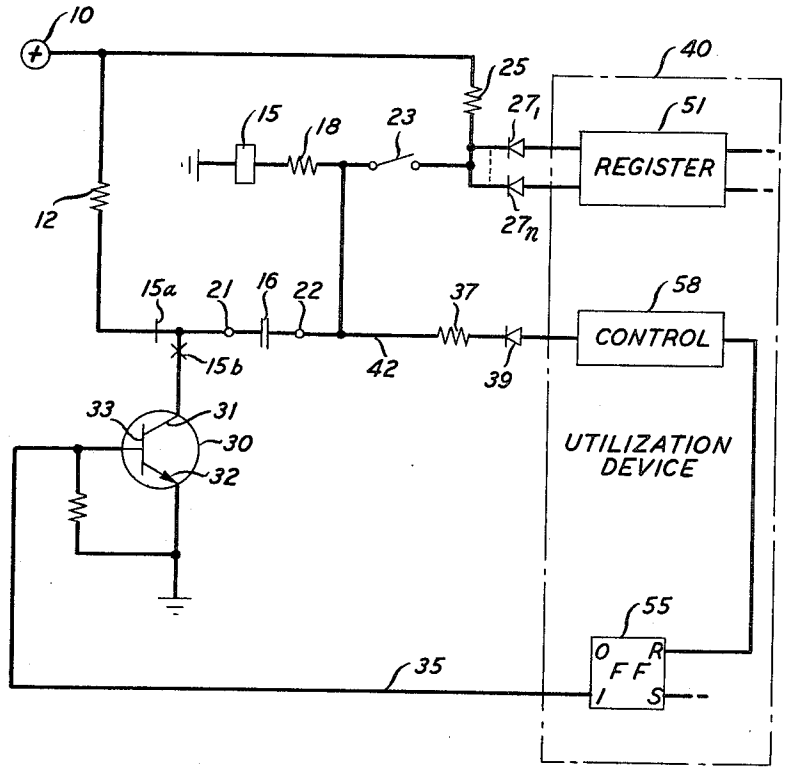


FIG. 1

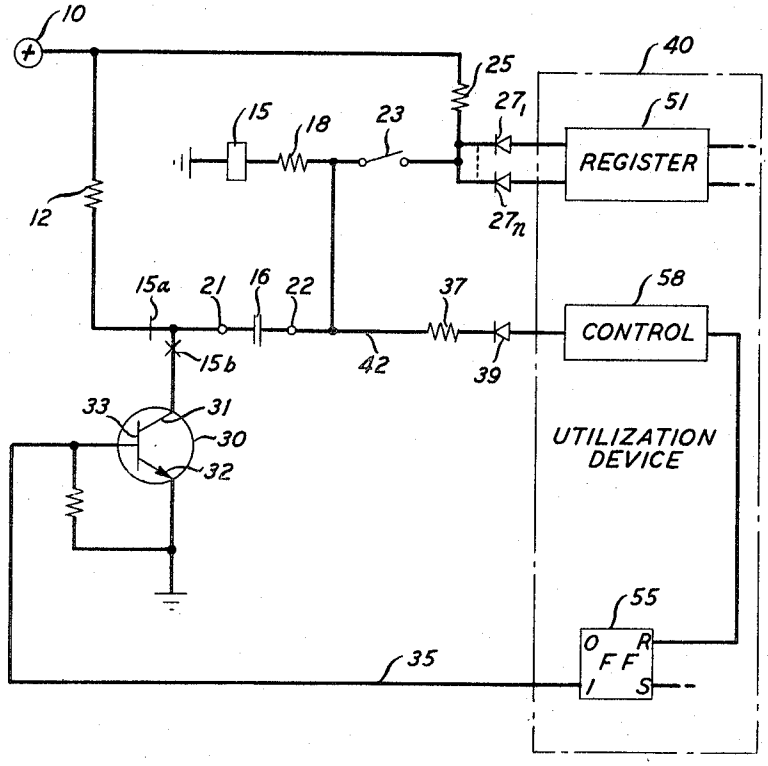
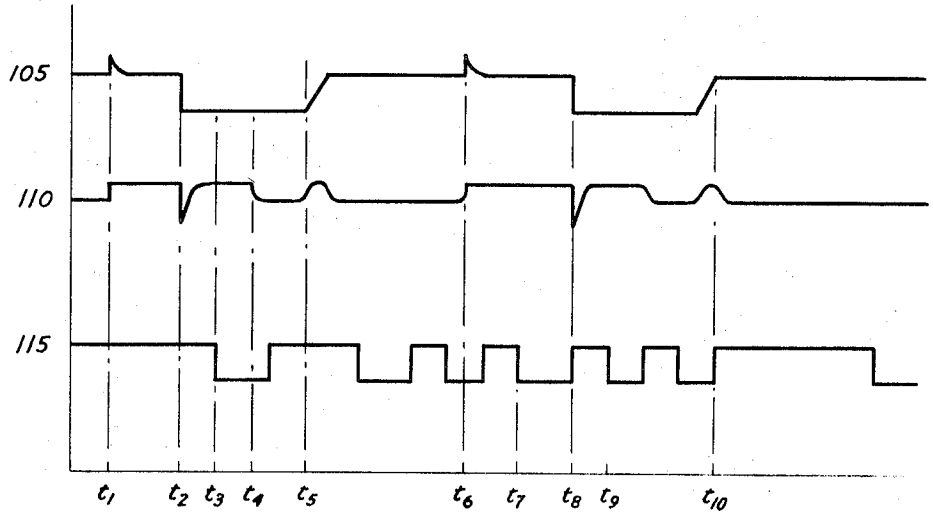


FIG. 2



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SINGLE PULSE GENERATING CIRCUIT

BACKGROUND OF THE INVENTION

This invention is related to signaling arrangements and, more particularly, to arrangements for inserting signals into data transmission systems.

In data processors and data transmission systems, it is often necessary to provide a manually operated signal source such as a keyboard on an operator's console. The signal source may be used to control the operation of the system or to insert information therein and usually includes a plurality of mechanical switches which are operated as keys in accordance with the signaling information to be inserted. Since the switches operate independently from the connected data processor or data transmitter, apparatus must be employed to control the time of insertion so that the inserted signals do not interfere with the operation of the connected system.

The control apparatus may simply interrupt the system operation during the manual insertion of signals. The speed of manual signal insertion, however, is generally slow compared to the normal system operating time. In high speed data systems, such interruptions may substantially delay and slow down system operation. Alternatively, the manually inserted information can be temporarily stored and inserted when the data system is available. The storage element may be a capacitor which is charged or discharged through an operator controlled switch. For example, the voltage pulse generated during the capacitor discharge can be applied through the switch to the input devices of the connected data system. If, however, the switch contacts are held closed for an extended period of time or close a number of times in rapid succession due to bounce or operator action, erroneous signals can result.

BRIEF SUMMARY OF THE INVENTION

My invention is a pulse generator circuit for inserting single pulses into a data system in which a charge storage device is transferred between the charging path and the switchable discharge path after a predetermined time delay. The start of the time delay is controlled by a manual switch. The discharge path is completed and the storage device is discharged in response to a signal occurring when the data system is available to receive pulses from the generator circuit. This discharge causes a single pulse to be coupled to the data system. Because of the time delay in connecting the storage device to the discharge path, the closing of the manual switch for an extended period of time or the occurrence of successively repeated switch closings does not operate to generate a plurality of pulses.

In an illustrative embodiment of my invention, one terminal of a capacitor store is connected to a current source through a normally closed relay contact and the other capacitor terminal is connected via a manually controlled switch to a data system input. The closing of the switch operates the relay so that the normally closed contact pair is opened and the first capacitor terminal is connected to a transistor switch via a second normally open relay contact pair. The transistor switch closes in response to a signal which indicates the data system is available and the connected capacitor is discharged in the event that the data system availability signal is applied a predetermined time interval after the relay operation has been started.

DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts an illustrative embodiment of my invention; and

FIG. 2 shows waveforms useful in describing the embodiment of FIG. 1.

DETAILED DESCRIPTION

The circuit of FIG. 1 shows a single pulse generator which inserts a pulse into utilization device **40** in response to the operation of switch **23** and transistor **30**. The circuit includes capacitor **16** which is used as a storage device, a charging or

energizing path including resistor **12**, normally closed relay contact **15***a*, resistor **18**, and relay coil **15**, and a discharge or deenergizing path including switch **23**, normally open relay contact **15***b*, and transistor **30**. Capacitor **16** is charged via the aforementioned charging path to the voltage determined by positive voltage supply **10**; the charging current, however, is insufficient to energize relay **15**. The closing of switch **23** transfers terminal **21** of capacitor **16** from the charging path to the discharge path after relay **15** pulls in. When transistor **30** in the discharge path is turned on, capacitor **16** is discharged through diodes 27_1 through 27_n and diode **39** to input devices in utilization device **40**. These devices may include an input register **51** connected to diodes 27_1 through 27_n and control **58** connected to diode **39** or other input devices well known in the art.

Switch **23** may be a mechanical switch which is controlled by an operator. As is well known in the art, many mechanical switches suffer from transient mechanical resonances for a period of time after its contacts are initially closed or opened. This mechanical resonance may persist for several hundred microseconds so that a plurality of pulses are conducted therethrough from a discharging storage device. According to my invention, the operation of switch **23** controls the charge or discharge of capacitor **16** through relay **15**. This relay, which may appropriately be a mercury relay well known in the art, operates without bounce only after a fixed period of at least 1 millisecond from the time voltage is applied to its coil. In the circuit of FIG. 1 the discharge of capacitor **16** does not occur until 1 millisecond after the closing of switch **23**. At this time the mechanical resonance effects in switch **23** are no longer present. Relay **15** therefore acts as a time delay device which prevents circuit operation until transient mechanical resonance has been completed.

If switch **23** has been opened for an extended period of time, relay contact **15***a* is closed and capacitor **16** is charged via resistors **12** and **18** and relay **15** to a predetermined positive voltage. Terminal **22** is then at a ground reference potential and terminal **21** is positive. The closing of switch **23** permits current to be applied to relay **15** through resistor **25** and resistor **18**. After a 1 millisecond time interval, in which interval the mechanical resonance transients of switch **23** are over, relay contact **15***a* opens and relay contact **15***b* closes so that terminal **21** is transferred from its charging path to a discharge path. This discharge path connects terminal **22** to device **40** via diodes 27_1—27_n and **39** but no discharge can occur until transistor **30** is rendered conductive.

Transistor switch **30** is controlled by a signal from the one output of flip-flop **55** in device **40**. This positive going signal causes current to flow through the base emitter path of transistor **30** when device **40** is in a state that permits the application of input signals controlled by switch **23**. In this way, according to my invention, it is only possible to insert a pulse if device **40** is in an available state. Transistor **30** operates as a control element in the discharge path. Collector **31** is connected via contact **15***b* to terminal **21** and emitter **32** is connected to a ground reference potential. The positive signal at base **33** causes a low impedance to appear between collector **31** and emitter **32**. Since emitter **32** is connected to a ground reference potential, collector **31** at this time is substantially at the same reference potential. The low impedance path of transistor **30** completes the discharge path and a negative signal is available at terminal **22**. The negative signal is applied via current limiting resistor **37** and diode **39** to control device **58** and via diodes 27_1 through 27_n to input register **51**. It is to be understood that collector **31** may be connected to several capacitor storage device arrangements and the signal from flip-flop **55** may complete a plurality of discharge paths, each including a switch such as switch **23** and a relay such as relay **15**.

Flip-flop **55** remains set until the negative pulses from terminal **22** have initiated an operation in device **40**. The operation causes flip-flop **55** to reset so that the input signal to base **33** is removed and transistor **30** is rendered nonconductive.

The reset of flip-flop 55 is due to a pulse from control 58 which in turn receives a negative pulse from diode 39. As long as switch 23 remains closed no charge can be applied to capacitor 16 so that a further signal from flip-flop 55 cannot produce another output pulse at terminal 22. The opening of switch 23 at this time starts to release relay 15. If, however, switch 23 bounces, the delay in the release of relay 15 ensures that no charge can be transferred to capacitor 16 via contact 15*a*. In this way only a single pulse may be applied to device 40. Thus, according to my invention, the charge placed on capacitor 16 can only cause one negative pulse to be applied to each associated input of device 40 in response to a data system available signal occurring concurrently if switch 23 has been previously closed.

FIG. 2 shows waveforms describing the operation of the circuit of FIG. 1. Waveform 105 represents the voltage at terminal 21, while waveform 110 represents the waveform that appears at terminal 22. Waveform 115 is the one output of flip-flop 55 that is applied to base 33 when device 40 is available for input signals. Assume that prior to time t_1 switch 23 has been opened and capacitor 16 has been completely charged. The closing of switch 23 at t_1 causes current to be applied to relay 15. Because of the delay in pull-in of relay 15, the transfer of terminal 21 from the charging path to the discharge path via contacts 15*a* and 15*b* does not occur until time t_2. The closing of switch 23 connects resistor 25 to terminal 22 and the voltage at terminal 22 goes positive at t_1 in accordance with the voltage divider effect of series connected resistors 25 and 18 and relay 15. This increase in voltage is shown on waveform 110 at t_1 and results in the positive transient on terminal 21 which is shown on waveform 105 at t_1.

Waveform 115 at base 33 is positive at time t_2 so that the base-emitter path of transistor 30 is a low impedance path. Therefore, at time t_2 the voltage at terminal 21 changes from a positive value to the ground reference potential. Since the voltage across a fixed value of capacitance cannot change instantaneously, the negative going voltage at terminal 21 causes the voltage at terminal 22 to go negative from the ground reference potential. This is shown at t_2 in waveform 110. In the time interval between t_2 and t_3, capacitor 16 discharges via diodes 27_1 through 27_n, diode 39 and charges toward a voltage determined by the source 10, resistors 25 and 18. At time t_3 utilization device 40 starts operating in response to the applied negative pulses and flip-flop 55 is reset. Waveform 115 goes to the ground reference potential, and the collector-emitter path of transistor 30 is rendered nonconductive. In this way a single pulse has been transmitted to device 40 and any transient opening of switch 23 between times t_1 and t_2 does not result in multiple pulses at terminal 22.

The opening of switch 23 at time t_4 starts to release relay 15. At t_5, relay 15 releases and capacitor 16 charges to the voltage of positive source 10 via the path including resistor 12. During this relatively short charging interval, a positive voltage may appear at terminal 22 (waveform 110), because of the impedance of series connected resistor 18 and relay 15. This is due to the charging current of capacitor 16 which flows through resistor 18 and relay 15. Since switch 23 is open and diode 39 is arranged to pass only negative pulses, the positive waveforms appearing at terminal 22 do not affect device 40.

As indicated in waveform 115, device 40 may be made available at any time between t_5 and t_7. Because capacitor 16 is disconnected from transistor 30 by normally open relay contact 15*b*, such signals do not discharge capacitor 16. At time t_6, switch 23 is closed so that relay 15 pulls in at time t_7. Because of the delay in the operation of the relay, the signal from flip-flop 55 occurring between t_6 and t_7 is ineffective to discharge capacitor 16. At t_7 contacts 15*a* are opened and contacts 15*b* are closed. This permits capacitor 16 to be discharged on the occurrence of the next signal from flip-flop 55 at t_8. A negative pulse is then transmitted to device 40 in the aforementioned manner between t_8 and t_9. The subsequent pulse from flip-flop 55 occurring between t_9 and t_{10} does not produce a negative pulse at terminal 22 because relay 15 is still pulled in until t_{10}. The enabling pulse occurring at t_{10} on waveform 115 cannot affect capacitor 16 during its recharge through resistor 12 if switch 23 is again closed just after time t_{10}. This is so because the pull-in delay of relay 15 does not permit contacts 15*b* to close until the delay period has been completed.

Although my invention has been described with reference to a particular embodiment, it is to be understood that the arrangements disclosed are merely illustrative of the principles of my invention. Numerous modifications and other arrangements may be devised without departing from the spirit and scope of my invention.

I claim:

1. A pulse generating circuit for applying a pulse to a device comprising capacitor means having first and second terminals, a charging path, a discharge path including first switching means, normally closed switching means connected between said charging path and said capacitor means first terminal, normally open switching means connected between said discharge path and said capacitor means first terminal, and second means responsive to a first signal for opening said normally closed switching means and for closing said normally open switching means after a predetermined time delay, said capacitor means second terminal being connected to said second means, and means for applying a second signal from said device to said first switching means to complete said discharge path after said time delay.

2. A pulse generating circuit according to claim 1 wherein said discharge path switching means comprises a transistor having a base, an emitter and a collector, said emitter being connected to a reference potential, said collector being connected to said normally open switching means and said base being connected to said second signal applying means.

3. A pulse generating circuit according to claim 2 wherein said discharge path comprises diode coupling means having one terminal connected to said device, and said first signal applying means comprises a switch connected between said capacitor second terminal and the other terminal of said diode coupling means.

4. A pulse generating circuit for applying a pulse to a device comprising capacitor means having first and second terminals, a charging path, a discharge path including first switching means, relay means having a normally closed contact pair connected between said charging path and said capacitor means first terminal, a normally open contact pair connected between said discharge path and said capacitor means first terminal, said relay means having a third terminal and being operative in response to a first signal being applied to said third terminal to disconnect said normally closed contact pair and to connect said normally open contact pair after a predetermined time delay, said capacitor means second terminal being connected to said third terminal, and means for applying a second signal from said device to said first switching means to complete said discharge path after said time delay.

5. A circuit for generating and applying a single pulse to a device comprising a capacitor having first and second terminals, means for charging said capacitor, means for discharging said capacitor including switching means, a switch connected to said second terminal, relay means responsive to the closing of said switch for transferring said first terminal from said charging means to said discharging means after a predetermined time interval, and means for applying a signal from said device to said switching means to discharge said capacitor whereby a single pulse is applied to said device upon the application of said signal after said time interval.

6. A circuit for generating and applying a single pulse to a device according to claim 5 wherein said device signal applying means comprises means responsive to the discharge of said capacitor for terminating the signal from said device whereby the duration of said single pulse is controlled.

7. A circuit for generating and applying a single pulse to an output lead comprising a voltage source, a capacitor having

first and second terminals, a relay, a first path including a manual switch connecting said relay to said voltage source, a second path including normally closed contacts of said relay connecting said voltage source to said capacitor first terminal, diode means connecting the output lead to said switch in said first path, transistor switching means including a control electrode, means including normally open contacts of said relay connected between said capacitor first terminal and said transistor switching means for discharging said capacitor through said transistor switching means and said switch in said first path, and means for enabling said transistor switching means to complete said discharge path, said enabling means including means for applying a signal to said control electrode.