

(19) World Intellectual Property Organization  
International Bureau(43) International Publication Date  
19 March 2009 (19.03.2009)

PCT

(10) International Publication Number  
WO 2009/035953 A1(51) International Patent Classification:  
*H02J 7/00* (2006.01)      *G03B 15/05* (2006.01)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BI, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(21) International Application Number:  
PCT/US2008/075643(22) International Filing Date:  
8 September 2008 (08.09.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
60/971,184      10 September 2007 (10.09.2007)      US  
12/203,357      3 September 2008 (03.09.2008)      US(71) Applicant (for all designated States except US): **MAXIM INTEGRATED PRODUCTS, INC.** [US/US]; 120 San Gabriel Drive, Sunnyvale, CA 94086 (US).

(72) Inventor; and

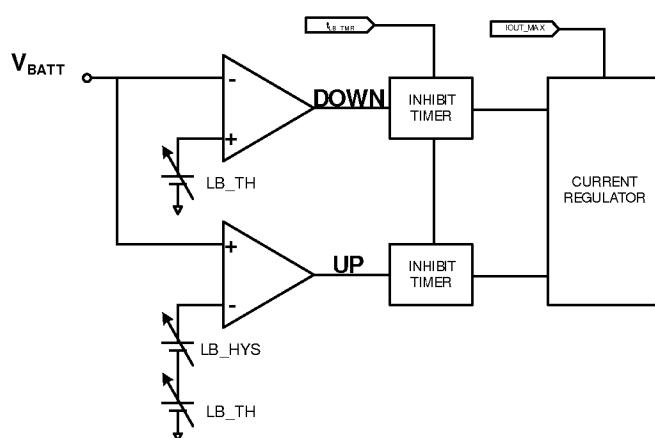
(75) Inventor/Applicant (for US only): **VOIGT, Martin, Palle** [DK/DK]; Molleskoven 36, DK-09260 Gistrup (DK).(74) Agents: **VINCENT, Lester, J.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, CA 94085-4040 (US).

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(54) Title: ADAPTIVE CURRENT LIMITING FOR ANY POWER SOURCE WITH OUTPUT EQUIVALENT SERIES RESISTANCE



(57) Abstract: Adaptive current limiting for any power source to limit power drain of one load on the power source to maintain a minimum power source voltage for proper operation of other loads on the power source. For battery applications, such as for flash systems, the invention allows the maximum output current of a boost converter to be utilized without having to calculate the system equivalent series resistance first. The invention also adjusts the current load up or down during a high load event to compensate for changes in other loads. The changes in current load are made in increments, with a hysteresis region avoiding constant up and down incrementing.

Fig. 6

**ADAPTIVE CURRENT LIMITING  
FOR ANY POWER SOURCE  
WITH OUTPUT EQUIVALENT SERIES RESISTANCE**

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application No. 60/971,184 filed September 10, 2007.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of battery load management in battery powered systems.

2. Prior Art

In various battery powered devices, there are a number of subsystems that need power. Typically at least one of the subsystems can operate at a reduced power if necessary. Such devices include devices with a camera flash, using a Xenon or LED Flash element, including cell phones, and TDMA transmission systems, where a capacitor is charged to provide power amplifier power during the TDMA transmission burst.

Taking devices with a camera flash, it is desirable to charge the flash capacitor as quickly as possible. However during high load currents, the system voltage will momentarily drop due to the internal ESR (equivalent series resistance) of the battery, together with any serial impedance between the battery and the load. For equipment requiring a minimum voltage for stable operation, the ESR of the system (battery plus serial impedance) needs to be calculated in order to estimate the maximum current that can be drawn from the battery without causing system voltage drop below the threshold for stable operation.

If the above is not done, then two scenarios are possible:

1. The system cut-off voltage, a pre-determined voltage at which the system ceases operation and powers down, will have to be set artificially high, to provide sufficient margin above the point at which the battery no longer reliably operates. The result is reduced operating time.

2. In a cell phone, high current peaks cause erratic behavior, or possibly even phone shut-off, even though the battery has plenty of remaining capacity.

For the foregoing reasons, it is desirable to limit the battery current drain of flash capacitor charging systems, when necessary, to below the nominal design value to maintain the required battery voltage for operation of other subsystems, thereby extending the useful battery life, or time between charges for rechargeable batteries.

In the prior art, additional hardware and software were added. The hardware added is a high precision high speed ADC. During the initial loading of the system, the voltage drop of the battery is measured with the ADC, and using software the battery ESR is calculated, from which the maximum load that the battery is able to support is determined.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates system voltage drop due to System ESR (equivalent series resistance) of the battery and line impedances.

Figure 2 illustrates the use of an ESR calculation to insure minimum system voltage at the end of FLASH/MOVIE event normal case.

Figure 3 illustrates the use of an ESR calculation at the beginning of an FLASH/MOVIE event to insure minimum system voltage at the end of FLASH/MOVIE event, with additional load event during FLASH/MOVE event.

Figure 4 illustrates the use of an ESR calculation to insure minimum system voltage at the end of FLASH/MOVIE event with load release during FLASH/MOVIE event.

Figure 5 illustrates the use of a flash driver with MAXFLASH adjusting FLASH current in a battery operated system having an optional buck/boost switching regulator.

Figure 6 is a block diagram illustrating a preferred implementation of the MAXFLASH function.

Figure 7 illustrates the MAXFLASH function operation with increasing system loads during the FLASH/MOVIE event.

Figure 8 illustrates the MAXFLASH function operation with decreasing system loads during the FLASH/MOVIE event.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

For battery applications, the invention allows the maximum output current of a boost converter to be utilized without having to first calculate the system equivalent series resistance (ESR). As mentioned before, this is useful in the applications such as:

1. A camera flash, using a Xenon or an LED Flash element.
2. TDMA (Time Division Multiple Access) transmission systems, where a capacitor is charged to provide power amplifier power during the TDMA transmission burst.

An exemplary method, referred to herein as MAXFLASH, eliminates the need for measuring battery ESR during FLASH/MOVIE events in battery powered equipment.

Figure 1 shows the voltage drop due to system ESR. For applications like a camera flash or a movie light (also

referred to as torch light), the system ESR should be measured in order to calculate the maximum current that can be consumed by the flash in order to ensure that at the end of the flash, the system voltage has not dropped below the minimum required system voltage for the remaining system (cut-off voltage).

Battery cell ESR depends on battery chemistry, load current, temperature, and age of the cell. For these reasons, ESR must be calculated on a real-time basis in order to get the most accurate determination. In most systems, the camera flash is triggered by the camera module itself. Therefore the battery ESR has to be measured in real time during the beginning of the flash event. Figure 2 illustrates the use of a ESR calculation to insure minimum system voltage at the end of FLASH/MOVIE event normal case.

Since most systems contain many complex functions that operate independent of each other, the load current might change during the FLASH/MOVIE duration. If other loads within the system start drawing significantly more current during the FLASH/MOVE duration, this can cause the system voltage to drop below the minimum required operation voltage for the system, hence causing spurious events. This is illustrated in Figure 3, which shows the use of an initial ESR calculation to insure minimum system voltage at the end of the FLASH/MOVIE event, with additional load events during the FLASH/MOVE event.

On the other hand, if an application is going from a high current mode to a lower current mode during the FLASH/MOVIE event, the battery voltage at the end of the FLASH/MOVE duration will be above the minimum battery voltage. This means that the actual FLASH/MOVIE current could have been set higher for the remaining duration, allowing the highest possible output current to be utilized.

This is illustrated in Figure 4, which shows the use of an initial ESR calculation to insure minimum system voltage at the end of the FLASH/MOVIE event with load release during the FLASH/MOVIE event.

Figure 5 illustrates a system using MAXFLASH for adjusting the FLASH driver current to maintain adequate operating voltages for the rest of the system. Figure 6 shows a block diagram of the MAXFLASH to control the current IOUT\_MAX provided to the charging circuit for the driver output storage capacitor, in this case to power a flash lamp, and Figures 7 and 8 show examples of MAXFLASH operation. To avoid having to measure the ESR of the system and still achieve the goal of ensuring that the system voltage doesn't drop below a predefined threshold, the circuit of Figure 6 operates as follows (see Figures 7 and 8): During a FLASH/MOVIE event the input voltage of the device is monitored using a Kelvin connection to the system rail, referred to as  $V_{SYS}$  or  $V_{BATT}$ . If the input voltage drops below a predefined threshold, referred to as  $V_{LB\_TH}$  as sensed by comparator CP1, this is an indication that the FLASH/MOVIE event is drawing more current than the system can support.

As a reaction to this, the current regulator driving the FLASH/MOVIE will reduce (DOWN) the output current one step (LSB). This will reduce the input current to the current regulator driving the FLASH/MOVIE, hence reducing the total current drawn from the system battery. Since the system current is now reduced, the battery voltage will start to rise due to the internal ESR of the battery cell and remaining system. The current regulator will then delay (INHIBIT TIMER) a user predefined time, referred to as  $t_{LB\_TMR\_F}$ , for falling edge detection (i.e. battery voltage less than  $V_{LB\_TH}$ ), and  $t_{LB\_TMR\_R}$  for raising edge detection (i.e.

battery voltage greater than  $V_{LB\_TH} + V_{LB\_HYS}$ , sensed by comparator CP2).

The battery voltage is then sampled again and compared to  $V_{LB\_TH}$ . If the battery voltage is still below the  $V_{LB\_TH}$  threshold, the current regulator will be caused to reduce output current one unit once again to insure that minimum battery voltage is available for the remaining parts of the system. If the battery voltage rises above the  $V_{LB\_TH}$  threshold plus a user defined hysteresis, referred to as  $V_{LB\_HYS}$ , the Current Regulator will be caused to increase (UP) the output current one unit (LSB), but only if the output current is less than the user defined output current. A DOWN or UP increment in the preferred embodiment resets both inhibit timers to initiate new time delays, though this is not a limitation of the invention.

The delays  $t_{LB\_TMR\_F}$  and  $t_{LB\_TMR\_R}$  may be the same or different time periods, and are typically, though not necessarily, in the range of seconds to milliseconds. These delays may be in hardware or under program control by the system processor. Note from Figures 7 and 8 that the delays are minimum delays before the circuit is responsive to the system voltage again, after which the circuit will immediately respond to a system voltage going below  $V_{LB\_TH}$  threshold or above  $V_{LB\_TH}$  threshold plus  $V_{LB\_HYS}$  hysteresis. Alternatively, the system voltage could be periodically sampled, and current increased or decreased in increments as in the preferred embodiment. Sampling as used herein means responding to the output of the comparators, and not necessarily initially sensing the battery voltage or the output of the comparators. Also, while the preferred embodiment shown in Figure 6, once the time delays are programmed and typically permanently stored, functions without system processor intervention, the sampling and/or

increasing or decreasing the current drain could be done under system processor control, though this generally is undesirable.

The unit reduction and the unit increase in converter output may be the same or different, as desired. If the same however, the increments should have an effect on the battery voltage of less than  $V_{LB\_HYS}$ , as otherwise a voltage decline to  $V_{LB\_TH}$  would cause a battery voltage change to over  $V_{LB\_TH} + V_{LB\_HYS}$ , with the next change bringing the battery voltage back to  $V_{LB\_TH}$ , or lower. Instead, the effect of a unit reduction in the converter output current on battery voltage should be less than  $V_{LB\_HYS}$  and repeated often enough to keep the battery voltage from going below  $V_{LB\_TH}$ . Alternatively, the unit reduction in the converter output current should be more than the unit increase in the converter output current, so that a unit reduction in the converter output current followed by a unit increase in the converter output current will not bring the battery voltage back to where it was before these two changes occurred.

The one LSB-at-a-time up/down adjustment will continue for the entire duration of the FLASH/MOVIE event, ensuring that, by way of example, the FLASH/MOVIE output current is always maximized for the specific operating conditions, regardless of the changing loads on the battery during the event.

Thus while certain preferred embodiments of the present invention have been disclosed and described herein for purposes of illustration and not for purposes of limitation, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A method of maintaining a minimum system voltage in a battery operated system having a component preferably operated at a first current, but operable with currents less than the first current, comprising:
  - 1) sensing system voltage; and,
  - 2) when the system voltage falls below a predefined threshold, incrementally decreasing the current provided to the component; and
  - 3) when the system voltage goes above a predefined threshold plus a hysteresis current, incrementally increasing the current provided to the component; and,
  - 4) if the system voltage falls below a predefined threshold after a first time period after an incremental decrease in current, again incrementally decreasing the current provided to the component; and,
  - 5) if the system voltage goes above a predefined threshold plus a hysteresis voltage increment after a second time period after an incremental increase in current, again incrementally increasing the current provided to the component;
  - 6) repeating 4) and 5) multiple times.
2. The method of claim 1 wherein the first and second time periods are unequal time periods.
3. The method of claim 1 wherein the first and second time periods are equal time periods.
4. The method of claim 1 wherein the incremental decrease in current in 2) is equal to the incremental increase in current in 3).

5. The method of claim 1 wherein the incremental decrease in current in 2) is not equal to the incremental increase in current in 3).

6. The method of claim 1 wherein on each subsequent repeat of a) through c), the current is incrementally decreased when the system voltage falls below a predefined threshold at any time after the first time period after an incremental decrease or increase in current, or the current is incrementally increased when the system voltage is above a predefined threshold plus a hysteresis current at any time after the second time period after an incremental increase in current.

7. A method of maintaining a minimum system voltage in a battery operated system having a component preferably operated at a first current, but operable with currents less than the first current, comprising:

- a) sensing system voltage; and,
  - 1) when the system voltage falls below a predefined threshold, incrementally decreasing the current provided to the component; and
  - 2) when the system voltage goes above a predefined threshold plus a hysteresis current, incrementally increasing the current provided to the component; and,
- b) after an incremental decrease or an incremental decrease in current;
  - 1) if the system voltage falls below a predefined threshold after a first time period after an incremental decrease or an incremental increase in current, incrementally decreasing the current provided to the component; and,
  - 2) if the system voltage goes above a predefined threshold plus a hysteresis voltage component after a second time period after an incremental decrease or an

incremental increase in current, incrementally increasing the current provided to the component;

c) repeating b) multiple times.

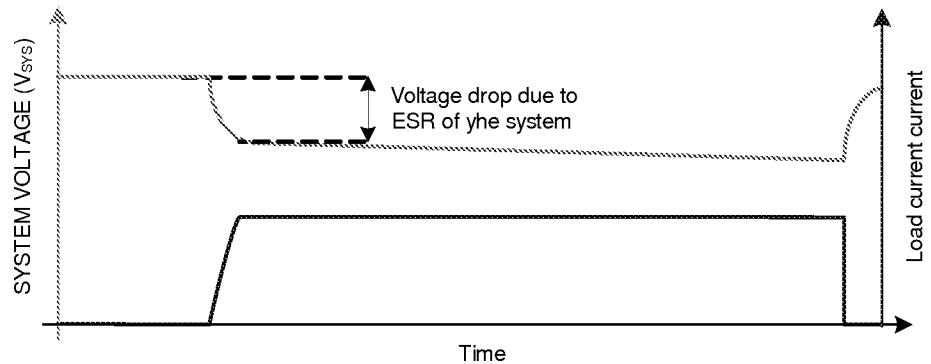
8. The method of claim 7 wherein the first and second time periods are unequal time periods.

9. The method of claim 7 wherein the first and second time periods are equal time periods.

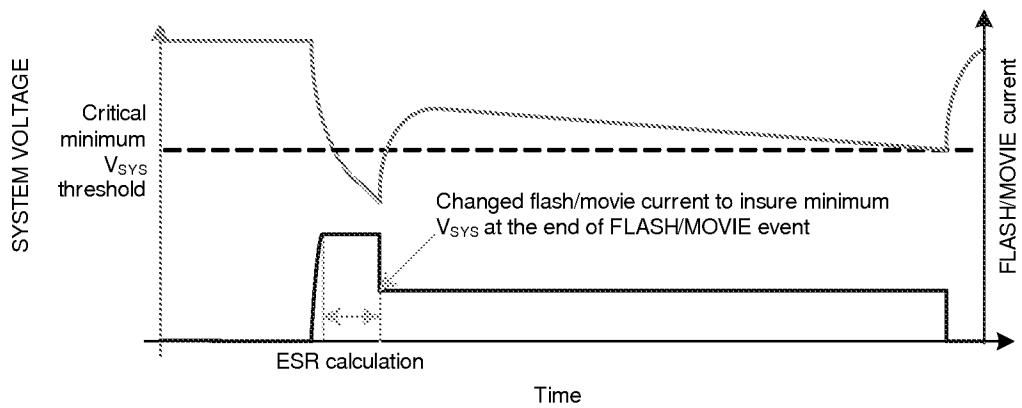
10. The method of claim 7 wherein the incremental decrease in current in b), 1) is equal to the incremental decrease in current in b), 2).

11. The method of claim 7 wherein the incremental decrease in current in b), 1) is not equal to the incremental decrease in current in b), 2).

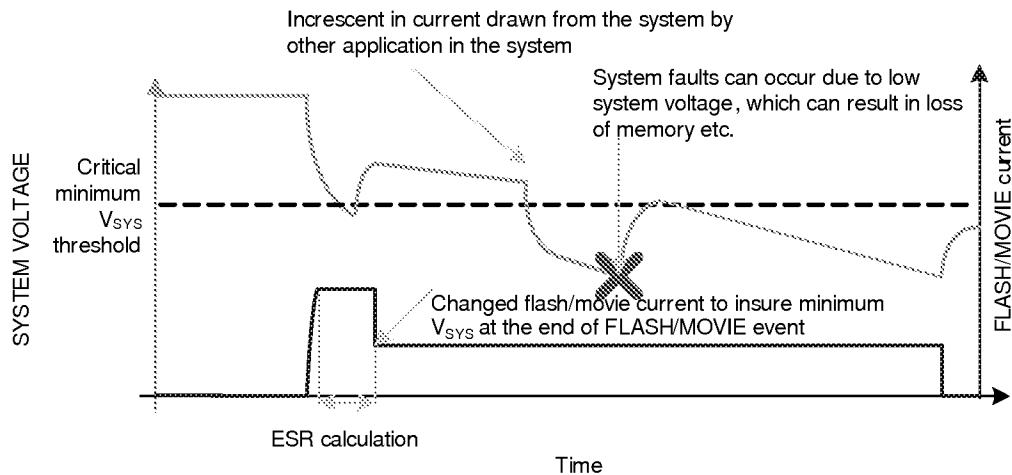
12. The method of claim 7 wherein on each subsequent repeat of b), the current is incrementally decreased when the system voltage falls below a predefined threshold at any time after the first time period, or the current is incrementally increased when the system voltage is above a predefined threshold plus a hysteresis current at any time after the second time period.



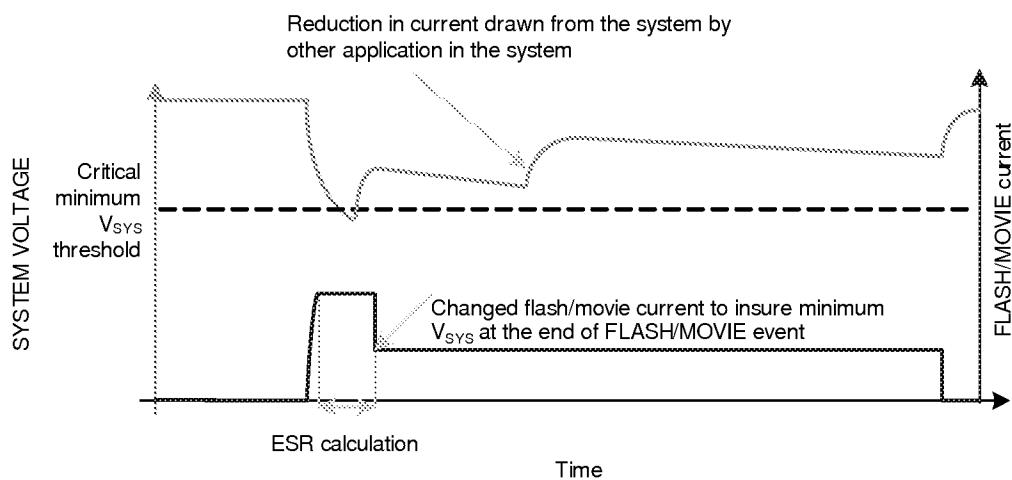
**Fig. 1**



**Fig. 2**



**Fig. 3**



**Fig. 4**

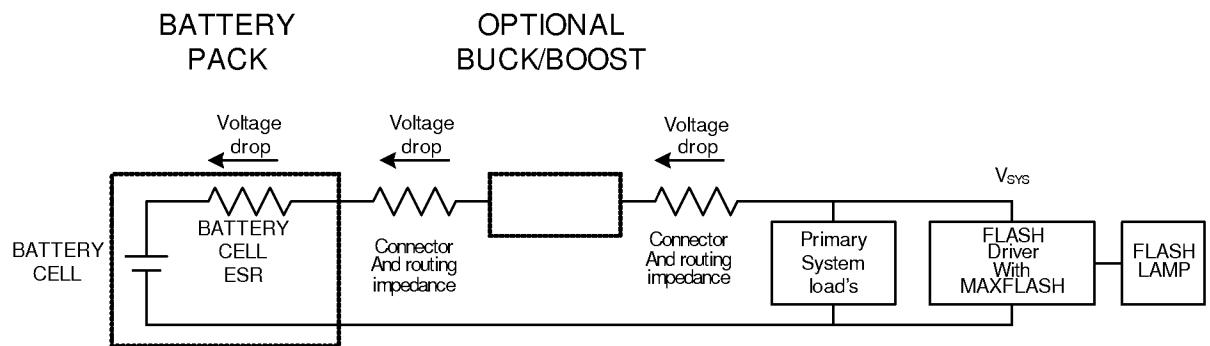


Fig. 5

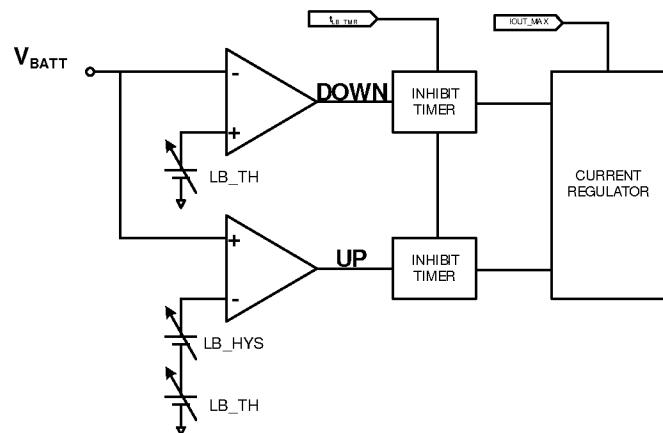


Fig. 6

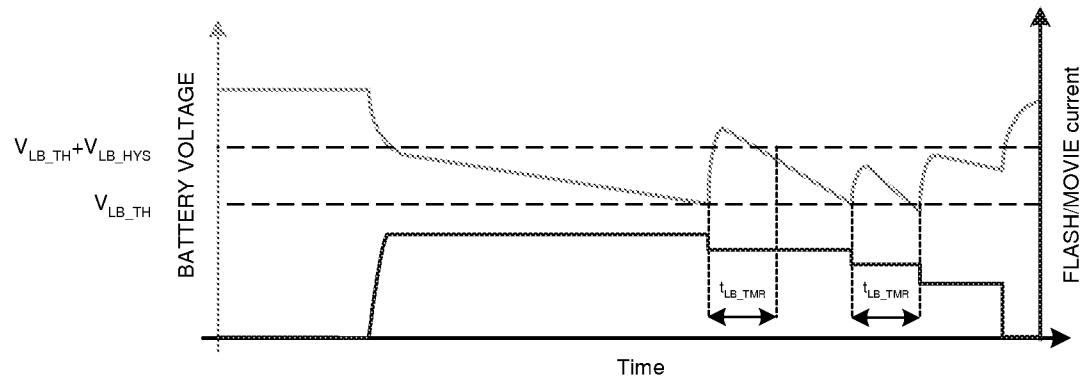


Fig. 7

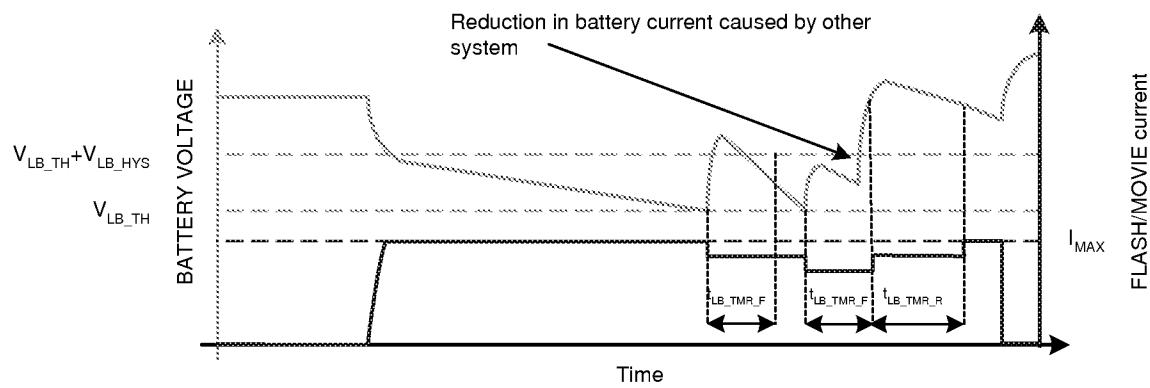


Fig. 8

# INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2008/075643

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H02J7/00 G03B15/05

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
H02J G03B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/269082 A1 (DANIELSEN FINN [DK] ET AL) 30 November 2006 (2006-11-30) the whole document -----	1
A	US 2006/233405 A1 (BROOKS MARK [DK] ET AL) 19 October 2006 (2006-10-19) the whole document -----	1
A	US 2006/050910 A1 (DANIELSEN FINN [DK]) 9 March 2006 (2006-03-09) the whole document -----	1
A	JP 2003 348197 A (TOKYO SHIBAURA ELECTRIC CO) 5 December 2003 (2003-12-05) abstract ----- -/-	1

Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents :

- \*A\* document defining the general state of the art which is not considered to be of particular relevance
- \*E\* earlier document but published on or after the international filing date
- \*L\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

\*T\* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

\*X\* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

\*Y\* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

\*&\* document member of the same patent family

Date of the actual completion of the international search

30 January 2009

Date of mailing of the international search report

11/02/2009

Name and mailing address of the ISA/  
European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

Lorenzo Feijoo, S

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2008/075643

## C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2004 014329 A (CANON KK) 15 January 2004 (2004-01-15) abstract -----	1
A	US 6 188 142 B1 (LOTH-KRAUSSER HARTMUT [DE]) 13 February 2001 (2001-02-13) the whole document -----	1
A	US 6 922 151 B2 (KAWAKAMI CHIKUNI [JP]) 26 July 2005 (2005-07-26) the whole document -----	1

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/US2008/075643
---

Patent document cited in search report	Publication date	Patent family member(s)			Publication date
US 2006269082	A1 30-11-2006	AT 413082 T CN 1870837 A EP 1727394 A1			15-11-2008 29-11-2006 29-11-2006
US 2006233405	A1 19-10-2006	NONE			
US 2006050910	A1 09-03-2006	AT 330233 T AU 2003266933 A1 DE 60306181 T2 WO 2004034073 A1 EP 1552319 A1			15-07-2006 04-05-2004 24-05-2007 22-04-2004 13-07-2005
JP 2003348197	A 05-12-2003	NONE			
JP 2004014329	A 15-01-2004	JP 4136471 B2			20-08-2008
US 6188142	B1 13-02-2001	AT 208968 T CN 1230303 A DE 19637574 A1 WO 9811644 A1 EP 0925626 A1 ES 2167788 T3 HK 1021263 A1 JP 3789488 B2 JP 2001500355 T			15-11-2001 29-09-1999 26-03-1998 19-03-1998 30-06-1999 16-05-2002 11-09-2003 21-06-2006 09-01-2001
US 6922151	B2 26-07-2005	JP 2004045170 A US 2004008117 A1			12-02-2004 15-01-2004