

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
29 January 2009 (29.01.2009)

PCT

(10) International Publication Number  
**WO 2009/013531 A3**

(51) International Patent Classification:  
H01L 21/266 (2006.01) H01L 21/77 (2006.01)

(21) International Application Number:  
PCT/GB2008/050598

(22) International Filing Date: 18 July 2008 (18.07.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
0714071.8 20 July 2007 (20.07.2007) GB

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(81) Designated States (unless otherwise indicated, for every  
kind of national protection available): AE, AG, AL, AM,  
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA,  
CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE,  
EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID,  
IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK,  
LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW,  
MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT,  
RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ,  
TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM,  
ZW.

(84) Designated States (unless otherwise indicated, for every  
kind of regional protection available): ARIPO (BW, GH,  
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,  
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),  
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,  
FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL,  
NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG,  
CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

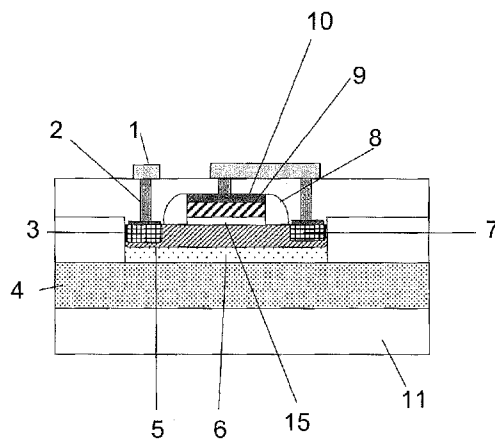
Published:

- with international search report
- before the expiration of the time limit for amending the  
claims and to be republished in the event of receipt of  
amendments

(88) Date of publication of the international search report:  
19 March 2009

(54) Title: A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE, AND A SEMICONDUCTOR DEVICE

Fig 6(a) Polysilicon resistor



(57) Abstract: A method of manufacturing a semiconductor device comprises the steps of, in sequence: depositing a first silicon layer; patterning the first silicon layer to obtain a first silicon region; implanting a first dopant into a first part of the first silicon region, the first part of the first silicon region defined using a first mask; depositing a second silicon layer; patterning the second silicon layer to obtain a second silicon region; and implanting a second dopant into a second part of the first silicon region, the second part of the first silicon region defined by the first mask and the second silicon region. A device comprises a semiconductor layer (6); a first doped region (5) within the semiconductor layer; a second doped region (7) within the first doped region (5); and a silicon layer (9) disposed over a part of the semiconductor layer; wherein the silicon layer is disposed over a part of the first doped region (5) but not over the second doped region (7).

WO 2009/013531 A3

## INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2008/050598

A. CLASSIFICATION OF SUBJECT MATTER  
 INV. H01L21/266 H01L21/77

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

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Y	paragraph [0099] - paragraph [0102]; figures 5, 9-11  paragraph [0132] - paragraph [0142]	6-8, 13-15, 22, 26-28
X	US 5 466 958 A (KAKUMU MASAKAZU [JP]) 14 November 1995 (1995-11-14)	9-12, 16, 19
Y	figures 7-10	8, 22
Y	EP 1 796 161 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 13 June 2007 (2007-06-13)  figures 1G-1I	6, 7, 13-15, 26-28
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Date of the actual completion of the international search

5 January 2009

Date of mailing of the international search report

27/01/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
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Authorized officer

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## INTERNATIONAL SEARCH REPORT

International application No

PCT/GB2008/050598

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	EP 0 683 515 A (SAMSUNG ELECTRONICS CO LTD [KR]) 22 November 1995 (1995-11-22) figures 3-8 -----	1-31
A	US 2005/106898 A1 (TAKAYAMA TORU [JP] ET AL) 19 May 2005 (2005-05-19) abstract -----	1-31
A	US 5 001 076 A (MIKKELSON JAMES M [US]) 19 March 1991 (1991-03-19) the whole document -----	1-31

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No <b>PCT/GB2008/050598</b>
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