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(54) **Title:** N-PHASE POLARITY OUTPUT PIN MODE MULTIPLEXER

(57) **Abstract:** System, methods and apparatus are described that facilitate transmission of data, particularly between two devices within an electronic apparatus. Data is selectively transmitted as N-phase polarity encoded symbols or as packets on differentially driven connectors. A desired operational mode for communicating between the two devices is determined, an encoder is selected to drive a plurality of connectors communicatively coupling the two devices, and a plurality of drivers is configured to receive encoded data from the encoder and drive the plurality of connectors. Switches may couple outputs of the selected encoder to the plurality of drivers. One or more outputs of another encoder may be caused or forced to enter a high impedance mode.



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N-PHASE POLARITY OUTPUT PIN MODE MULTIPLEXER

CROSS-REFERENCE TO RELATED APPLICATIONS

- [0001]** The present Application for Patent claims priority to Provisional Application No. 61/666,197 entitled “N-Phase Polarity Output Pin Mode Multiplexer” filed June 29, 2012, which is assigned to the assignee hereof, which application is hereby expressly incorporated by reference herein.

BACKGROUND

Field

- [0002]** At least one aspect generally relates to high-speed data communications interfaces, and more particularly, multiplexing the input and output pins of an application processor.

Background

- [0003]** Manufacturers of mobile devices, such as cellular phones, may obtain components of the mobile devices from various sources, including different manufacturers. For example, the application processor in a cellular phone may be obtained from a first manufacturer, while the display for the cellular phone may be obtained from a second manufacturer. Moreover, multiple standards are defined for interconnecting certain components of the mobile devices. For example, there are multiple types of interface defined for communications between an application processor and a display within mobile device. Some displays provide an interface that conforms to the Display System Interface (DSI) standard specified by the Mobile Industry Processor Interface Alliance (MIPI). Other displays may utilize other kinds of physical interfaces, which may be more efficient than the conventional DSI. It would be economical for the same application processor to be configured for use with more than one display interface.

SUMMARY

- [0004] Embodiments disclosed herein provide systems, methods and apparatus that enable an application processor to communicate with a display using any of a plurality of interface standards. According to certain aspects described herein, two or more Integrated Circuit (IC) devices may be collocated in an electronic apparatus and communicatively coupled through one or more data links that can be configured as desired for compatibility with one of a plurality of interface standards.
- [0005] In an aspect of the disclosure, a data transfer method comprises determining a type of physical interface to be used for communicating between two devices in a wireless mobile terminal, selecting an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices, and configuring a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices. The type of physical interface may be one of a plurality of types of physical interface supported by at least one of the two devices.
- [0006] In an aspect of the disclosure, the data transfer method comprises controlling a plurality of switches to couple outputs of the selected encoder to the plurality of drivers.
- [0007] In an aspect of the disclosure, the plurality of connectors comprises at least some bidirectional connectors. In an aspect of the disclosure, the plurality of connectors comprises at least some unidirectional connectors. In an aspect of the disclosure, the plurality of connectors comprises a combination of bidirectional and unidirectional connectors.
- [0008] In an aspect of the disclosure, the encoder may provide the encoded data in differentially encoded signals. The plurality of drivers may be configured to receive the encoded data by causing one or more outputs of another encoder to enter a high impedance mode. The other encoder may be a different type of encoder and may comprise an *N*-phase encoder, for example.
- [0009] In an aspect of the disclosure, the encoder provides encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the connectors, a polarity of a second pair of connectors, and a selection of at least one

undriven connector. The first pair of the connectors may comprise the same wires as the second pair of connectors. One or more outputs of a differential encoder may be caused to enter a high impedance mode. In one example, the encoded data may include video data related to a camera or a display controlled by one of the two devices.

[0010] In an aspect of the disclosure, an apparatus comprises a plurality of connectors communicatively coupling a first IC device with a second IC device, means for generating encoded data consistent with the type of physical interface to be used for communicating between the two devices, and means for configuring a plurality of drivers to receive the encoded data from one of the at least two encoders and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices. The means for generating encoded data may include at least two encoders that are configured to encode data in different manners. The plurality of connectors may comprise wires, traces or other electrically conductive connectors.

[0011] In an aspect of the disclosure, an apparatus comprises a plurality of connectors communicatively coupling a first device with a second device in a wireless mobile terminal, and a processing system configured to determine an operational mode for communicating between the first device and the second device, select an encoder to drive the plurality of connectors, and configure a plurality of drivers to receive encoded data from the encoder. The plurality of drivers may drive the plurality of connectors.

In an aspect of the disclosure, a processor-readable storage medium has one or more instructions that, when executed by at least one processing circuit, cause the at least one processing circuit to determine a type of physical interface to be used for communicating between two devices in a wireless mobile terminal, select an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices, and configure a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices. The

type of physical interface may be one of a plurality of types of physical interface supported by at least one of the two devices.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0012] FIG. 1 depicts an apparatus employing a data link between IC devices that selectively operates according to one of plurality of available standards.
- [0013] FIG. 2 illustrates a system architecture for an apparatus employing a data link between IC devices that selectively operates according to one of plurality of available standards.
- [0014] FIG. 3 illustrates an example of a data link using differential signaling.
- [0015] FIG. 4 illustrates an example of an *N*-phase polarity data encoder.
- [0016] FIG. 5 illustrates signaling in an example of an *N*-phase polarity encoded interface.
- [0017] FIG. 6 illustrates an example of an *N*-phase polarity decoder.
- [0018] FIG. 7 illustrates a system architecture for an apparatus that may selectively use *N*-phase polarity encoding or differential signaling.
- [0019] FIG. 8 is a flow chart of a method for selective *N*-phase polarity encoding.
- [0020] FIG. 9 is a diagram illustrating an example of a hardware implementation for an apparatus employing *N*-phase polarity data encoding.

DETAILED DESCRIPTION

- [0021] Various aspects are now described with reference to the drawings. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of one or more aspects. It may be evident, however, that such aspect(s) may be practiced without these specific details.
- [0022] As used in this application, the terms “component,” “module,” “system” and the like are intended to include a computer-related entity, such as, but not limited to hardware, firmware, a combination of hardware and software, software, or software in execution. For example, a component may be, but is not limited to being, a process running on a processor, a processor, an object, an executable, a thread of execution, a program and/or a computer. By way of illustration, both an application running on a computing device and the computing device can be a component. One or more components can reside within a process and/or thread of execution and a

component may be localized on one computing device and/or distributed between two or more computing devices. In addition, these components can execute from various computer readable media having various data structures stored thereon. The components may communicate by way of local and/or remote processes such as in accordance with a signal having one or more data packets, such as data from one component interacting with another component in a local system, distributed system, and/or across a network such as the Internet with other systems by way of the signal.

[0023] Moreover, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or.” That is, unless specified otherwise, or clear from the context, the phrase “X employs A or B” is intended to mean any of the natural inclusive permutations. That is, the phrase “X employs A or B” is satisfied by any of the following instances: X employs A; X employs B; or X employs both A and B. In addition, the articles “a” and “an” as used in this application and the appended claims should generally be construed to mean “one or more” unless specified otherwise or clear from the context to be directed to a singular form.

[0024] Certain embodiments of the invention may be applicable to communications links deployed between electronic components that may include subcomponents of a device, such as a telephone, a mobile computing device, an appliance, an automobile electronics, an avionics system, etc. FIG. 1 depicts an example of an apparatus 100 employing a data link between IC devices that selectively operates according to one of plurality of available standards. The apparatus 100 may comprise a wireless communication device that communicates wirelessly with a radio access network (RAN), a core access network, the Internet and/or another network. The apparatus 100 may include a communications transceiver 106 operably coupled to a processing circuit 102. The processing circuit 102 may comprise one or more IC devices, such as an application-specific IC (ASIC) 108. The ASIC 108 may include one or more processing devices, sequencers, logic circuits, and so on. The processing circuit 102 may include and/or be coupled to processor readable storage such as a memory device 112 that may maintain instructions and data the may be executed and otherwise used by the processing circuit 102. The processing circuit 102 may be controlled by one or more of an operating system and an application programming interface (API) 110 layer that supports and enables execution of software modules residing in the memory device 112. The memory device 112 may

comprise read-only memory (ROM) and/or random-access memory (RAM), electrically-erasable programmable read only memory (EEPROM), a flash memory device, or any memory device that can be used in processing systems and computing platforms. Processing circuit 102 may include and/or access a local database 114 that can maintain operational parameters and other information used to configure and operate the apparatus 100. The local database 114 may be implemented using one or more of a database module or server, flash memory, magnetic media, EEPROM, optical media, tape, soft or hard disk, or the like. The processing circuit may also be operably coupled to external devices such as an antenna 122, a display 124, operator controls, such as a button 128 and a keypad 126, among other components.

[0025] FIG. 2 is a block schematic 200 illustrating certain aspects of an apparatus such as a wireless mobile device, a mobile telephone, a mobile computing system, a wireless telephone, a notebook computer, a tablet computing device, a media player, a gaming device, or the like. Apparatus 200 may comprise a plurality of IC devices 202 and 230 that exchange data and control information through a communications link 220. The communications link 220 may be used to connect the IC devices 202 and 222, which may be located in close proximity to one another or physically located in different parts of the apparatus 200. In one example, the communications link 220 may be provided on a chip carrier, substrate or circuit board that carries the IC devices 202 and 230. In another example, a first IC device 202 may be located in a keypad section of a flip-phone while a second IC device 230 may be located in a display section of the flip-phone. In another example, a portion of the communications link 220 may comprise a cable or optical connection.

[0026] The communications link 220 may comprise multiple channels 222, 224 and 226. One or more channel 226 may be bidirectional, and may operate in half-duplex and/or full-duplex modes. One or more channel 222 and 224 may be unidirectional. The communications link 220 may be asymmetrical, providing higher bandwidth in one direction. In one example described herein, a first communications channel 222 may be referred to as a forward link 222 while a second communications channel 224 may be referred to as a reverse link 224. The first IC device 202 may be designated as a host system or transmitter, while the second IC device 230 may be designated as a client system or receiver, even if both IC devices 202 and 230 are

configured to transmit and receive on the communications link 222. In one example, the forward link 222 may operate at a higher data rate when communicating data from a first IC device 202 to a second IC device 230, while the reverse link 224 may operate at a lower data rate when communicating data from the second IC device 230 to the first IC device 202.

[0027] The IC devices 202 and 230 may each comprise a processor or other processing and/or computing circuit or device 206, 236. In one example, the first IC device 202 may perform core functions of the apparatus 200, including maintaining wireless communications through a wireless transceiver 204 and an antenna 214, while the second IC device 230 may support a user interface that manages or operates a display controller 232, and may control operations of a camera or video input device using a camera controller 234. Other features supported by one or more of the IC devices 202 and 230 may include a keyboard, a voice-recognition component, and other input or output devices. The display controller 232 may comprise circuits and software drivers that support a display such as a liquid crystal display (LCD) panel, a touch-screen display, an indicator and so on. The storage media 208 and 238 may comprise transitory and/or non-transitory storage devices adapted to maintain instructions and data used by the respective processors 206 and 236, and/or other components of the IC devices 202 and 230. Communication between each processor 206, 236 and its corresponding storage media 208 and 238 and other modules and circuits may be facilitated by one or more bus 212 and 242, respectively.

[0028] The reverse link 224 may be operated in the same manner as the forward link 222, and the forward link 222 and the reverse link 224 may be capable of transmitting at comparable speeds or at different speeds, where speed may be expressed as data transfer rate and/or clocking rates. The forward and reverse data rates may be substantially the same or may differ by orders of magnitude, depending on the application. In some applications a single bidirectional link 226 may support communications between the first IC device 202 and the second IC device 230. The forward link 222 and/or the reverse link 224 may be configurable to operate in a bidirectional mode when, for example, the forward and reverse links 222 and 224 share the same physical connections and operate in a half-duplex manner.

[0029] In one example, the communications link 220 may be operated to communicate control, command and other information between the first IC device 202 and the

second IC device 230 in accordance with an industry or other standard. Industry standards may be application specific. For example, the MIPI standard defines physical layer interfaces including a synchronous interface specification (D-PHY) between an application processor IC device 202 and an IC device 230 that supports the camera or display in a mobile device. The D-PHY specification governs the operational characteristics of products that comply with MIPI specifications for mobile devices. A D-PHY interface may support data transfers using a flexible, low-cost, high-speed serial interface that interconnects IC devices 202, 230 and/or other components within a mobile device. These interfaces may comprise complimentary metal-oxide-semiconductor (CMOS) compatible parallel busses providing relatively low bit rates with slow edges to avoid electromagnetic interference (EMI) issues.

[0030] FIG. 3 is a schematic diagram illustrating a differential signaling example of an implementation of the communication link 220 depicted in FIG. 2. Differential signaling typically involves transmitting information electrically using two complementary signals sent on a pair of wires 310a, 310b or 310c, which may be referred to as a differential pair. The use of differential pairs can significantly reduce EMI by canceling the effect of common-mode interference that affects both wires in a differential pair. On the forward link 222, a pair of wires 310a may be driven by a host differential amplifier 304. The differential amplifier 304 receives an input data stream 302 and generates positive and negative versions of the input 302, which are then provided to the pair of wires 310a. The differential receiver 306 on the client side generates an output data stream 308 by performing a comparison of the signals carried on the pair of wires 310a.

[0031] On the reverse link 224, one or more pairs of wires 310c may be driven by a client-side differential amplifier 326. The differential amplifier 326 receives an input data stream 328 and generates positive and negative versions of the input 328, which are provided to the pair of wires 310c. The differential receiver 324 on the host generates an output data stream 322 by performing a comparison of the signals carried on the pair of wires 310c.

[0032] In a bidirectional link 226, the host and client may be configured for half-duplex mode and may transmit and receive data on the same wire pair 310b. A bidirectional bus may alternatively or additionally be operated in full-duplex mode using combinations of the forward and reverse link drivers 304, 326 to drive multiple wire

pairs 310a, 310c. In the half-duplex bidirectional implementation depicted for the bidirectional link 226, the transmitters 314 and 314' may be prevented from driving the wire pair 310b simultaneously using, for example, an output enable (OE) control 320a, 320c (respectively) to force the transmitters 314 and 314' into a high impedance state. The differential receiver 316' may be prevented from driving the input/output 312 while the differential transmitter 314 is active, typically using an OE control 320b to force the differential receiver 316' into a high impedance state. The differential receiver 316 may be prevented from driving the input/output 318 while the differential transmitter 314' is active, typically using an OE control 320d to force the differential receiver 316 into a high impedance state. In some instances, the outputs of the differential transmitters 314 and 314' and the differential receivers 316 and 316' may be in a high-impedance state when the interface is not active. Accordingly, the OE controls 320a, 320c, 320b and 320d of the differential transmitters 314, 314', and the differential receivers 316 and 316' may be operated independently of one another.

[0033] Each of the differential amplifiers 304, 314, 314' and 326 may comprise a pair of amplifiers, one receiving at one input the inverse of the input of the other amplifier. The differential amplifiers 304, 314, 314' and 326 may each receive a single input and comprise an internal inverter that generates an inverse input for use with a pair of amplifiers. The differential amplifiers 304, 314, 314' and 326 may also be constructed using two separately controlled amplifiers, such that their respective outputs can be placed in high impedance mode independently of one another.

[0034] According to certain aspects disclosed herein, systems and apparatus may employ multi-phase data encoding and decoding interface methods for communicating between IC devices 202 and 230. A multi-phase encoder may drive a plurality of conductors (i.e., M conductors). The M conductors typically comprise three or more conductors, and each conductor may be referred to as a wire, although the M conductors may comprise conductive traces on a circuit board or within a conductive layer of a semiconductor IC device. The M conductors may be divided into a plurality of transmission groups, each group encoding a portion of a block of data to be transmitted. An N -phase encoding scheme is defined in which bits of data are encoded in phase transitions and polarity changes on the M conductors. In one example, an N -phase encoding scheme for a three-wire system may comprise three

phase states and two polarities, providing 6 states and 5 possible transitions from each state. Deterministic voltage and/or current changes may be detected and decoded to extract data from the M conductors. Decoding does not rely on independent conductors or pairs of conductors and timing information can be derived directly from phase and/or polarity transitions in the M conductors. N -Phase polarity data transfer can be applied to any physical signaling interface, including electrical, optical and radio frequency (RF) interfaces, for example.

[0035] FIG. 4 is a schematic diagram illustrating the use of N -phase polarity encoding to implement certain aspects of the communication link 220 depicted in FIG. 2. The illustrated example may relate to a three-wire link or to a portion of a link that has more than three wires. The communication link 220 may comprise a wired bus having a plurality of signal wires, which may be configured to carry N -phase encoded data in a high-speed digital interface, such as a mobile display digital interface (MDDI). One or more of the channels 222, 224 and 226 may use N -phase polarity encoding. The physical layer drivers 210 and 240 may be adapted to encode and decode N -phase polarity encoded data transmitted on link 220. The use of N -phase polarity encoding provides for high speed data transfer and may consume half or less of the power of other interfaces because fewer than N drivers are active in N -phase polarity encoded data links 220 at any time. N -phase polarity encoding devices 210 and/or 240 can encode multiple bits per transition on the communications link 220. In one example, a combination of 3-phase encoding and polarity encoding may be used to support a wide video graphics array (WVGA), 80 frames per second LCD driver IC without a frame buffer, delivering pixel data for display refresh at 810 Mbps over three or more wires.

[0036] In the depicted example 400, an M -wire, N -phase polarity encoding transmitter is configured for $M=3$ and $N=3$. The example of three-wire, three-phase encoding is selected solely for the purpose of simplifying descriptions of certain aspects of this disclosure. The principles and techniques disclosed for three-wire, three-phase encoders can be applied in other configurations of M -wire, N -phase polarity encoders, and may comply or be compatible with other interface standards.

[0037] When N -phase polarity encoding is used, connectors such as signal wires 410a, 410b and 410c on an N -line bus may be undriven, driven positive, or driven negative. An undriven signal wire 410a, 410b or 410c may be in a high-impedance state. An

undriven signal wire 410a, 410b or 410c may be driven or pulled to a voltage level that lies substantially halfway between the positive and negative voltage levels provided on driven signal wires. An undriven signal wire 410a, 410b or 410c may have no current flowing through it. In the example 400, each signal wire 410a, 410b and 410c may be in one of three states (denoted as +1, -1, or 0) using drivers 408. In one example, drivers 408 may comprise unit-level current-mode drivers. In another example, drivers 408 may drive opposite polarity voltages on two signals 410a and 410b while the third signal 410c is at high impedance and/or pulled to ground. For each transmitted symbol interval, at least one signal is in the undriven (0) state, while the number of signals driven positive (+1 state) is equal to the number of signals driven negative (-1 state), such that the sum of current flowing to the receiver is always zero. For each symbol, the state of at least one signal wire 410a, 410b or 410c is changed from the symbol transmitted in the preceding transmission interval.

[0038] In the example, 400, a mapper 402 may receive 16 bit data 418, and the mapper 402 may map the input data 418 to 7 symbols 412 for transmitting sequentially over the signal wires 410a, 410b and 410c. An *M*-wire, *N*-phase encoder 406 configured for three-wire, three-phase encoding receives the 7 symbols 412 produced by the mapper one symbol 414 at a time and computes the state of each signal wire 410a, 410b and 410c for each symbol interval. The 7 symbols 412 may be serialized using parallel-to-serial converters 404, for example. The encoder 406 selects the states of the signal wires 410a, 410b and 410c based on the input symbol 414 and the previous states of signal wires 410a, 410b and 410c.

[0039] The use of *M*-wire, *N*-phase encoding permits a number of bits to be encoded in a plurality of symbols where the bits per symbol is not an integer. In the simple example of a three-wire, three-phase system, there are 3 available combinations of 2 wires, which may be driven simultaneously, and 2 possible combinations of polarity on any pair of wires that is driven simultaneously, yielding 6 possible states. Since each transition occurs from a current state, 5 of the 6 states are available at every transition. The state of at least one wire is typically required to change at each transition. With 5 states, $\log_2(5) \cong 2.32$ bits may be encoded per symbol. Accordingly, a mapper may accept a 16-bit word and convert it to 7 symbols because 7 symbols carrying 2.32 bits per symbol can encode 16.24 bits. In other

words, a combination of seven symbols that encodes five states has 5^7 (78,125) permutations. Accordingly, the 7 symbols may be used to encode the 2^{16} (65,536) permutations of 16 bits.

[0040] FIG. 5 illustrates an example of signaling 500 employing a three-phase modulation data-encoding scheme based on the circular state diagram 550. According to the data-encoding scheme, a three-phase signal may rotate in two directions and may be transmitted on three conductors 410a, 410b and 410c. Each of the three signals carried by the conductors 410a, 410b, 410c comprises the three-phase signal each conductor 410a, 410b and 410c being independently driven, with each signal being 120 degrees out of phase relative to the other two signals. At any point in time, each of the three wires is in a different state (represented by V+, V- and open) from the other two wires. The encoding scheme also encodes information in the polarity of the two of the conductors 410a, 410b and 410c that are actively driven to a positive and negative level. Polarity is indicated at 508 for the sequence of states depicted.

[0041] At any phase state in a three-wire example, exactly two of the conductors 410a, 410b, 410c carry a signal which is effectively a differential signal for that phase state, while the third conductor 410a, 410b or 410c is undriven. The phase state for each conductor 410a, 410b, 410c may be defined by voltage difference between the conductor 410a, 410b, 410c and at least one other conductor 410a, 410b, 410c, or by the direction of current flow, or lack of current flow, in the conductor 410a, 410b, 410c. As shown in the state diagram 550, three phase states (corresponding respectively to states A, B and C) are defined with signal flow from state A to state B, state B to state C, and state C to state A in a first direction and signal flow from state A to state C, state C to state B, and state B to state A in a second direction. For other values of N , transitions between the N states may be defined according to a corresponding state diagram to obtain circular rotation between state transitions.

[0042] In the example of a three-wire, three-phase link, clockwise rotation (A to B), (B to C) or (C to A) at a state transition may be used to encode a logic 1, while counter-clockwise rotations (A to C), (C to B) or (B to A) at the state transition may be used to encode a logic 0. Accordingly a bit may be encoded at each transition by controlling whether the signal is “rotating” clockwise or counter-clockwise. For example, a logic 1 may be encoded when the three wires transition from state A to state B and a logic 0 may be encoded when the three wires transition from state B to

state A. In the simple three-wire example depicted, direction of rotation may be easily determined based on which of the three wires is undriven before and after the transition.

[0043] Information may also be encoded in polarity of the driven conductors 410a, 410b, 410c or direction of current flow between two conductors 410a, 410b, 410c. Signals 502, 504, and 506 illustrate voltage levels applied to conductors 410a, 410b, 410c, respectively at each phase state in a three-wire, three-phase link. At any time, a first conductor 410a, 410b, 410c is coupled to a positive voltage (+V, for example), a second conductor 410a, 410b, 410c is coupled to a negative voltage (-V, for example), while the third conductor 410a, 410b, 410c may be open-circuited. As such, one polarity encoding state may be determined by the current flow between the first and second conductors 410a, 410b, 410c or the voltage polarities of the first and second conductors 410a, 410b, 410c. In some embodiments, two bits of data may be encoded at each phase transition. A decoder may determine rotation to obtain the first bit, and the second bit may be determined based on the polarity. The decoder having determined direction of rotation can determine the current phase state and the polarity of the voltage applied between the two active connectors 410a, 410b and/or 410c, or the direction of current flow through the two active conductors 410a, 410b and/or 410c.

[0044] In the example of the three-wire, three-phase link described herein, one bit of data may be encoded in the rotation, or phase change in the three-wire, three-phase link, and an additional bit may be encoded in the polarity of two driven wires. Certain embodiments, encode more than two bits in each transition of a three-wire, three-phase encoding system by allowing transition to any of the possible states from a current state. Given three rotational phases and two polarities for each phase, 6 states are defined, such that 5 states are available from any current state. Accordingly, there may be $\log_2(5) \cong 2.32$ bits per symbol (transition) and the mapper may accept a 16-bit word and convert it to 7 symbols.

[0045] N-Phase data transfer may use more than three wires provided in a communication link or bus. The use of additional signal wires that can be driven simultaneously provides more combinations of states and polarities and allows more bits of data to be encoded at each transition between states. This can significantly improve throughput of the system, and reduce the power consumption over approaches that

use multiple differential pairs to transmit data bits, while providing increased bandwidth.

- [0046] In one example, an encoder may transmit symbols using 6 wires with two pairs of wires driven for each state. The 6 wires may be labeled A through F, such that in one state, wires A and F are driven positive, wires B and E negative, and C and D are undriven (or carry no current). For six wires, there may be:

$$C(6,4) = \frac{6!}{(6-4)! \cdot 4!} = 15$$

possible combinations of actively driven wires, with:

$$C(4,2) = \frac{4!}{(4-2)! \cdot 2!} = 6$$

different combinations of polarity for each phase state.

- [0047] The 15 different combinations of actively driven wires may include:

A B C D	A B C E	A B C F	A B D E	A B D F
A B E F	A C D E	A C D F	A C E F	A D E F
B C D E	B C D F	B C E F	B D E F	C D E F

- [0048] Of the 4 wires driven, the possible combinations of two wires driven positive (and the other two must be negative). The combinations of polarity may comprise:

++-- +-+- +-+- -++- -++- --++

- [0049] Accordingly, the total number of different states may be calculated as $15 \times 6 = 90$. To guarantee a transition between symbols, 89 states are available from any current state, and the number of bits that may be encoded in each symbol may be calculated as: $\log_2(89) \cong 6.47$ bits per symbol. In this example, a 32-bit word can be encoded by the mapper into 5 symbols, given that $5 \times 6.47 = 32.35$ bits.

- [0050] The general equation for the number of combinations of wires that can be driven for a bus of any size, as a function of the number of wires in the bus and number of wires simultaneously driven:

$$C(N_{wires}, N_{driven}) = \frac{N_{wires}!}{(N_{wires} - N_{driven})! \cdot N_{driven}!}$$

- [0051] The equation for the number of combinations of polarity for the wires being driven is:

$$C\left(N_{driven}, \frac{N_{driven}}{2}\right) = \frac{N_{driven}!}{\left(\left(\frac{N_{driven}}{2}\right)!\right)^2}$$

[0052] The number of bits per symbol is:

$$\log_2 \left(C(N_{wires}, N_{driven}) \cdot C \left(N_{driven}, \frac{N_{driven}}{2} \right) - 1 \right).$$

[0053] FIG. 6 illustrates an example 600 of a receiver in a three-wire, three-phase physical layer (PHY). The three-wire, three-phase example is illustrative of certain principles of operation applicable to other configurations of M -wire, N -phase receivers. Comparators 602 and decoder 604 are configured to provide a digital representation of the state of each of three transmission lines 612a, 612b and 612c, as well as the change in the state of the three transmission lines compared to the state transmitted in the previous symbol period. Seven consecutive states are assembled by serial-to-parallel convertors 606 to produce a set of 7 symbols to be processed by demapper 608 to obtain 16 bits of data that may be buffered in FIFO 610.

[0054] According to certain aspects disclosed herein, a plurality of three-state amplifiers can be controlled to produce a set of output states defined by a differential encoder, an N -phase polarity encoder, or another encoder that encodes information in wires or connectors that can assume one of the three states described.

[0055] With reference again to FIGs. 2 and 4, the communication link 220 may comprise a high-speed digital interface that can be configured to support both differential encoding scheme and N -phase polarity encoding. Physical layer drivers 210 and 240 may comprise N -phase polarity encoders and decoders, which can encode multiple bits per transition on the interface, and line drivers to drive connectors 410a, 410b and 410c. The line drivers may be constructed with amplifiers that produce an active output that can have a positive or negative voltage, or a high impedance output whereby a connector 410a, 410b or 410c is in an undefined state or a state that is defined by external electrical components. Accordingly, the output drivers 408 may receive by a pair of signals 416 that includes data and output control (high-impedance mode control). In this regard, the three-state amplifiers used for N -phase polarity encoding and differential encoding can produce the same or similar three output states. When used for differential encoding, pairs of the three-state amplifiers in a differential line driver 306, 316, 316' or 324 (see FIG. 3) may receive a same input signal and output control signal, whereas each of the N -phase polarity encoding line drivers 408 receive individual inputs that define output state. According to certain aspects disclosed herein, the inputs provided to each the N -phase polarity encoding line driver 408 may be controlled by logic and/or switches

such that pairs of the line drivers 408 may be operated as a differential line driver 306, 316, 316' and 324.

[0056] Certain embodiments provide a configurable interface that can selectively activate a desired number of wires to communicate data, and/or to reconfigure an *M*-wire, *N*-Phase Polarity encoded interface to serve as a differential interface. FIG. 7 illustrates an example in which mobile platform 700 employs pin multiplexing to provide a reconfigurable communications interface. In the depicted example, a display processor 702 generates display data for a display device 124 (see FIG. 1). The display processor 702 may be integrated with a processing circuit 206, for example. With reference also to FIG. 2, data may be transmitted through a communications link 220 to a device 230 that includes a display controller 232. The communications link 220 may be configurable to comply with or be compatible with a MIPI standard DSI or an *N*-Phase Polarity interface as described herein. FIG. 7 shows an example configuration in which a switching element 726 selects between the outputs of three differential drivers 714 and the outputs of two three-wire, three-phase encoders 716 to drive 6 output pins 728. Other combinations and configurations of the output pins 718, drivers 714 and encoders 716 may be supported. In one example, the switching element 724 may comprise a switching matrix that allows output pins 728 to be mapped to any output of any differential driver 714 or any output of any *M*-wire, *N*-phase encoder.

[0057] When a MIPI DSI interface is configured, display pixel data originating from display processor 702 is provided to MIPI DSI Link Controller 704, which formats the display pixel data into packets to be sent over a high-speed serial interface 728 to Display, typically through device 230 and/or display controller 232. Both pixel data and control information may be transmitted over this link 728. A reverse link may be provided for reading status from display 124, or to receive other information.

[0058] Data packets generated by the MIPI DSI Link Controller 704 in the digital core logic circuitry 720 may be provided to a MIPI D-PHY Pre-Driver 706, which may be realized in an input/output section (Pad Ring) 724. The data packets may be provided to a set of output drivers 718 through differential drivers 714 and/or an electronic switch multiplexer 726. The differential drivers 714 may be enabled while *N*-Phase drivers 716 are disabled. In one example, the *N*-Phase drivers 716 may be

disabled when the *N*-Phase drivers 716 are forced or otherwise placed in high-impedance output mode.

[0059] In another example, the switch multiplexer 726 may select between differential drivers 714 and *N*-Phase drivers 716 to provide inputs to line drivers 718 when *N*-Phase Polarity encoding is required. The switch multiplexer 726 may be operated to select the outputs of the *N*-Phase drivers 716 as inputs to the output line drivers 718. Alternatively or additionally, the *N*-Phase drivers 716 may be enabled while differential drivers 714 are disabled and vice versa. In this configuration, data packets generated by MIPI DSI Link Controller 704 may be encoded using an *N*-Phase Polarity encoder 710 and provided to *N*-Phase Polarity pre-driver 712.

[0060] The determination of whether one or more of the line drivers 718 is in high impedance mode may be made by the encoder used to format data. In one example, output control (high impedance control) of the line drivers 718 may be controlled by the MIPI D-PHY Pre-Driver 706, when the interface is driven in a differential encoding mode. In another example, output control of the line drivers 718 may be controlled by the *N*-Phase Polarity pre-driver 712, when the interface is driven in *N*-Phase Polarity encoding mode.

[0061] According to certain aspects described herein, data packets similar to MIPI DSI packets are sent over an *N*-Phase Polarity link. Some packets may be reformatted to make proper use of symbol groups on the *N*-Phase Polarity link. For example, a byte may be added to odd-length packets when the MIPI DSI may be byte-oriented, while the *N*-Phase Polarity link is configured for transferring 16-bit words at a time. Transmitters and receivers may be configurable to account for differences in link synchronization between *N*-Phase Polarity encoding and differential encoding.

[0062] An *M*-wire *N*-phase link controller 708 may provide input data words to data as input to a mapper 402 (*cf.* FIG. 4), which maps the input word to a series of symbols to be sent over the bus. The mapper 402 may be embodied in an encoding element 710. One purpose of the mapper 402 is to compute the values of a group of symbols based on an input data word. This may be particularly useful if the number of bits per symbol is not an integer. In the simple example described in relation to FIG. 4, a three-wire, three-phase system is employed in which there are 3 possible combinations of 2 wires to be driven simultaneously, given that one wire is undriven. There are also 2 possible combinations of polarity for each pair of wires

that may be driven, yielding 6 possible states. 5 of the 6 states are usable because a transition is required between any two symbols. With 5 states there may be $\log_2(5) \cong 2.32$ bits per symbol. The mapper may accept a 16-bit word and convert it to 7 symbols.

[0063] Data packets generated by *N*-Phase Polarity Adaptation Link Controller 708 may be provided to *N*-Phase Polarity Encoder 710 to encode groups of link data (for example, 16-bit or 32-bit words) into groups of symbols, and outputs one symbol at a time to *N*-Phase Polarity Pre-Driver 712. In one example, *N*-Phase Polarity Adaptation Link Controller 708 may be realized in Digital Core Logic 720, and *N*-Phase Polarity Encoder 710 may be realized in the Pad Ring 724. The pre-driver 712 may amplify received input signals to a level sufficient to drive buffers 716 and/or Output Driver 718.

[0064] The switch multiplexer 726 may select either MIPI D-PHY Pre-Driver 706 output or *N*-Phase Polarity Pre-Driver 712 output to be provided to Output Drivers 718. The switch multiplexer 726 may transmit signals having a voltage or current level much lower than the output of Output Drivers 718. Accordingly, the output signals from MIPI D-PHY Pre-Driver 706 and/or *N*-Phase Polarity Pre-Driver 712 may be easily switched using an IC device. In some instances, control signals that determine if one or more output drivers should be in a high impedance state may be switched using switch multiplexer 726 or a related switching device.

[0065] The mode select 730 state of the switch multiplexer 726 may be set to a default or preconfigured selection when the system is powered up. Typically, this state need be configured only once because the display 124 may be permanently or semi-permanently attached to the processing circuit 102 (see FIG 1). Consequently, the switch multiplexer may be configured during manufacture and the setting need not be changed during normal operation of the system. In one example, the switch multiplexer 726 may be addressed by a processor 206 or 236 through one or more configuration registers, which may be non-volatile. Code for programming the switch multiplexer may be stored in storage 112. The use of the switch multiplexer 726 to switch low-level signals permits the same application processor to be used for more than one interface, without the need to duplicate I/O pads or pins. The same I/O pads or pins 728 may therefore be used for more than one interface, where programming of the switch multiplexer need only be performed once per system.

- [0066] The principles of operation described in relation to FIG. 7 may be applied in a wide variety of applications and a pin multiplexer may be employed to provide a flexible and reconfigurable communications link between different types of devices and in different types of apparatus, including applications that are not governed by industry standards.
- [0067] FIG. 8 is a flowchart illustrating an encoding system according to certain aspects of the invention. The method may be performed by one or more IC devices. At step 802, the one or more IC devices may determine a type of physical interface to be used for communicating between two devices in a wireless mobile terminal. The type of physical interface may be one of a plurality of types of physical interface supported by at least one of the two devices. One or more of the devices may include an *N*-phase encoder and a differential encoder, for example.
- [0068] At step 804, the one or more IC devices may select an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices. The data may be communicated over a bus having a plurality of connectors communicatively coupling the two devices. The plurality of connectors may include at least some bidirectional connectors. The connectors may include electrical or optical connectors.
- [0069] According to certain aspects disclosed herein, the encoder may provide the encoded data in differentially encoded signals. Configuring the plurality of drivers to receive the encoded data may include causing one or more outputs of another encoder to enter a high impedance mode. The other encoder may include an *N*-phase encoder.
- [0070] According to certain aspects disclosed herein, the selected encoder may provide the encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the connectors, a polarity of a second pair of connectors, and a selection of at least one undriven connector. The first pair of the connectors may comprise the same wires as the second pair of connectors or at least one different wire. Configuring the plurality of drivers to receive the encoded data may include causing one or more outputs of a differential encoder to enter a high impedance mode.
- [0071] At step 806, the one or more IC devices may configure a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical

interface to be used for communicating between the two devices. The plurality of drivers may be configured by controlling a plurality of switches to couple outputs of the encoder to the plurality of drivers.

[0072] In an aspect of the disclosure, the encoded data may relate to a camera or a display controlled by one of the two IC devices.

[0073] FIG. 9 is a diagram 900 illustrating a simplified example of a hardware implementation for an apparatus employing a processing circuit 902. The processing circuit 902 may be implemented with a bus architecture, represented generally by the bus 920. The bus 920 may include any number of interconnecting buses and bridges depending on the specific application of the processing circuit 902 and the overall design constraints. The bus 920 links together various circuits including one or more processors and/or hardware modules, represented by the processor 916, the modules or circuits 904, 906 and 908, a plurality of different encoders 910, line drivers configurable to drive connectors or wires 914 and the computer-readable storage medium 918. The bus 920 may also link various other circuits such as timing sources, peripherals, voltage regulators, and power management circuits, which are well known in the art, and therefore, will not be described any further.

[0074] The processor 916 is responsible for general processing, including the execution of software stored on the computer-readable storage medium 916. The software, when executed by the processor 916, causes the processing circuit 902 to perform the various functions described *supra* for any particular apparatus. The computer-readable storage medium 918 may also be used for storing data that is manipulated by the processor 916 when executing software. The processing circuit 902 further includes at least one of the modules 904, 906 and 908. The modules may be software modules running in the processor 916, resident/stored in the computer readable storage medium 918, one or more hardware modules coupled to the processor 916, or some combination thereof.

[0075] In one configuration, the apparatus 900 for wireless communication includes means 904 for determining an operational mode for communicating between the two IC devices, means 906 for selecting one of encoders 910 to provide encoded data for transmission on the plurality of connectors 914, and means 908 for configuring a plurality of drivers 912 to receive encoded data from the encoder 910 and to drive the connectors and/or wires 914. The aforementioned means may be one or more of

the aforementioned modules of the apparatus 900 and/or the processing circuit 902 of the apparatus 902 configured to perform the functions recited by the aforementioned means. The aforementioned means may be implemented, for example, using some combination of a processor 206 or 236, physical layer drivers 210 or 240 and storage media 208 and 238.

[0076] It is understood that the specific order or hierarchy of steps in the processes disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of steps in the processes may be rearranged. The accompanying method claims present elements of the various steps in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0077] The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean “one and only one” unless specifically so stated, but rather “one or more.” Unless specifically stated otherwise, the term “some” refers to one or more. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase “means for.”

WHAT IS CLAIMED IS:

CLAIMS

1. A data transfer method operational on at least one of two devices in a terminal, comprising:
 - determining a type of physical interface to be used for communicating between the two devices, wherein the type of physical interface is one of a plurality of types of physical interface supported by at least one of the two devices;
 - selecting an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices; and
 - configuring a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices.
2. The method of claim 1, further comprising:
 - controlling a plurality of switches to couple outputs of the encoder to the plurality of drivers.
3. The method of claim 1, wherein the plurality of connectors comprises at least some bidirectional connectors.
4. The method of claim 1, wherein the plurality of connectors comprises at least some unidirectional connectors.
5. The method of claim 1, wherein the encoder provides the encoded data in differentially encoded signals.
6. The method of claim 5, wherein configuring the plurality of drivers to receive the encoded data includes causing one or more outputs of a different encoder to enter a high impedance mode.
7. The method of claim 6, wherein the different encoder comprises an N-phase encoder.

8. The method of claim 1, wherein the encoder provides the encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the connectors and a polarity of a second pair of connectors.
9. The method of claim 8, wherein the sequence of symbols is encoded using one or more undriven connector.
10. The method of claim 8, wherein the first pair of the connectors comprises the same connectors as the second pair of connectors.
11. The method of claim 8, wherein configuring the plurality of drivers to receive the encoded data includes causing one or more outputs of a differential encoder to enter a high impedance mode.
12. An apparatus comprising:
a plurality of connectors communicatively coupling a first integrated circuit (IC) device with a second IC device;
means for determining a type of physical interface to be used for communicating between two devices in a terminal, wherein the type of physical interface is one of a plurality of types of physical interface supported by at least one of the two devices;
means for generating encoded data consistent with the type of physical interface to be used for communicating between the two devices, wherein the means for generating encoded data includes at least two encoders that are configured to encode data in different manners; and
means for configuring a plurality of drivers to receive the encoded data from one of the at least two encoders and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices.
13. The apparatus of claim 12, wherein the means for configuring the plurality of drivers comprises a plurality of switches that selectively connects outputs of the one of the at least two encoders to the plurality of drivers.

14. The apparatus of claim 12, wherein the plurality of connectors comprises at least some bidirectional connectors.
15. The apparatus of claim 12, wherein the plurality of connectors comprises at least some unidirectional connectors.
16. The apparatus of claim 12, wherein the one of the at least two encoders is configured to provide the encoded data in differentially encoded signals.
17. The apparatus of claim 16, wherein the means for configuring the plurality of drivers is configured to cause one or more outputs of a different one of the at least two encoders to enter a high impedance mode.
18. The apparatus of claim 16, wherein the at least two encoders comprise an N-phase encoder.
19. The apparatus of claim 12, wherein the one of the at least two encoders is adapted to provide the encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the connectors and a polarity of a second pair of connectors, and a selection of at least one undriven connector.
20. The apparatus of claim 19, wherein the sequence of symbols is encoded using a selection of at least one undriven connector.
21. The apparatus of claim 19, wherein the first pair of the connectors comprises the same connectors as the second pair of connectors.
22. The apparatus of claim 19, wherein the means for configuring the plurality of drivers is configured to cause one or more outputs of a differential encoder to enter a high impedance mode.

23. An apparatus, comprising:
a plurality of connectors communicatively coupling two devices in a terminal;
and
a processing circuit configured to:
determine a type of physical interface to be used for communicating between the two devices, wherein the type of physical interface is one of a plurality of types of physical interface supported by at least one of the two devices;
select an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices; and
configure a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of connectors communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices.
24. The apparatus of claim 23, wherein the processing circuit is configured to control a plurality of switches to couple outputs of the encoder to the plurality of drivers.
25. The apparatus of claim 23, wherein the plurality of connectors comprises at least some bidirectional connectors.
26. The apparatus of claim 23, wherein the plurality of connectors comprises at least some unidirectional connectors.
27. The apparatus of claim 23, wherein the encoder provides the encoded data in differentially encoded signals.
28. The apparatus of claim 27, wherein configuring the plurality of drivers to receive the encoded data includes causing one or more outputs of a different encoder to enter a high impedance mode.

29. The apparatus of claim 28, wherein the different encoder comprises an N-phase encoder.

30. The apparatus of claim 23, wherein the encoder provides the encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the connectors and a polarity of a second pair of connectors.

31. The apparatus of claim 30, wherein the sequence of symbols is encoded using a selection of at least one undriven connector.

32. The apparatus of claim 30, wherein the first pair of the connectors comprises the same connectors as the second pair of connectors.

33. The apparatus of claim 30, wherein configuring the plurality of drivers to receive the encoded data includes causing one or more outputs of a differential encoder to enter a high impedance mode.

34. A non-transitory processor-readable storage medium having one or more instructions which, when executed by at least one processing circuit, cause the at least one processing circuit to:

determine a type of physical interface to be used for communicating between two devices in a terminal, wherein the type of physical interface is one of a plurality of types of physical interface supported by at least one of the two devices;

select an encoder to generate encoded data consistent with the type of physical interface to be used for communicating between the two devices; and

configure a plurality of drivers to receive the encoded data from the encoder and to drive a plurality of wires communicatively coupling the two devices in accordance with the type of physical interface to be used for communicating between the two devices.

35. The non-transitory processor-readable storage medium of claim 34, wherein one or more instructions cause the at least one processing circuit to couple outputs of the encoder to the plurality of drivers.

36. The non-transitory processor-readable storage medium of claim 34, wherein the plurality of wires comprises at least some bidirectional wires.

37. The non-transitory processor-readable storage medium of claim 34, wherein the plurality of wires comprises at least some unidirectional wires.

38. The non-transitory processor-readable storage medium of claim 34, wherein the encoder provides the encoded data in differentially encoded signals.

39. The non-transitory processor-readable storage medium of claim 38, one or more instructions which, when executed by at least one processing circuit, cause the at least one processing circuit to force one or more outputs of a different encoder to enter a high impedance mode.

40. The non-transitory processor-readable storage medium of claim 39, wherein the different encoder comprises an N-phase encoder.

41. The non-transitory processor-readable storage medium of claim 34, wherein the encoder provides the encoded data in a sequence of symbols encoded using a combination of a phase state of a first pair of the wires and a polarity of a second pair of wires.

42. The processor-readable storage medium of claim 41, wherein the sequence of symbols is encoded using a selection of at least one undriven wire.

43. The non-transitory processor-readable storage medium of claim 41, wherein the first pair of the wires comprises the same wires as the second pair of wires.

44. The non-transitory processor-readable storage medium of claim 41, one or more instructions which, when executed by at least one processing circuit, cause the at least one processing circuit to force one or more outputs of a differential encoder to enter a high impedance mode.

100

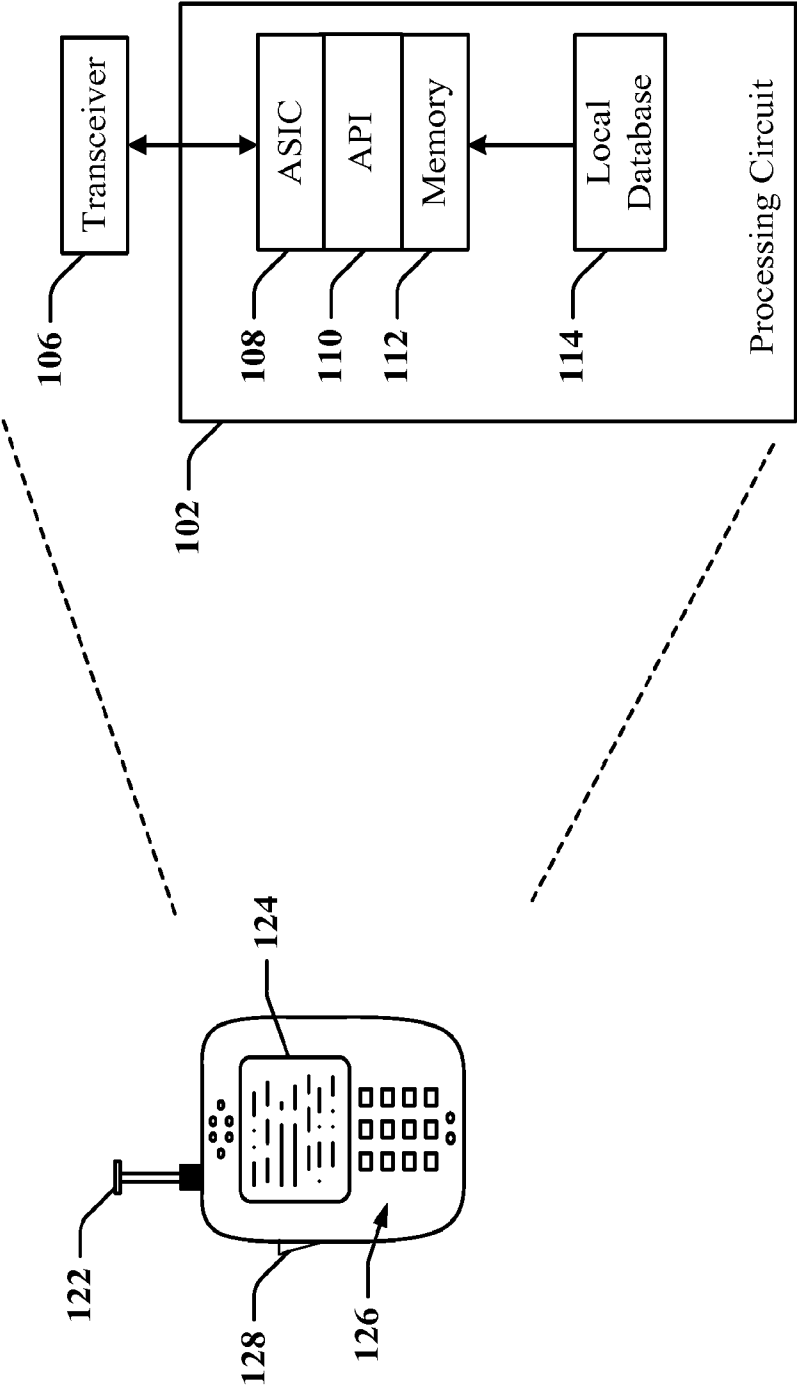


FIG. 1

200

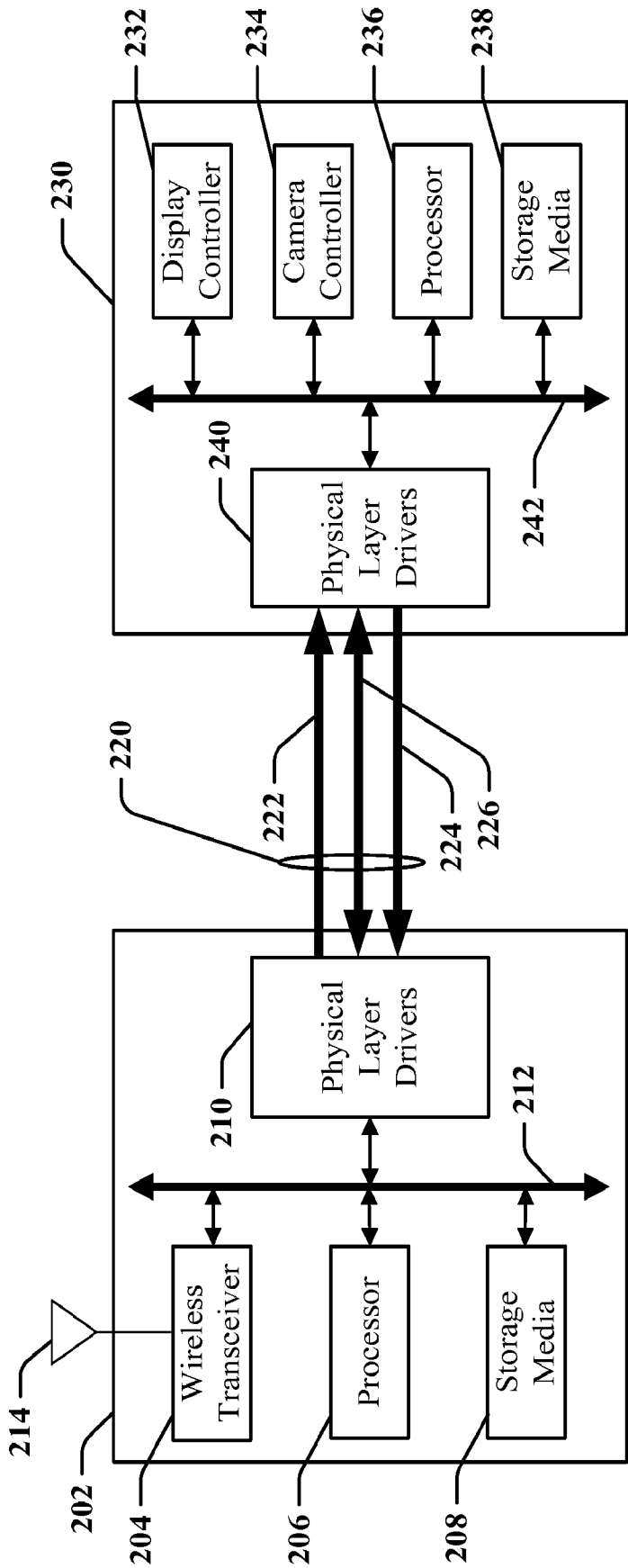


FIG. 2

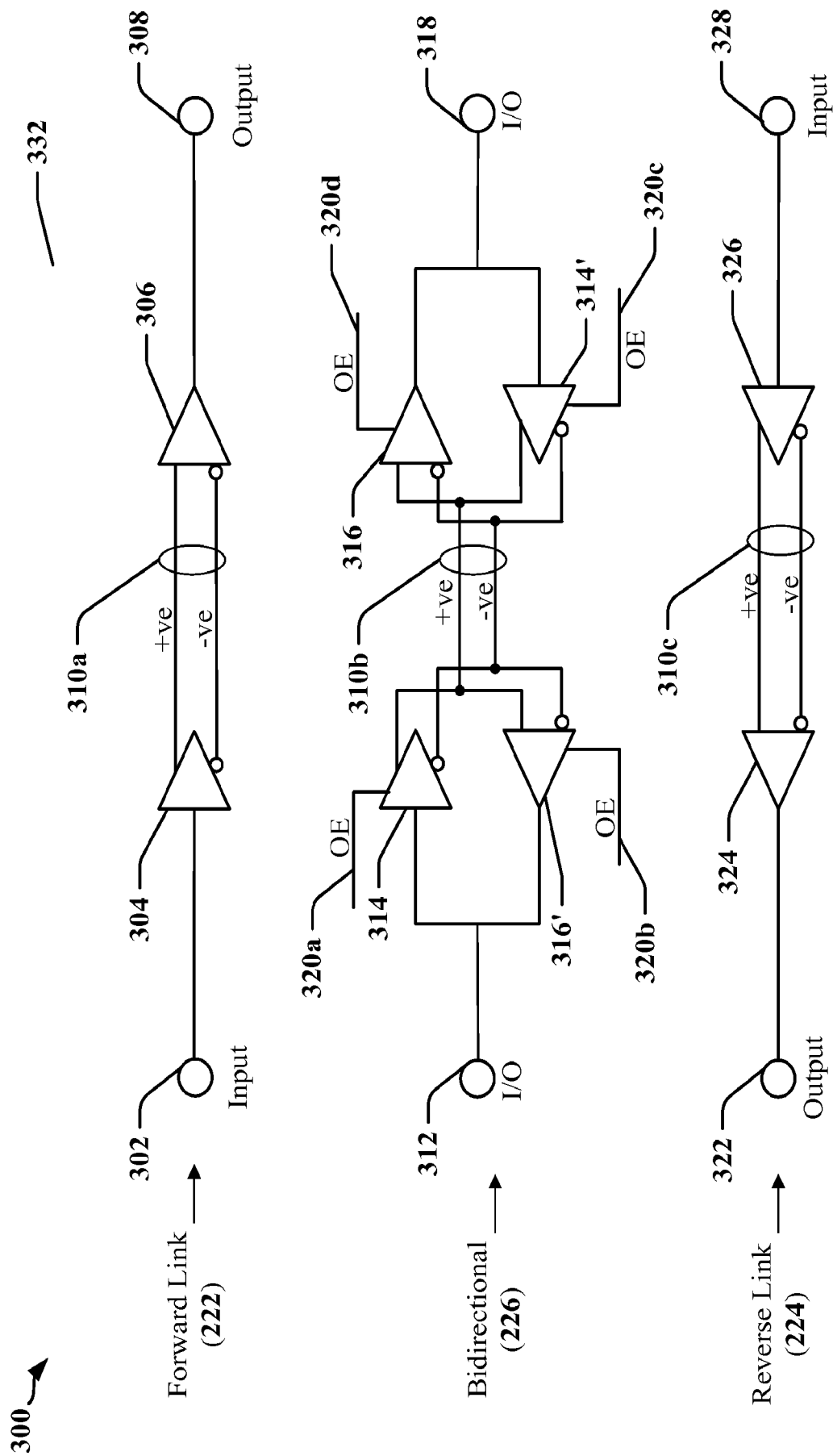


FIG. 3

400

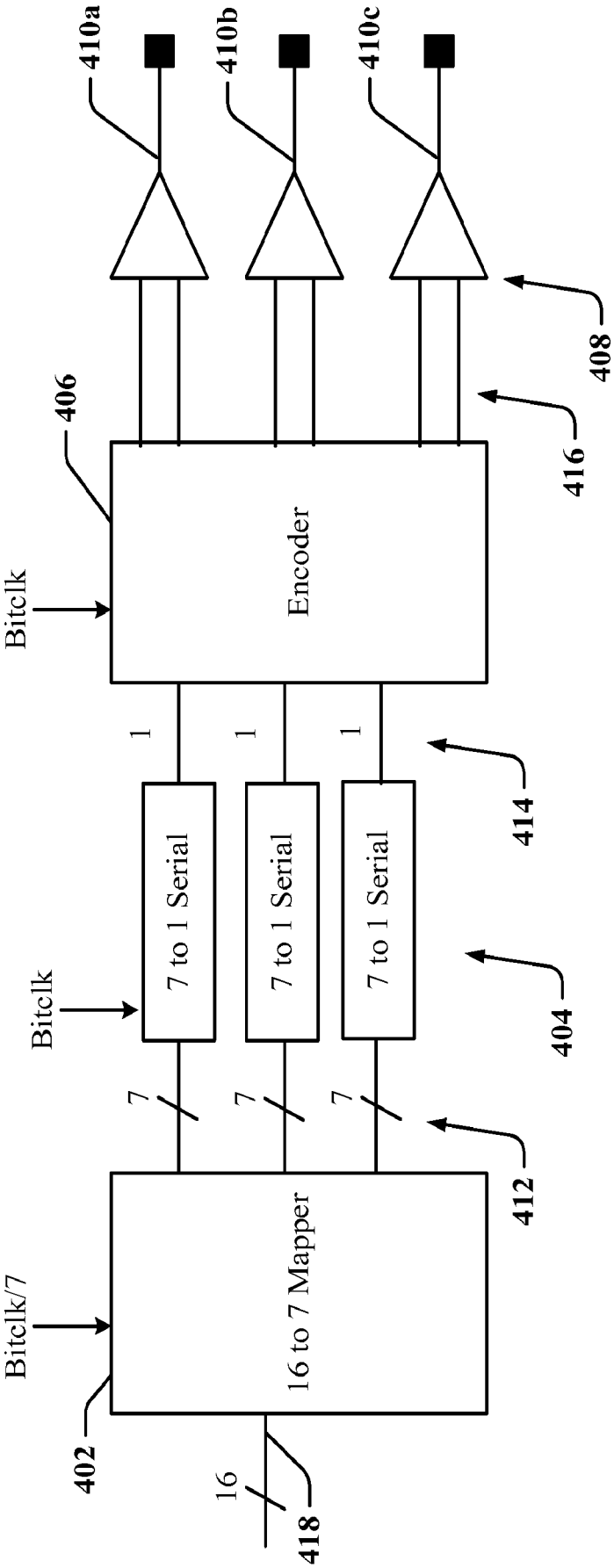


FIG. 4

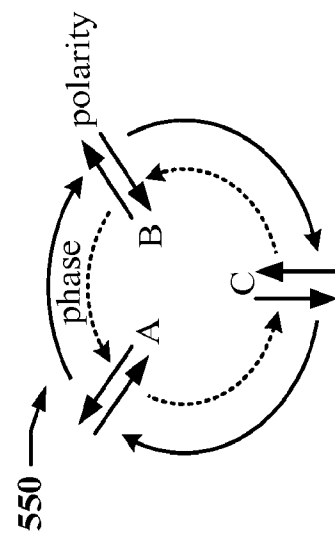
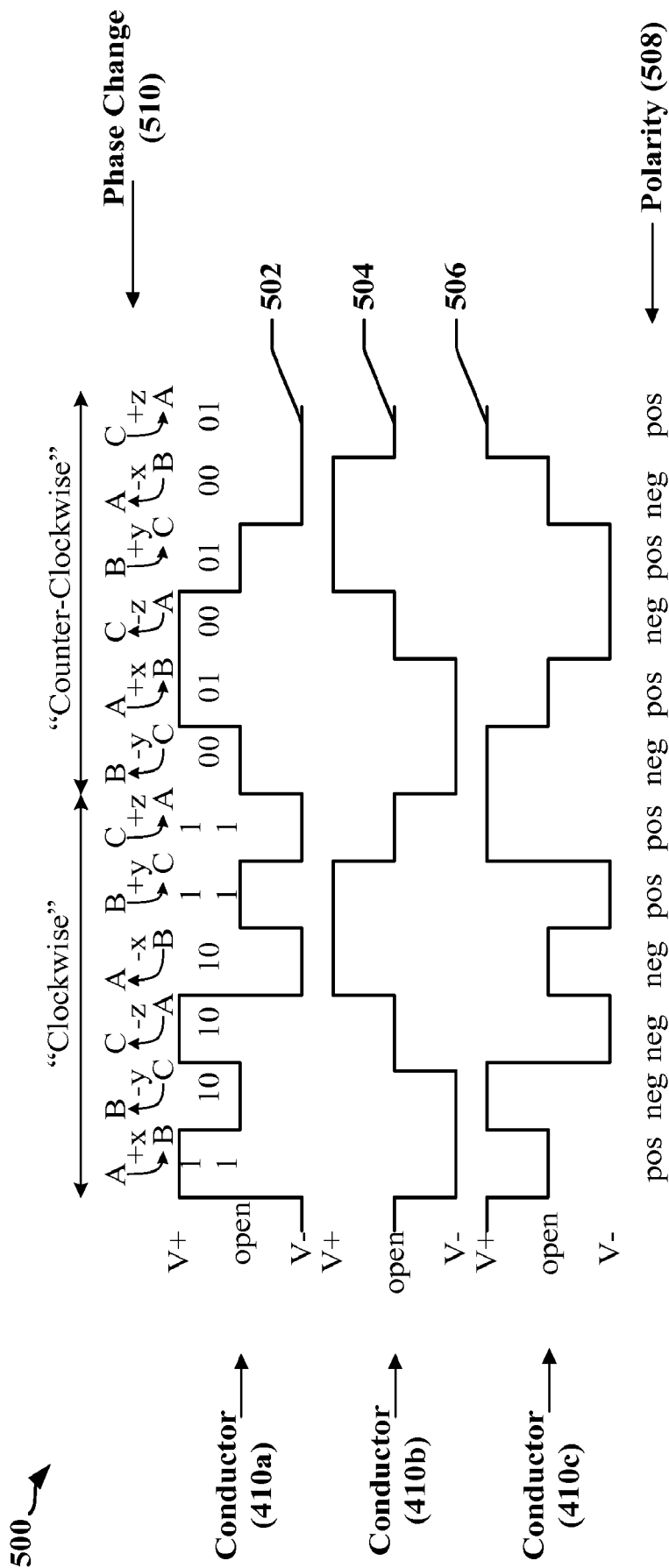
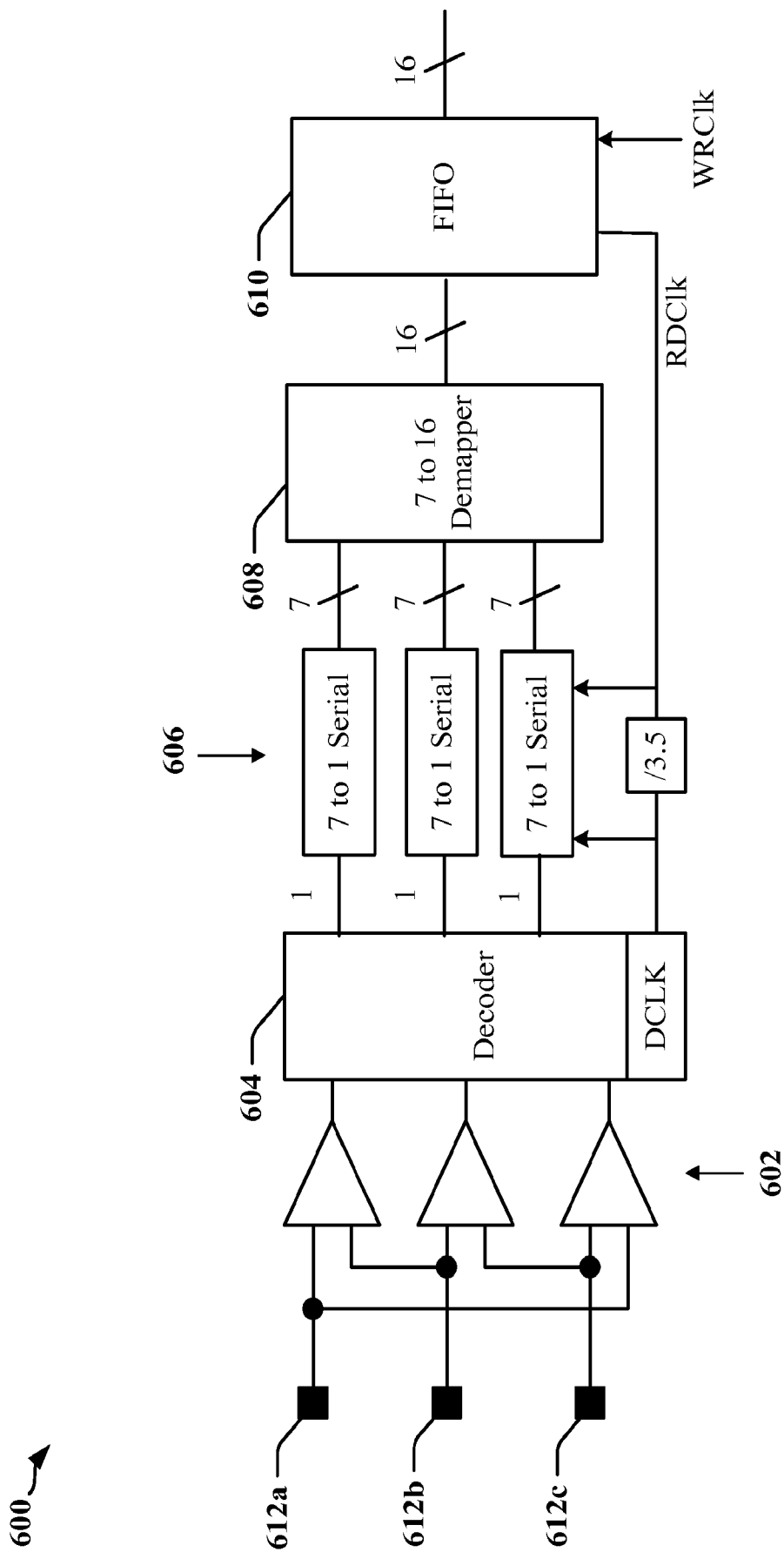


FIG. 5



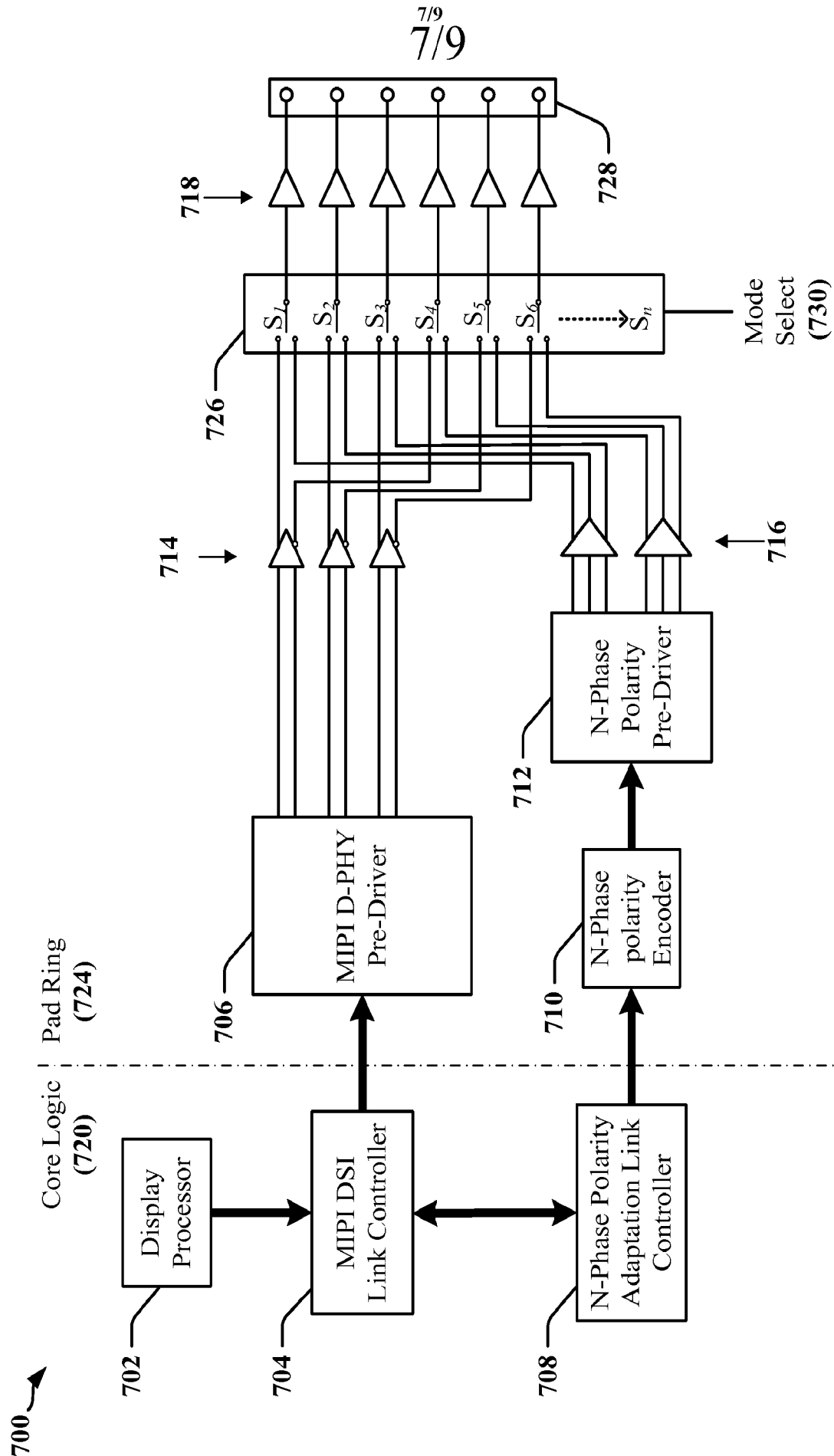
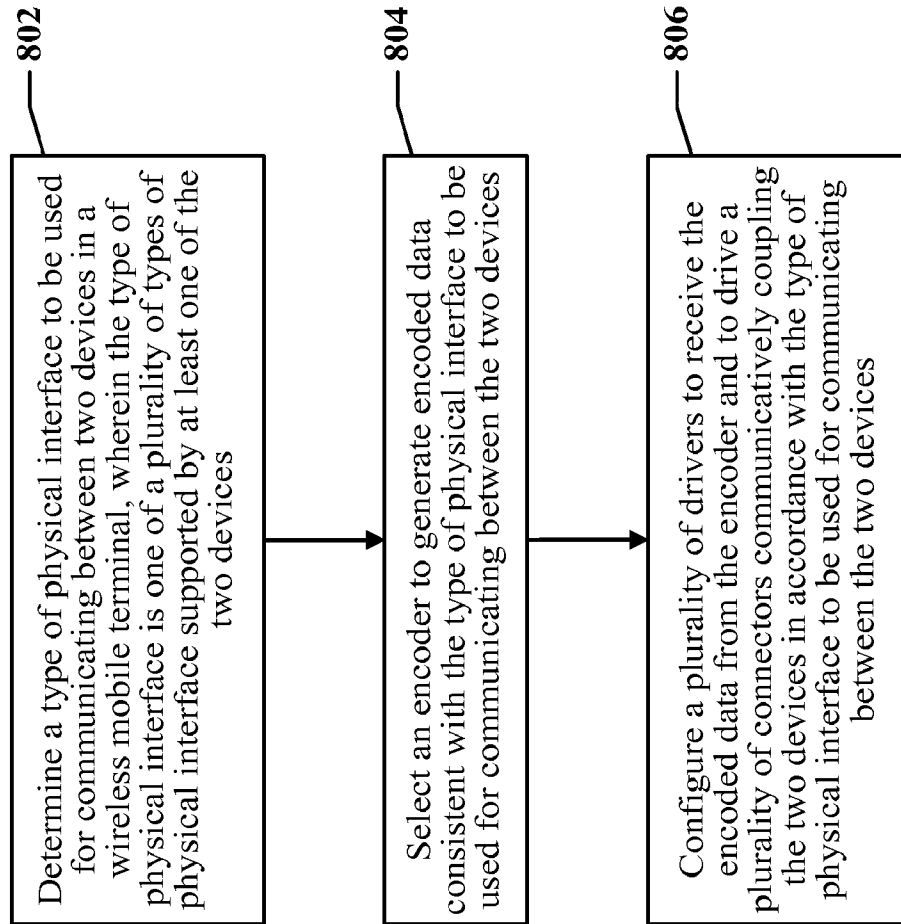


FIG. 7

800 ↗

**FIG. 8**

900 ↗

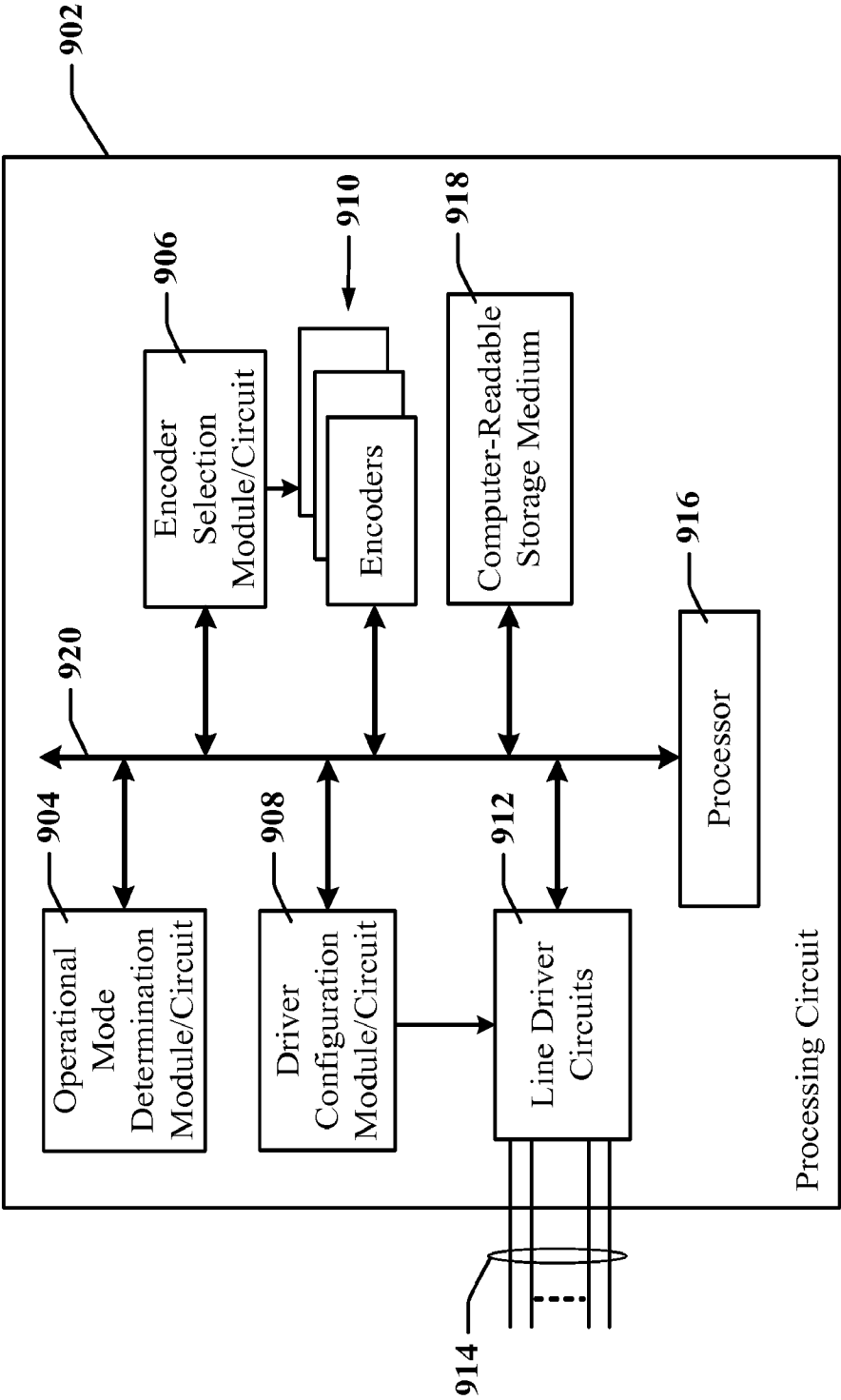


FIG. 9