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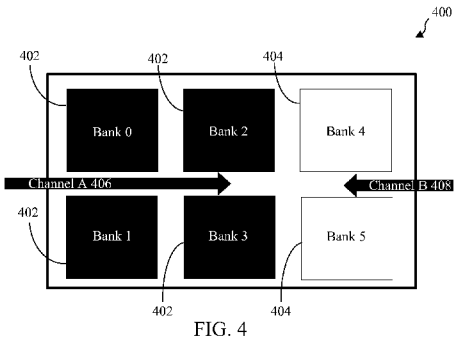

FIG. 4

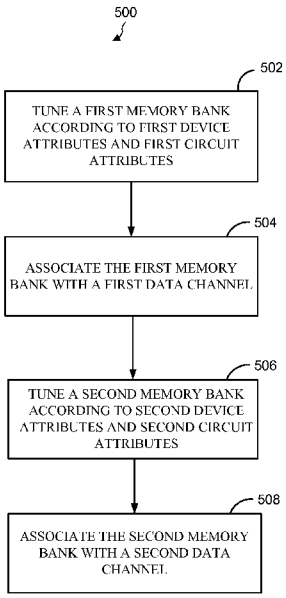

FIG. 5

(57) Abstract: A monolithic multi-channel resistive memory includes at least one first bank associated with a first channel and tuned according to first device attributes and/or first circuit attributes. The memory also includes at least one second bank associated with a second channel and tuned according to second device attributes and/or second circuit attributes.

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MONOLITHIC MULTI-CHANNEL ADAPTABLE STT-MRAM

TECHNICAL FIELD

[0001] The present disclosure relates generally to magnetoresistive random-access memory (MRAM) cells. More specifically, the disclosure relates to multi-channel adaptable MRAM.

BACKGROUND

[0002] In a conventional memory subsystem, such as a memory subsystem used for computing, different types of standalone memory, such as dynamic random access memory (DRAM) and flash memory (NAND, NOR), are adopted .

[0003] DRAM is a high-throughput and low-cost commodity working memory. DRAM, however, is volatile and has a large power consumption.

[0004] Hybrid DRAM (e.g., OneDRAM^{TM}) is a variant of DRAM, which is a single DRAM die with two ports for serving two processors (e.g., a modem and an application processor). Similar to conventional DRAM, however, hybrid DRAM is volatile and has a large power consumption.

[0005] Flash (NAND, NOR) is a storage memory technology which is nonvolatile and low-cost. But, flash is slow and limited in its endurance. Hybrid flash (e.g., NAND memory with an integrated NOR block) is a variant of flash, which couples NOR's performance advantage with NAND's density advantage. Compared with a working memory like DRAM, however, hybrid flash, however is still much slower and limited in its endurance.

[0006] None of the conventional memory technologies can simultaneously serve as a working memory and a nonvolatile storage memory. Accordingly, multiple memory chip solutions are provided in a multi-chip package (MCP) or in a system-in- package (SiP). For example, for mobile systems, it is common to have pseudo-static RAM (PSRAM)-NOR or DRAM-NAND that combines multiple memory chips having unique attributes. Still, MCP and SiP have a higher system cost and a larger form factor than a system using a single memory solution.

[0007] For various reasons, such as cost, speed and capacity, known types of memory have generic limitations, so that each serves its unique application. Thus, it would be desirable to provide a low-cost memory that provides the benefits of each of the current memory types but does not have the short comings described above. It is also desirable for such memory to be tunable for speed, power, and density.

SUMMARY

[0008] According to an aspect of the present disclosure a monolithic multi-channel resistive memory is presented. The memory includes at least one first bank associated with a first channel and tuned according to first device attributes and/or first circuit attributes. The memory also includes at least one second bank associated with a second channel and tuned according to second device attributes and/or second circuit attributes.

[0009] According to another aspect, a monolithic multi-channel resistive memory is presented. The memory includes at least one first storage means associated with a first channel and tuned according to first device attributes and/or first circuit attributes. The memory also includes at least one second storage means associated with a second channel and tuned according to second device attributes and/or second circuit attributes.

[0010] According to another aspect, a method of associating memory banks with channels in a monolithic multi-channel resistive memory. The method includes associating at least one first bank with a first channel, the at least one first bank tuned according to first device attributes and/or first circuit attributes. The method also includes associating at least one second bank with a second channel, the at least one second bank tuned according to second device attributes and/or second circuit attributes.

[0011] According to still another aspect, a method for fabricating memory banks for a monolithic multi-channel resistive memory is presented. The method includes tuning at least one first bank according to first device attributes and/or first circuit attributes. The method also includes tuning at least one second bank according to second device attributes and/or second circuit attributes.

[0012] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It

should be appreciated by those skilled in the art that this disclosure may be readily used as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The features, nature, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings.

[0014] FIGURE 1 illustrates a prior art memory system.

[0015] FIGURE 2 is a block diagram of a monolithic multi-tiered MRAM system according to an aspect of the disclosure.

[0016] FIGURE 3 illustrates an example of monolithic multi-tiered MRAM according to an aspect of the disclosure.

[0017] FIGURE 4 illustrates an example of monolithic multi-tiered MRAM according to an aspect of the disclosure.

[0018] FIGURE 5 is a block diagram of a method for fabricating a monolithic multi-tiered MRAM according to an aspect of the disclosure.

[0019] FIGURE 6 illustrates an exemplary wireless communication system in which an embodiment of the disclosure may be advantageously employed.

[0020] FIGURE 7 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one aspect of the present disclosure.

DETAILED DESCRIPTION

[0021] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts.

[0022] Proposed is a monolithic multi-channel spin transfer torque (STT)-MRAM architecture that is tunable for speed, power, and density, and therefore desirable for providing a low cost, universal memory.

[0023] Unlike conventional random access memory (RAM) chip technologies, in magnetoresistive RAM (MRAM) data is not stored as electric charge, but is instead stored by magnetic polarization of storage elements. The storage elements are formed from two ferromagnetic layers separated by a tunneling layer. One of the two ferromagnetic layers, which is referred to as the fixed layer or pinned layer, has a magnetization that is fixed in a particular direction. The other ferromagnetic magnetic layer, which is referred to as the free layer, has a magnitization direction that can be altered to represent either"1" when the free layer magnetization is anti-parallel to the fixed layer magnitization or "0" when the free layer magnetization is parallel to the fixed layer magnitization or vice versa. One such device having a fixed layer, a tunneling layer, and a free layer is a magnetic tunnel junction (MTJ). The electrical resistance of an MTJ depends on whether the free layer magnitization and fixed layer magnitization are parallel or anti-parallel with each other. A memory device such as MRAM is built from an array of individually addressable MTJs.

[0024] It should be noted that MRAM may be referrrd as resistive memory. Alternatively, a resistive memory may be any memory type that is configurable similar to a MRAM.

[0025] STT-MRAM is a type of MRAM. The free layer magnetization of STT-MRAM may be switched by an electrical current that passes through an MTJ. Thus, STT-MRAM is differentiated from conventional MRAM which uses a magnetic field. STT-

MRAM is tunable for speed, power, and density. STT-MRAM may be tailored as an alternative to working memories (e.g., DRAM, SRAM) and storage memories (e.g., Flash, ROM). STT-MRAM cells and macros can be fabricated in multiple configurations (e.g., multi-tiered) in a monolithic die without incurring extra process steps and cost. By incorporating multi-channels, a multi-tiered monolithic STT-MRAM may be used as a memory subsystem consisting of different types of memories (e.g., universal memory).

[0026] Prior art systems may use different types of memory chips configured according to the system specification. FIGURE 1 illustrates a prior art system 100 including a processor 102 a first memory type 104, a second memory type 106, a first channel 108, and a second channel 110. The first memory type 104 and the second memory type 106 are different memory chips.

[0027] As an example, the processor 102 may be configured as a modem. The modem may use a first memory type 104, such as a pseudo static random access memory (PSRAM) and a second memory type 106, such as a flash memory. The first channel 108 and second channel 110 may be external bus interfaces (EBIs).

[0028] As another example, the processor 102 may be configured as a modem or an application processor. The processor 102 may use a first memory type 104, such as a low power double data rate memory (LPDDR) DRAM and a second memory type 106, such as a flash memory. Furthermore, the first channel 108 may be an external bus interface and the second channel 110 may be an external bus interface or an embedded multimedia card (eMMC).

[0029] The present disclosure provides a monolithic multi-channel multi-tiered MRAM that may be used as a custom memory to replace the various memory types of the prior art systems, such as the prior art system 100. Although the following description is primarily with respect to STT-MRAM, other types of MRAM are also contemplated. As illustrated in FIGURE 2, according to the present solution, a system 200 may include a processor 202 coupled with a monolithic multi-channel, multi-tiered STT-MRAM 204. The processor 202 may any type of processor, such a processor for a modem or an application processor. The processor 202 is coupled to the STT-MRAM 204 via a first channel 206 and a second channel 208. In some aspects of the present disclosure, the STT-MRAM includes sets

of memory banks that may be configured to replace different memory types, such as, for example, DRAM, flash, and PSRAM-flash MCP.

[0030] FIGURE 3 illustrates an example of a multi-channel and multi-tiered STT-MRAM 300 according to an aspect of the present disclosure. As illustrated in FIGURE 3 the STT-MRAM 300 includes a first set of banks (Bank 0) 302 and a second set of banks (Bank 1) 304. The first set of banks 302 may be accessed by a first channel 306 and the second set of banks may be accessed by a second channel 308. That is, the dual channels, i.e., the first channel 306 and the second channel 308, allow independent access to the different banks 302 and 304.

[0031] According to one aspect, each bank may be independently tuned (e.g., configured) based on various characteristics. As one example of the present aspect, the STT-MRAM 300 of FIGURE 3 is configured to replace a DRAM chip and a flash chip. That is, the first set of banks 302 are configured for a DRAM interface and the second set of banks 304 are configured for a flash interface (e.g., NOR interface).

[0032] Specifically, for configuration as a DRAM interference, the first set of banks 302 are configured as a nonvolatile working memory block with high endurance and fast read/write cycles. Furthermore, the first set of banks 302 may be configured as a first bitcell type (in this example, tuned for DRAM specifications). It should be noted that nonvolatile refers to a memory that does not refresh. Moreover, for configuration as the flash interface, the second set of banks 304 may be configured as a storage memory block for long data retention (e.g., program code storage). According to the present aspect, the second set of banks 304 would operate faster in comparison to a typical flash chip. Furthermore, the second set of banks 304 may be configured as a second bitcell type (in this example, a high retention bitcell).

[0033] According to another example of the present aspect, the STT-MRAM 300 of FIGURE 3 are configured to replace a PSRAM-flash MCP. That is, the first set of banks 302 are configured for a PSRAM interface and the second set of banks 304 are configured for a flash interface. Specifically, for configuration as the PSRAM interference, the first set of banks 302 are configured as a nonvolatile working memory block with a high endurance and fast read and write cycles. Furthermore, the first set of banks 302 are configured as a third bitcell type in this example, tuned for PSRAM specifications. Moreover, for configuration as

the flash interface, the second set of banks 304 are configured as a storage memory block for long data retention (e.g., code storage). According to the present aspect, the second set of banks 304 would operate faster in comparison to a typical Flash chip. Furthermore, the second set of banks 304 may be configured as the second bitcell type.

[0034] FIGURE 4 illustrates an example of a multi-channel and multi-tiered STT-MRAM 400 according to an other aspect of the present disclosure. As illustrated in FIGURE 4, the STT-MRAM 400 includes a first set of banks (Banks 0-3) 402 and a second set of banks (Banks 4 and 5) 404. The first set of banks 402 may be accessed by a first channel 406 and the second set of banks may be accessed by a second channel 408. That is, the dual channels 406, 408 allow independent access to the different banks 402 and 404. Banks 0 and Bank 1 may be provided in a first tier whereas Bank 2 and Bank 3 may be provided in a second tier.

[0035] According to aspects of the present disclosure, the die area of the STT-MRAM 300 may be adjusted according to custom product applications. That is, the relative memory capacity may be adjusted. Furthermore, as illustrated in FIGURES 3 and 4, the bank configuration (internal and relative) may be adjustable. For example, FIGURE 3 illustrates an aspect with two banks in the first set of banks 302 and two banks in the second set of banks 304. Moreover, FIGURE 4 illustrates an aspect with four banks (Banks 0-3) in the first set of banks 402 and two banks (Banks 4 and 5) in the second set of banks 404. The bank configurations are not limited to the aspects illustrated in FIGURES 3 and 4, and may be adjusted as desired. The density range of the banks may be anywhere from tens of megabits (Mbits) to multi-gigabits (MGbits).

[0036] It should be noted that the aspect illustrated in FIGURE 4 may be configurable similar to the aspects disclosed for FIGURE 3. That is, the STT-MRAM 400 may be configured to replace, for example, a DRAM and flash (e.g., two chips), or may be configured to replace a PSRAM-Flash MCP. The configurations of the STT-MRAM 400 are not limited to the aforementioned examples and the present disclosure contemplates other memory configurations.

[0037] According to an aspect of the disclosure, the monolithic multi-tier STT-MRAM may be fabricated by a process that maintains a baseline among the different tiers. The fabrication process includes a front-end-of-line (FEOL) and back-end-of line (BEOL)

processes. Furthermore, the fabrication includes creating a magnetic tunnel junction (MTJ) materials stack.

[0038] Although a base line is maintained across the tiers, each tier (e.g., set of banks) may be configured according to various device options. A configurable device option may include a bitcell architecture, such as one transistor-one junction (1T-1J), two transistors-one junction (2T-1J), cross-point array, etc. Other configurable device options may be also include bitcell size, transistor size, MTJ size, or a combination thereof. The configurations of the device options may include permutations of all or some of the attributes listed above.

[0039] Furthermore, each tier may also be configured according to various circuit options. The configurable circuit options may include an operating voltage, input/output (IO) width, IO speed/frequency, array organization, redundancy, error correcting code (ECC), or a combination thereof. The configurations of the circuit options may include permutations of all or some of the attributes listed above. It should be noted that in the present disclosure attributes and options include parameters.

[0040] In some aspects, the STT-MRAM utilizes a homogeneous lower level process integration resulting in no extra process overhead because the different banks are simultaneously fabricated. That is, the same fabrication processes may be used for each type of STT-MRAM with only slight variation in the overall process flow. For example different mask layouts may be used within the same process flow to create the differently tuned banks.

[0041] It should be noted that although the aspects above are disclosed for a STT-MRAM, the aspects are not limited to a STT-MRAM and are contemplated for other memory types that are configurable similar to STT-MRAM.

[0042] FIGURE 5 illustrates a block diagram of a method 500 for tuning memory banks in a monolithic multi-channel resistive memory chip. As illustrated in FIGURE 5, shown in block 502, a first memory bank is tuned according to first device attributes and first circuit attributes. As shown in block 504, the first memory bank is associated with a first data channel. Furthermore, as shown in block 506, a second memory bank is tuned according to second device attributes and second circuit attributes. Additionally, the second memory bank is associated with a second data channel, as shown in block 508.

[0043] FIGURE 6 shows an exemplary wireless communication system 600 in which an embodiment of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 6 shows three remote units 620, 630, and 650 and two base stations 640. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 620, 630, and 650 include monolithic multi-tiered STT-MRAM 625A, 625B, 625C. FIGURE 6 shows forward link signals 660 from the base stations 640 and the remote units 620, 630, and 650 and reverse link signals 660 from the remote units 620, 630, and 650 to base stations 640.

[0044] In FIGURE 6, the remote unit 620 is shown as a mobile telephone, remote unit 630 is shown as a portable computer, and remote unit 650 is shown as a fixed location remote unit in a wireless local loop system. For example, the remote units may be cell phones, hand-held personal communication systems (PCS) units, a set top box, a music player, a video player, an entertainment unit, a navigation device, portable data units, such as personal data assistants, or fixed location data units such as meter reading equipment. Although FIGURE 6 illustrates remote units, which may employ monolithic multi-tiered STT-MRAM 625A, 625B, 625C according to the teachings of the disclosure, the disclosure is not limited to these exemplary illustrated units. For instance, monolithic multi-tiered STT-MRAM according to aspects of the present disclosure may be suitably employed in any device.

[0045] FIGURE 7 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the monolithic multi-tiered STT-MRAM disclosed above. A design workstation 700 includes a hard disk 701 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 700 also includes a display 702 to facilitate design of a circuit 710 or a semiconductor component 712 such as a monolithic multi-tiered STT-MRAM. A storage medium 704 is provided for tangibly storing the circuit design 710 or the semiconductor component 712. The circuit design 710 or the semiconductor component 712 may be stored on the storage medium 704 in a file format such as GDSII or GERBER. The storage medium 704 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 700 includes a drive apparatus 703 for accepting input from or writing output to the storage medium 704.

[0046] Data recorded on the storage medium 704 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 704 facilitates the design of the circuit design 710 or the semiconductor component 712 by decreasing the number of processes for designing semiconductor wafers.

[0047] In one configuration, the memory apparatus includes at least one first storage means associated with a first channel and tuned according to first device attributes and/or first circuit attributes. The memory apparatus also includes at least one second storage means associated with a second channel and tuned according to second device attributes and/or second circuit attributes. The storage means may be the multi-tiered STT-MRAM 204, a first set of banks 302 402, and/or a second set of banks 304 404 configured to perform the functions recited by the storage means.

[0048] Although specific circuitry has been set forth, it will be appreciated by those skilled in the art that not all of the disclosed circuitry is required to practice the disclosed embodiments. Moreover, certain well known circuits have not been described, to maintain focus on the disclosure.

[0049] The methodologies described herein may be implemented by various means depending upon the application. For example, these methodologies may be implemented in hardware, firmware, software, or any combination thereof. For a hardware implementation, the processing units may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, electronic devices, other electronic units designed to perform the functions described herein, or a combination thereof.

[0050] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. Any machine or computer readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software code may be stored in a memory and executed by a processor. When executed by the processor, the executing software code generates the operational environment that

implements the various methodologies and functionalities of the different aspects of the teachings presented herein. Memory may be implemented within the processor or external to the processor. As used herein, the term "memory" refers to any type of long term, short term, volatile, nonvolatile, or other memory and is not limited to any particular type of memory or number of memories, or type of media upon which memory is stored.

[0051] The machine or computer readable medium that stores the software code defining the methodologies and functions described herein includes physical computer storage media. A storage medium may be any available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer. As used herein, disk and/or disc includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and blu-ray disc where *disks* usually reproduce data magnetically, while *discs* reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer readable media.

[0052] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0053] Although the present teachings and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the teachings as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular aspects of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding aspects described herein may be used according to the present teachings. Accordingly, the

appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A monolithic multi-channel resistive memory, comprising:

at least one first bank associated with a first channel and tuned according to first device attributes and/or first circuit attributes; and

at least one second bank associated with a second channel and tuned according to second device attributes and/or second circuit attributes.

2. The memory of claim 1, in which the first device attributes and the second device attributes comprise at least a bitcell architecture, bitcell size, transistor size, and/or MTJ size.

3. The memory of claim 1, in which the first circuit attributes and the second circuit attributes comprise at least an operating voltage, input/output (IO) width, IO speed/frequency, array organization, redundancy, and/or error correcting code (ECC).

4. The memory of claim 1, in which the memory is a spin transfer torque magnetoresistive random-access memory (STT-MRAM).

5. The memory of claim 1, in which the memory is a magnetoresistive random-access memory (MRAM).

6. The memory of claim 1, in which the memory is coupled to a processor via the first channel and the second channel.

7. The memory of claim 1, further comprising at least one third bank associated with a third channel and tuned according to third device attributes and/or third circuit attributes.

8. The memory of claim 1, in which the memory is integrated in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a

computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

9. A monolithic multi-channel resistive memory, comprising:

at least one first storage means associated with a first channel and tuned according to first device attributes and/or first circuit attributes; and

at least one second storage means associated with a second channel and tuned according to second device attributes and/or second circuit attributes.

10. The memory of claim 9, integrated in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

11. A method of associating memory banks with channels in a monolithic multi-channel resistive memory, the method comprising:

a step of associating at least one first bank with a first channel, the at least one first bank tuned according to first device attributes and/or first circuit attributes; and

a step of associating at least one second bank with a second channel, the at least one second bank tuned according to second device attributes and/or second circuit attributes.

12. The method of claim 11, further comprising a step of integrating the memory in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

13. A method of associating memory banks with channels in a monolithic multi-channel resistive memory, the method comprising:

associating at least one first bank with a first channel, the at least one first bank tuned according to first device attributes and/or first circuit attributes; and

associating at least one second bank with a second channel, the at least one second bank tuned according to second device attributes and/or second circuit attributes.

14. The method of claim 13, further comprising coupling the memory to a processor via the first channel and the second channel.

15. The method of claim 13, further comprising integrating the memory in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

16. A method for fabricating memory banks for a monolithic multi-channel resistive memory, the method comprising:

tuning at least one first bank according to first device attributes and/or first circuit attributes; and

tuning at least one second bank according to second device attributes and/or second circuit attributes.

17. The method of claim 16, in which the first device attributes and the second device attributes comprise at least a bitcell architecture, bitcell size, transistor size, and/or MTJ size.

18. The method of claim 16, in which the first circuit attributes and the second circuit attributes comprise at least an operating voltage, input/output (IO) width, IO speed/frequency, array organization, redundancy, and/or error correcting code (ECC).

19. The method of claim 16, further comprising tuning at least one third bank according to third device attributes and/or third circuit attributes.

20. The method of claim 16, further comprising integrating the memory in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

21. A method for fabricating memory banks for a monolithic multi-channel resistive memory, the method comprising:

a step of tuning at least one first bank according to first device attributes and/or first circuit attributes; and

a step of tuning at least one second bank according to second device attributes and/or second circuit attributes.

22. The method of claim 21, further comprising a step of integrating the memory in a mobile phone, a set top box, a music player, a video player, an entertainment unit, a navigation device, a computer, a hand-held personal communication systems (PCS) unit, a portable data unit, and/or a fixed location data unit.

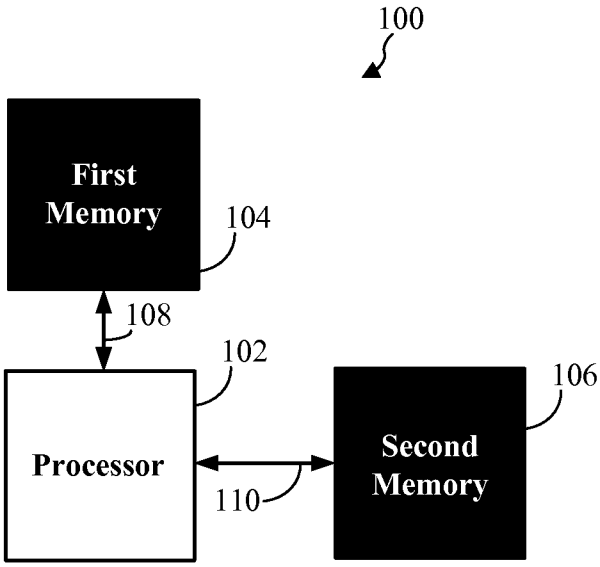

FIG. 1
(PRIOR ART)

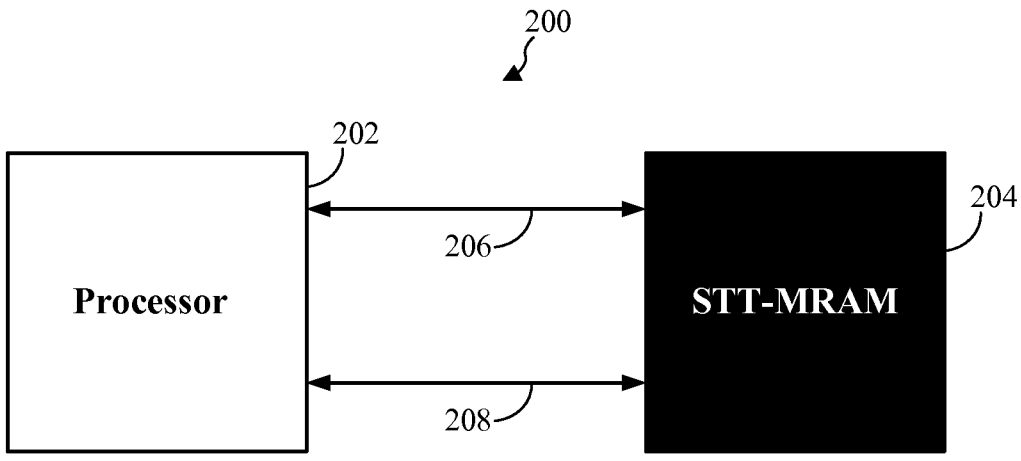

FIG. 2

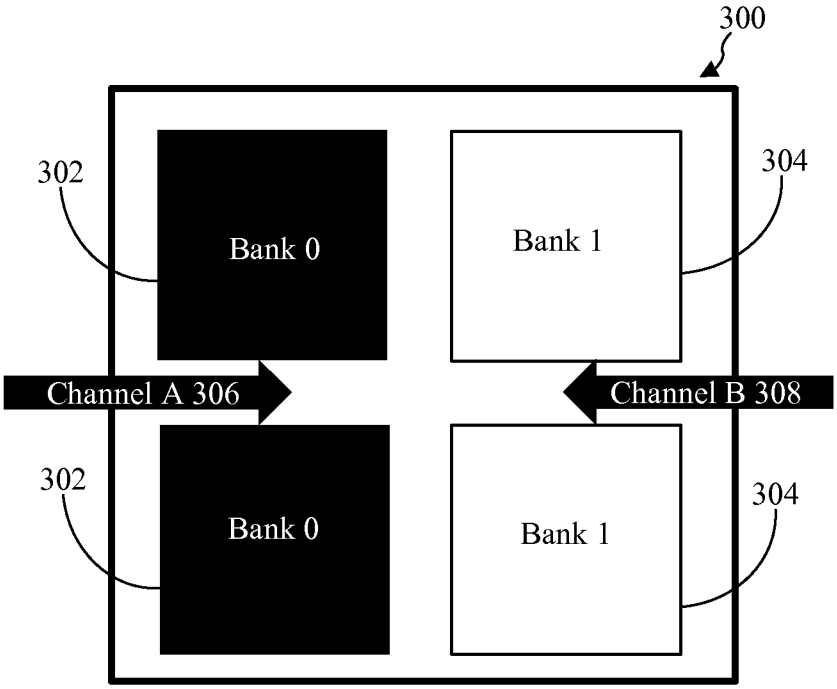
300
302
Bank 0
Bank 1
304
Channel A 306
Channel B 308
302
Bank 0
Bank 1
304

FIG. 3

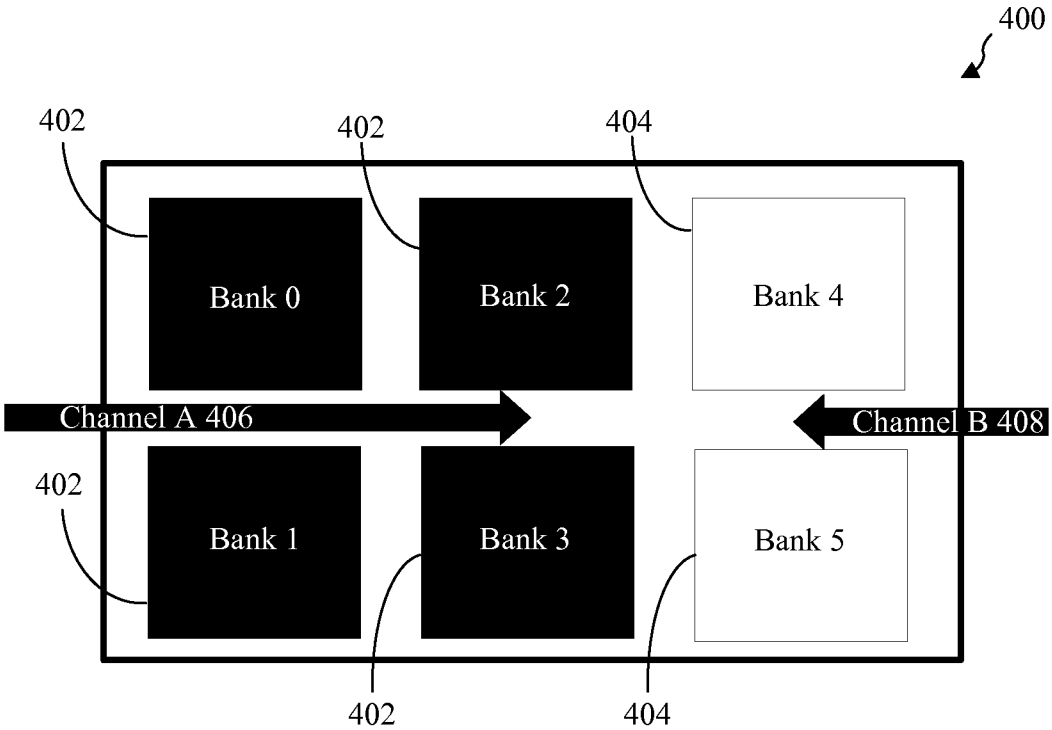
400
402
402
404
Bank 0
Bank 2
Bank 4
Channel A 406
Channel B 408
402
Bank 1
Bank 3
Bank 5
402
404

FIG. 4

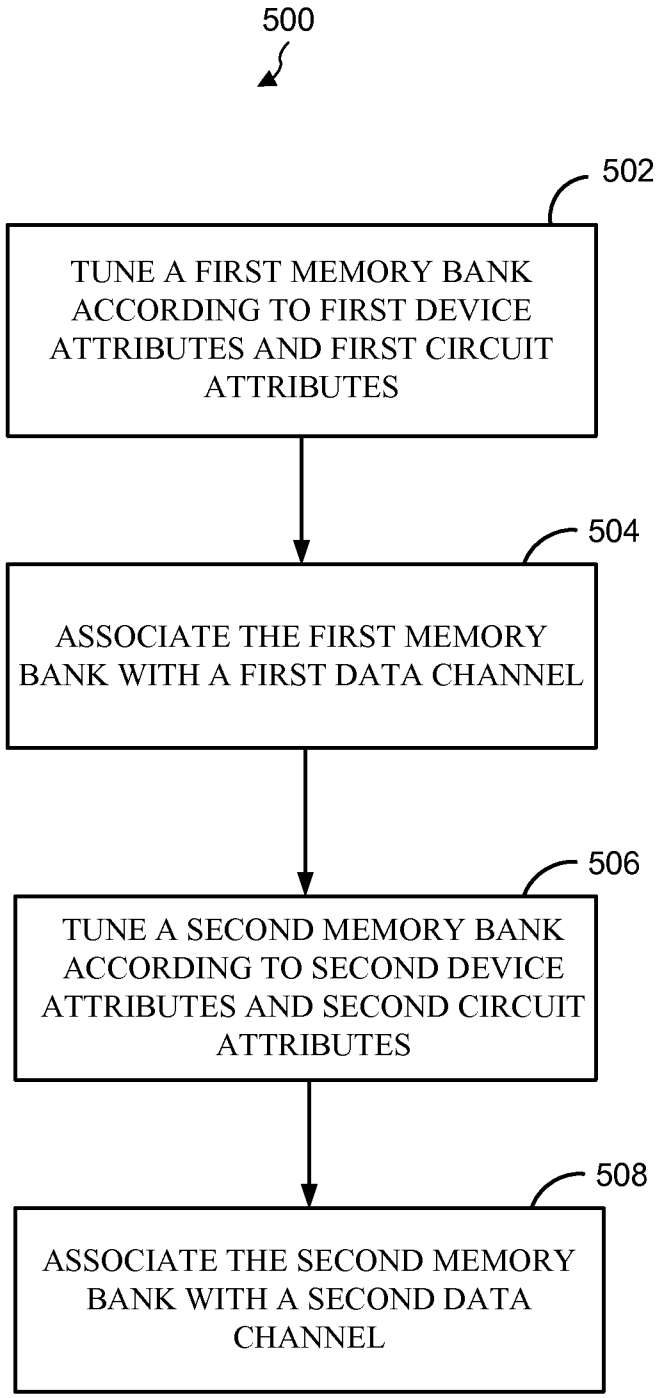
500
502
TUNE A FIRST MEMORY BANK ACCORDING TO FIRST DEVICE ATTRIBUTES AND FIRST CIRCUIT ATTRIBUTES
504
ASSOCIATE THE FIRST MEMORY BANK WITH A FIRST DATA CHANNEL
506
TUNE A SECOND MEMORY BANK ACCORDING TO SECOND DEVICE ATTRIBUTES AND SECOND CIRCUIT ATTRIBUTES
508
ASSOCIATE THE SECOND MEMORY BANK WITH A SECOND DATA CHANNEL

FIG. 5

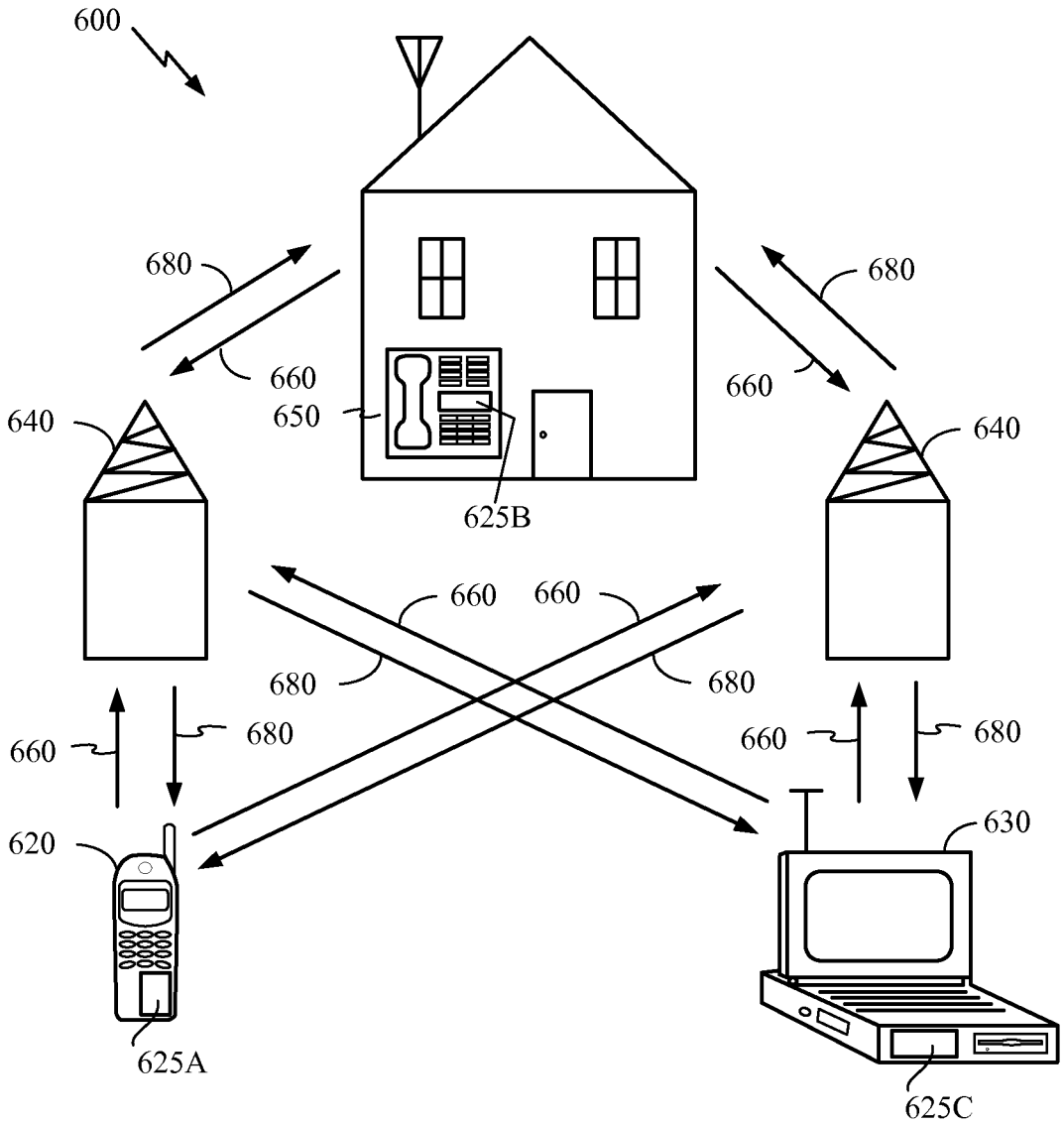
600
680
660
650
625B
680
660
640
640
660
660
680
680
660
680
660
680
620
630
625A
625C

FIG. 6

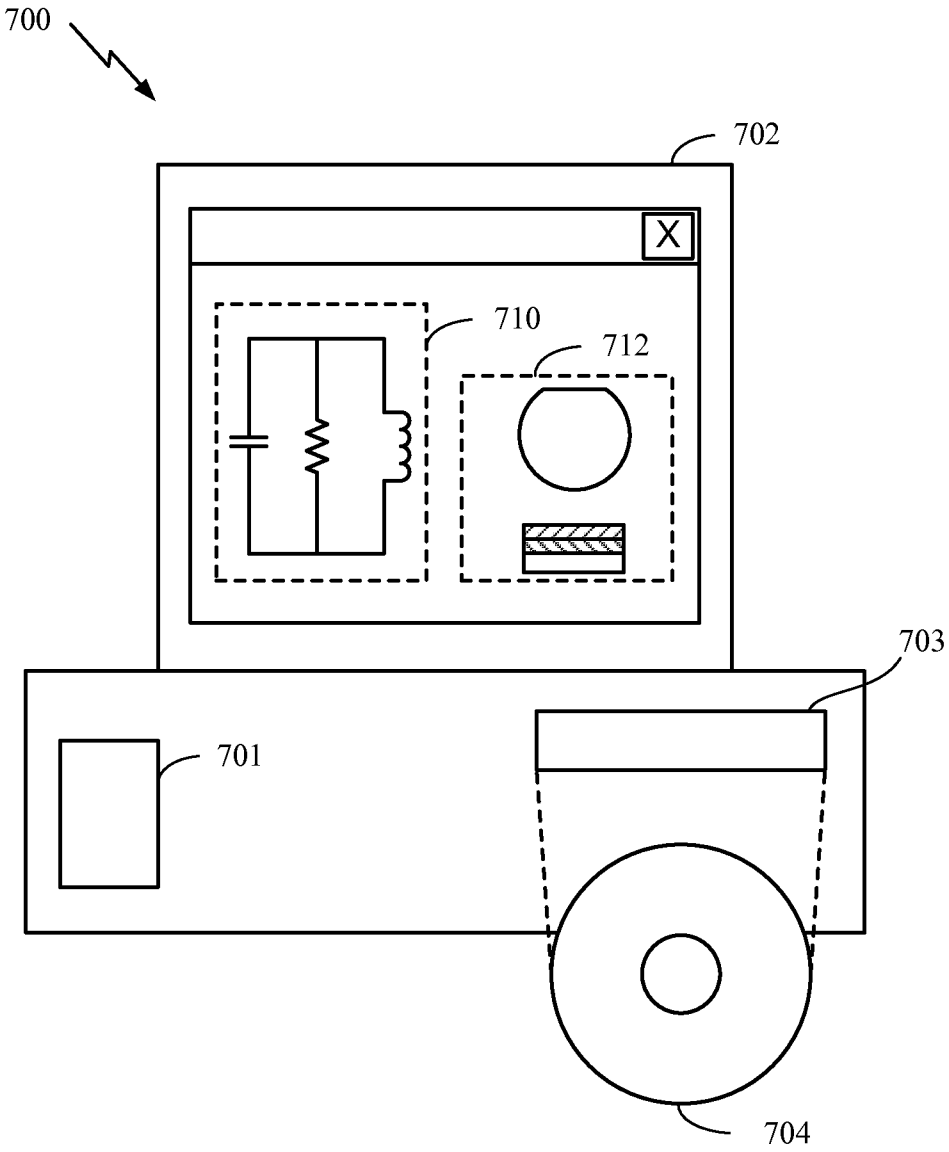

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/054002

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C29/02 G11C11/16
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/124105 A1 (WANG QI [KR] ET AL) 20 May 2010 (2010-05-20) paragraph [0105] - paragraph [0106]; claims 1,2,4,7; figures 5,21 -----	1,9,11, 13,16,21
X	US 2009/213644 A1 (PARKINSON WARD [US]) 27 August 2009 (2009-08-27) paragraph [0020] - paragraph [0031]; figures 1,2 -----	1,9,11, 13,16,21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 November 2013	13/11/2013

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wolff, Norbert

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/054002

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of Box II.2

Claims Nos.: 2-8, 10, 12, 14, 15, 17-20, 22(completely); 1, 9, 11, 13, 16, 21(partially)

Independent claim 1 defines a monolithic multi-channel resistive memory in nine (9) possible different configurations and constitutes thereby nine distinguished independent device claims. Dependent claim 2 defines four (4) attributes which may alternatively either alone or in a non-specified manner be combined as specification of a first one of the features of claim 1. Dependent claim 3 defines six (6) attributes which may alternatively either alone or in a non-specified manner be combined as specification of a second one of the features of claim 1. Dependent claims 4 - 8 define a plurality of further specifications of claim 1 which may alternatively either alone or in a non-specified manner be combined, which in case of claim 10 are ten (10) alternatives of broadly defined possible applications. The alternatives are not only numerous, but are also related to distinguished technical fields. The subject-matter of claims 9 - 22 corresponds in its broadness to the subject-matter of claims 1 - 9.

Notwithstanding the numerous configurations resulting from the possible alternatives claimed, core features of the independent claims, like bank or channel, and many of said alternatives are defined by terms that broad that their inherent technical features are not clear.

A meaningful search is therefore on basis of the claims not possible. The search was thus carried out on basis of what may legitimately be understood from the description par.[0006] - par.[0007] as considered by the applicant as the underlying concept of this application, namely a monolithic resistive memory comprising a first storage area and a second storage area, wherein said first storage area and said second storage are individually tuned to simultaneously serve as a working memory and as a non-volatile storage memory, respectively. The search report is accordingly valid for the independent claims only, and in particular the said subject-matter identified on basis of the description as the true idea of this application.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guidelines C-IV, 7.2), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/054002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010124105 A1	20-05-2010	NONE	
US 2009213644 A1	27-08-2009	CN 101965616 A	02-02-2011
		JP 2011513884 A	28-04-2011
		KR 20100117133 A	02-11-2010
		TW 200951957 A	16-12-2009
		US 2009213644 A1	27-08-2009
		WO 2009108279 A2	03-09-2009