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(54) Title: MULTIPLE CHANNEL MODULES AND BUS SYSTEMS

(57) Abstract: Various module structures are disclosed which may be used to implement modules having (1) to (N) channels. Bus systems may be formed by the interconnection of such modules.

MULTIPLE CHANNEL MODULES AND BUS SYSTEMS

TECHNICAL FIELD

The present invention is directed to bus systems. More particularly, the present invention is directed to a bus system including one or more modules implementing one or more communications channel(s).

BACKGROUND OF THE INVENTION

Conventional bus systems are typically implemented in single channel architectures. While conventional bus systems have been implemented using modules, the modules in such systems have merely been arranged in a serial relationship on a motherboard. For example, consider the bus system shown in Fig. 1. This bus system is characterized by a master 11 mounted on a motherboard 10. A number of connectors 13 are also mounted on motherboard 10. Each connector 13 is adapted to receive a module 14 comprising one or more integrated circuits 15. Thus, by means of a connector 13, a module 14 is mechanically mounted and electrically connected within the bus system.

One or more bus(es) 16 forms the communications channel between master 11 and a termination resistor 12. Bus 16 typically comprises a number of signals lines communicating control information, address information, and/or data. The signal lines forming bus 16 traverse the motherboard and/or the modules to electrically connect the integrated circuits 15 to master 11.

There are numerous problems associated with such conventional bus systems. For example, the serial arrangement of the connectors and associated modules creates a relatively lengthy communications channel. Since there are

many factors limiting the maximum practical length of a communications channel, channel length should, wherever reasonably possible, be minimized.

Conventional bus systems are also characterized by numerous electrical connection points between the connectors and the bus portions traversing the motherboard, between the modules and the connectors, and between the integrated circuits and the bus portion traversing the modules. Improperly matched electrical connections often produce impedance discontinuities that tend to degrade signal transmission characteristics on the bus. Accordingly, the number of impedance discontinuities associated with the bus connections should be minimized.

Such conventional bus systems present a very static architecture that may not lend itself to the efficient utilization of available space within a larger system. For example, a maximum, pre-set number of connectors is typically provided within the conventional bus system, regardless of the actual number of modules initially contemplated for the bus system. Upgrading the bus system to include additional modules requires that a sufficient number of connectors be provided up to the maximum length (or capacity) of the channel. Typically, empty connectors are filled with dummy modules until they are needed. Absent these spare connectors, upgrading the bus system to include an additional module would require that the motherboard be replaced.

The static architecture of the conventional bus system provides a "one size fits all" approach to larger systems incorporating the bus system. The serial arrangement of connectors and modules on a motherboard may produce an undesirably large footprint within the larger system. Further, this configuration does not lend itself to irregular or crowded spaces within the larger system.

Of further concern is the routing of clock signals. High-speed clock signals require special treatment, in that they are particularly susceptible to reflections based on discontinuities in the clock loop circuit.

SUMMARY OF THE INVENTION

The present invention provides, in certain implementations, modules and bus system architectures that reduce channel length and/or minimize bus connection discontinuities. Bus system architectures provided by the present invention may be flexibly configured according to an end user's requirements. Numerous possibilities exist for customized bus system configurations using the modules and interconnection schemes provided by the present invention. Multiple channels may be implemented on a single module and multiple modules may be connected to provide bus systems having relative small vertical profiles and/or horizontal footprints. The modules and/or bus system architectures may utilize various types of connectors, including for example finger connectors, edge connectors, and edge fingers. Any other element capable of providing an electrical connection (e.g., contacts, pins, leads, wire bonds, solder balls, etc.) may be substituted for the connectors of the modules, bus systems architectures and memory systems of the present invention. Also, a single connector may be substituted for a plurality of connectors. From the perspective of a module, a connector may allow signals to enter the module from elsewhere and/or may allow signals to exit the module. Certain connectors are referred to herein as "ingress" or "input" connectors while certain others are referred to herein as "egress" or "output" connectors. It is understood that input connectors, ingress connectors, output connectors and egress connectors may allow signals to travel in a first direction, a second direction or bidirectionally. In preferred implementations however, a data signal sent from a

memory controller to a memory device on a module will pass onto the module through an "input" or "ingress" connector and off of the module through an "output" or "egress" connector. Such data signal may be sampled by the memory device after passing onto the module.

In one aspect, the present invention provides a module formed from a printed circuit board (PCB) having primary first and second surfaces and having first and second ends, a plurality of integrated circuits (ICs) populating at least one of the first and second surfaces, a first set of edge fingers disposed at the first end and on the first surface of the PCB, a second set of edge fingers disposed at the first end and on the second surface of the PCB, a folded bus extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back at the second end, substantially traversing the length of the second surface and terminating at the second set of edge fingers, and a right-angle connector mounted on either the first or second surface at the first end, and adapted to mechanically receive and electrically connect another module.

In another aspect, the present invention provides a module adapted for use in a bus system and including; a printed circuit board (PCB) having primary first and second surfaces, and having first and second ends, a plurality of integrated circuits (ICs) populating at least one of the first and second surfaces, a set of edge fingers disposed at the first end of the PCB and on either the top or bottom surface of the PCB, a right-angle connector adapted to mechanically receive and electrically connect another module, the right-angle connector being mounted on either the bottom or top surface of the PCB opposite the surface on which the set of edge fingers are disposed and at the second end of the PCB, and a bus extending from the set of edge fingers, substantially traversing the length of the module, and terminating at the right-angle connector.

In yet another aspect, the present invention provides a module adapted to be connected within a plurality of bus system modules, the module including a printed circuit board (PCB) having first and second primary surfaces, first and second primary edges, and first and second ends, a plurality of integrated circuits (ICs) populating at least one of the primary first and second surfaces, a first set of edge fingers disposed on the first primary edge between first and second ends and on the first surface of the PCB, a second set of edge fingers disposed on the first primary edge between first and second ends and on the second surface of the PCB, wherein the first and second set of edge fingers are adapted to connect with an electrical connector associated with another module or a motherboard, a bus comprising a plurality of signal lines running from at least one of the first and second set of edge fingers to a flex tape connector connected at the second primary edge of the PCB between the first and second ends, and an electrical connector connected to the flex tape.

In still another aspect, the present invention provides a motherboard and a plurality of modules arranged from a first module to a last module, wherein the motherboard comprises a controller and a right-angle connector adapted to mechanically receive and electrically connect the first module, and wherein each one of the plurality of modules comprises a right-angle connector adapted to receive another one of the plurality of modules, such that, once connected via respective right-angle connectors, the motherboard and the plurality of modules are disposed in parallel one to another.

In a further aspect, the present invention provides a module formed from a printed circuit board (PCB) having first and second primary surfaces and having a first end, a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces, a first and second set of input finger connectors

disposed on at least one of the first and second primary surfaces proximate to the first end, a first and second set of output finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end, and a bus having a first channel extending from the first set of input finger connectors to the first set of output finger connectors and having a second channel extending from the second set of input finger connectors to the second set of output finger connectors, the bus connected to the plurality of ICs. In a preferred implementation, the first and second set of input finger connectors and the first and second set of output finger connectors are disposed on at least one of the first and second primary surfaces at the first end.

In yet another aspect, the present invention provides a module including a first printed circuit board (PCB) having first and second primary surfaces and having a first and second ends, one or more integrated circuits (ICs) populating at least one of the first and second primary surfaces, a set of finger connectors disposed proximate to the first end of the first PCB and on either the first or second primary surface of the first PCB, a conductive interconnect electrically connected to the first PCB proximate to the second end of the first PCB, and a bus extending from the set of finger connectors, substantially traversing the first PCB between the first and second ends and traversing the conductive interconnect. The conductive interconnect is adapted to receive a second PCB populated with one or more ICs. In one preferred implementation, the module further comprises a connector connecting the conductive interconnect to the first PCB. In another preferred implementation, the module further comprises a spacer disposed between the first and second PCB's. In yet another preferred implementation, the set of finger connectors are disposed at the first end of the first PCB, the spacer is attached to the first PCB at the second end of the first PCB, and

the conductive interconnect electrically connects the connector to the first PCB at the second end of the first PCB.

In accordance with still other aspects of the present invention, improved clock routing methods and arrangements suitable for use with modular components are provided.

For example, by an apparatus is provided, which includes a memory interface circuit, a clock signal generating circuit, and a plurality of memory circuits. The memory circuits are operatively coupled and arranged in an order on a plurality of memory modules, such that the memory module positioned at the beginning of the order is coupled to an output of the clock signal generating circuit and the memory interface circuit. The memory module that is positioned at the end of the order is unique in that it includes a clock signal terminating circuit connected to the last memory integrated circuit. With this configuration, a clock loop is formed by directly routing the clock signal from the output of the clock signal generating circuit through each of the memory modules in the order (without connecting to any of the intervening memory integrated circuits) to the memory integrated circuit positioned at the end of the order. Then, the clock signal is asserted on the previous memory modules by routing it back through the memory integrated circuits thereon, in reverse order to the memory integrated circuit positioned at the beginning of the order and from there to the memory interface circuit. To complete the clock loop, the clock signal is again asserted by routing it from the memory interface circuit back through the memory integrated circuits in order to the memory integrated circuit positioned at the end of the order. Finally, the clock signal is terminated at the clock signal terminating circuit on the memory module positioned at the end of the order.

By employing certain layouts, the memory module positioned at the end of the order can be moved between various positions depending upon the number/arrangement of memory integrated circuits. For example, a terminating memory module may be the only memory module in the order, at which point it can be operatively configured in a first slot of a multiple slot arrangement. However, should additional memory modules be required this terminating memory module can be moved to a slot further in the order to allow for the additional memory modules there between. Certain exemplary configurations of such arrangements are shown in the detailed description. These exemplary implementations have a three-slot order. However, those skilled in the art will recognize that orders of three or greater slots/memory modules can be supported by the clock routing schemes in accordance with the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the various methods and arrangements of the present invention may be had by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

Fig. 1 illustrates a conventional bus system architecture;

Fig. 2 illustrates a module adapted for use within the present invention;

Fig. 3A is an edge view of one implementation of a module according to the present invention;

Figs. 3B and 3C are respectively top and bottom views of a single channel module according to the implementation shown in Fig. 3A;

Fig. 3D illustrates a two channel module consistent with the implementation shown in Fig. 3A;

Fig. 4 illustrates a bus system formed by the interconnection of multiple modules according to the implementation shown in Figs. 3A through 3D;

Fig. 5A is an edge view of another implementation of a module according to the present invention;

Figs. 5B and 5C are respectively top and bottom views of a single channel module according to the implementation shown in Fig. 5A;

Fig. 5D illustrates a two channel module consistent with the implementation shown in Fig. 5A;

Fig. 6 illustrates a bus system formed by the interconnection of multiple modules according to the implementation shown in Figs. 5A through 5D;

Fig. 7A is an edge view of yet another implementation of a module according to the present invention;

Figs. 7B is a top view of the module of Fig. 7A further illustrating a two channel option to the module's implementation;

Fig. 8 illustrates a bus system formed by the interconnection of multiple modules according to the implementation shown in Figs. 7A and 7B;

Figs. 9A and 9B illustrate yet another implementation of a single channel module according to the present invention;

Fig. 9C illustrates a bus system formed by the interconnection of multiple modules according to the implementation shown in Figs. 9A and 9B;

Figs. 10A and 10B illustrate still another implementation of a two channel module according to the present invention;

Figs. 11A and 11B illustrate another implementation of a four channel module according to the present invention;

Figs. 11C and 11D illustrate stacked horizontal and vertical module configurations using the modules shown in Figs. 11A and 11B;

Figs. 12A illustrates yet another one channel implementation of the present invention;

Figs. 12B illustrates yet another two channel implementation of the present invention;

Figs. 12C illustrates yet another four channel implementation of the present invention;

Figs. 13A, 13B, 13C, and 13D illustrate various two channel bus systems implemented using variations on the modules described in Figs. 12a, 12B, and 12C;

Figs. 14A, 14B, and 14C further illustrate various two channel bus systems having a number of different termination options; and,

Figs. 15A and 15B illustrate implementations using a top edge mounted flexible connector.

Fig. 16 is a perspective diagram illustrating yet another implementation of a two channel module in accordance with the present invention.

Fig. 17 is a perspective diagram illustrating a bus system formed by the interconnection of multiple modules in accordance with the implementation illustrated in Fig. 16.

Fig. 18 is a perspective diagram illustrating yet another implementation of a four channel module in accordance with the present invention.

Fig. 19 is a perspective diagram illustrating an implementation of a module with a second printed circuit board (PCB) attached to a connector in accordance with the present invention.

Fig. 20 is a perspective diagram illustrating the implementation of Fig. 19 with the second PCB undergoing attachment to the connector in accordance with the present invention.

Fig. 21 is a plan view diagram illustrating an implementation of a two channel module in accordance with the present invention.

Fig. 22 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21.

Fig. 23 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21.

Fig. 24 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21.

Fig. 25 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21.

Fig. 26 is a plan view diagram illustrating an example of a bus system formed by the interconnection of multiple modules, including modules having multiple channels.

Fig. 27 is a plan view diagram of an example of a circuit board of a bus system according to an implementation of the invention.

Fig. 28 plan view diagram of an example of a circuit board of a bus system according to an implementation of the invention.

Fig. 29 is a plan view diagram of an implementation of a two channel module in accordance with the present invention.

Fig. 30 is a block diagram illustrating an example of a two-channel bus system in accordance with an implementation of the invention.

Fig. 31 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention.

Fig. 32 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention.

Fig. 33 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention.

Fig. 34 is a block diagram of an implementation of a two-channel module in accordance with the present invention.

Fig. 35 is a schematic diagram illustrating a technique for splitting a bus into multiple paths while maintaining controlled impedance in accordance with an implementation of the present invention.

Fig. 36 is a schematic diagram illustrating impedances for a bus, which does not split into multiple paths in accordance with an implementation of the present invention.

Fig. 37 is a schematic diagram illustrating impedances for a bus, which splits into multiple paths in accordance with an implementation of the present invention.

Fig. 38 illustrates a clock routing scheme, wherein a plurality of continuity modules are provided to complete the clock loop circuit to a configured memory module.

Figs 39A-B illustrate an improved clock routing scheme, in accordance with certain implementations of the present invention.

Fig. 40 illustrates another improved clock routing scheme, in accordance with certain further implementations of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An exemplary implementation of the module claimed in the related application is shown in Fig. 2. The module comprises a printed circuit board 20 and a plurality of integrated circuits (ICs) 23a-23f mounted thereon. At one end of PCB 20, a first set of edge fingers 21 are disposed on a first primary surface of the PCB and a second set of edge fingers 22 are disposed on an opposing second primary surface of the PCB. Edge fingers are a well known connection mechanism which allow the module to be mechanically secured within a connector (not shown) and electrically connected to a plurality of signal lines provided at the connector. As used herein, the phrase "disposed on" is understood to include locations on, under, and over the relevant surface or surfaces. Thus, for example, connectors, which may be described as finger connectors or edge fingers, located near an end would fall within the scope of connectors disposed on at least one of first and second primary surfaces proximate to that end. The phrase "printed circuit board" or the word "motherboard" is understood to include any type of dielectric body that may support conductors. In preferred implementations, the dielectric body is comprised of an epoxy, a fiberglass, a ceramic, or a polyamide, and may be rigid or flexible. In more preferred implementations, the dielectric body is comprised of a fiberglass. In particularly preferred implementations, the dielectric body is comprised of FR4, FR5 or BT resin.

A bus 25 internal to the module extends from the first set of edge fingers 21, traverses substantially the entire first primary surface of the PCB, folds back at the distant end of the PCB, traverses substantially the entire second primary surface of the PCB, and terminates at the second set of edge fingers 22. Bus 25 typically comprises a plurality of signal lines. The signal lines forming bus 25 may run on top the first and second surfaces of PCB 20. Alternatively, bus 25 may be formed

within the body of PCB 20. ICs 23a-23f are respectively connected to this plurality of signal lines.

As described in the related application, the foregoing module may be used in conjunction with a related connector to implement bus systems having improved signal transmission characteristics. Overall channel length and impedance discontinuities related to motherboard connections are reduced. Further, by means of the novel connector and associated module structure described in the related application, bus systems may be implemented in a number of ways. For example, modules may be vertically stacked one above the other, or horizontally racked one next top the other within a single connector.

The present invention allows additional flexibility in the design and implementation of bus systems. Whereas the former invention relies substantially upon the design of the multi-slot connector to flexibly implement bus systems, the present invention relies more on module design.

To this end, consider the module shown in Fig. 3A. Like the module shown in Fig. 2, the module of Fig. 3A comprises a printed circuit board 30 and a plurality of integrated circuits (ICs), here 23a-23d. Of note, the exemplary module of Fig. 2 mounts six (6) ICs connected to bus 25 which is formed within the body of PCB 20, whereas the example shown in Fig. 3A mounts only four (4) ICs connected to bus 25 running on top of the first and second primary surfaces of PCB 30. Within the context of the present invention, any reasonable number of ICs may be mounted on the module. ICs may populate one or both primary surfaces of the module. However, it is presently preferred to populate both primary surfaces of the module since this tends to further reduce channel length.

The module shown in Fig. 3A further comprises a right angle connector 32. Right angle connector 32 is mounted on PCB 30 and comprises a connection slot

33 adapted to receive another module. The "right-angle" nature of the connector nominally provides that slot 33 opens at a right angle to the surface upon which it is mounted. Such an arrangement allows modules to connected one to another in parallel planes. However, one or more modules might be configured with a multi-slot connector as described in the related application.

In the illustrated example of Fig. 3A, bus 25 extends from a first set of edge fingers 21 at a first end of PCB 30, substantially traverses the first primary surface 34, folds back at a second end of PCB 30, substantially traverses the second primary surface 35, and terminates at right angle connector 32. Thus, whereas the module bus portion shown in Fig. 2 extends from first edge fingers 21 to second set of edge fingers 22, the module bus portion shown in Fig. 3 extends from first set of edge fingers 21 to right angle connector 32. ICs 23a-23d respectively connect to the signal lines forming bus 25.

Right angle connector 32 may include one or more signal lines 36 connected back to edge fingers 21, and/or connected to a second set of edge fingers 22. Signal lines 36 might be used, for example, as ground connections.

Modules according to the present invention may implement one or more channels. The term "channel" is broadly defined to include one or more signal lines providing electrical continuity and capable of communicating information between two points. A signal line may be comprised of, for example, an electrically conductive trace or wire. Preferably, a channel provides a direct metallic connection between components coupled to the channel. In the following examples, one or more ICs are typically associated with a channel, and the channel communicates information from a master (a controlling device) to a slave (a responding device). However, one of ordinary skill in the art will understand that the ICs in the following examples may be replaced with connectors allowing

connection of an auxiliary channel. The ICs in the following examples may be memory devices, receivers, transceivers, logic devices, or other control devices. Figs. 3B and 3C shown top and bottom views of module illustrated in Fig. 3A.

Fig. 3D illustrates a module similar to the one illustrated in Figs. 3A-3C. However, the module shown in Fig. 3D implements two channels 37 and 38 on a single module. First channel 37 is associated with a first bus running from a first plurality of edge fingers 21a. Second channel 37 is associated with a second bus running from a second plurality of edge fingers 21b.

Whether the modules of the present invention implement one or more channels, they may be flexibly configured to form a bus system. Fig. 4 illustrates one such bus system. For clarity, Fig. 4 and subsequent illustrations of modules and bus systems omit labeling readily discernable elements such as the ICs and the PCB, which have been described above.

In Fig. 4, a motherboard 40 comprises a first right angle connector 50. The "motherboard" is nominally any printed circuit board having the first right angle connector, but typically comprises a master controlling signal transmissions on the bus. In the example, a first module 41a comprising right angle connector 51a is mechanically secured and electrically connected to motherboard 40 through right angle connector 50. Similarly, right angle connector 51a connects module 41b, and right angle connector 51b connects module 41c.

Such module-to-module connection may continue until a bus system of desired size and configuration is completed. Alternatively, at some point, the channel(s) defined between the master on motherboard 40 and the ICs on the last module will reach its maximum practical length. In either event, when the bus system is complete the signal lines of the bus are preferably terminated in a matched impedance. Signal line termination may be done in a set of termination

resistors on the last module, or by means of a special termination module 42 connected to the right angle connector 51c of the last module. By using termination module 42, the other modules need not include termination resistors.

Another implementation of the modules according to the present invention is shown in Figs. 5A-5D. The module shown in Fig. 5A does not make use of the folded bus structure described above. Rather, one or more sets of finger connectors (53a and 53b) are disposed on either the first or second primary surfaces of the module PCB. Alternatively, the first and second primary surfaces may each include one or more sets of edge fingers. The one or more bus(es) associated with these edge fingers substantially traverse the length of the module from one (1^{st}) end to another (2^{nd}) end connecting related ICs along the way. The one or more bus(es) then terminate at right angle connector 52.

Figs. 5B and 5C shown respectively top and bottom views of the module shown in Fig. 5A. Fig. 5D illustrates a two channel version of this module.

An exemplary bus system configured with the modules of Figs. 5A-5D is shown in Fig. 6. When used to configure a horizontally disposed bus system, the bus system of Fig. 6 may provide additional mechanical stability over the bus system illustrated in Fig. 4, since right angle connectors will be placed on both left and right "ends" of the bus system.

In the example shown in Fig. 6, the right angle connector on motherboard 60 receives first module 61a, which receives second module 61b. Module 62 is a base module incorporating termination impedance 63.

Yet another implementation of the modules according to the present invention is shown in Figs. 7A and 7B. This module does not use the right angle connectors illustrated in Figs. 4 through 6 inclusive. Rather, the one or more bus(es) terminate at one end of the module in a flex tape connector 70 coupled to an

electrical connector 72. Electrical connector 72 may be of conventional implementation. As before, one or more sets of edge fingers (21 and 22) are disposed at the other end of the module on the first primary surface and/or the second primary surface of the PCB. While the implementation shown in Fig. 7A lends itself to the same channel structures shown in Figs. 5B-5D, a further refinement of the channel structures is illustrated in Fig. 7B.

In Fig. 7B, a first sub-plurality of ICs 77 populate the first primary surface 71 of the PCB and a second sub-plurality of ICs 78 populate the second primary surface 73 of the PCB. A first bus originates at one set of edge fingers 21, laterally traverses the first plurality of ICs 77 and terminates at flex tape connector 70. A second bus originates at another set of edge fingers 22, laterally traverses the second plurality of ICs 78 and terminates at flex tape connector 70. In this manner, two channels are implemented which traverse opposing primary surfaces of the PCB in opposite directions. The width of the PCB can therefore be reduced. Compare the width of the module in Fig. 5D.

An exemplary memory system configured with the module of Fig. 7A is shown in Fig. 8. Within this system motherboard 80 comprises connector 83, which receives first module 81a, which in turn receives second module 81b in connector 84a. Connector 84b on second module 81b receives a base module 82 incorporating termination resistor 85. The combination of flex tape and connector allows a bus system comprising multiple modules to be implemented in a variety of forms.

In fact, single channel and multiple channel modules may be implemented in a number forms using conventional electrical connectors. Figs. 9A and 9B illustrate a single channel module which may be "stacked" or otherwise combined with similar modules to form a bus system having a reduced footprint and a

relatively short channel length. Within the module shown in Figs. 9A and 9B, the bus runs from a first connector 90 mounted on a first primary surface of the module, across the length of the module, and terminates in second connector 91 mounted on the second primary surface of the module.

Fig. 9C illustrates a bus system implemented with a number of these modules. A channel path 92 is indicated through the bus system, which enters the first module at its first connector and thereafter zigzags though the connected modules as shown until it reaches termination resistor 93. The modules used in the bus system of claim 9C are shown with a single bus traversing ICs populating only one primary surface of each respective PCB. As noted above, a plurality of buses may occupy the channel and one or more of the modules may include ICs on both primary surfaces.

An exemplary two channel module is illustrated in Figs. 10A and 10B. Here, a first channel path extends from a first connector 100 on the first primary surface of the PCB across the length of the PCB to a second connector 101 on the second primary surface of the PCB. A second channel path extends from a third connector 102 on the first primary surface of the PCB across the length of the PCB to a fourth connector 103 on the second primary surface of the PCB. Thus, first and second channels run counter-directional to one another.

The module of shown in Figs. 10A and 10B includes a single row of ICs. One of ordinary skill in the art will appreciate that a number of IC rows might be mounted on the module.

An exemplary four channel module is illustrated in Figs. 11A and 11B. The module includes four sets of (area array) connectors 111, 112, 113, and 114, each set having a first connector mounted on the first primary surface and a second connector mounted on the second primary surface of the PCB. As shown in Fig.

11B, a bus is formed between the first and second connector in each connector set. That is, each bus originates at a first edge of the PCB at a first connector, traverses the width of the module, folds back at a second edge of the PCB, and re-traverses the width of the module until it reaches the second connector in the connector set. The modules shown in Figs. 11A and 11B may be stacked in horizontal 115 and vertical 116 configurations on motherboard 10 as illustrated in Figs. 11C and 11D. The vertically stacked configuration 116 of Fig. 11D is connected through a flexible connector 114.

Each one of the foregoing examples makes use of a number of connectors. In addition to providing a connection path between respective buses, the structure of the connector may also be used to provides mechanical support for modules, which are stacked one above the other, or racked one next to the other in a bus system. While this feature is often desirable in the implementation of certain bus system architectures, the present invention has broader applications.

For example, the present invention may be adapted to take full advantage of conventional ribbon connectors and similar flexible connectors. By means of these connectors, modules forming a bus system need not be stacked or racked in close proximity one to another. Rather, module may be placed at greater distances one to another and may be mounted within a larger system at odd angles one to another. While separating modules will increase the channel length, there are many applications where reduced channel length will be happily traded away for ease and flexibility of implementation.

Before illustrating the use of flexible connectors, several modules structures will be described. Each of these module structures makes use of "finger connectors." The term "set of edge fingers" has been used above to described a class of electrical connectors characterized by a number of parallel electrical

contacts disposed near the edge of a PCB and adapted to "mate" with a corresponding connector slot. Edge fingers are generally pushed into the connector slot to make electrical bus connections and provide mechanical support to the module.

While often located near or at the edge of a PCB, a set of finger connectors need not be located on the edge of the PCB. A set of finger connectors, like a set of edge fingers, typically comprises a set of parallel electrical contacts. In the context of a bus, each electrical contact typically corresponds to a bus signal line. Ribbon connectors and other flexible parallel connectors are well adapted to interconnect such parallel electrical contact structures. However, a ribbon connector may be coupled to a set of finger connectors anywhere on the PCB, not just the edge. Thus, the term finger connector may denote an edge finger, but may also denote a more generic electrical contact.

Figs. 12A, 12B, and 12C illustrate a single channel module, a two channel module, and a four channel module respectively. The single channel module shown in Fig. 12A comprises a set of input finger connectors 120 and a set of output finger connectors 121. A bus substantially traverses the length of the module running from the set of input finger connectors 120 to the set of output finger connectors 121. Along the way, a plurality of ICs are connected to the bus. The multi-channel modules shown in Figs. 12B and 12C includes additional sets of input finger connections and additional sets of output finger connectors. The third and fourth buses on the module shown in Fig. 12C are disposed the other primary surface (i.e., the bottom surface in relation to the illustration).

In these examples, the respective sets of input finger connectors (120 and 120a-120d) as well as the output connector 121 in Fig. 12A are edge fingers. Accordingly, the modules may be coupled within a bus system by pushing the edge

fingers into a corresponding connector(s). The corresponding connector(s) provide the input signals to the module's bus(es). However, the sets of output finger connectors (121a-121d) on the modules shown in Figs. 12B and 12C are adapted to be connected with one or more ribbon or similar flexible connector(s).

Utilizing one or more of the modules illustrated above, bus systems having various configurations may be implemented using one or more flexible connector(s). Consider the examples shown in Figs. 13A, 13B, 13C, and 13D. Only two channel bus systems are illustrated, but from these examples one of ordinary skill in the art will readily discern how any reasonable number of "N" channels may be implemented in a bus system. Note that the various channels may be terminated in either a set of output finger connectors (Figs. 13A and 13C), and/or in an on-module set of termination resistors (Figs. 13B and 13D).

Figs. 14A, 14B, and 14C illustrate further examples of two channels bus systems having various connection and termination schemes. Like the ICs on these modules, more than one termination element may be mounted on either primary surface. See termination elements 140 and 141 in Figs. 14B and 14C.

In Figs. 15A and 15B, a flexible connector 154 is used to connect modules. However, unlike the former examples in which a flexible connector was attached to the modules via a lateral edge, the bus systems shown in Figs. 15A and 15B use a flexible connector attached via a top edge. In particular, adjacent modules 152a and 152b are respectively mounted on motherboard 159 via connectors 151a and 151b. Module 152a comprises ICs 153a and 153b arranged in a vertical column. Module 152b comprises ICS 153c and 153d, which are likewise arranged in a column.

In one further implementation of the present invention, ICs 153a, 153b, 153c, and 153d are connected in a channel extending from a edge lower fingers on

module 152a, through a bus portion on module 152a, through flexible connector 154, down through a bus portion on module 152b, to be terminated at a lower set of edge fingers on module 152b. Other channels may be similarly implemented.

The bus system shown in Fig. 15B illustrates another way in which a plurality of ICs may be effectively mounted on a module in one or more channels. Here, rather than arranging ICs in vertical columns, the ICs are arranged in rows. A single channel may begin at a centrally located set of edge fingers, make a right turn near the center of the module, extend laterally through the row of ICs, and then make another right turn into flexible connector 154. This path is reversed in the adjacent module. In this manner, first and second pluralities of ICs (156a 156b) may be arranged in rows on each one of the modules and connected as shown.

Fig. 16 is a perspective diagram illustrating yet another implementation of a two channel module in accordance with the present invention. Module 162 includes a first primary surface 1611 and a second primary surface 1612, which opposes the first primary surface 1611. Module 162 also has a first end 1613. Proximate to the first end 1613 are a first set of input finger connectors 167, a first set of output finger connectors 168, a second set of input finger connectors 169, and a second set of output finger connectors 1610. Alternatively, the first set of input finger connectors 167 and/or the second set of input finger connectors 169 may provide ingress elsewhere on module 162. Likewise, the first set of output finger connectors 168 and the second set of output finger connectors 1610 may provide egress elsewhere on module 162. The first set of input finger connectors 167, the first set of output finger connectors 168, the second set of input finger connectors 169, and the second set of output finger connectors 1610 are disposed on at least one of the first primary surface 1611 and the second primary surface 1612.

A plurality of integrated circuits (ICs) populate at least one of the first primary surface 1611 and the second primary surface 1612. The plurality of integrated circuits include ICs 163 and ICs 164. A bus is coupled to the plurality of ICs. The bus includes a first channel 165 extending from the first set of input finger connectors 167 to the first set of output finger connectors 168. The bus also includes a second channel 166 extending from the second set of input finger connectors 169 to the second set of output finger connectors 1610. The first channel 165 is coupled to ICs 163, and the second channel 166 is coupled to ICs 164. The first set of input finger connectors 167, the first set of output finger connectors 168, the second set of input finger connectors 169, and the second set of output finger connectors 1610 mate with a motherboard connector 161 mounted on a motherboard 160.

The first channel 165 and the second channel 166 may be implemented in a variety of configurations. For example, the first set of output finger connectors 168 may be disposed in a similar direction from the first set of input finger connectors 167 as the direction in which the second set of output finger connectors 1610 are disposed from the second set of input finger connectors 169. Consequently, the first channel 165 and the second channel 166 may be configured to convey signals in a generally similar direction across at least one of the first primary surface 1611 and the second primary surface 1612.

As another example, the first set of output finger connectors 168 may be disposed in an opposite direction from the first set of input finger connectors 167 of the direction in which the second set of output finger connectors 1610 are disposed from the second set of input finger connectors 169. Consequently, the first channel 165 and the second channel 166 may be configured to convey signals in generally

opposite directions across at least one of the first primary surface 1611 and the second primary surface 1612.

In one instance, the first set of input finger connectors 167 and the second set of input finger connectors 169 may be disposed near the middle of first end 1613, with the first set of output finger connectors 168 and the second set of output finger connectors 1610 disposed opposite one another along the periphery of first end 1613. In another instance, the first set of input finger connectors 167 and the second set of input finger connectors 169 may be disposed opposite one another along the periphery of first end 1613, with the first set of output finger connectors 168 and the second set of output finger connectors 1610 disposed near the middle of first end 1613. As noted previously, other locations and/or orientations of the connectors and the channels may be implemented.

By providing multiple channels, simultaneous independent accesses may be made to the plurality of ICs. For example, while a first element on the motherboard 160 is communicating with ICs 163 through first channel 165, a second element on the motherboard 160 may be communicating independently with ICs 164 through second channel 166. Thus, the effective bandwidth, or amount of information that may be transferred per unit time, of the bus is effectively increased through the use of multiple channels.

Fig. 17 is a perspective diagram illustrating a bus system formed by the interconnection of multiple modules in accordance with the implementation illustrated in Fig. 16. The bus system includes motherboard 170, motherboard connectors 171a, 171b, 171c, and 171d, and modules 172a, 172b, 172c, and 172d. Module 172a is coupled to motherboard 170 via motherboard connector 171a. Module 172b is coupled to motherboard 170 via motherboard connector 171b.

Module 172c is coupled to motherboard 170 via motherboard connector 171c. Module 172d is coupled to motherboard 170 via motherboard connector 171d.

Module 172a has a first primary surface 1711a, a second primary surface 1712a, and a first end 1713a. ICs 173a and ICs 174a populate at least one of the first primary surface 1711a and the second primary surface 1712a. Module 172b has a first primary surface 1711b, a second primary surface 1712b, and a first end 1713b. ICs 173b and ICs 174b populate at least one of the first primary surface 1711b and the second primary surface 1712b. Module 172c has a first primary surface 1711c, a second primary surface 1712c, and a first end 1713c. ICs 173c and ICs 174c populate at least one of the first primary surface 1711c and the second primary surface 1712c. Module 172d has a first primary surface 1711d, a second primary surface 1712d, and a first end 1713d. ICs 173d and ICs 174d populate at least one of the first primary surface 1711d and the second primary surface 1712d.

Motherboard 170 includes a bus coupled to motherboard connector 171a. The bus includes first channel 1714 and second channel 1715. The first channel 1714 is coupled through motherboard connector 171a and the first set of input finger connectors 177a to the first channel 175a the bus of module 172a. The first channel 175a of the bus of module 172a is coupled through the first set of output finger connectors 178a and through motherboard connector 171a to a bus segment on motherboard 170. The bus segment is coupled through motherboard connector 171b to the first channel 175b of the bus of module 172b. The first channel 175b of the bus of module 172b is coupled through output finger connectors 178b and through motherboard connector 171b to another bus segment of motherboard 170. This bus segment is coupled through motherboard connector 171c and through input finger connectors 177c to the first channel 175c of the bus of module 172c. The first channel 175c of the bus of module 172c is coupled through motherboard

connector 171c to another bus segment on motherboard 170. This bus segment is coupled through motherboard connector 171d to the first channel 175d of the bus of module 172d. Motherboard 170 includes a bus coupled to motherboard connector 171d. The bus includes a first channel 1716 and a second channel 1717. The first channel 175d of the bus of module 172d is coupled through output finger connectors 178d and through motherboard connector 171d to the first channel 1716 of the bus on motherboard 170.

The first channel 1716 of the bus on motherboard 170 may continue to additional circuitry on motherboard 170 or, optionally, may be terminated using bus termination 1718. Bus termination 1718 provides an impedance to match the characteristic impedance of the first channel 1716 of the bus and is coupled to a termination voltage VTERM. A bus termination may include any impedance element terminating a bus. Examples of bus terminations include, but are not limited to, passive bus terminations utilizing resistive elements, active bus terminations utilizing semiconductor devices, conductive stubs, etc. Preferred bus terminations include passive bus terminations utilizing resistive elements and active bus terminations utilizing semiconductor devices. The terms bus termination, termination, and terminator may be used interchangeably.

The second channel 1715 of the bus on motherboard 170 coupled to motherboard connector 171a is coupled to the second set of input finger connectors 179a to the second channel 176a of the bus of module 172a. The second channel 176a of the bus of module 172a is coupled through the second set of output finger connectors 1710a and through motherboard connector 171a to a bus segment on motherboard 170. The bus segment is coupled through motherboard connector 171b to the second channel 176b of the bus of module 172b. The second channel 176b of the bus of module 172b is coupled through motherboard connector 171b to

another bus segment of motherboard 170. This bus segment is coupled through motherboard connector 171c to the second channel 176c of the bus of module 172c. The second channel 176c of the bus of module 172c is coupled through motherboard connector 171c to another bus segment on motherboard 170. This bus segment is coupled through motherboard connector 171d to the second channel 176d of the bus of module 172d. The second channel 176d of the bus of module 172d is coupled through motherboard connector 171d to the second channel 1717 of the bus on motherboard 170.

The second channel 1717 of the bus of motherboard 170 may continue to additional circuitry on motherboard 170 or, optionally, may be terminated using bus termination 1719. Bus termination 1719 provides an impedance to match the characteristic impedance of the second channel 1717 of the bus and is coupled to a termination voltage VTERM.

The bus system may be implemented in a variety of configurations. For example, modules 172a, 172b, 172c, and 172d may be implemented according to any of the configurations of the module 162 described in reference to Fig. 16, including various combinations of different configurations among the modules. First and second channels of the modules may be configured to pass signals in similar or different directions, either within each module or between modules. For example, module 172a may be configured to pass signals for the first channel in the same direction as signals for the second channel, and module 172b may be configured to pass signals for the first channel in the same direction as signals for the second channel, but in an opposite direction of module 172a. As another example, module 172a may be configured to pass signals for the first channel and the second channel in opposite directions within module 172a, but with module 172b passing signals for the first channel in a direction opposite that of the first

channel of module 172a and passing signals for the second channel in a direction opposite that of the second channel of module 172a. Other variations of the same or different directions within or between modules may be implemented.

Fig. 18 is a perspective diagram illustrating yet another implementation of a four channel module in accordance with the present invention. As noted above in reference to Fig. 16, providing multiple channels allows multiple simultaneous independent accesses to be made to the ICs within a module, thereby increasing the effective bandwidth of the bus of a module. As the number of channels is increased, the effective bandwidth is also increased. While various numbers of channels may be provided, Fig. 18 illustrates, as an example, a module providing four channels.

Given that module 182 has a first primary surface 1811 and a second primary surface 1812, each of which can accommodate integrated circuits (ICs), it is beneficial to populate both first primary surface 1811 and second primary surface 1812 with ICs. For example, ICs 183 and ICs 184 populate the first primary surface 1811, while ICs 1814 and ICs 1815 populate the second primary surface 1812. The bus of module 182 includes a first channel 185, a second channel 186, a third channel 1816, and a fourth channel 1817. The first channel 185 is coupled to ICs 183. The second channel 186 is coupled to ICs 184. The third channel 1816 is coupled to ICs 1814. The fourth channel 1817 is coupled to ICs 1815.

Module 182 is removably coupled at its first end 1813 to motherboard connector 181, which is coupled to motherboard 180. Motherboard 180 conducts signals for the first channel 185 of the bus of module 182 through motherboard connector 181 to a first set of input finger connectors 187 of module 182 and signals for the second channel 186 of the bus of module 182 through motherboard connector 181 to a second set of input finger connectors 189 of module 182.

Motherboard 180 conducts signals for the third channel 1816 of the bus of module 182 through motherboard connector 181 to a third set of input finger connectors 1818 of module 182 and signals for the fourth channel 1817 of module 182 through motherboard connector 181 to a fourth set of input finger connectors 1820 of module 182.

The first channel 185 of the bus of module 182 is coupled through the first set of output finger connectors 188 and through motherboard connector 181 to motherboard 180. The second channel 186 of the bus of module 182 is coupled through the second set of output finger connectors 1810 and through motherboard connector 181 to motherboard 180. The third channel 1816 of the bus of module 182 is coupled through the third set of output finger connectors 1819 and through motherboard connector 181 to motherboard 180. The fourth channel 1817 of the bus of module 182 is coupled through the fourth set of output finger connectors 1821 and through motherboard connector 181 to motherboard 180.

Fig. 19 is a perspective diagram illustrating an implementation of a module with a second printed circuit board (PCB) attached to a connector in accordance with the present invention. The module is formed from PCB 192, which has a first primary surface 1911 and a second primary surface 1912. PCB 192 has a first end 1913 and a second end 1914. A set of finger connectors is disposed on at least one of the first primary surface 1911 and the second primary surface 1912 proximate to the first end 1913 of PCB 192. The set of finger connectors are removably coupled to motherboard connector 191, which is mounted on motherboard 190.

A plurality of integrated circuits (ICs) populate at least one of the first primary surface 1911 and the second primary surface 1912 of PCB 192. The plurality of ICs include ICs 193 and ICs 194. A conductive interconnect 195 is connected proximate to the second end 1914 of PCB 192. A conductive

interconnect 195 may include anything that provides an electrical connection. Examples of conductive interconnects 195 include, but are not limited to, flexible cables, flex circuits, and conductive elastomeric interconnects. A bus extends from the set of finger connectors, substantially traversing PCB 192 between the first end 1913 and the second end 1914. The bus further traverses the conductive interconnect 195 so as to couple the bus to a connector 197 that is coupled to the conductive interconnect 195. As an alternative, the conductive interconnect 195 may be connected elsewhere on PCB 192, and the bus may be routed elsewhere on PCB 192.

The connector 197 is adapted to receive a second PCB 198 populated with at least one IC, which may include ICs 199 and ICs 1910. The second PCB has a first primary surface 1917 and a second primary surface 1918. The second PCB 198 has a first end 1919 and a second end 1920. The second PCB 198 includes a second bus that couples the connector 197 to at least one of the ICs 199 or ICs 1910. The second bus extends beyond the ICs and is terminated with a bus termination, such as bus termination 1915 and/or bus termination 1916.

A spacer 196 is attached to one of the first primary surface 1911 of the PCB 192 or the second primary surface 1912 of the PCB 192 proximate to the second end 1914 of PCB 192. The spacer 196 is adapted to maintain a space between the connector 197 and the PCB 192. The space is sufficient to maintain clearance between PCB 192 and any ICs that may populate the first primary surface 1911 of the PCB 192 and the second PCB 198 and any ICs that may populate the second primary surface 1918 of the second PCB 198. For example, while any desired amount of space may be provided, the space may be in the range of zero to ten millimeters.

The connector 197 is preferably oriented to maintain the second PCB 198 substantially parallel to the PCB 192. To maintain second PCB 198 in engagement with connector 197 at the first end 1919 of the second PCB 198 and to allow its removal from connector 197, connector 197 may be provided with latches 1921. Latches 1921 may be manipulated to remove the second PCB 198 from engagement with connector 197.

The implementation of Fig. 19 may be practiced with multiple channels to allow multiple simultaneous independent accesses to be made to ICs 193, 194, 199, and 1910. For example, the bus may comprise a first channel and a second channel. The set of finger connectors that engage motherboard connector 191 may include a first set of finger connectors and a second set of finger connectors, with the first channel coupled to the first set of finger connectors and the second channel coupled to the second set of finger connectors. The first channel may be coupled to ICs 193, while the second channel may be coupled to ICs 194. Likewise, the first channel and the second channel may be coupled to the second PCB 198 via conductive interconnect 195 and connector 197. On the second PCB 198, ICs 199 may be coupled to the first channel, while ICs 1910 may be coupled to the second channel. The first channel of the second bus of the second PCB 198 may terminate at bus termination 1915, while the second channel of the second bus of the second PCB 198 may terminate at bus termination 1916. Thus, the benefits of providing multiple channels may be extended from PCB 192 to include the second PCB 198.

Fig. 20 is a perspective diagram illustrating the implementation of Fig. 19 with the second PCB undergoing attachment to the connector in accordance with the present invention. As can be seen, the second PCB 198 is oriented at an angle relative to PCB 192 rather than being parallel to PCB 192. Depending on the particular type of connector 197 used, the first end 1919 of second PCB 198 may be

engaged in connector 197, and second PCB 198 may be rotated about the first end 1919 until the second PCB 198 is engaged by latches 1921. Alternatively, other types of connectors 197 may be used that provide for translational motion rather than, or in addition to, rotational motion during engagement and/or disengagement.

Referring to Fig. 19 and Fig. 20, the second PCB 198 may be implemented so as to be receivable in motherboard connector 191. Thus, the second PCB 198 may be installed in motherboard connector 191 without PCB 192. The configuration may be upgraded by removing the second PCB 198 from motherboard connector 191, inserting the second PCB 198 into connector 197, and inserting PCB 192 into motherboard connector 191. Since bus termination 1915 and bus termination 1916 are provided on the second PCB 198, proper bus termination is provided regardless of whether the second PCB 198 is inserted into motherboard connector 191 or the second PCB 198 is inserted into connector 197 and PCB 192 is inserted into motherboard connector 191.

Without such an implementation, a PCB lacking ICs 199 and 1910 but having bus terminations 1915 and 1916 would be installed in connector 197 if the use of PCB 192 without second PCB 198 is desired. However, by installing the second PCB 198 directly in motherboard connector 191 (without PCB 192), the use of a separate PCB merely to provide proper bus termination can be avoided. By relying on bus termination 1915 and bus termination 1916 to maintain proper termination impedance, the installation in connector 197 of a PCB containing bus termination 1915 and bus termination 1916 but without ICs 199 and 1910 is rendered unnecessary.

Fig. 21 is a plan view diagram illustrating an implementation of a two channel module in accordance with the present invention. The module 2101 includes a first channel 2102 and a second channel 2103.

First channel signals 2112 are provided to first channel 2102 via first channel connector 2104. First channel 2102 couples first channel connector 2104, memory device 2106, memory device 2108, and terminator 2110.

Second channel signals 2113 are provided to second channel 2103 via second channel connector 2105. Second channel 2103 couples second channel connector 2105, memory device 2107, memory device 2109, and terminator 2111.

Fig. 22 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21. The bus system includes first module 2214, second module 2220, and third module 2201.

First channel signals 2226 are provided to first channel 2215 of first module 2214. First channel 2215 of first module 2214 couples memory devices 2216, 2217, 2218, and 2219 of first module 2214. First channel 2215 of first module 2214 is coupled to first channel 2203 of third module 2201 via interconnection 2213.

Second channel signals 2227 are provided to second channel 2221 of second module 2220. Second channel 2221 of second module 2220 couples memory devices 2222, 2223, 2224, and 2225 of second module 2220. Second channel 2221 of second module 2220 is coupled to second channel 2202 of third module 2201 via interconnection 2212.

Within third module 2201, first channel 2203 couples memory devices 2207 and 2209 and terminates at terminator 2211. Second channel 2202 couples memory devices 2206 and 2208 and terminates at terminator 2210.

The bus system of Fig. 22 provides a useful feature in that the bus system may be configured with only third module 2201, omitting first module 2214 and second module 2220. In such a configuration, first channel signals 2226 may be

applied to either first channel 2203 or second channel 2202 of third module 2201, and second channel signals 2227 may be applied to whichever first channel 2203 and second channel 2202 does not have first channel signals 2226 applied to it. The first channel signals 2226 and the second channel signals 2227 may be applied, for example, by way of circuit board conductors coupled to the third module 2201 or, for example, by using "filler" modules in place of first module 2214 and second module 2220. The "filler" modules need not contain memory devices, but provide electrical conductors to implement channels between ingress connectors and egress connectors, thereby allowing channel signals to pass through to third module 2201.

The bus system of Fig. 22 also allows additional modules to be added, thereby enabling expansion of the bus system. For example, additional modules similar to first module 2214 or second module 2220 may be added. Such additional modules may, for example, be interposed between first module 2214 and third module 2201 and/or between second module 2220 and third module 2201. If additional connector slots are provided to receive such additional modules and the additional modules are not needed, "filler" modules may be inserted in the connector slots to provide continuity or those connector slots may be bypassed.

Fig. 23 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21. The bus system includes first module 2314, second module 2320, and third module 2301.

First channel signals 2326 are provided to first channel 2315 of first module 2314. First channel 2315 of first module 2314 couples memory devices 2316, 2317, 2318, and 2319 of first module 2314. First channel 2315 of first module 2314 is coupled to first channel 2302 of third module 2301 via interconnection 2312.

Second channel signals 2327 are provided to second channel 2321 of second module 2320. Second channel 2321 of second module 2320 couples memory devices 2322, 2323, 2324, and 2325 of second module 2320. Second channel 2321 of second module 2320 is coupled to second channel 2303 of third module 2301 via interconnection 2313.

Within third module 2301, first channel 2302 couples memory devices 2306 and 2308 and terminates at terminator 2310. Second channel 2303 couples memory devices 2307 and 2309 and terminates at terminator 2311.

As described above in reference to Fig. 22, the bus system of Fig. 23 is also expandable and may also be reduced to a bus system comprising only third module 2301, without first module 2314 and second module 2320. Likewise, additional modules and/or "filler" modules may be used with the bus system of Fig. 23.

Fig. 24 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21. The bus system includes first module 2414, second module 2420, and third module 2401.

First channel signals 2426 are provided to first channel 2415 of first module 2414. First channel 2415 of first module 2414 couples memory devices 2416, 2417, 2418, and 2419 of first module 2414. First channel 2415 of first module 2414 is coupled to first channel 2403 of third module 2401 via interconnection 2413.

Second channel signals 2427 are provided to second channel 2421 of second module 2420. Second channel 2421 of second module 2420 couples memory devices 2422, 2423, 2424, and 2425 of second module 2420. Second channel 2421 of second module 2420 is coupled to second channel 2402 of third module 2401 via interconnection 2412.

Within third module 2401, first channel 2403 couples memory devices 2407 and 2409 and terminates at terminator 2411. Second channel 2402 couples memory devices 2406 and 2408 and terminates at terminator 2410.

As described above in reference to Fig. 22, the bus system of Fig. 24 is also expandable and may also be reduced to a bus system comprising only third module 2401, without first module 2414 and second module 2420. Likewise, additional modules and/or "filler" modules may be used with the bus system of Fig. 24.

Fig. 25 is a plan view diagram illustrating a bus system formed by the interconnection of multiple modules, including a module in accordance with the implementation illustrated in Fig. 21. The bus system includes a controller 2530, a first module 2514, a second module 2520, and a third module 2501. Controller 2530 includes a first channel 2528 and a second channel 2529. First channel 2528 of controller 2530 is coupled to first channel ingress connector 2531 of first module 2514 via interconnection 2526. Second channel 2529 of controller 2530 is coupled to second channel ingress connector 2533 of second module 2520 via interconnection 2527.

First channel ingress connector 2531 of first module 2514 is coupled to first channel 2515 of first module 2515. First channel 2515 couples memory devices 2516, 2517, 2518, and 2519 and continues to first channel egress connector 2532 of first module 2514. First channel egress connector 2532 of first module 2514 is coupled to first channel ingress connector 2504 of third module 2501 via interconnection 2512.

Second channel ingress connector 2527 of second module 2520 is coupled to second channel 2521 of second module 2520. Second channel 2521 of second module 2520 couples memory modules 2522, 2523, 2524, and 2525 and continues to second channel egress connector 2534 of second module 2520. Second channel

egress connector 2534 of second module 2520 is coupled to second channel ingress connector 2505 of third module 2501 via interconnection 2513.

Within third module 2501, first channel ingress connector 2504 is coupled to first channel 2502. First channel 2502 couples memory devices 2506 and 2508 and continues to terminator 2510. Second channel ingress connector 2505 of third module 2501 is coupled to second channel 2503. Second channel 2503 couples memory devices 2507 and 2509 and continues to terminator 2511.

As described above in reference to Fig. 22, the bus system of Fig. 25 is also expandable and may also be reduced to a bus system comprising only third module 2501, without first module 2514 and second module 2520. Likewise, additional modules and/or "filler" modules may be used with the bus system of Fig. 25.

Fig. 26 is a plan view diagram illustrating an example of a bus system formed by the interconnection of multiple modules, including modules having multiple channels. The bus system includes a controller 2630, a first module 2614, a second module 2620, and a third module 2601. Controller 2630, which may be referred to as a control circuit, provides control of operations within the first module 2614, the second module 2620, and/or the third module 2601. Controller 2630 includes a first channel 2628, a second channel 2662, a third channel 2663, and a fourth channel 2629. First channel 2628 of controller 2630 is coupled to first channel ingress connector 2631 of first module 2614 via interconnection 2626. Second channel 2662 of controller 2630 is coupled to second channel ingress connector 2647 of second module 2620 via interconnection 2664. Third channel 2663 of controller 2630 is coupled to third channel ingress connector 2656 of second module 2620 via interconnection 2665. Fourth channel 2629 of controller 2630 is coupled to fourth channel ingress connector 2633 of second module 2620 via interconnection 2627.

First channel ingress connector 2631 of first module 2614 is coupled to first channel 2615 of first module 2615. First channel 2615 couples memory devices 2616, 2617, 2618, and 2619 and continues to first channel egress connector 2632 of first module 2614. First channel egress connector 2632 of first module 2614 is coupled to first channel ingress connector 2604 of third module 2601 via interconnection 2612.

Second channel ingress connector 2647 of first module 2614 is coupled to second channel 2649 of first module 2614. Second channel 2649 of first module 2614 couples memory devices 2650, 2651, 2652, and 2653 and continues to second channel egress connector 2648 of first module 2614. Second channel egress connector 2648 of first module 2614 is coupled to second channel ingress connector 2638 of third module 2601 via interconnection 2666.

Third channel ingress connector 2656 of second module 2620 is coupled to third channel 2657 of second module 2620. Third channel 2657 couples memory devices 2658, 2659, 2660, and 2661 and continues to third channel egress connector 2655 of second module 2620. Third channel egress connector 2655 of second module 2620 is coupled to third channel ingress connector 2639 of third module 2601 via interconnection 2667.

Fourth channel ingress connector 2633 of second module 2620 is coupled to fourth channel 2621 of second module 2620. Fourth channel 2621 couples memory devices 2622, 2623, 2624, and 2625 and continues to fourth channel egress connector 2634 of second module 2620. Fourth channel egress connector 2634 of second module 2620 is coupled to fourth channel ingress connector 2605 of third module 2601 via interconnection 2613.

Within third module 2601, first channel ingress connector 2604 is coupled to first channel 2602. First channel 2602 couples memory devices 2606 and 2608 and

continues to terminator 2610. Second channel ingress connector 2638 of third module 2601 is coupled to second channel 2636. Second channel 2636 couples memory devices 2640 and 2642 and continues to terminator 2644. Third channel ingress connector 2639 is coupled to third channel 2637. Third channel 2637 couples memory devices 2641 and 2643 and continues to terminator 2645. Fourth channel ingress connector 2605 is coupled to fourth channel 2603. Fourth channel 2603 couples memory devices 2607 and 2609 and continues to terminator 2611.

As described above in reference to Fig. 22, the bus system of Fig. 26 is also expandable and may also be reduced to a bus system comprising only third module 2601, without first module 2614 and second module 2620. Likewise, additional modules and/or "filler" modules may be used with the bus system of Fig. 26.

Fig. 27 is a plan view diagram of an example of a circuit board of a bus system according to an implementation of the invention. The circuit board comprises a first module slot 2701, a second module slot 2702, and a third module slot 2703. First channel signals are provided to a first channel ingress connector 2704 of the first module slot 2701 via first channel bus 2710. Second channel signals are provided to a second channel ingress connector 2707 of the second module slot 2702 via second channel bus 2711. A first channel egress connector 2705 of the first module slot 2701 is coupled to a first channel ingress connector 2709 of the third module slot 2703 via first channel bus segment 2712. A second channel egress connector 2706 of the second module slot 2702 is coupled to a second channel ingress connector 2708 of the third module slot 2703 via second channel bus segment 2713. Since each of the module slots are configured such that a space without connectors exists between the ingress connector and the egress connector, one or more conductors of one or more of the channel buses may be routed along the circuit board between a module's ingress connector and that

module's egress connector. Thus, more that one channel may approach the module slots from the same direction. Alternatively, one or more conductors of one or more channel buses may be routed around the end of an ingress or egress connector of a module opposite that module's respective egress or ingress connector.

While separate ingress and egress connectors are identified in reference to Fig. 27, it should be understood that the ingress and egress connectors may be implemented as separate connectors or may be combined into a single connector structure accommodating a plurality of conductors. For example, if a connector having a connector pin array is used, one set of one or more connector pins may be used to implement an ingress connector and a second set of one or more connector pins may be used to implement an egress connector. Optionally, a portion of the connector shell that would otherwise accommodate additional connector pins may be left vacant to provide a region near the vacancies where conductors may be routed, for example on a printed circuit board.

A plurality of the conductors of a channel bus may be configured to be of equal length. Thus, signals introduced at one end of those conductors of the channel bus will arrive at the opposite end of those conductors at the same time. Even if topological constraints cause some conductors to be longer than others, additional length may be introduced into the shorter conductors, for example by using a zigzag or switchback routing pattern, to compensate and cause all conductors to have the same length.

The circuit board of Fig. 27 may be practiced as a motherboard, with first channel ingress connector 2704, first channel egress connector 2705, second channel egress connector 2706, second channel ingress connector 2707, second channel ingress connector 2708, and first channel ingress connector 2709 practiced as motherboard connectors. Also, a controller or control circuit such as controller

2630 of Fig. 26 may be coupled to first channel bus 2710 and/or second channel bus 2711.

Fig. 28 plan view diagram of an example of a circuit board of a bus system according to an implementation of the invention. This example of a circuit board shares the configuration illustrated in Fig. 28 and includes illustration of channel coupling internal to modules and termination of channels within a module. The circuit board comprises a first module slot 2801, a second module slot 2802, and a third module slot 2803. First channel signals are provided to a first channel ingress connector 2804 of the first module slot 2801 via a first conductor 2810 of a first channel bus. Second channel signals are provided to a second channel ingress connector 2807 of the second module slot 2802 via a first conductor 2811 of a second channel bus. The first conductor 2810 of the first channel bus is coupled to a first conductor 2812 of a first channel bus segment at first channel egress connector 2805 via a first conductor 2816 of a channel of a first module coupled to the first channel ingress connector 2804 and to the first channel egress connector 2805. The first channel egress connector 2805 of the first module slot 2801 is coupled to a first channel ingress connector 2809 of the third module slot 2803 via a first conductor 2812 of the first channel bus segment.

The first conductor 2811 of the second channel bus is coupled to a first conductor 2813 of a second channel bus segment at second channel egress connector 2806 via a first conductor 2817 of a channel of a second module coupled to the second channel ingress connector 2802 and the second channel egress connector 2806. The second channel egress connector 2806 of the second module slot 2802 is coupled to a second channel ingress connector 2808 of the third module slot 2803 via the first conductor 2813 of the second channel bus segment.

Within a third module coupled to first channel ingress connector 2809 of the third module slot 2803 and to the second channel ingress connector 2808 of the third module slot 2803, a first conductor 2818 of a first channel couples the first conductor 2812 of the first channel bus segment to a first terminator 2815. A first conductor 2819 of a second channel couples the first conductor 2813 of the second channel bus segment to a second terminator 2814. The first conductor 2818 of the first channel and the first conductor 2819 of the second channel may also be coupled to the same or different memory devices within the third module. While the bus system has been described with respect to a single conductor, it can be readily appreciated that the single conductor may be instantiated as many times as desired to provide as many conductors as desired.

Fig. 29 is a plan view diagram of an implementation of a two channel module in accordance with the present invention. The module 2901 includes a first channel ingress connector 2904, a second channel ingress connector 2905, memory devices 2906, 2907, 2908, and 2909, and terminators 2910 and 2911. A first channel 2902 couples the first channel ingress connector 2904 to memory 2906 and 2908 and to terminator 2910. A second channel 2903 couples the second channel ingress connector 2905 to memory devices 2907 and 2909 and to terminator 2911. The first channel 2902 and the second channel 2903 each comprise a plurality of conductors. The length of each of the conductors that a channel comprises are preferably of equal length. The length between the ingress connector and the terminator is preferably equal among conductors of a channel. The length between the ingress connector and a memory device coupled to the channel is preferably equal among conductors of the channel. Techniques such as those described above may be used to adjust the lengths of the conductors to assure equal length.

Fig. 30 is a block diagram illustrating an example of a two-channel bus system in accordance with an implementation of the invention. The bus system comprises a first module 3001 and a second module 3002. The first module comprises memory devices 3003 and 3004 and terminators 3010 and 3014. The second module comprises memory devices 3005 and 3006 and terminators 3009 and 3013. A first data channel 3007 is coupled to a first ingress connector on the first module 3001, to a first memory device 3003 on the first module 3001, and to a first egress connector on the first module 3001. From there, the first data channel 3007 is coupled to a first ingress connector on the second module 3002, to a first memory device 3005 on the second module 3002, and to a terminator 3009 on the second module 3002. A second data channel 3008 is coupled to a second ingress connector on the second module 3002, to a second memory device 3006 on the second module 3002, and to a second egress connector on the second module 3002. From there, the second data channel 3008 is coupled to a second ingress connector on the first module 3001, to a second memory device 3004 on the first module 3001, and to a terminator 3010 on the first module 3001.

A first request channel 3012 is coupled to an ingress connector on first module 3001, to memory devices 3004 and 3003 on the first module 3001, and to terminator 3014 on the first module 3001. A second request channel 3011 is coupled to an ingress connector on second module 3002, to memory devices 3005 and 3006 on the second module 3002, and to terminator 3013.

Since the first module 3001 and the second module 3002 have an identical internal configuration (although they are depicted as reversed relative to one another in Fig. 30), a multiple module bus system may be constructed with a minimum number of distinct components. One or more additional modules comprising ingress connectors, memory devices, and egress connectors for either or

both channels may be interposed between first module 3001 and second module 3002 to allow expansion of the bus system.

As can be seen from Fig. 30, in this example, a module provides ingress and egress for one channel and ingress and termination for another channel. The module passes one channel through to another module while terminating the other channel. By using two such modules, as shown, one channel can pass through a first module and terminate on a second module while another channel can pass through the second module and terminate on the first module.

The bus system of Fig. 30 is expandable. Additional modules and/or "filler" modules may be added, for example, between first module 3001 and second module 3002. Such additional modules and/or "filler" modules need not provide terminators for the data channels, but may receive a data channel at an ingress connector, couple the data channel to one or more memory devices, and provide the data channel to an egress connector. Alternatively, such modules may provide termination. Additional request channels may be provided to the additional modules, or the existing request channels may be shared with the additional modules, for example, through the use of one or more splitters. As another alternative, either of first module 3001 and second module 3002 may be omitted and replace with a similar module lacking memory devices. Such a module provides continuity and termination, but saves the cost of the memory devices for systems in which such memory devices are not needed.

Fig. 31 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention. The bus system comprises a first module 3101 and a second module 3102. The first module comprises memory devices 3103, 3115, 3104, and 3116 and terminators 3110, 3122, and 3114. The second module comprises memory devices 3105, 3117, 3106,

and 3118 and terminators 3109, 3121, and 3113. A first data channel 3107 is coupled to an ingress connector on the first module 3101, to a memory device 3103 on the first module 3101, to a memory device 3115 on the first module 3101, and to an egress connector on the first module 3101. From there, the first data channel 3107 is coupled to an ingress connector on the second module 3102, to a memory device 3105 on the second module 3102, to a memory device 3117 on the second module 3102, and to a terminator 3109 on the second module 3102.

A second data channel 3119 is coupled to an ingress connector on the first module, to a memory device 3103 on the first module 3101, to a memory device 3115 on the first module 3101, and to an egress connector on the first module 3101. From there, the second data channel is coupled to an ingress connector on the second module 3102, to a memory device 3105 on the second module 3102, to a memory device 3117 on the second module 3102, and to terminator 3121 on the second module 3102.

A third data channel 3108 is coupled to an ingress connector on the second module 3102, to a memory device 3106 on the second module 3102, to a memory device 3118 on the second module 3102, and to an egress connector on the second module 3102. From there, the third data channel 3108 is coupled to an ingress connector on the first module 3101, to a memory device 3104 on the first module 3101, to a memory device 3116 on the first module 3101, and to a terminator 3110 on the first module 3101.

A fourth data channel 3120 is coupled to an ingress connector on the second module 3102, to a memory device 3106 on the second module 3102, to a memory device 3118 on the second module 3102, and to an egress connector on the second module 3102. From there, the fourth data channel 3120 is coupled to an ingress connector on the first module 3101, to a memory device 3104 on the first module

3101, to a memory device 3116 on the first module 3101, and to a terminator 3122 on the first module 3101.

A first request channel 3112 is coupled to an ingress connector on first module 3101, to memory devices 3104, 3116, 3103, and 3115 on the first module 3101, and to terminator 3114 on the first module 3101. A second request channel 3111 is coupled to an ingress connector on second module 3102, to memory devices 3105, 3117, 3106, and 3118 on the second module 3102, and to terminator 3113.

Since the first module 3101 and the second module 3102 have an identical internal configuration (although they are depicted as reversed relative to one another in Fig. 31), a multiple module bus system may be constructed with a minimum number of distinct components. One or more additional modules comprising ingress connectors, memory devices, and egress connectors for either or both channels may be interposed between first module 3101 and second module 3102 to allow expansion of the bus system.

The bus system of Fig. 31 is expandable. Additional modules and/or "filler" modules may be added, for example, between first module 3101 and second module 3102. Such additional modules and/or "filler" modules need not provide terminators for the data channels, but may receive a data channel at an ingress connector, couple the data channel to one or more memory devices, and provide the data channel to an egress connector. Alternatively, such modules may provide termination. Additional request channels may be provided to the additional modules, or the existing request channels may be shared with the additional modules, for example, through the use of one or more splitters.

It should be noted that other variations of Fig. 31 are possible. For example, the numbers of ingress connectors, memory devices, channels, egress connectors, and terminations may be varied.

Fig. 32 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention. The bus system comprises a first module 3201 and a second module 3202. The first module comprises memory devices 3203, 3215, 3204, and 3216 and terminators 3210, 3222, and 3214. The second module comprises memory devices 3205, 3217, 3206, and 3218 and terminators 3209, 3221, and 3213. A first data channel 3207 is coupled to an ingress connector on the first module 3201, to a memory device 3203 on the first module 3201, and to an egress connector on the first module 3201. From there, the first data channel 3207 is coupled to an ingress connector on the second module 3202, to a memory device 3205 on the second module 3202, and to a terminator 3209 on the second module 3202.

A second data channel 3219 is coupled to an ingress connector on the first module, to a memory device 3215 on the first module 3201, and to an egress connector on the first module 3201. From there, the second data channel is coupled to an ingress connector on the second module 3202, to a memory device 3217 on the second module 3202, and to terminator 3221 on the second module 3202.

A third data channel 3208 is coupled to an ingress connector on the second module 3202, to a memory device 3206 on the second module 3202, and to an egress connector on the second module 3202. From there, the third data channel 3208 is coupled to an ingress connector on the first module 3201, to a memory device 3204 on the first module 3201, and to a terminator 3210 on the first module 3201.

A fourth data channel 3220 is coupled to an ingress connector on the second module 3202, to a memory device 3218 on the second module 3202, and to an egress connector on the second module 3202. From there, the fourth data channel 3220 is coupled to an ingress connector on the first module 3201, to a memory device 3216 on the first module 3201, and to a terminator 3222 on the first module 3201.

A first request channel 3212 is coupled to an ingress connector on first module 3201, to memory devices 3204, 3216, 3203, and 3215 on the first module 3201, and to terminator 3214 on the first module 3201. A second request channel 3211 is coupled to an ingress connector on second module 3202, to memory devices 3205, 3217, 3206, and 3218 on the second module 3202, and to terminator 3213.

Since the first module 3201 and the second module 3202 have an identical internal configuration (although they are depicted as reversed relative to one another in Fig. 32), a multiple module bus system may be constructed with a minimum number of distinct components. One or more additional modules comprising ingress connectors, memory devices, and egress connectors for either or both channels may be interposed between first module 3201 and second module 3202 to allow expansion of the bus system.

The bus system of Fig. 32 is expandable. Additional modules and/or "filler" modules may be added, for example, between first module 3201 and second module 3202. Such additional modules and/or "filler" modules need not provide terminators for the data channels, but may receive a data channel at an ingress connector, couple the data channel to one or more memory devices, and provide the data channel to an egress connector. Alternatively, such modules may provide termination. Additional request channels may be provided to the additional

modules, or the existing request channels may be shared with the additional modules, for example, through the use of one or more splitters.

Fig. 33 is a block diagram illustrating an example of a four-channel bus system in accordance with an implementation of the invention. The bus system comprises a first module 3301 and a second module 3302. The first module comprises memory devices 3303, 3315, 3323, 3327, 3304, 3316, 3326, and 3330 and terminators 3310, 3322, 3314, and 3333. The second module comprises memory devices 3305, 3317, 3325, 3329, 3306, 3318, 3324, and 3328 and terminators 3309, 3321, 3313,and 3334. A first data channel 3307 is coupled to an ingress connector on the first module 3301, to a memory device 3303 on the first module 3301, to a memory device 3315 on the first module 3301, and to an egress connector on the first module 3301. From there, the first data channel 3307 is coupled to an ingress connector on the second module 3302, to a memory device 3305 on the second module 3302, to a memory device 3317 on the second module 3302, and to a terminator 3309 on the second module 3302.

A second data channel 3319 is coupled to an ingress connector on the first module, to a memory device 3323 on the first module 3301, to a memory device 3327 on the first module 3301, and to an egress connector on the first module 3301. From there, the second data channel is coupled to an ingress connector on the second module 3302, to a memory device 3325 on the second module 3302, to a memory device 3329 on the second module 3302, and to terminator 3321 on the second module 3302.

A third data channel 3308 is coupled to an ingress connector on the second module 3302, to a memory device 3306 on the second module 3302, to a memory device 3318 on the second module 3302, and to an egress connector on the second module 3302. From there, the third data channel 3308 is coupled to an ingress

connector on the first module 3301, to a memory device 3304 on the first module 3301, to a memory device 3316 on the first module 3301, and to a terminator 3310 on the first module 3301.

A fourth data channel 3320 is coupled to an ingress connector on the second module 3302, to a memory device 3324 on the second module 3302, to a memory device 3328 on the second module 3302, and to an egress connector on the second module 3302. From there, the fourth data channel 3320 is coupled to an ingress connector on the first module 3301, to a memory device 3326 on the first module 3301, to a memory device 3330 on the first module 3301, and to a terminator 3322 on the first module 3301.

A first request channel 3335 is coupled to an ingress connector on first module 3301. The first request channel is split into a first branch 3311 and a second branch 3331 using a splitter. The splitter preferably couples the first request channel 3335 to the first branch 3311 and to the second branch 3331 while maintaining continuity of impedance. The first branch 3311 is coupled to memory devices 3304, 3316, 3303, and 3315 on the first module 3301, and to terminator 3314 on the first module 3301. The second branch 3331 is coupled to the memory devices 3326, 3330, 3323, and 3327 on the first module 330, and to terminator 3333 on the first module 3301. A second request channel 3336 is split into a first branch 3312 and a second branch 3332 using a splitter. The splitter preferably couples the second request channel 3336 to the first branch 3312 and to the second branch 3332 while maintaining continuity of impedance. The first branch 3312 is coupled to memory devices 3305, 3317, 3306, and 3318 on the second module 3302, and to terminator 3313. The second branch 3332 is coupled to memory devices 3325, 3329, 3324, and 3328, and to terminator 3334.

The first request channel 3335 and the second request channel 3336 may be implemented in a variety of configurations. For example, instead of splitting a request channel into two branches, a request channel may be coupled to all of the memory devices on a module and terminated with a single terminator. Thus, the splitter and one terminator may be obviated. Also, a plurality of request channels may be coupled to each module, with termination provided for each request channel.

Since the first module 3301 and the second module 3302 have an identical internal configuration (although they are depicted as reversed relative to one another in Fig. 33), a multiple module bus system may be constructed with a minimum number of distinct components. One or more additional modules comprising ingress connectors, memory devices, and egress connectors for either or both channels may be interposed between first module 3301 and second module 3302 to allow expansion of the bus system.

The bus system of Fig. 33 is expandable. Additional modules and/or "filler" modules may be added, for example, between first module 3301 and second module 3302. Such additional modules and/or "filler" modules need not provide terminators for the data channels, but may receive a data channel at an ingress connector, couple the data channel to one or more memory devices, and provide the data channel to an egress connector. Additional request channels may be provided to the additional modules, or the existing request channels may be shared with the additional modules, for example, through the use of one or more splitters.

Fig. 34 is a block diagram of an implementation of a two-channel module in accordance with the present invention. This implementation provides buses that split into multiple paths while maintaining controlled impedance. For example, while other impedances may be used, a 28 ohm bus may be split into two 56 ohm

paths, which may optionally be merged into another 28 ohm bus. The two-channel module 3401 includes an RQ request bus 3402 that splits into paths 3440 and 3441. Path 3440 is coupled to memory devices 3412, 3414, 3416, and 3418, and terminates in resistor 3428 coupled to ground 3429. Path 3441 is coupled to memory devices 3420, 3422, 3424, and 3426, and terminates in resistor 3434 coupled to ground 3435. CFM(1) clock bus 3404 splits into paths 3444 and 3445. Path 3444 is coupled to memory devices 3412, 3414, 3416, and 3418 and terminates in resistor 3430 coupled to ground 3431. Path 3445 is coupled to memory devices 3420, 3422, 3424, and 3426 and terminates in resistor 3436 coupled to ground 3437. CTM(1) clock bus 3406 splits into paths 3448 and 3449. Path 3448 is coupled to memory devices 3412, 3414, 3416, and 3418. Path 3449 is coupled to memory devices 3420, 3422, 3424, and 3426. Paths 3448 and 3449 are combined into bus 3452, which may exit module 3401 and be coupled to other components, for example, other modules. Data signals are applied to DQ(A) data bus 3408, which enters module 3401 and is coupled to memory devices 3412, 3414, 3416, and 3418 and terminates in resistor 3432 coupled to ground 3433. Data signals are applied to DQ(B) data bus 3410, which is applied to module 3401 and coupled to memory devices 3420, 3422, 3424, and 3426 and terminated by resistor 3438 coupled to ground 3439.

RQ request bus 3403 splits into paths 3442 and 3443. Path 3442 is coupled to memory devices 3413, 3415, 3417, and 3419. Path 3443 is coupled to memory devices 3421, 3423, 3425, and 3427. Paths 3442 and 3443 are merged to provide bus 3453, which may exit module 3401 and, for example, be coupled to other components such as other modules. CFM(2) clock bus 3405 enters module 3401 and splits into paths 3446 and 3447. Path 3446 is coupled to memory devices 3413, 3415, 3417, and 3419. Path 3447 is coupled to memory devices 3421, 3423,

3425, and 3427. Paths 3446 and 3447 are merged to form bus 3454, which may exit module 3401 and be coupled to other components, for example, other modules. CTM(2) clock bus 3407 enters module 3401 and splits into paths 3450 and 3451. Path 3450 is coupled to memory devices 3413, 3415, 3417, and 3419. Path 3451 is coupled to memory devices 3421, 3423, 3425, and 3427. Paths 3450 and 3451 are merged to form bus 3455, which may exit module 3401 and be coupled to other components, for example, other modules. Data signals are applied to DQ(C) data bus 3409, which enters module 3401 and is coupled to memory devices 3413, 3415, 3417, and 3419. DQ(C) data bus 3409 may also exit module 3401 and be coupled to other components, for example, other modules. Data signals are applied to DQ(D) data bus 3411, which enters module 3401 and is coupled to memory devices 3421, 3423, 3425, and 3427. DQ(D) data bus 3411 may exit module 3401 and be coupled to other components, for example, other modules.

While various bus terminations are described as resistors coupled to ground, it is understood that other bus terminations may be used. For example, resistors may be coupled to any termination voltage, such as any DC voltage or any voltage that exhibits the properties of such a DC voltage when used for termination of a bus. As additional examples, other types of passive terminations, active terminations, and/or stub terminations may be used. Terminations may be implemented within an integrated circuit, separately from an integrated circuit, and, in some cases, terminations may be omitted. For example, terminations may be omitted when a bus is configured so as to prevent any reflections from exceeding a specified amplitude or when any reflections that occur will not impair one or more bus performance parameters, such as a data rate or an error rate, to a meaningful degree.

Thus, in accordance with an implementation of the invention, a module may be formed from a printed circuit board (PCB). The module comprises a first set of integrated circuits (ICs), a second set of ICs, a first input connector, and a first ingress bus. The first set of ICs is mounted on the PCB. The second set of ICs is mounted on the PCB. The first input connector is disposed on the PCB. The first ingress bus is coupled to the first input connector. The first ingress bus is split into a first path and a second path. The first path is coupled to the first set of ICs, and the second path is coupled to the second set of ICs. The first ingress bus has a first characteristic impedance, and the first path and the second path have a combined effective impedance substantially equal to the first characteristic impedance. By being substantially equal, the impedances prevent interference from impedance discontinuities, for example, interference caused by reflections. Such interference is effectively prevented if performance parameters, for example, a data rate or an error rate, are not adversely affected by the interference to a meaningful degree. In preferred implementations, the impedances are substantially equal if the difference between the first characteristic impedance and the combined effective impedance does not exceed 15%. In more preferred implementations, the difference does not exceed 10%.

Optionally, the first path is coupled to a first terminator, and the second path is coupled to a second terminator. As another option, the module further comprises a first output connector disposed on the PCB and a first egress bus coupled to the first output connector. The first path and the second path are merged into the first egress bus. The first egress bus has a second characteristic impedance substantially equal to the first characteristic impedance. By being substantially equal, the impedances prevent interference from impedance discontinuities, for example, interference caused by reflections.

Fig. 35 is a schematic diagram illustrating a technique for splitting a bus into multiple paths while maintaining controlled impedance in accordance with an implementation of the present invention. An ingress bus is represented by transmission line 3501. The ingress bus splits into a plurality of paths represented by transmission lines 3502, 3503, and 3504. The plurality of paths are merged to form an egress bus represented by transmission line 3505. Signals are applied to a first end of transmission line 3501. A second end of transmission line 3501 is coupled to a first end of each of transmission lines 3502, 3503, and 3504 at node 3506. A second end of each of transmission lines 3502, 3503, and 3504 is coupled to a first end of transmission line 3505 at node 3507. A second end of transmission line 3505 provides an output for signals.

Transmission lines 3501 and 3505 have a characteristic impedance of Z0. Each of transmission lines 3502, 3503, and 3504 have a characteristic impedance N x Z0, where N equals the number of transmission lines 3502, 3503, and 3504 representing the plurality of paths. The parallel combination of the plurality of paths has an effective impedance of the characteristic impedance of the transmission lines representing each of the paths divided by the number of paths. Expressed mathematically, the effective impedance for the parallel combination of paths is N x Z0 divided by N, which equals Z0, the impedance of transmission lines 3501 and 3505. By configuring the paths such that each path has a characteristic impedance equal to the number of paths times the characteristic impedance of the bus to which the paths are coupled, continuity of impedance is provided and interference of impedance mismatches, such as reflection, is avoided.

For example, a signal applied to transmission line 3501 propagates to node 3506. The signal arriving at node 3506 causes parallel signals to propagate along transmission lines 3502, 3503, and 3504. The waves representing the signal

propagating along transmission lines 3502, 3503, and 3504 retain substantially the same timing relationship among transmission lines 3502, 3503, and 3504, arriving at node 3507 substantially simultaneously. By arriving at node 3507 substantially simultaneously, these waves are recombined at node 3507, driving the signal onto transmission line 3505 without detrimental levels of reflection or attenuation. Thus, the fidelity of the signal is preserved throughout the splitting, propagation, merging, and subsequent propagation.

In accordance with Fig. 35, a module is provided wherein a bus includes a first channel. The first channel has a first characteristic impedance and is coupled to a plurality of paths. The plurality of paths are coupled to a plurality of ICs. The plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

Fig. 36 is a schematic diagram illustrating impedances for a bus, which does not split into multiple paths in accordance with an implementation of the present invention. Driver 3601 is coupled to RACPKG device 3602. This RACPKG device may, for example, be a component of a memory controller or an interface for coupling a memory controller to a memory device. RACPKG device 3602 is coupled through a 28 ohm motherboard conductor 3603 to via 3604. Via 3604 is coupled to connector 3605. Connector 3605 is coupled to 28 ohm module conductor 3606. 28 ohm module conductor 3606 is coupled to connector 3607. Connector 3607 is coupled to via 3608 and 28 ohm motherboard conductor 3609. 28 ohm motherboard conductor 3609 is coupled to via 3610 and connector 3611. Connector 3611 is coupled to 28 ohm module conductor 3612. 28 ohm module conductor 3612 is coupled to connector 3613. Connector 3613 is coupled to via 3614 and 28 ohm motherboard conductor 3615. 28 ohm motherboard conductor

3615 is coupled to 28 ohm termination resistor 3616, which is coupled to ground 3617.

Fig. 37 is a schematic diagram illustrating impedances for a bus that splits into multiple paths in accordance with an implementation of the present invention. Driver 3701 provides an output that is split into separate paths, with one path going to RACPKG device 3702 and the other path going to RACPKG device 3703. These RACPKG devices may, for example, be components of a memory controller or interfaces for coupling a memory controller to a memory device. The outputs of RACPKG device 3702 and RACPKG device 3703 are merged and coupled to 14 ohm motherboard conductor 3704. 14 ohm motherboard conductor 3704 splits into multiple paths, with one path coupled to via 3705, and the other path coupled to via 3710.

Via 3705 is coupled to connector 3706. Connector 3706 is coupled to 28 ohm module conductor 3707. 28 ohm module conductor 3707 is coupled to connector 3708. Via 3710 is coupled to connector 3711. Connector 3711 is coupled to 28 ohm module conductor 3712. 28 ohm module conductor 3712 is coupled to connector 3713.

Connector 3708 is coupled to via 3709 and merges to 14 ohm motherboard conductor 3715. Connector 3713 is coupled to via 3714 and merges to 14 ohm motherboard conductor 3715. 14 ohm motherboard conductor 3715 splits into multiple paths, with a first path coupled to via 3716 and connector 3717 and a second path coupled to via 3721 and connector 3722.

Connector 3717 is coupled to 28 ohm module conductor 3718. 28 ohm module conductor 3718 is coupled to connector 3719. Connector 3722 is coupled to 28 ohm module conductor 3723. 28 ohm module conductor 3723 is coupled to connector 3724. Connector 3719 is coupled to via 3720 and merges to 14 ohm

motherboard conductor 3726. Connector 3724 is coupled to via 3725 and merges to motherboard conductor 3726. Motherboard conductor 3726 is coupled to 14 ohm termination resistor 3727, which is coupled to ground 3728.

While Fig. 37 illustrates splitting and merging occurring outside of a module, for example on a motherboard, such a configuration does not necessarily serve to minimize the number of conductors needed to be coupled by connectors. Thus, it may be preferable to perform splitting and merging on a module, thereby reducing the number of conductors coupled by connectors. Likewise, use of 14 and 28 ohm conductors does not necessarily maximize conductor density and conductor routing efficiency. Thus, it may be preferable to use other impedances, for example, 28 and 56 ohms.

The values for impedances stated in reference to Figs. 36 and 37 are exemplary. Implementations of the invention may be practiced with various impedance values. Likewise, the number of paths that split from or merge to buses may be varied. Moreover, Figs. 36 and 37 provide examples of points in the system where splitting and merging may occur. An implementation of the invention may be practiced with splitting and merging occurring at different points. For example, as illustrated in Fig. 34, splitting and merging may occur within a module. In such an implementation, multiple paths are merged to single conductor, with the single conductor coupled to connectors and a RACPKG device. However, as noted above, splitting and merging may alternatively occur at other points within the system.

Regarding Figs. 34 to 37, to maintain signal integrity and impedance matching, signals should be applied to the non-split portion of the bus. For example, signals should be driven onto a bus either before a single conductor is split into multiple paths or after the multiple paths have merged into a single

conductor. Also, the multiple paths should be matched so as to ensure equal propagation delay along each of the multiple paths split from a single conductor between the point where the multiple paths split and the point where the multiple paths are combined. Matching the multiple paths is most readily done by matching the lengths of the multiple paths, although any technique that maintains equal propagation delay may be used. Also, matching of propagation delay from the point where the multiple paths split to the points where the multiple paths reach devices coupled to the multiple paths may be performed. Moreover, the propagation delays of different buses, for example, address, control, clock, and/or data buses, may be matched to simplify timing considerations of one or more devices coupled to the different buses or multiple paths of one or more of the different buses. With appropriate delay matching and/or impedance matching, noise and/or interference, for example reflection noise, can be minimized.

The modules and bus systems described with reference to Figs. 21 to 26 and 29 to 37 may be implemented using modules wherein the elements described for each module are disposed on at least one of a first primary surface and a second primary surface of the module. The elements described for each module may be disposed on the first primary surface and replicated to allow replicated elements to be disposed on the second primary surface. Thus, it is possible for the modules and bus systems to provide twice the capacity of the single primary surfaces illustrated in Figs. 21 to 26 and 29 to 37.

Other implementations are also provided in accordance with the invention. For example, a module is provided wherein a first channel enters and exits the module, providing continuity from a point of ingress at a first connector contact pin to a point of egress at a second connector contact pin and carrying a first signal, and a second channel enters the module at a third connector contact pin, the second

channel carrying a second signal. The second channel is optionally connected to a terminator on the module. Entry and exit of the channels can occur at respective connector contact pins. In preferred implementations, the first and second signals are "functionally equivalent", wherein the term functionally equivalent in this context refers to the signals performing functions that are equivalent. The function of the first signal and the second signal would be equivalent if, for example, both signals function to carry data information. In preferred implementations, the function of the first signal is selected from one of the following functions: 1) carry data information, 2) carry control information, 3) carry address information, 4) carry data and control information, 5) carry data and address information, 6) carry control and address information, or 7) carry data, control and address information, and the function of the second signal is the same as the first signal. Stated another way, the signals would be considered to be functionally equivalent if they are both of the same type selected from one of the following types: data signals, control signals, address signals, data plus control signals, data plus address signals, control plus address signals, and data plus control plus address signals. It should be noted that a request bus or request channel may carry control signals, address signals, or control plus address signals.

As another example of an implementation in accordance with the invention, a module is provided having two similar devices, wherein the term similar in this context refers to the devices being of the same type. For example, two devices would be considered to be similar devices if they are both memory devices. A first channel is connected to the first device, and a second channel is connected to the second device. The first channel and the second channel carry functionally equivalent signals, but have different topologies. Different topologies may result from different routing patterns of the channels within the module. The first channel

is connected to a first contact, while the second channel is connected to a second contact and a third contact, wherein a controlled non-zero propagation delay exists between the second contact and the third contact. The first channel is terminated on the module. The second channel may, but need not, be terminated on the module. Variations of this implementation encompass modules wherein the first, second and/or third contact is replaced by a plurality of contacts. Other variations of this implementation encompass modules wherein the first channel is coupled to a different number of contacts than the second channel.

As yet another example of an implementation in accordance with the invention, a system is provided having a first module and a second module. A first channel enters and exits the first module and enters and is terminated on the second module. A second channel enters and exits the second module and enters and is terminated on the first module.

As a further example of an implementation in accordance with the invention, a module is provided wherein a first request channel carrying a signal associated with data enters the module at a third contact and terminates on the module, while a first channel carrying the data enters the module at a first contact and exits the module at a second contact.

As another example of an implementation in accordance with the invention, a system is provided having a first module and a second module, wherein a first channel enters the first module on a first contact, exits the first module on a second contact, enters the second module on a third contact, and terminates on the second module. A second channel enters the second module on a fourth contact, exits the second module on a fifth contact, enters the first module on a sixth contact, and terminates on the first module. Optionally, the first channel and the second channel carry functionally equivalent signals.

In preferred implementations, a module such as those described above is adapted to be connected to a motherboard. There may be more than one module connected to a motherboard. A memory controller may be coupled to one or more modules. Collectively, the modules, motherboard, and/or memory controller may form a system. Optionally, integrated circuits are mounted on modules, preferably memory integrated circuits.

While channel signals described above in reference to the various Figs. are described as being provided to the modules and continuing until they reach a terminator, it should be understood that the channels carrying these channel signals are not necessarily unidirectional. Rather, channel signals may be communicated bidirectionally over the channels. For example, some channel signals may propagate from a memory controller to a memory device and, ultimately, to a terminator, other channel signals may propagate from a memory device to a memory controller (with the possibility of an incident terminating wave propagating from the memory device to the terminator). Thus, either or both of the data channels and request channels may be implemented as either unidirectional (in either direction) channels or bi-directional channels. Likewise, unidirectional and/or bi-directional communication may occur between various devices coupled to a channel, for example, between a memory controller, a first memory device, a second memory device, a third memory device, etc.

Terms such as enter, exit, ingress, egress, input, and output are used for clarity to denote aspects of a module or bus system that yield a relationship between modules, module slots, and/or other components, for example, a controller. For example, signals from a controller can be understood to enter a module via an ingress connector and exit that module via an egress connector. However, it should be understood that signals may pass in the opposite direction, entering via an egress

connector and exiting via an ingress connector. Additionally, under some circumstances, for example, when signals originate on a module, the signals may propagate along a channel in both directions, exiting the module at both an ingress connector and an egress connector. Thus, terms such as enter, exit, ingress, egress, input, and output should be understood to promote clarity, not to impose directional limitations on elements to which such terms refer.

References to a first channel and a second channel do not imply that every module of a bus system necessarily needs to have two channels. Likewise, references to a first, second, third, and fourth channel do not imply that every module of a bus system necessarily needs to have four channels. Rather, modules having the same or different numbers of channels may be used together within the bus system.

The present invention may be used to implement a variety of implementations, including modules comprising integrated circuits, modules comprising memory devices, modules comprising bus terminations, and modules comprising conductors coupling one connector to another connector. Such modules need not be mutually exclusive; a module may include various combinations of such components. Moreover, such combinations may vary between different channels. Examples of modules include, but are not limited to, a module comprising an integrated circuit, a module comprising a bus termination, and a continuity module providing continuity between connectors of the module.

As illustrated in these examples, the present invention provides modules adapted to be configured with one or more channels. While the foregoing examples have been drawn to multiple channel implementations, in every case a single channel may be implemented. The modules may be interconnected using various connectors to form bus systems. Such bus systems may be implemented in a

variety of configurations and channel definitions. Relative channel lengths may be reduced given a defined set of configuration requirements. Bus interconnections within the system may also be reduced, thereby reducing the potential for impedance mismatches and undesired channel loading.

As with many mechanical systems, the examples given above may be modified in many ways. The use of right angle connectors has been described, as well as the use of conventional connectors including ribbon and other flexible connectors. Other connector types may be used within the present invention. Channel path definition, integrated circuit layout, and internal bus routing on the various modules may also be readily adapted to suit the system designer's purpose

Reference is now made to the exemplary single channel clock routing scheme depicted in Fig. 38. Here, a plurality of circuit components and modules are provided as part of PCB 200. As shown, a direct Rambus ASIC Cell (RAC) 202 is provided and configured as an interface to a high-speed channel, which carries data and control signals, including timing (i.e., clock signals), to a plurality of memory modules(204a-c) and other mounted circuitry. Only one of these memory modules, namely memory module 204c, is populated with at least one memory integrated circuit 210. Two "continuity" memory modules 204a-b are provided and interconnected between memory module 204c and RAC 202. Memory module 204c and continuity memory modules 204a-b are connected to PCB 200 using connectors 206.

In this example, only the clock routing circuitry is depicted, as beginning at clock generator 212 passing through traces 224 on PCB 200, memory module 204c, continuity modules 204b and 204a to RAC 202. Then the clock signal loops back from RAC 202 through traces on PCB 200, continuity modules 204a and 204b, memory module 204c (and integrated circuit 210) to terminating circuit 214.

One of the problems with this clock routing scheme is that continuity modules 204a-b are required to complete the clock loop. Note that while the traces shown in Fig. 38 are depicted as having sharp turns, in reality the traces will likely have more subtle transitions to avoid unwanted discontinuities/reflections. In any case, the clock routing scheme depicted in Fig. 38 tends to be more expensive due to the need for continuity memory modules 204a-b, which are essentially place holders for future modular expansion of the available memory. For example, at some future stage the user may wish to replace continuity memory modules 204a-b with additional memory modules. Hence, there is a need for an improved clock routing scheme.

With this in mind, reference is now made to Figs 17a-b, wherein a new clock routing scheme is provided, which advantageously allows an improved "terminating" memory module 220 to be placed in different locations depending upon the users needs. For example, as depicted in Fig. 39A, clock generator 212 has been moved closer to RAC 202 on PCB 300 and configured to provide the clock signal to a first positioned module, and in this case terminating memory module 220. On terminating memory module 220 the clock signal is passed through memory integrated circuits 210 and back through tracings 224 to RAC 202. In this example, the clock signal is returned from RAC 202 to terminating memory module 220 through tracings 224 and passed one again through memory integrated circuits 210 to a terminator circuit 222. By locating terminator circuit 222 on terminating memory module 220 and rearranging the location of clock generator 212, terminating memory module 220 can be placed, in this example, in either the first slot as in Fig 17a, or in the third slot, as will be seen in Fig. 39B. When placed in the first slot, memory module 220 does not require any additional continuity or

place holding modules to complete the clock loop. Therefore, there will be cost savings to the manufacturer and user.

Should a user wish to expand the amount of memory at some stage in the future, then, in this example, terminating memory module 220 can be moved to the third slot as depicted in Fig. 39B. Here, additional memory modules 226 having memory integrated circuits 210 thereon are positioned in the first and second slots and interconnected via flexible conductor portion 228. Now, the clock signal travels from clock generator 212 through traces 224 and connector 206 to the memory module 226 in the first slot. The clock signal is then provided through flexible conductor portion 228 to the memory module 226 in the second slot. Next, the clock signal passes through traces 224 between the connectors 206 in the second and third slots. Once the clock signal reaches terminating memory module 220 it is provided to the memory integrated circuit(s) 210 thereon, to begin the clock loop. As depicted, the clock signal is then routed back through memory modules 226 in the second and first slots, and more particularly through the respective memory integrated circuit(s) 210 thereon.

From memory module 226 in the first slot, the clock signal is routed through traces 224 to RAC 202, and then back again. The clock signal is then routed from memory module 226 in the first slot to memory module 226 in the second slot, again over the flexible conductor portion 228, passing through their respective memory integrated circuit(s) 210 on each memory module. The clock signal is then passed through traces 224 to memory module 220 in the third slot. The clock signal then passes through memory integrated circuit(s) 210 on terminating memory module 220, and finally to terminator circuit 222 thereon.

Those skilled in the art will further recognize that additional signals (e.g., control and/or data) can also be routed in the same manner, as is the clock signal in

Figs 17a-b, using like traces, lines, connectors, etc. Furthermore, additional channels having clock signals can be routed likewise.

Fig. 40 depicts an alternative exemplary implementation of a PCB 300' in which memory modules 226' are configured to route the clock signal from clock generator 212 to terminating memory module 220 via trace 230 on PCB 300' rather than through a flexible conductor portion 228'. Such a configuration will alter the required number of traces/conductors/pins associated with flexible conductor portion 228' and connectors 206.

One of the main goals in the clock routing schemes depicted in the examples above is to provide a uniform transmission line without significant reflections, which could cause standing waves in the clock circuit. These exemplary arrangements support this goal by allowing the designer to reduce the number of discontinuities in the clock loop circuit.

Although some preferred implementations of the various methods and arrangements of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the exemplary implementations disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

CLAIMS

What is claimed is:

1. A module having first and second primary surfaces and having a first end, the module comprising:

a first set of input finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a first set of output finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end;

a second set of output finger connectors disposed on at least one of the first and second primary surfaces proximate to the first end; and

a bus including a first channel extending from the first set of input finger connectors to the first set of output finger connectors and a second channel extending from the second set of input finger connectors to the second set of output finger connectors.

2. The module of claim 1 further comprising

at least one first integrated circuit (IC) populating at least one of the first and second primary surfaces, the first channel connected to the at least one first IC; and

at least one second IC populating at least one of the first and second primary surfaces, the second channel connected to the at least one second IC.

3. The module of claim 2, wherein the first IC and the second IC are memory devices.

4. The module of claim 2, wherein the at least one first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

5. The module of claim 4 wherein the first channel and the second channel allow simultaneous independent access to at least some of the first and second ICs.

6. The module of claim 2 further comprising:

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a third set of output finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces; and

a fourth set of output finger connectors disposed on at least one of the first and second primary surfaces, wherein the bus further includes:

a third channel extending from the third set of input finger connectors to the third set of output finger connectors; and

a fourth channel extending from the fourth set of input finger connectors to the fourth set of output finger connectors.

7. The module of claim 6, further comprising:

at least one third IC populating at least one of the first and second primary surfaces, the third channel connected to the at least one third IC; and

at least one fourth IC populating at least one of the first and second primary surfaces, the fourth channel connected to the at least one fourth IC.

8. The module of claim 7 wherein the first channel, the second channel, the third channel, and the fourth channel each allow simultaneous independent access to the respective ICs.

9. The module of claim 6 wherein the first set of input finger connectors, the first set of output finger connectors, the second set of input finger connectors, and the second set of output finger connectors are disposed on the first primary surface, and the third set of input finger connectors, the third set of output finger connectors, the fourth set of input finger connectors, and the fourth set of output finger connectors are disposed on the second primary surface.

10. The module of claim 2 wherein

the at least one first IC is a plurality of first ICs;

the first channel has a first characteristic impedance and is coupled to a plurality of paths, each of the paths is coupled to one of the first ICs, and

the plurality of paths has a combined effective impedance substantially equal to the first characteristic impedance.

11. The module of claim 6, wherein the first set of input finger connectors, the first set of output finger connectors, the second set of input finger connectors, and the second set of output finger connectors are disposed on the first primary surface and the third set of input finger connectors, the third set of output finger connectors, the fourth set of input finger connectors, and the fourth set of output finger connectors are disposed on the second primary surface.

12. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors; and

a plurality of modules arranged from a first module to a last module, wherein each of the plurality of modules includes a bus having a first channel and a second channel, the first channel connecting a first set of input finger connectors proximate to a first end to a first set of output finger connectors proximate to the first end and the second channel connecting a second set of input finger connectors proximate to the first end to a second set of output finger connectors proximate to the first end, the bus electrically coupled to one of the motherboard connectors, wherein each of the modules is mechanically coupled to one of the motherboard connectors.

13. The bus system of claim 12, wherein each of the modules further comprises at least one first IC connected to the first channel and at least one second IC connected to the second channel.

14. The bus system of claim 13 wherein the bus segments of the motherboard electrically connect the first set of output finger connectors of the first module to the first set of input finger connectors of a second module of the plurality of modules and the second set of output finger connectors of the first module to the second set of input finger connectors of the second module.

15. The bus system of claim 14 wherein the bus segments of the motherboard electrically connect the first set of output finger connectors of the last module to a first bus termination and the second set of output finger connectors of the last module to a second bus termination.

16. The bus system of claim 13 wherein, within each of the modules, the first channel and the second channel allow simultaneous independent access to the at least one first IC and the at least one second IC.

17. A module comprising:

a first printed circuit board having first and second primary surfaces and having a first end and a second end;

at least one first integrated circuit (IC) populating at least one of the first and second primary surfaces;

a set of finger connectors disposed on the first printed circuit board proximate to the first end;

a first bus segment disposed on the first printed circuit board and coupled to the set of finger connectors and the at least one first IC;

a conductive interconnect having a second bus segment, the conductive interconnect connected to the first printed circuit board proximate to the

second end and adapted to mechanically connect to a second printed circuit board, the second bus segment electrically coupled to the first bus segment and capable of being electrically coupled to a third bus segment disposed on the second printed circuit board; and

a bus comprising at least the first and second bus segments.

18. The module of claim 17 further comprising the second printed circuit board having the third bus segment disposed thereon, wherein the conductive interconnect is mechanically connected to the second printed circuit board and the third bus segment is electrically coupled to the second bus segment.

19. The module of claim 18 further comprising a connector electrically and mechanically connecting the conductive interconnect to the second printed circuit board.

20. The module of claim 19, wherein the conductive interconnect has a first edge and a second edge opposite the first edge, the first printed circuit board being connected to the conductive interconnect at the first edge, the connector being connected to the conductive interconnect at the second edge.

21. The module of claim 20, further comprising at least one second IC disposed on the second printed circuit board.

22. The module of claim 21, wherein the at least one second IC is coupled to the third bus segment.

23. The module of claim 22 wherein the third bus segment is terminated with a first bus termination.

24. The module of claim 22 wherein the bus further comprises the third bus segments.

25. The module of claim 24, wherein the bus includes a first channel and a second channel, the first channel terminated with the first bus termination and the second channel terminated with a second bus termination.

26. The module of claim 21 wherein the bus substantially traverses the first printed circuit board between the first and second ends.

27. The module of claim 21 wherein the bus comprises a first channel and a second channel and the set of finger connectors comprises a first set of finger connectors and a second set of finger connectors, the first channel coupled to the first set of finger connectors and the second channel coupled to the second set of finger connectors, the first channel and the second channel allowing simultaneous independent access to the at least one first IC and the at least one second IC.

28. The module of claim 19 wherein the second printed circuit board is removably engaged with the connector.

29. The module of claim 18 further comprising a spacer adapted to maintain the first and second printed circuit boards in substantially parallel, spaced apart relation to one another.

30. The module of claim 29, wherein the spacer is attached to one of the first and second primary surfaces of the first printed circuit board proximate to the second end.

31. The module of claim 19 wherein the connector is oriented to maintain the second printed circuit board substantially parallel to at least one of the first and second primary surfaces of the first printed circuit board.

32. The module of claim 17 wherein the conductive interconnect is flexible.

33 . The module of claim 32, wherein the conductive interconnect is a flex circuit.

34. The module of claim 21, wherein the at least first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

35. The module of claim 34, wherein each of the first and second ICs are memory devices.

36. A bus system comprising:

a motherboard including a motherboard connector and a first bus segment electrically coupled to the motherboard connector; and

a module comprising:

a first printed circuit board having first and second primary surfaces and having a first end and a second end;

a set of finger connectors disposed on the first printed circuit board proximate to the first end, the finger connectors electrically connected to the motherboard connector;

at least one first integrated circuit (IC) disposed on the first printed circuit board;

a second bus segment disposed on the first printed circuit board and coupled to the set of finger connectors and the at least one first IC; and

a conductive interconnect having a third bus segment, the conductive interconnect connected to the first printed circuit board proximate to the second end and adapted to mechanically connect to a second printed circuit board, the third bus segment electrically coupled to the second bus segment and capable of being electrically coupled to a fourth bus segment disposed on the second printed circuit board.

37. The bus system of claim 36, wherein the module is mechanically connected to the motherboard connector.

38. The bus system of claim 37, wherein the module further comprises the second printed circuit board having the fourth bus segment disposed thereon, wherein the conductive interconnect is mechanically connected to the second printed circuit board and the fourth bus segment is electrically coupled to the third bus segment.

39. The bus system of claim 38, further comprising a connector electrically and mechanically connecting the conductive interconnect to the second printed circuit board.

40. The bus system of claim 38, wherein the module further comprises at least one second IC disposed on the second printed circuit board and coupled to the fourth bus segment.

41. The bus system of claim 40, wherein the second printed circuit board is removably engaged with the connector.

42. The bus system of claim 38, wherein the fourth bus segment is terminated with a first bus termination.

43. The bus system of claim 38, wherein the first, second, third and fourth bus segments form a bus.

44. The bus system of claim 43, wherein the bus includes a first channel and a second channel, the first channel terminated with the first bus termination and the second channel terminated with a second bus termination.

45. The bus system of claim 44, wherein the first and second channel allow simultaneous independent access to the at least one first IC and the at least one second IC.

46. The bus system of claim 36, wherein conductive interconnect is flexible.

47. The bus system of claim 36, wherein the at least first IC is a plurality of first ICs and the at least one second IC is a plurality of second ICs.

48. The module of claim 47, wherein each of the first and second ICs are memory devices.

49. The bus system of claim 38, wherein the second printed circuit board has a set of printed circuit board finger connectors, wherein the set of printed circuit board finger connectors and the set of finger connectors are adapted to alternatively engage the motherboard connector.

50. A module having first and second primary surfaces and having a first end, the module comprising:

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first terminator disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a first channel extending from the first set of input finger connectors to the first terminator, the first channel connected to a first IC of the plurality of ICs; and

a second channel extending from the second IC of input finger connectors to the second terminator, the second channel connected to a second IC of the plurality of ICs.

51. The module of claim 50 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

52. The module of claim 50 wherein the first IC of the plurality of ICs and the second IC of the plurality of ICs are mutually exclusive.

53. The module of claim 50 wherein the first channel and the second channel allow simultaneous independent access to the plurality of ICs.

54. The module of claim 50 further comprising:

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a third terminator disposed on at least one of the first and second primary surfaces;

a fourth terminator disposed on at least one of the first and second primary surfaces; and

a third channel extending from the third set of input finger connectors to the third terminator; and

a fourth channel extending from the fourth set of input finger connectors to the fourth terminator.

55. The module of claim 54 wherein the third bus is connected to a third IC of the plurality of ICs and wherein the fourth bus is connected to a fourth IC of the plurality of ICs.

56. The module of claim 55 wherein the first IC of the plurality of ICs, the second IC of the plurality of ICs, the third IC of the plurality of ICs, and the fourth IC of the plurality of ICs are mutually exclusive.

57. The module of claim 54 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

58. The module of claim 54 wherein the first set of input finger connectors and the second set of input finger connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input finger connectors are disposed on the second primary surface.

59. The module of claim 54 wherein the first channel, the second channel, the third channel, and the fourth channel each allow simultaneous independent access to the plurality of ICs.

60. The module of claim 50 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, each of the paths being coupled to at least one of the plurality of ICs, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

61. The module of claim 50 wherein the first channel is connected to a first set of the plurality of ICs, the first set comprising the first IC, and the second channel is connected to a second set of the plurality of ICs, the second set comprising the second IC.

62. The module of claim 61, wherein each of the ICs are memory devices.

63. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors;

a first module including a first ingress connector, a first egress connector, a first integrated circuit (IC), and a first channel, the first channel coupled to the first ingress connector, the first egress connector, and the first IC;

a second module including a second ingress connector, a second egress connector, a second IC, and a second channel, the second channel coupled to the second ingress connector, the second egress connector, and the second IC; and

a termination module including a first channel terminator and a second channel terminator, the first channel terminator coupled to the first channel of the first module through a first set of the motherboard connectors and the second channel terminator coupled to the second channel of the second module through a second set of the motherboard connectors.

64. The bus system of claim 63, wherein the first and second ICs are memory devices.

65. The bus system of claim 64 wherein the first channel and the second channel allow simultaneous independent access to the first memory device and the second memory device.

66. The bus system of claim 63 wherein the termination module further includes a third IC coupled to the first channel.

67. The bus system of claim 66, wherein the third IC is a memory device.

68. The bus system of claim 63 wherein the bus segments of the motherboard electrically connect the first egress connector to the first channel terminator and the second egress connector to the second channel terminator.

69. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors, the motherboard connectors including a first ingress connector for a first module slot, a first egress connector for the first module slot, a second ingress connector for a second module slot, a second egress connector for the second module slot, a third ingress connector for a third module slot, and a fourth ingress connector for the third module slot, and the bus segments including a first bus segment coupled to the first ingress connector, a second bus segment routed so as to occupy a region of the motherboard located between the first ingress connector and the first egress connector and coupled to the second ingress connector.

70. The bus system of claim 69 wherein the bus segments further comprise a third bus segment coupling the first egress connector to the third ingress connector and a fourth bus segment coupling the second egress connector to the fourth ingress connector.

71. The bus system of claim 70 wherein the first bus segment and the third bus segment are electrically connected by a first module connected to the first ingress connector and the first egress connector and the second bus segment and the fourth bus segment are electrically connected by a second module connected to the second ingress connector and the second egress connector.

72. A bus system comprising:

a motherboard including motherboard connectors and bus segments electrically coupling the motherboard connectors;

a first module including a first ingress connector, a first egress connector, a second ingress connector, and a first terminator, wherein the first ingress connector is electrically coupled to the first egress connector and the second ingress connector is electrically coupled to the first terminator;

a second module including a third ingress connector, a second egress connector, a fourth ingress connector, and a second terminator, wherein the third ingress connector is electrically coupled to the second egress connector and the fourth ingress connector is electrically coupled to the second terminator; and wherein the first ingress connector, the first egress connector, the second ingress connector, the second egress connector, the third ingress connector, and the fourth ingress connector are coupled to the motherboard connectors and wherein a first set of the bus segments couple the first egress connector to the fourth ingress connector and a second set of the bus segments couple the second egress connector to the second ingress connector, thereby providing a first channel coupling the first ingress connector, the first egress connector, the fourth ingress connector, and the second terminator and a second channel coupling the third ingress connector, the second egress connector, the second ingress connector, and the first terminator

73. The bus system of claim 72 wherein the first channel is coupled to a first integrated circuit (IC) of the first module and the second channel is coupled to a second IC of the second module, the first channel and the second channel allowing simultaneous independent access to the first IC and the second IC.

74. The bus system of claim 73, wherein the first and second ICs are memory devices.

75. The bus system of claim 74 wherein the first channel is further coupled to a third IC of the second module and the second channel is further coupled to a fourth IC of the first module.

76. The bus system of claim 75, wherein the third and fourth ICs are memory devices.

77. The bus system of claim 72 wherein the first channel is coupled to a first memory device of the second module and the second channel is coupled to a second memory device of the first module, the first channel and the second channel allowing simultaneous independent access to the first memory device and the second memory device.

78. The bus system of claim 72 further comprising a third module coupled to first channel and the second channel via the motherboard connectors.

79. The bus system of claim 72 wherein the first module further includes a first IC coupled to the first channel, and the second module includes a second IC coupled to the second channel.

80. The bus system of claim 79 wherein the first module further includes a third IC coupled to the second channel and the second module further includes a fourth IC coupled to the first channel.

81. The bus system of claim 80, wherein the first, second, third and fourth ICs are memory devices.

82. The bus system of claim 80 further comprising a first request channel coupled to the first memory device and the third memory device and a second request channel coupled to the second memory device and the fourth memory device.

83. The bus system of claim 72 wherein the bus segments further couple additional ingress connectors and additional egress connectors on the first module and the second module to provide a third channel and a fourth channel.

84. The bus system of claim 83 wherein the first channel, the second channel, the third channel, and the fourth channel allow simultaneous independent access to a plurality of ICs including a first IC of the first module and a second IC of the second module.

85. A module having first and second primary surfaces and having a first end, the module comprising:

a first integrated circuit (IC) populating at least one of the first and second primary surfaces;

a first set of input finger connectors disposed on at least one of the first and second primary surfaces;

a first set of output finger connectors disposed on at least one of the first and second primary surfaces;

a second set of input finger connectors disposed on at least one of the first and second primary surfaces;

a terminator disposed on at least one of the first and second primary surfaces;

first channel extending from the first set of input finger connectors to the first set of output finger connectors, the first channel connected to the first IC; and

a second channel extending from the second set of input finger connectors to the terminator.

86. The module of claim 85 further comprising:

a second IC, wherein the second channel is coupled to the second IC.

87. The module of claim 86 wherein the first channel and the second channel allow simultaneous independent access to the first IC and the second IC.

88. The module of claim 85 wherein the first set of input finger connectors and the second set of input finger connectors are disposed proximate to the first end.

89. The module of claim 85 further comprising:

a third integrated circuit (IC) populating at least one of the first and second primary surfaces;

a fourth integrated circuit (IC) populating at least one of the first and second primary surfaces;

a third set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second set of output finger connectors disposed on at least one of the first and second primary surfaces;

a fourth set of input finger connectors disposed on at least one of the first and second primary surfaces;

a second terminator disposed on at least one of the first and second primary surfaces;

a third channel extending from the third set of input finger connectors to the second set of output finger connectors, the third channel connected to the third IC; and

a fourth channel extending from the fourth set of input finger connectors to the second terminator.

90. The module of claim 89 wherein the first channel, the second channel, the third channel, and the fourth channel allow simultaneous independent access to the first IC, the second IC, the third IC, and the fourth IC.

91. The module of claim 89 wherein the first set of input finger connectors, the second set of input finger connectors, the third set of input finger connectors, and the fourth set of input finger connectors are disposed proximate to the first end.

92. The module of claim 89 wherein the first set of input finger connectors and the second set of input finger connectors are disposed on the first primary surface, and the third set of input finger connectors and the fourth set of input finger connectors are disposed on the second primary surface.

93. The module of claim 85 wherein the first channel has a first characteristic impedance and is coupled to a plurality of paths, and wherein the plurality of paths have a combined effective impedance substantially equal to the first characteristic impedance.

94. A module comprising:

a printed circuit board;

a first set of integrated circuits (ICs) mounted on the printed circu board;

a second set of ICs mounted on the printed circuit board;

a first input connector disposed on the printed circuit board; and

a first ingress bus coupled to the first input connector, the first ingres bus split into a first path and a second path, the first path coupled to the first set o ICs and the second path coupled to the second set of ICs, the first ingress bu having a first characteristic impedance and the first path and the second path havin a combined effective impedance substantially equal to the first characteristi impedance.

95. The module of claim 94 wherein the first path is coupled to a firs terminator and the second path is coupled to a second terminator.

96. The module of claim 94 wherein the module further comprises:

a first output connector disposed on the printed circuit board; and

a first egress bus coupled to the first output connector, the first patl and the second path merged into the first egress bus, the first egress bus having a second characteristic impedance substantially equal to the first characteristic impedance.

97. A module adapted for use in a bus system and comprising:

a printed circuit board (PCB) having primary first and second surfaces and having first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second surfaces;

a first set of edge fingers disposed at the first end and on the first surface of the PCB;

a second set of edge fingers disposed at the first end and on the second surface of the PCB;

an internal bus extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back proximate the second end, substantially traversing the length of the second surface, and terminating at the second set of edge fingers;

a right-angle connector mounted on either the first or second surface at the first end, and

adapted to mechanically receive and electrically connect another module.

98. The module of claim 97, wherein the folded internal bus is disposed on the first and second surfaces of the PCB.

99. The module of claim 97, wherein the folded internal bus is disposed within the body of the PCB; and

wherein the plurality of ICs is connected to the folded internal bus through vias formed in the at least one of the first and second surfaces of the PCB.

100. The module of claim 97, wherein the plurality of ICs populates the first and second surfaces of the PCB.

101. The module of claim 97, wherein the folded internal bus comprises a single high-speed bus connecting the plurality of ICs.

102. The module of claim 97, wherein the folded internal bus comprises a plurality of high speed buses, each one of the plurality of high-speed bus connecting a respective number of the plurality of ICs.

103. A bus system comprising:

a motherboard; and,

a plurality of modules arranged from a first module to a last module;

wherein the motherboard comprises a controller and a right-angle connector adapted to mechanically receive and electrically connect the first module;

wherein each one of the plurality of modules comprises a right-angle connector adapted to receive another one of the plurality of modules, such that, once connected via respective right angle connectors, the motherboard and the plurality of modules are disposed in parallel one to another.

104. The bus system of claim 103, wherein each one of the plurality of modules comprises:

a printed circuit board (PCB) having primary first and second surfaces and first and second ends, and a plurality of integrated circuits (ICs) populating at least one of the top and bottom surfaces;

a first set of edge fingers disposed at the first end and on the first surface of the PCB;

a second set of edge fingers disposed at the first end and on the second surface of the PCB;

a folded internal bus extending from the first set of edge fingers, substantially traversing the length of the first surface, folding back at the second end, substantially traversing the length of the second surface and terminating at the second set of edge fingers;

a right-angle connector mounted on at least one of the first and second surfaces, and

adapted to mechanically receive and electrically connect another one of the plurality of modules.

105. The bus system of claim 104, further comprising a termination module connected to the right-angle connector on the last module.

106. The bus system of claim 105, wherein the combination of the right-angle connector and the folded internal bus on each module forms a corresponding segment of a system bus.

107. The bus system of claim 106, further comprising a single high-speed bus running from the controller on the motherboard through the respective system bus segments to the termination module.

108. The bus system of claim 106, further comprising a plurality of high-speed buses running from the controller on the motherboard through the respective system bus segments to the termination module.

109. A module adapted for use in a bus system and comprising:

a printed circuit board (PCB) having primary first and second surfaces, and having first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second surfaces;

a set of edge fingers disposed at the first end of the PCB and on either the top or bottom surface of the PCB;

a right-angle connector adapted to mechanically receive and electrically connect another module, the right-angle connector being mounted on either the bottom or top surface of the PCB opposite the surface on which the set of edge fingers are disposed and at the second end of the PCB; and

an internal bus extending from the set of edge fingers, substantially traversing the length of the module, and terminating at the right-angle connector.

110. The module of claim 109, wherein the internal bus is disposed within the body of the PCB, and wherein the plurality of ICs is connected to the internal bus through vias formed in the at least one of the top and bottom surfaces of the PCB.

111. The module of claim 110, wherein the plurality of ICs populates the first and second surfaces of the PCB.

112. The module of claim 111, wherein the internal bus comprises a single high-speed bus connecting the entire plurality of ICs.

113. The module of claim 111, wherein the internal bus comprises a plurality of high-speed buses, each one of the plurality of high-speed bus connecting a respective number of the plurality of ICs.

114. The module of claim 113, wherein the set of edge fingers comprises a plurality of subsets, each subset of edge fingers corresponding to one of the plurality of high-speed buses.

115. The bus system of claim 103, wherein each one of the plurality of modules comprises:

a printed circuit board (PCB) having primary first and second surfaces, and having first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second surfaces;

a set of edge fingers disposed at the first end of the PCB and on either the top or bottom surface of the PCB;

a right-angle connector adapted to mechanically receive and electrically connect another module, the right-angle connector being mounted on either the bottom or top surface of the PCB opposite the surface on which the set of edge fingers are disposed and at the second end of the PCB; and

an internal bus extending from the set of edge fingers, substantially traversing the length of the module, and terminating at the right-angle connector.

116. A module adapted to be connected within a plurality of bus system modules, the module comprising:

a printed circuit board (PCB) having first and second primary surfaces, first and second primary edges, and first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the primary first and second surfaces;

a first set of edge fingers disposed on the first primary edge between first and second ends and on the first surface of the PCB;

a second set of edge fingers disposed on the first primary edge between first and second ends and on the second surface of the PCB, wherein the first and second set of edge fingers are adapted to connect with an electrical connector associated with another module or a motherboard;

an internal bus comprising a plurality of signal lines running from at least one of the first and second set of edge fingers to a flex tape connector connected at the second primary edge of the PCB between the first and second ends; and,

an electrical connector connected to the flex tape.

117. The module of claim 116, further comprising a first channel and a second channel;

wherein the first channel comprises the first set of edge fingers, a first portion of the flex tape connector, and a first sub-plurality of the ICs connected to a first portion of the internal bus running from the first set of edge fingers to the first portion of the flex tape; and

wherein the second channel comprises the second set of edge fingers, a second portion of the flex tape connector, and a second sub-plurality of the ICs connected to a second portion of the internal bus running from the second set of edge fingers to the second portion of the flex tape.

118. The module of claim 117, wherein the ICs of the first sub-plurality of ICs are disposed in one or more rows on the first surface of the PCB and the ICs of the second sub-plurality of ICs are disposed in one or more row on the second surface of the PCB.

119. The module of claim 118, wherein the first set of edge fingers is disposed on the first primary edge of the PCB proximate the first end of the PCB, and the first portion of the flex tape connector is disposed on the second primary edge of the PCB proximate the second end of the PCB, such that the first portion of the internal bus traverses the first sub-plurality of ICs in a first direction from the first end of the PCB to second end of the PCB.

120. The module of claim 119, wherein the second set of edge fingers is disposed on the second primary edge of the PCB proximate the second end of the PCB, and the second portion of the flex tape connector is disposed on the second primary edge of the PCB proximate the first end of the PCB, such that the second portion of the internal bus traverses the second sub-plurality of ICs in a second direction opposite the first direction from the second end of the PCB to the first end of the PCB.

121. A one channel module comprising:

a printed circuit board having first and second primary surfaces, and first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces and arranged in one or more rows;

an internal bus laterally traversing the one or more rows, the internal bus running from a first connector disposed on the first primary surface of the PCB proximate the first end of the PCB to a second connector disposed on the second primary surface of the PCB proximate the second end of the PCB;

wherein the one channel module is mechanically stacked and electrically connected within a bus system comprising a plurality of modules by operation of the first and second connectors.

122. A two channel module comprising:

a printed circuit board having first and second primary surfaces, and first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces and arranged in one or more rows;

a first internal bus laterally traversing the one or more rows in a first direction, the first internal bus running from a first connector disposed on the first primary surface of the PCB proximate the first end of the PCB to a second connector disposed on the second primary surface of the PCB proximate the second end of the PCB;

a second internal bus laterally traversing the one or more rows in a second direction opposite the first direction, the second internal bus running from a third connector disposed on the first primary surface of the PCB proximate the second end of

the PCB to a fourth connector disposed on the second primary surface of the PCB proximate the first end of the PCB;

wherein the two channel module is mechanically stacked and electrically connected within a bus system comprising a plurality of modules by operation of the first, second, third and fourth connectors.

123. An N channel module comprising:

a printed circuit board having first and second primary surfaces, first and second ends, and first and second edges of the first and second primary surfaces running between the first and second ends;

a plurality of integrated circuits (ICs) populating at least one of the first and second primary surfaces, the plurality of ICs being arranged in N columns, each column extending from the first edge of the PCB towards the second edge of the PCB;

a plurality of N first connectors disposed on the first primary surface of the PCB proximate the first edge of the PCB, each one on the first connectors being substantially aligned with one of the N columns;

a plurality of N second connectors disposed on the second primary surface of the PCB proximate the first edge of the PCB, each one on the second connectors being substantially aligned with one of the N columns;

an internal bus comprising N bus portions, each one of the N bus portions extending from a respective one of the plurality of first connectors, substantially traversing the breadth of the PCB from first primary edge to the second primary edge, folding back at the second primary edge, substantially traversing the breadth of the PCB from second primary edge to the first primary edge, and terminating at a respective one of the plurality of second connectors;

wherein the N channel module is mechanically stacked and electrically connected within a bus system comprising a plurality of modules by operation of the first and second connectors.

124. A module configured to implement N channel(s) in a bus system comprising a plurality of modules, the module comprising:

a printed circuit board (PCB) having first and second primary surfaces, first and second primary edges, and first and second lateral edges;

a plurality of integrated circuits (ICs) arranged in one or more rows and disposed on at least one of the first and second primary surfaces of the PCB;

at least one set of input finger connectors disposed on the first primary edge and adapted for connection to a corresponding electrical connector;

at least one set of output finger connectors disposed on one of the first primary edge, the second primary edge, the first lateral edge, or the second lateral edge, and adapted for connection to a corresponding electrical connector; and,

an internal bus forming a plurality of signal paths between the at least one set of input finger connectors and the at last one set of output finger connectors , and connected to at least one of the plurality of ICs.

125. The module of claim 124 adapted to implement one channel, wherein the at least one set of output finger connectors comprises one set of output edge fingers disposed on the first primary edge, and wherein the internal bus traverses substantially the length of the PCB between first and second lateral edges connecting the plurality of ICs.

126. The module of claim 124 adapted to implement two channels, wherein the at least one set of input finger connectors comprises a first set of input edge fingers and a second set of input edge fingers disposed on the first primary edge of the PCB;

wherein the at least one set of output finger connectors comprises a first set of output edge fingers disposed on the first lateral edge of the PCB and a second set of output edge fingers disposed on the second lateral edge of the PCB;

wherein the plurality of ICs comprises a first sub-plurality of ICs arranged in one or more rows and a second sub-plurality of ICs arranged in one or more rows, wherein the internal bus comprises first internal bus segment and second internal bus segment, wherein the first internal bus segment extends from the first set of input edge fingers towards a center location proximate the center of the PCB, then traverses substantially one half the length of the PCB from the center location to the first set of output edge fingers, and connects the first sub-plurality of ICs, and wherein the second internal bus segment extends from the second set of input edge fingers towards the center location, then traverses substantially one half the length of the PCB from the center location to the second set of output edge fingers, and connects the second sub-plurality of ICs.

127. The module of claim 124 adapted to implement four channels, wherein the at least one set of input finger connectors comprises 1st and 2nd first sets of input edge fingers disposed on the first primary edge of the first primary surface of the PCB, and 1sl and 2nd second sets of input edge fingers disposed on the first primary edge of the second primary surface of the PCB;

wherein the at least one set of output finger connectors comprises 1sl and 2nd first sets of output edge fingers respectively disposed on the first lateral edge of the first and second primary surfaces of the PCB, and 1sl and 2nd second sets of output edge fingers

respectively disposed on the second lateral edge of the first and second primary surfaces of the PCB;

wherein the plurality of ICs comprises a first, second, third and fourth sub-pluralities of ICs arranged in one or more rows;

wherein the internal bus comprises:

a first internal bus segment connecting the first sub-plurality of ICs by extending from the 1st first set of input edge fingers to a first center location proximate the center of the first surface of the PCB and then from the first center location to the 1st first set of output edge fingers;

a second internal bus segment connecting the second sub-plurality of ICs by extending from the 2nd first set of input edge fingers to the first center location and then from the first center location to the 2nd first set of output edge fingers;

a third internal bus segment connecting the third sub-plurality of ICs by extending from the 1st second set of input edge fingers to a second center location proximate the center of the second surface of the PCB and then from the second center location to the 1st second set of output edge fingers; and

a fourth internal bus segment connecting the fourth sub-plurality of ICs by extending from the 2nd second set of input edge fingers to the second center location and then from the second center location to the 2nd second set of output edge fingers.

128. A bus system comprising a plurality of modules, wherein each one of the modules comprises a first and second primary surface, each primary surface being adapted to receive one or more integrated circuits (ICs) thereon, first and second primary edges, and first and second lateral edges, the system comprising first and second modules connected via first and second flexible connectors;

wherein the first module comprises;

first and second sets of input edge fingers disposed on the first primary edge, a first set of output finger connectors disposed on the first lateral edge and a second set of output edge fingers disposed on the second lateral edge, a first plurality of ICs and a second plurality of ICs, and a first internal bus segment connecting the first plurality of ICs between the first set of input edge fingers and the first set of output finger connectors and a second internal bus segment connecting the second plurality of ICs between the second set of input edge fingers and the second set of output finger connectors.

129. The bus system of claim 128, wherein the second module comprises:

a third set of input edge fingers disposed on the first lateral edge and a fourth set of input edge fingers disposed on the second lateral edge, third and fourth sets of output edge fingers disposed on the first primary edge, a third plurality of ICs and a fourth plurality of ICs, and a third internal bus segment connecting the third plurality of ICs between the third set of input edge fingers and the third set of output edge fingers and a fourth internal bus segment connecting the fourth plurality of ICs between the fourth set of input edge fingers and the fourth set of output edge fingers; and

wherein the first flexible connector connects the first output set of edge fingers on the first module with the third set of input fingers on the second module, and the second flexible connector connects the second output set of edge fingers on the first module with the forth set of input fingers on the second module.

130. The bus system of claim 128, wherein the second module comprises:

a third set of input edge fingers disposed on the first lateral edge and a fourth set of input edge fingers disposed on the second lateral edge, a first termination element disposed proximate the first lateral edge and a second termination element disposed proximate the second lateral edge;

a third plurality of ICs arranged in one or more rows between the first and second termination elements;

a third internal bus segment connecting at least one of the third plurality of ICs between the third set of input edge fingers and the second termination element, and a fourth internal bus segment connecting at least one of the third plurality of ICs between the fourth set of input edge fingers and the first termination element; and

wherein the first flexible connector connects the first output set of edge fingers on the first module with the third set of input fingers on the second module, and the second flexible connector connects the second output set of edge fingers on the first module with the forth set of input fingers on the second module.

131. The bus system of claim 128, wherein the second module comprises:

a third set of input edge fingers disposed on the first lateral edge and a fourth set of input edge fingers disposed on the second lateral edge, first and second termination elements disposed adjacent one to another at a location proximate the center of the second module;

a third plurality of ICs arranged in one or more rows between the third set of input edge fingers and the first termination element and a fourth plurality of ICs arranged in one or more rows between the fourth set of input edge fingers and the second termination element;

a third internal bus segment connecting the third plurality of ICs between the third set of input edge fingers and the first termination element, and a fourth internal bus segment

connecting the fourth plurality of ICs between the fourth set of input edge fingers and the second termination element; and

wherein the first flexible connector connects the first output set of edge fingers on the first module with the third set of input fingers on the second module, and the second flexible connector connects the second output set of edge fingers on the first module with the forth set of input fingers on the second module.

132. A bus system comprising a plurality of modules, wherein each one of the modules comprises a first and second primary surface, each primary surface being adapted to receive one or more integrated circuits (ICs) thereon, first and second primary edges, and first and second lateral edges, the system comprising:

a central module comprising;

first and second sets of input edge fingers disposed on the first primary edge, a first set of output edge fingers disposed on the first lateral edge and a second set of output edge fingers disposed on the second lateral edge, a first plurality of ICs and a second plurality of ICs, and a first internal bus segment connecting the first plurality of ICs between the first set of input edge fingers and the first set of output edge fingers and a second internal bus segment connecting the second plurality of ICs between the second set of input edge fingers and the second set of output edge fingers.

133. The bus system of claim 132, further comprising at least one secondary module, comprising:

a third set of input edge fingers disposed on either one of the first or second lateral edge, the third set of input edge fingers being connected to either one of the first or second set of output edge fingers via a flexible connector; and

a third plurality of ICs disposed on at least one of the first and second primary surfaces of the PCB; and, a third internal bus segment connecting the third plurality of ICs between the third set of input edge fingers and one of a termination element or a third set of output edge fingers disposed on the first primary edge of the PCB.

134. A module comprising:

a printed circuit board (PCB) having first and second primary surfaces, first and second lateral ends, and top and bottom edges, wherein the bottom edge is adapted to be mechanically secured and electrically connected within a connector;

a plurality of integrated circuits (ICs) arranged on at least one of the first and second primary surfaces;

a flexible connector connected to the top edge of the PCB; and,

an internal bus extending from a first set of edge fingers located on the bottom edge of the PCB and traversing the arrangement of the plurality of ICs to the flexible connector.

135. The module of claim 134, wherein the plurality of ICs are arranged in one or more vertical columns, and the internal bus extends vertically from the first set of edge fingers to the flexible connector.

136. The module of claim 134, wherein the plurality of ICs are arranged in one or more rows, and the internal bus first extends vertically from the first set of edge fingers to the one or more rows of ICs, then laterally through the one or more rows of ICs, and then vertically to the flexible connector.

137. A terminating module comprising:

at least one integrated circuit; and

a termination circuit coupled to receive a timing signal from the integrated circuit.

138. The terminating module as recited in Claim 137, further comprising:

a plurality of integrated circuits; and

a plurality of termination circuits coupled to receive a timing signal from the plurality of integrated circuits.

139. The terminating module as recited in Claim 137, wherein the integrated circuit includes memory circuitry.

140. The terminating module as recited in Claim 137, wherein the termination circuit includes a resistor.

141. A non-terminating apparatus comprising:

a first non-terminating module having at least one integrated circuit;

a second non-terminating module having at least one integrated circuit; and

a flexible interface operatively connecting the first and the second non-terminating modules and configured to carry timing signals directly there between and also between the at least one integrated circuits on both the first and the second non-terminating modules.

142. The non-terminating apparatus as recited in Claim 141, wherein each of the at least one integrated circuits on the first and the second non-terminating modules includes memory circuitry.

143. A non-terminating apparatus comprising:

a first non-terminating module having at least one integrated circuit;

a second non-terminating module having at least one integrated circuit; and

a flexible interface operatively connecting the first and the second non-terminating modules and configured to carry timing signals between the at least one integrated circuits on both the first and the second non-terminating modules.

144. The non-terminating apparatus as recited in Claim 143, wherein each of the at least one integrated circuits on the first and the second non-terminating modules includes memory circuitry.

145. An apparatus comprising:

a memory interface circuit;

a clock signal generating circuit;

a plurality of memory modules, each having memory circuitry thereon, the memory modules being operatively coupled and arranged in an order, wherein the memory module positioned at the beginning of the order is coupled to an output of the clock signal generating circuit and the memory interface circuit, and the memory module positioned at the end of the order includes a clock signal terminating circuit, and

wherein a clock loop is formed by initially directly routing a clock signal from the output of the clock signal generating circuit through each of the memory

modules in the order to the memory module positioned at the end of the order without asserting the clock signal on the memory circuitry, then routing and asserting the clock signal back through the memory modules and the memory circuitry thereon in reverse order to the memory module positioned at the beginning of the order and from there to the memory interface circuit, then routing and asserting the clock signal from the memory interface circuit back through the memory modules and memory circuitry thereon in order to the memory module positioned at the end of the order, and then terminating the clock signal at the clock signal terminating circuit.

146. The apparatus as recited in Claim 145, wherein apparatus is provided as part of a computer.

147. An apparatus comprising:

a circuit board;

at least one clock generating circuit mounted on the circuit board;

a first connector, a second connector and a third connector mounted on the circuit board.

a first conductor connecting an output node of the clock generating circuit with the first connector;

a first non-terminating memory circuit card operatively arranged in the first connector and configured to receive a timing signal as output by the clock generating circuit and provided via the first conductor and first connector;

a second non-terminating memory circuit card operatively arranged in the second connector.

a flexible conductor coupled between the first and second non-terminating memory circuit cards and configured to carry the timing signal from the first non-terminating memory card to the second non-terminating memory card;

a second conductor connecting the second connector with the third connector;

a terminating memory card operatively arranged in the third connector and configured to receive the timing signal from the second non-terminating memory card via the second connector, the second conductor and third connector.

148. The apparatus as recited in Claim 147, wherein apparatus is provided as part of a computer.

149. An apparatus comprising:

a circuit board;

at least one clock generating circuit mounted on the circuit board;

a first connector, a second connector and a third connector mounted on the circuit board.

a first conductor connecting an output node of the clock generating circuit with the first connector;

a first non-terminating memory circuit card operatively arranged in the first connector and configured to receive a timing signal as output by the clock generating circuit and provided via the first conductor and first connector;

a second conductor connecting the first connector with the second connector;

a second non-terminating memory circuit card operatively arranged in the second connector and configured to receive the timing signal from the first non-terminating memory circuit card via the second conductor and second connector.

a third conductor connecting the second connector with the third connector;

a terminating memory card operatively arranged in the third connector and configured to receive the timing signal from the second non-terminating memory card via the second connector, the third conductor and third connector.

150. The apparatus as recited in Claim 149, wherein apparatus is provided as part of a computer.

151. A method for routing a clock signal in a device capable of supporting multiple memory modules, the method comprising:

generating a clock signal;

directly passing the clock signal to a terminating memory module;

configuring the terminating memory module to provide the clock signal to at least one memory integrated circuit provided on the terminating memory module; then

routing the clock signal from the terminating memory module to a memory interface circuit and then from the memory interface circuit back to the terminating memory module; and then

terminating the clock signal at the terminating memory module.

152. A module, comprising:

a first input connector;

a first output connector;

a first channel coupled to the first input connector and the first output connector, the first channel carrying a first signal;

a second input connector; and

a second channel coupled to the second input connector, the second channel carrying a second signal;

wherein the first and second signals are functionally equivalent.

153. The module of claim 152, further comprising a terminator coupled to the second channel.

154. The module of claim 152, further comprising a first integrated circuit coupled to the first channel and a second integrated circuit coupled to the second channel.

155. A bus system, comprising:

a motherboard including a motherboard connector and a first bus segment coupled to the motherboard connector;

a module comprising

a first input connector coupled to the motherboard connector;

a first output connector coupled to the motherboard connector;

a second input connector coupled to the motherboard connector; and

a second bus segment comprising

a first channel coupled to the first input connector and the first output connector, the first channel carrying a first signal; and

a second channel coupled to the second input connector, the second channel carrying a second signal;

wherein the first and second signals are functionally equivalent.

156. The module of claim 155, wherein the module further comprises a terminator coupled to the second channel.

157. The module of claim 155, further comprising a first integrated circuit coupled to the first channel and a second integrated circuit coupled to the second channel.

158. A module, comprising:

a first integrated circuit;

a second integrated circuit;

a first input connector;

a second input connector;

a first terminator;

a second terminator;

a first channel extending from the first input connector to the first terminator, the first channel carrying a first signal; and

a second channel extending from the second input connector to the second terminator, the second channel carrying a second signal;

wherein the first and second signals are functionally equivalent.

159. The module of claim 158 further comprising a first integrated circuit coupled to the first channel and a second integrated circuit coupled to the second channel.

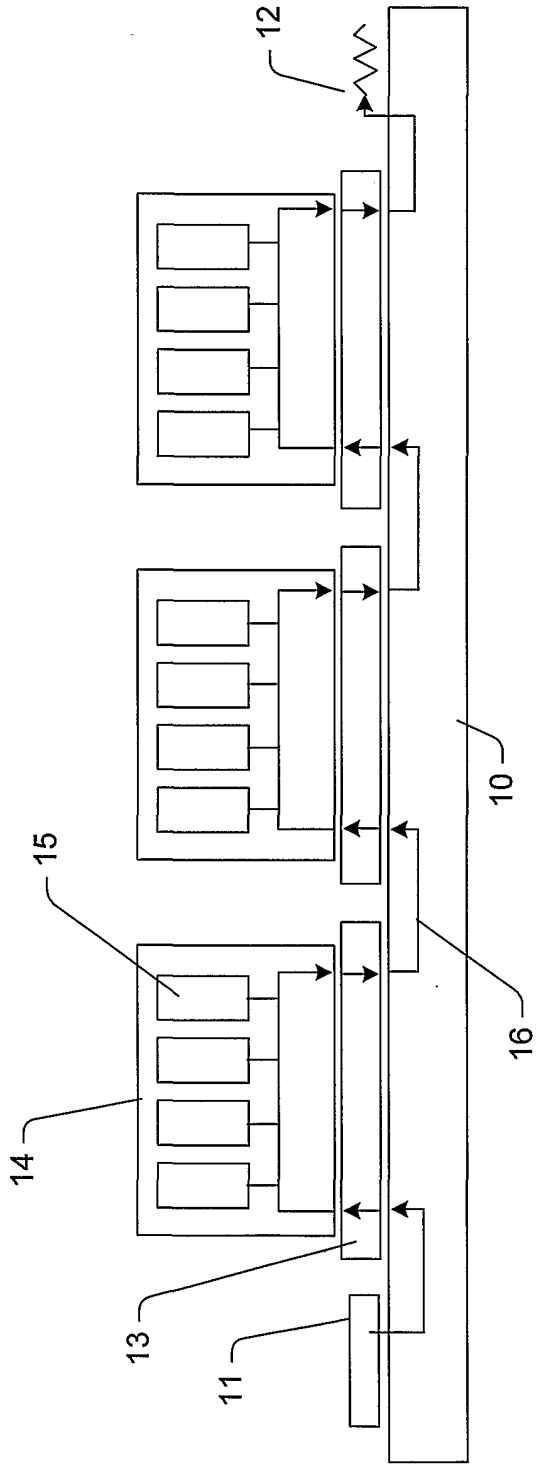


Fig. 1 (Prior Art)

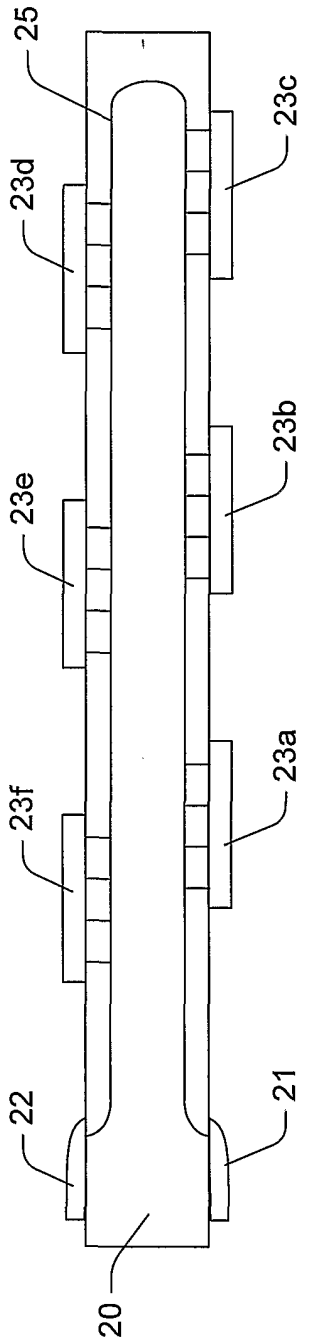


Fig. 2

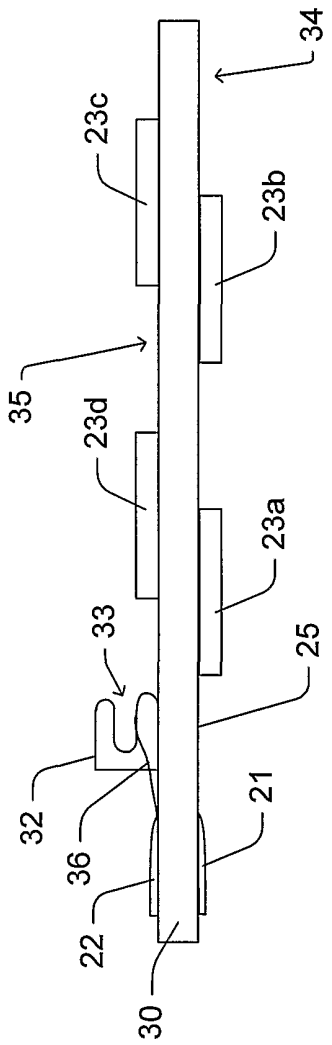


Fig. 34

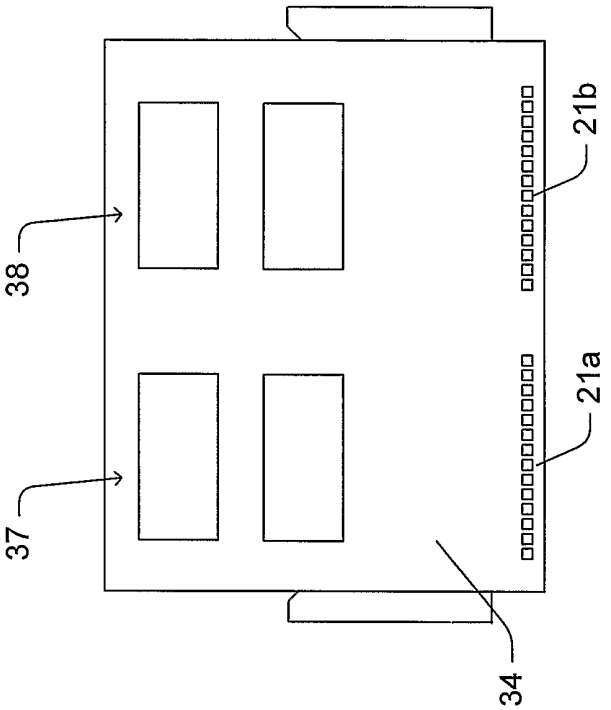


Fig. 3D

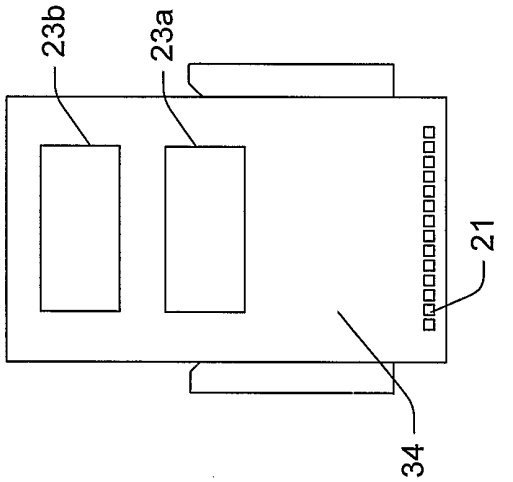


Fig. 3C

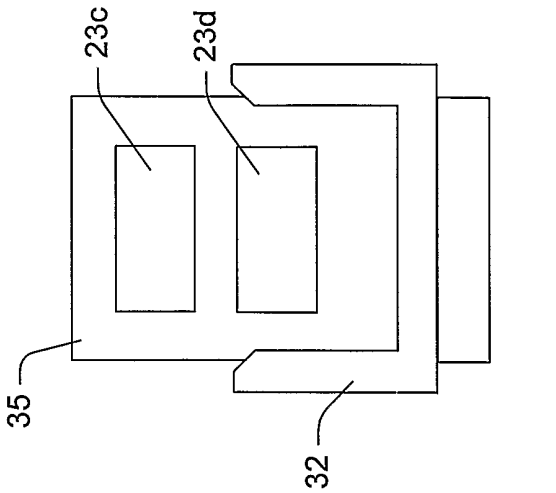


Fig. 3B

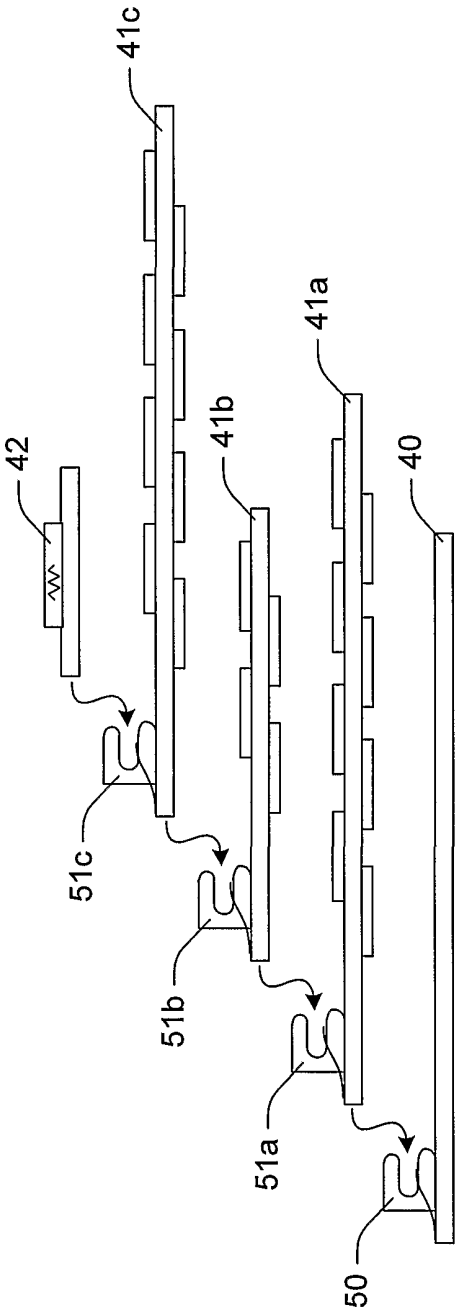


Fig. 4

Fig. 5A

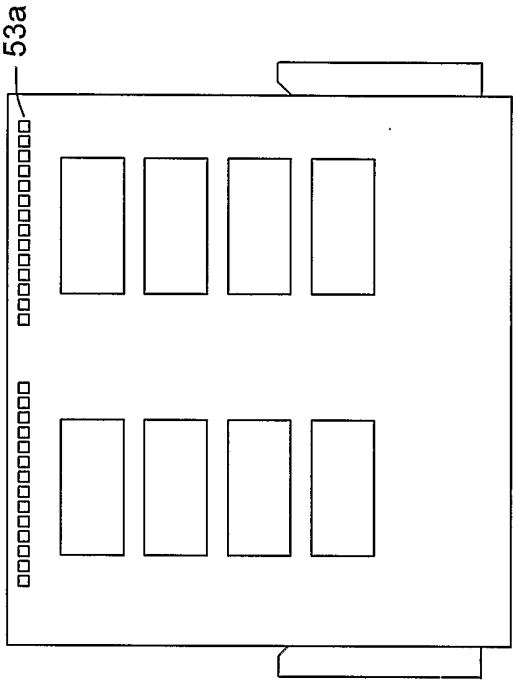


Fig. 5D

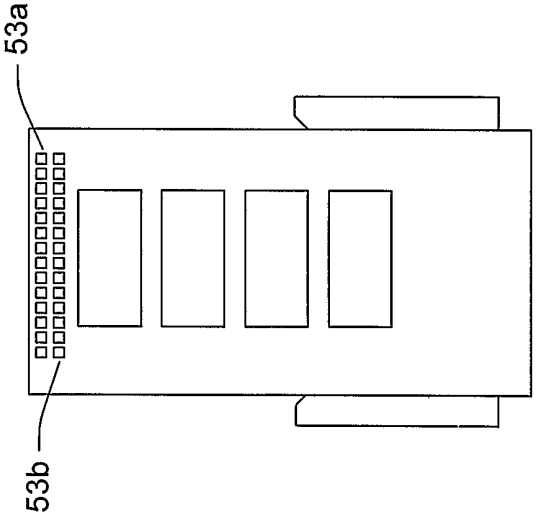


Fig. 5C

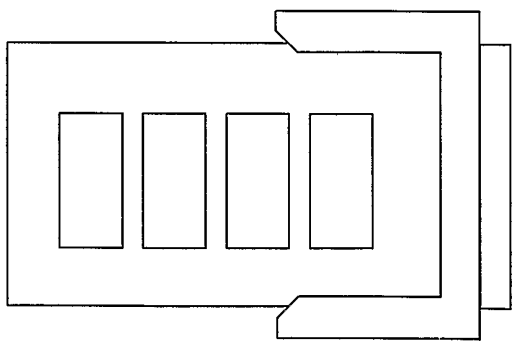


Fig. 5B

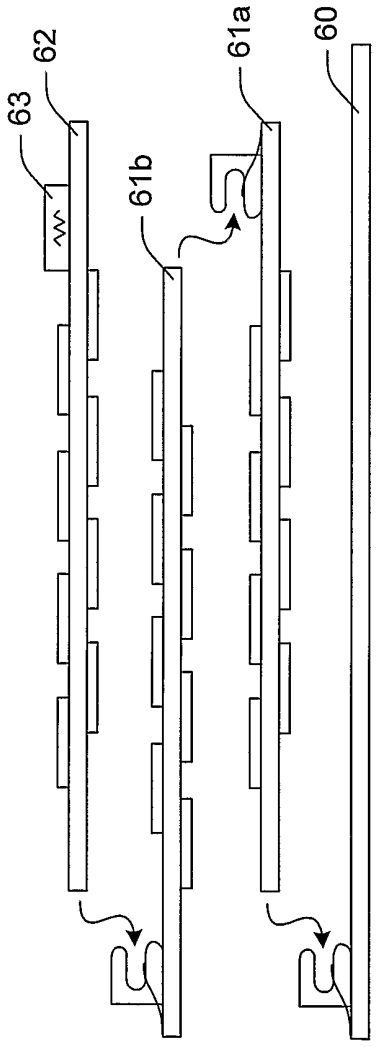


Fig. 6

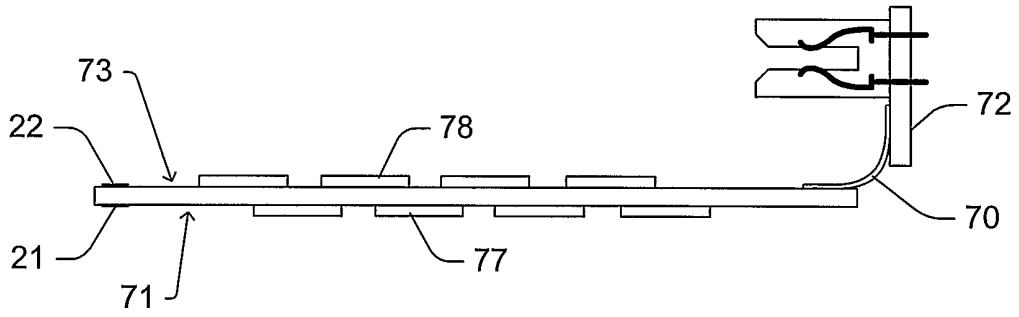


Fig. 7A

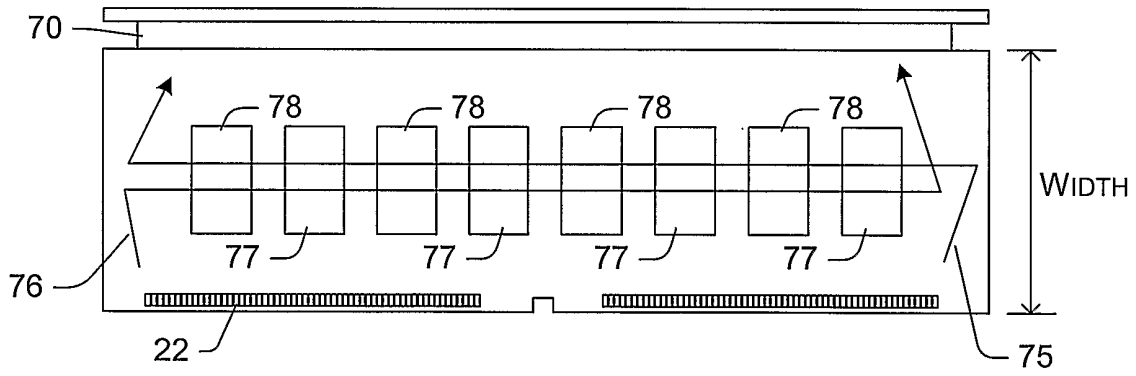


Fig. 7B

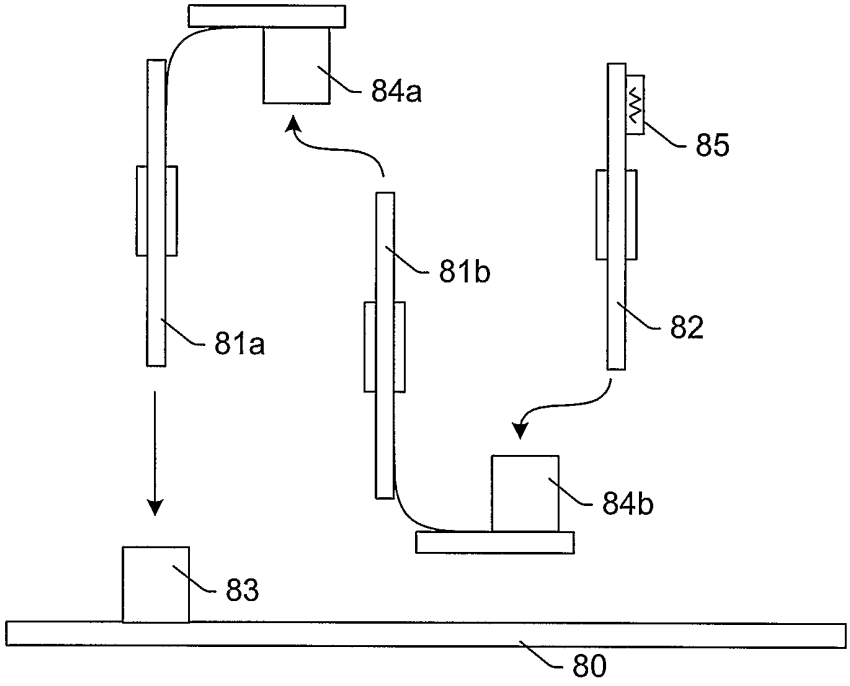


Fig. 8

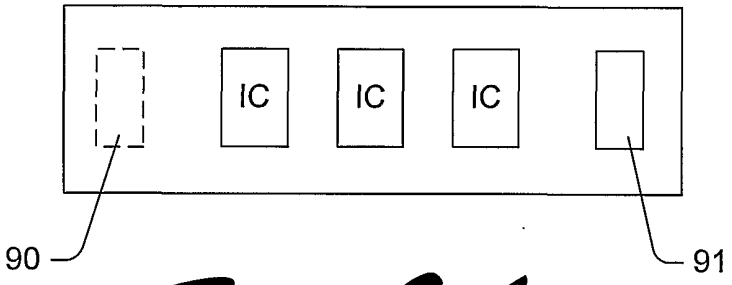


Fig. 9A

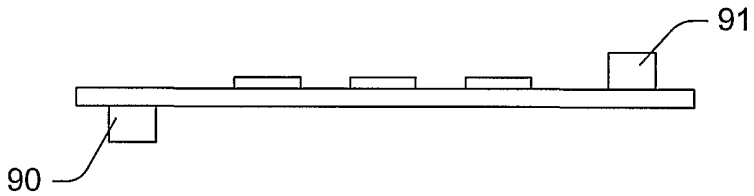


Fig. 9B

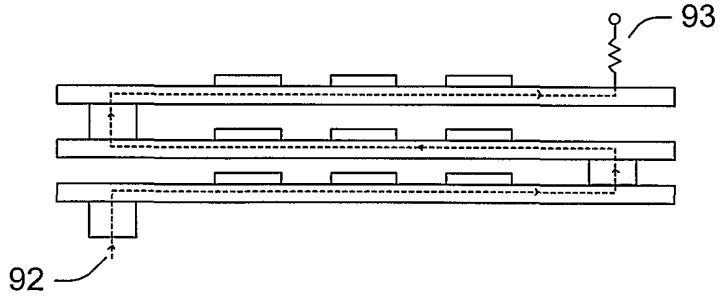


Fig. 9C

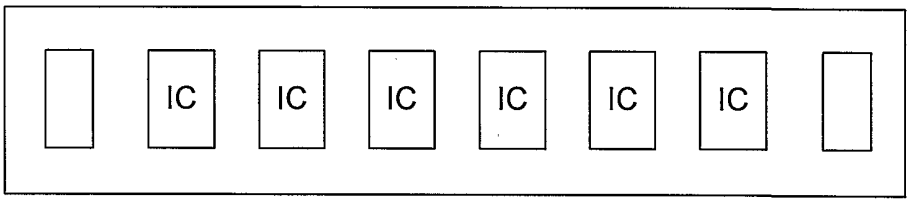


Fig. 10A

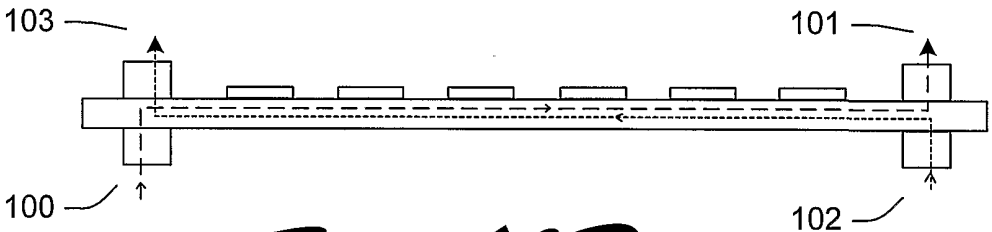


Fig. 10B

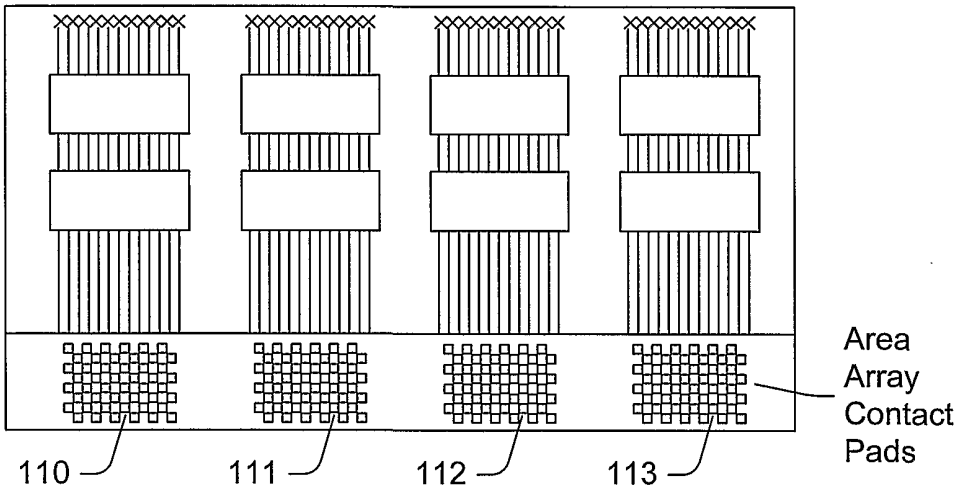


Fig. 11A

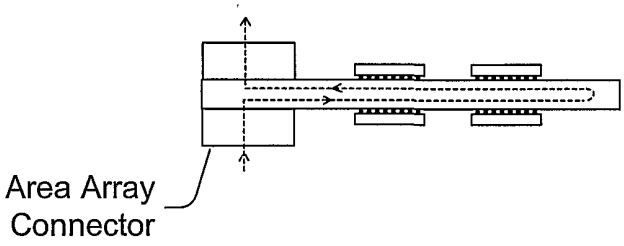


Fig. 11B

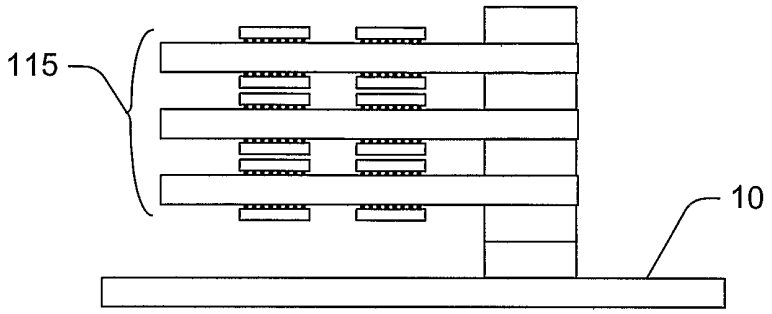


Fig. 11C

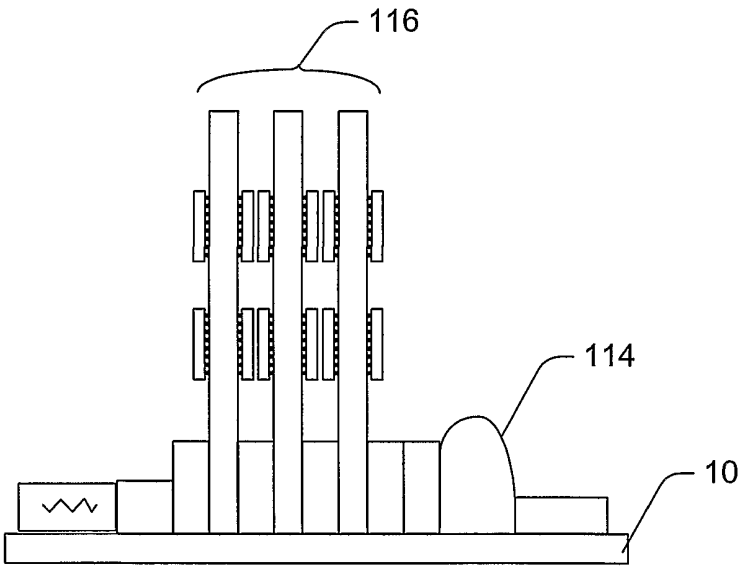


Fig. 11D

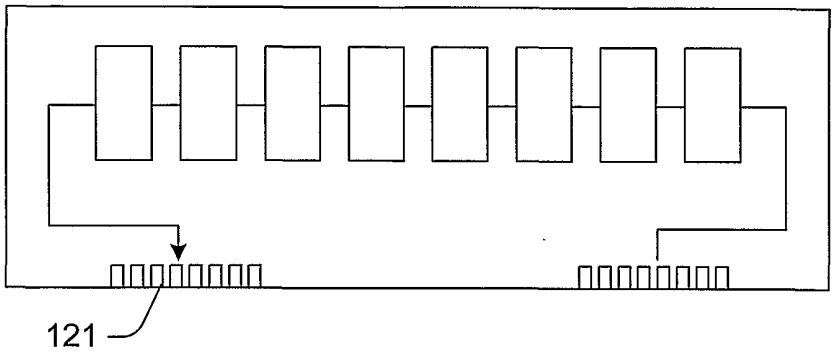


Fig. 12A

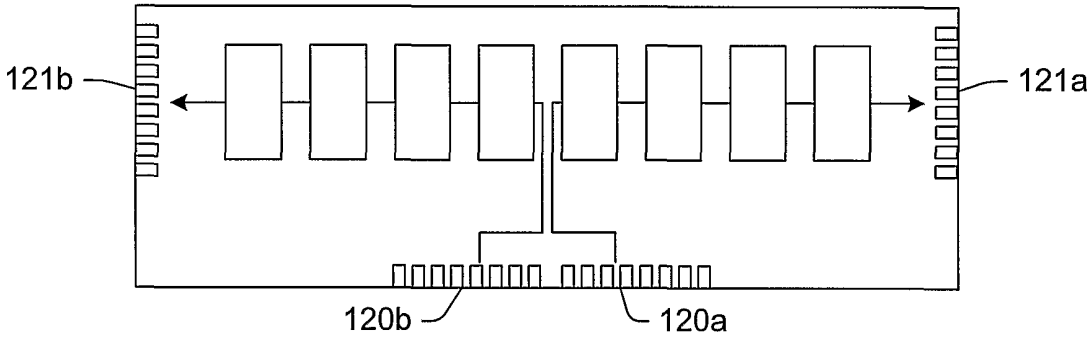


Fig. 12B

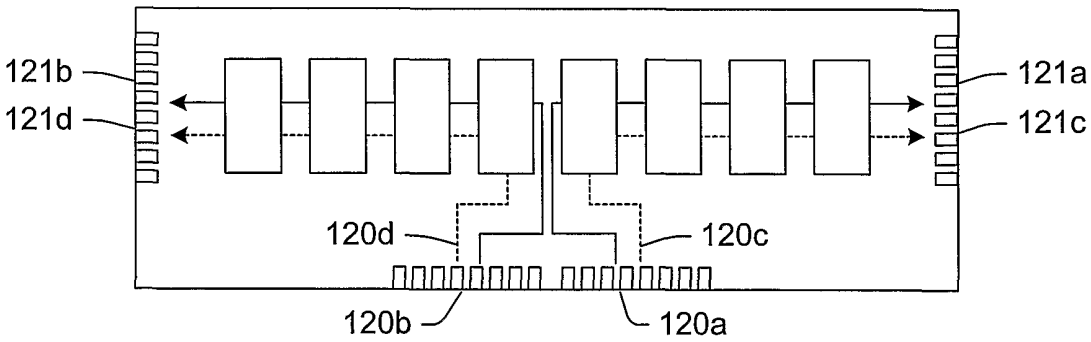


Fig. 12C

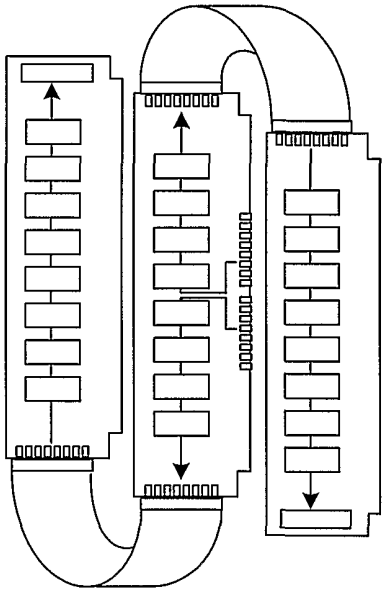


Fig. 13B

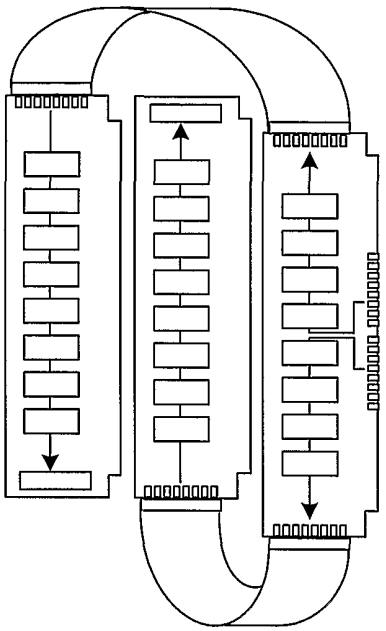


Fig. 13D

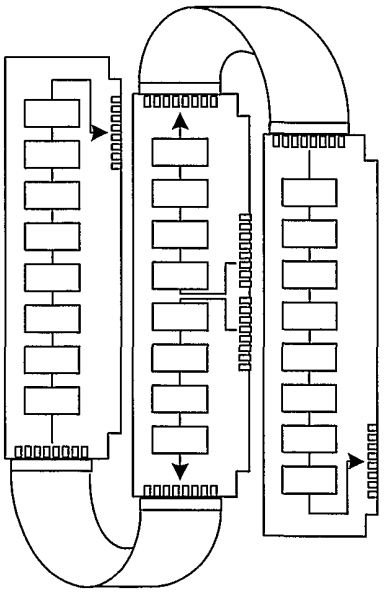


Fig. 13A

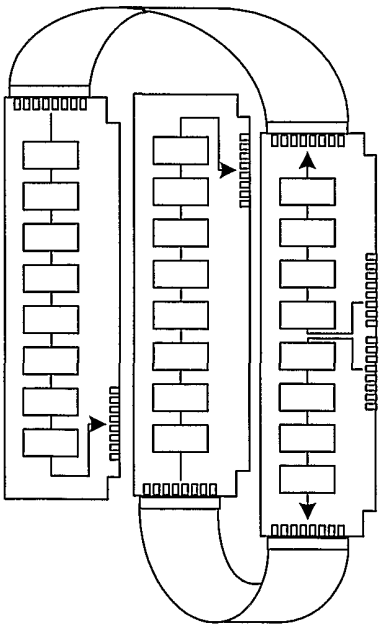


Fig. 13C

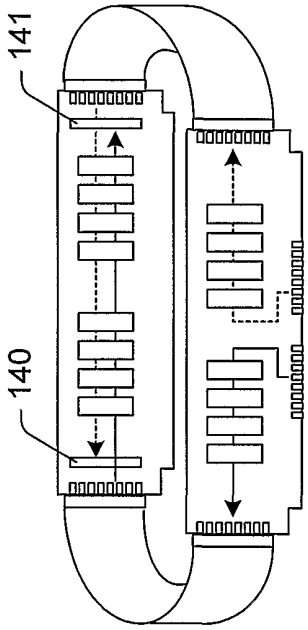


Fig. 14B

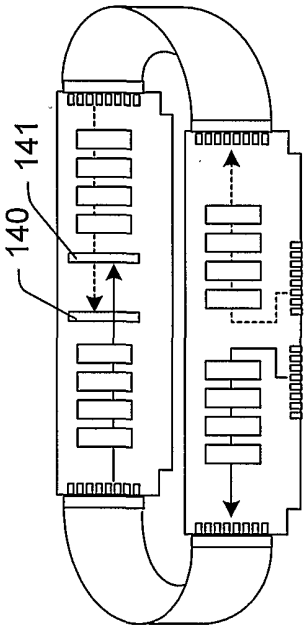


Fig. 14C

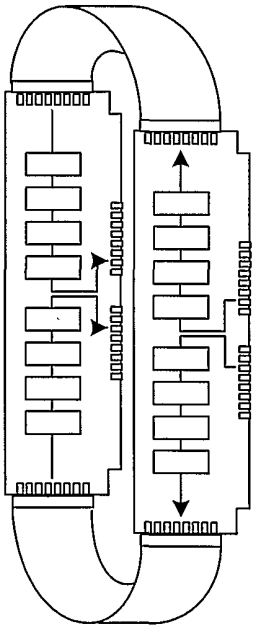


Fig. 14A

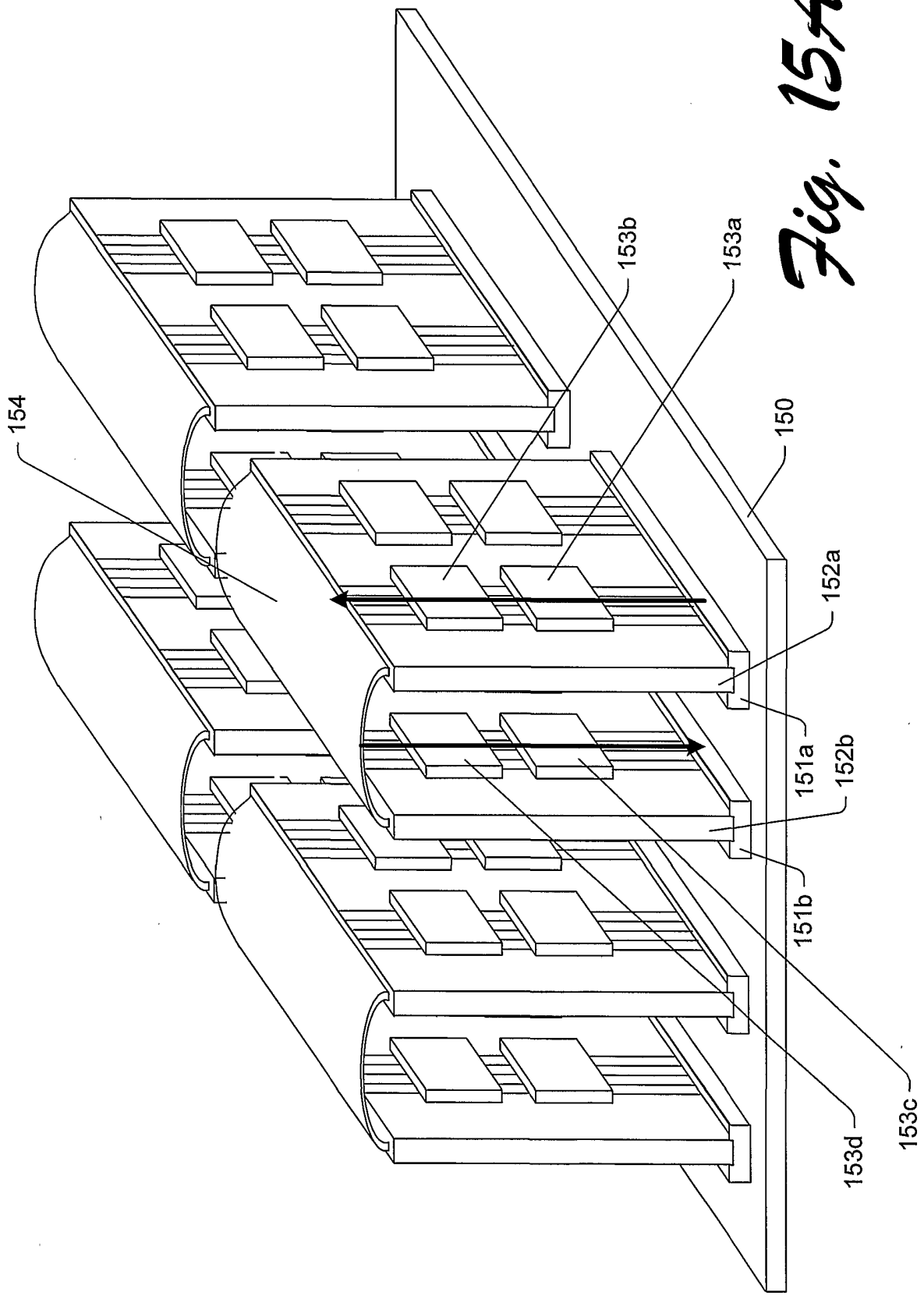


Fig. 154

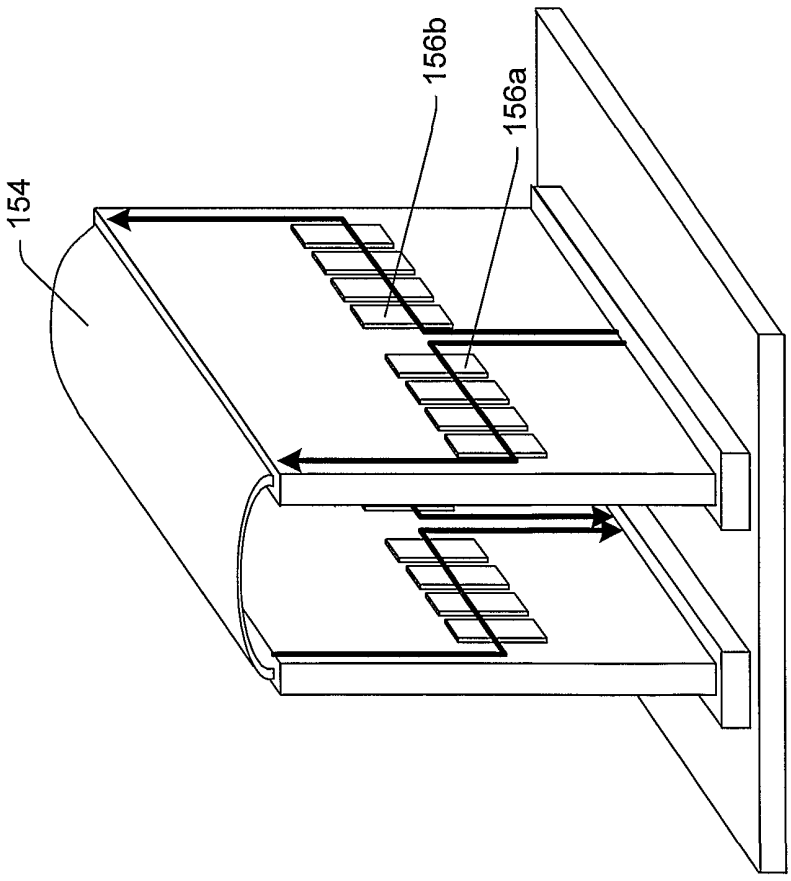


Fig. 15B

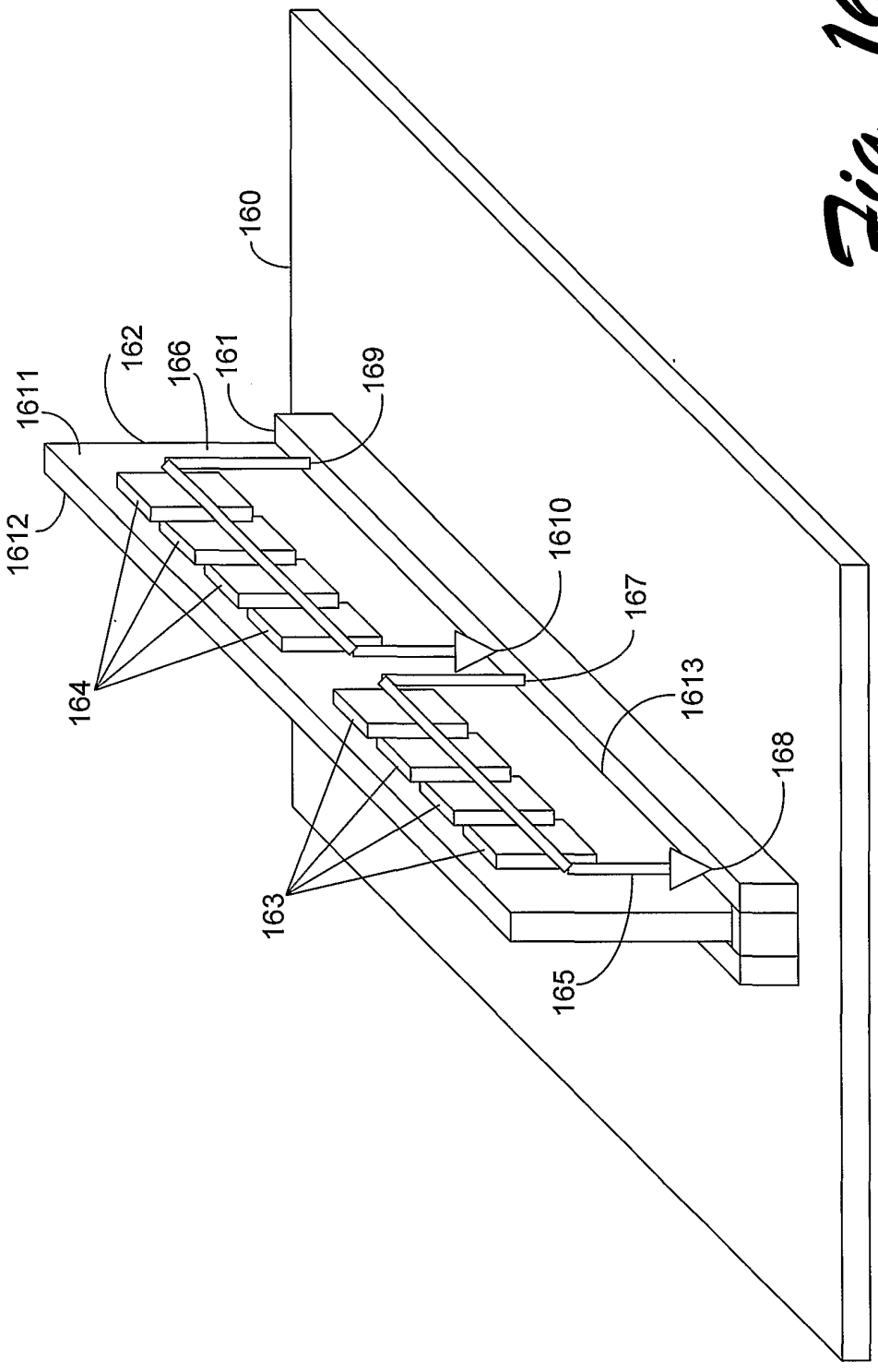
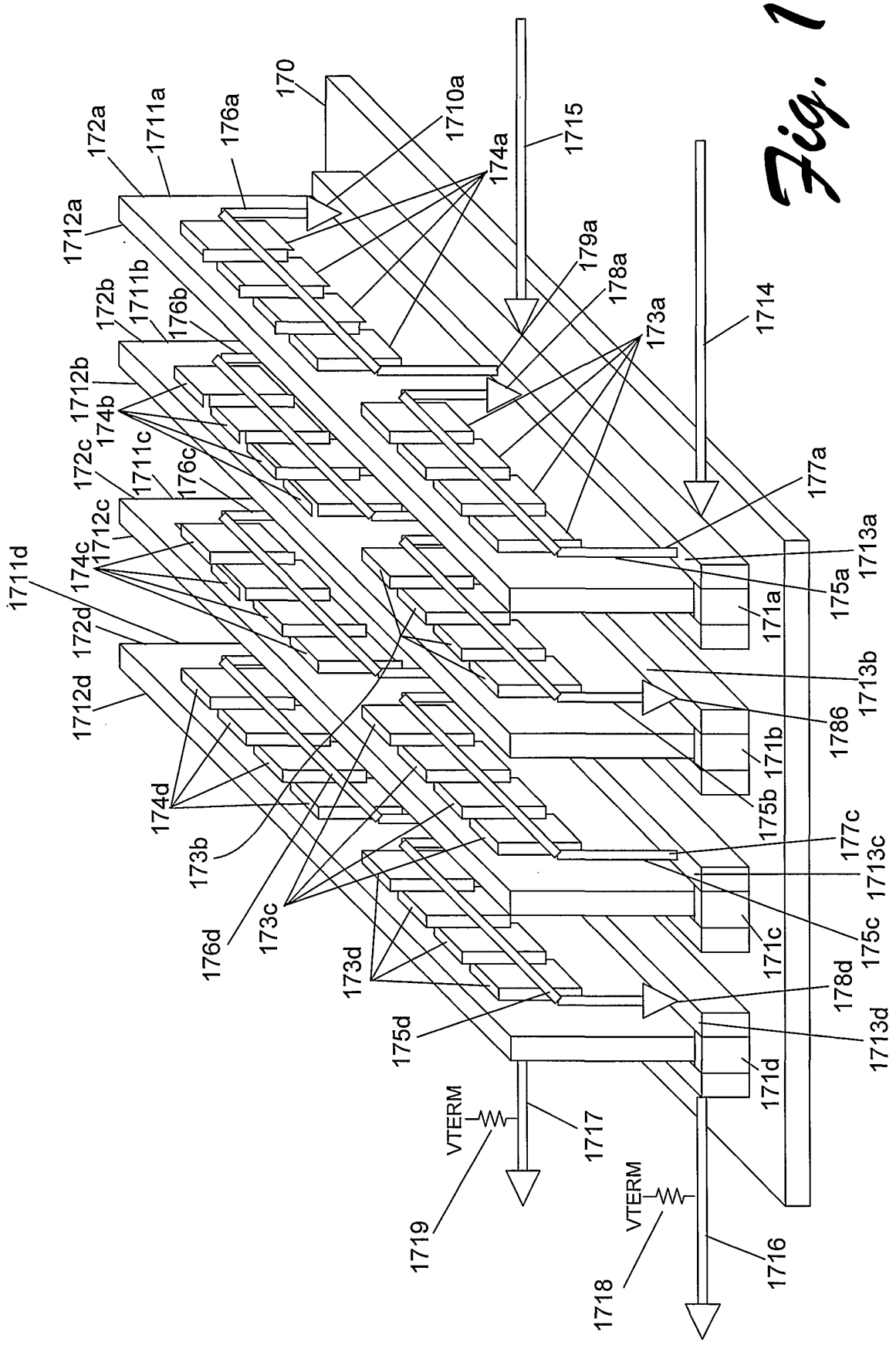


Fig. 16


170
1710a
1715
1714
1711a
1712a
172a
176a
174a
179a
178a
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1711b
1712b
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1713c
175c
171c
178d
1713d
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Fig. 17

Fig. 18

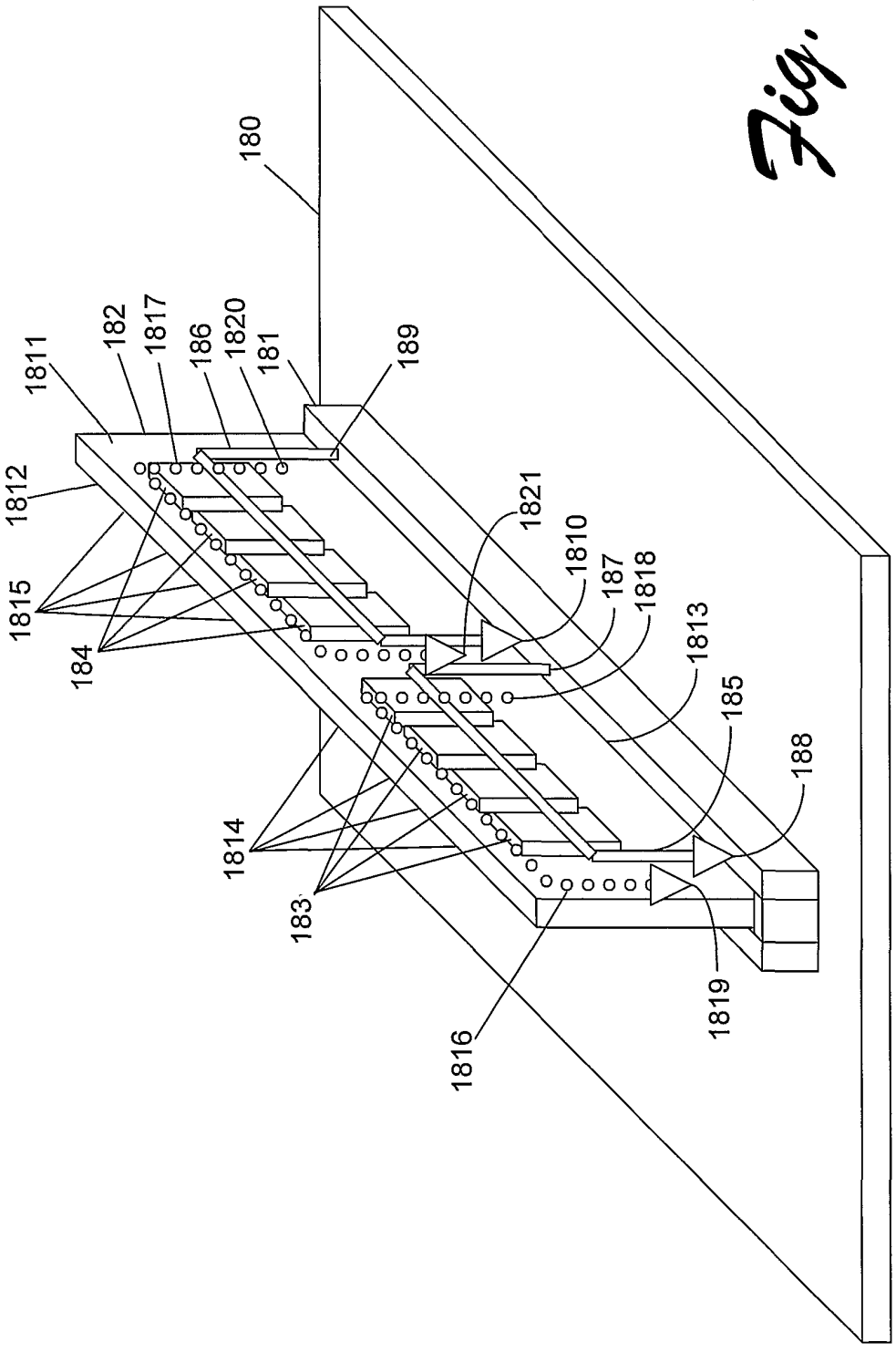
180
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Fig. 19

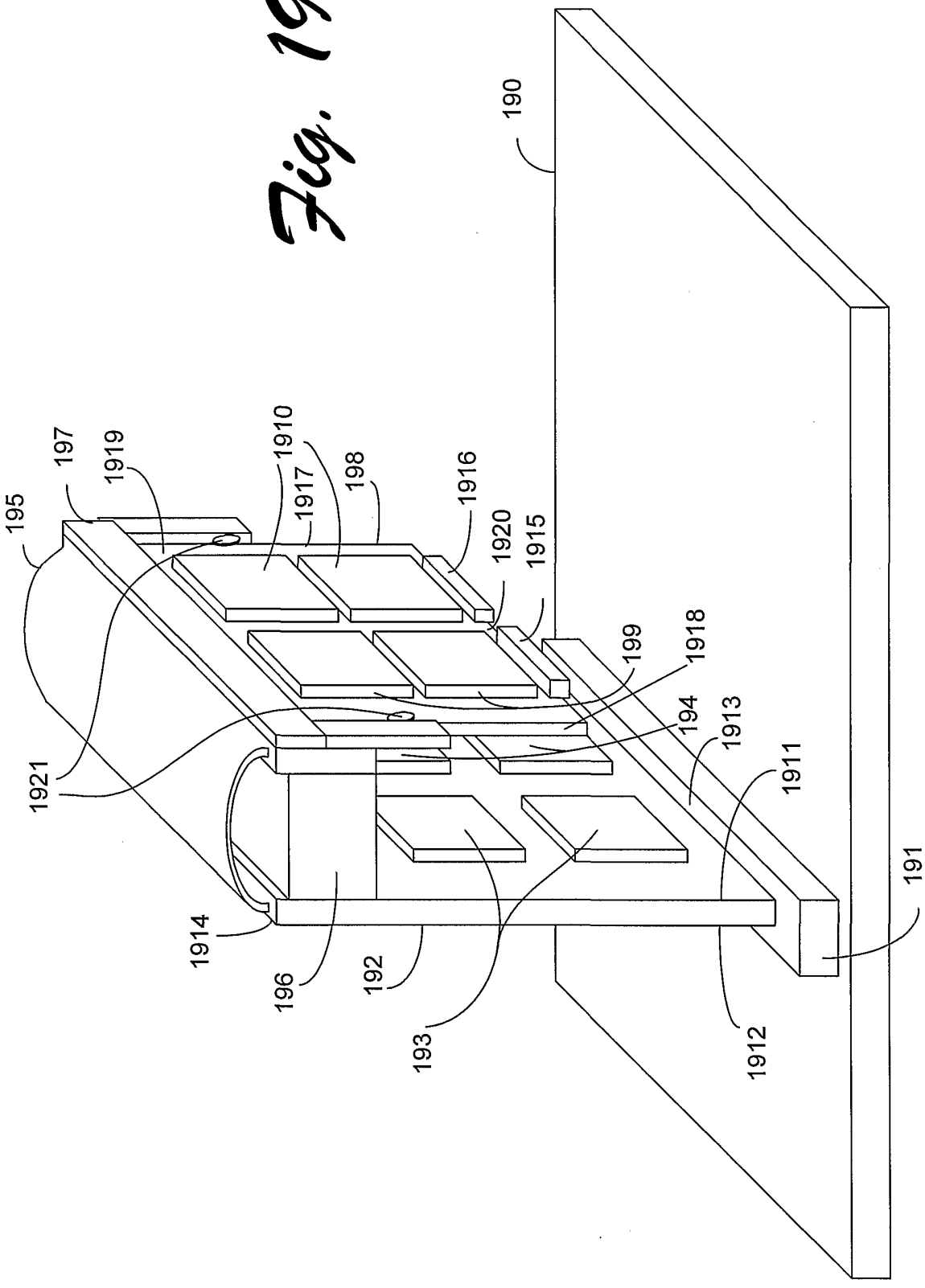
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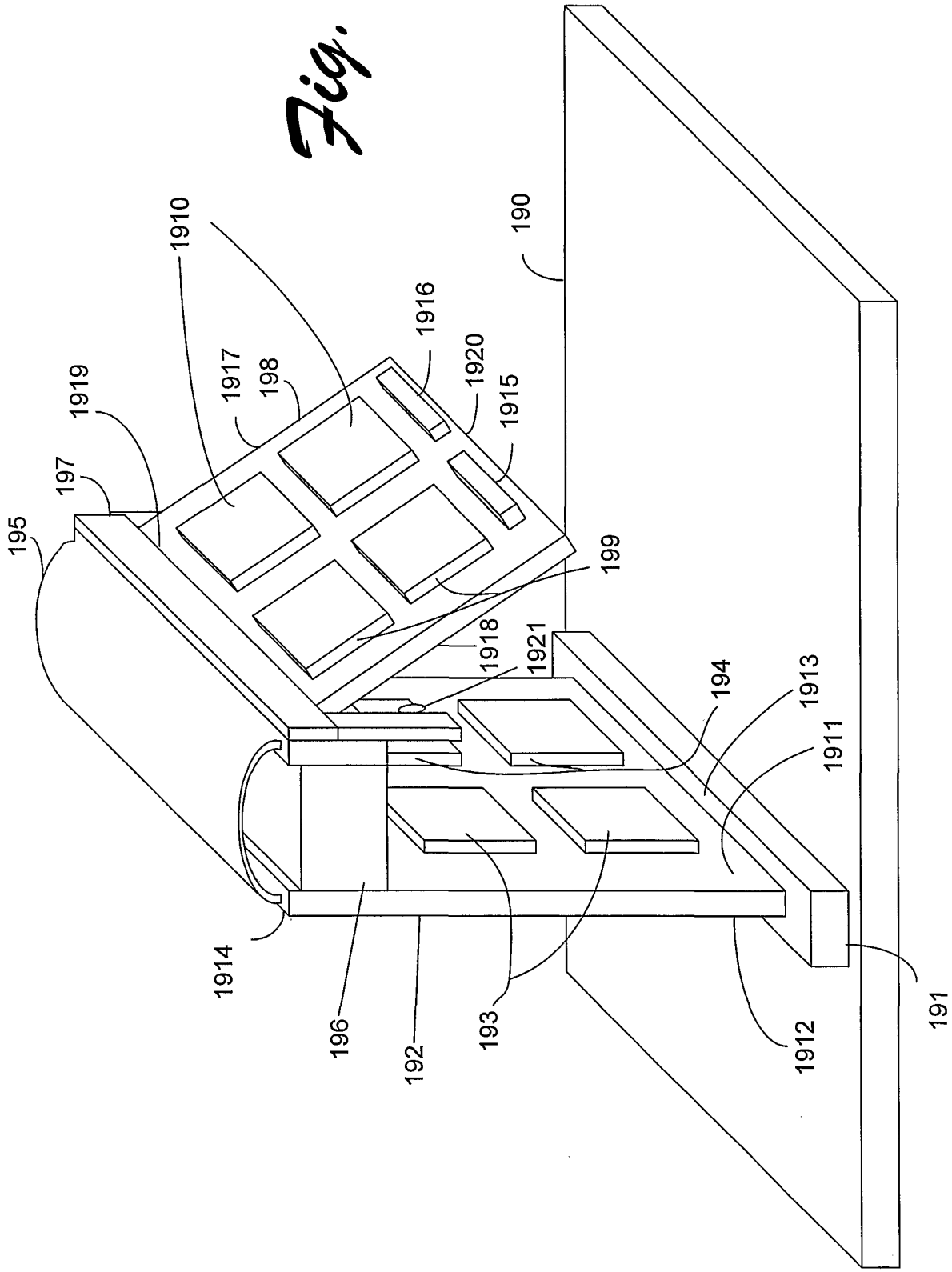
Fig. 20


1910
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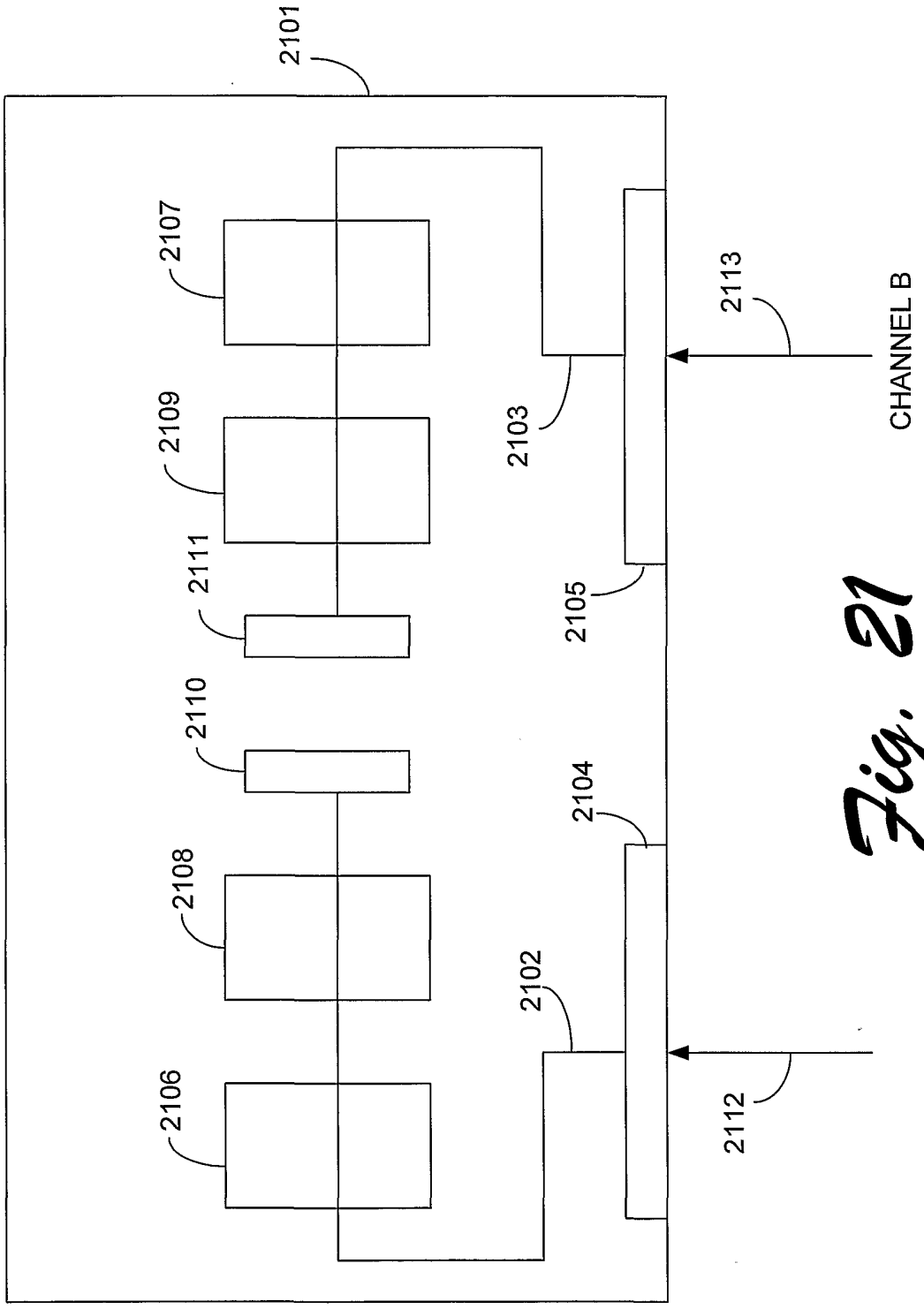
2101
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Fig. 21

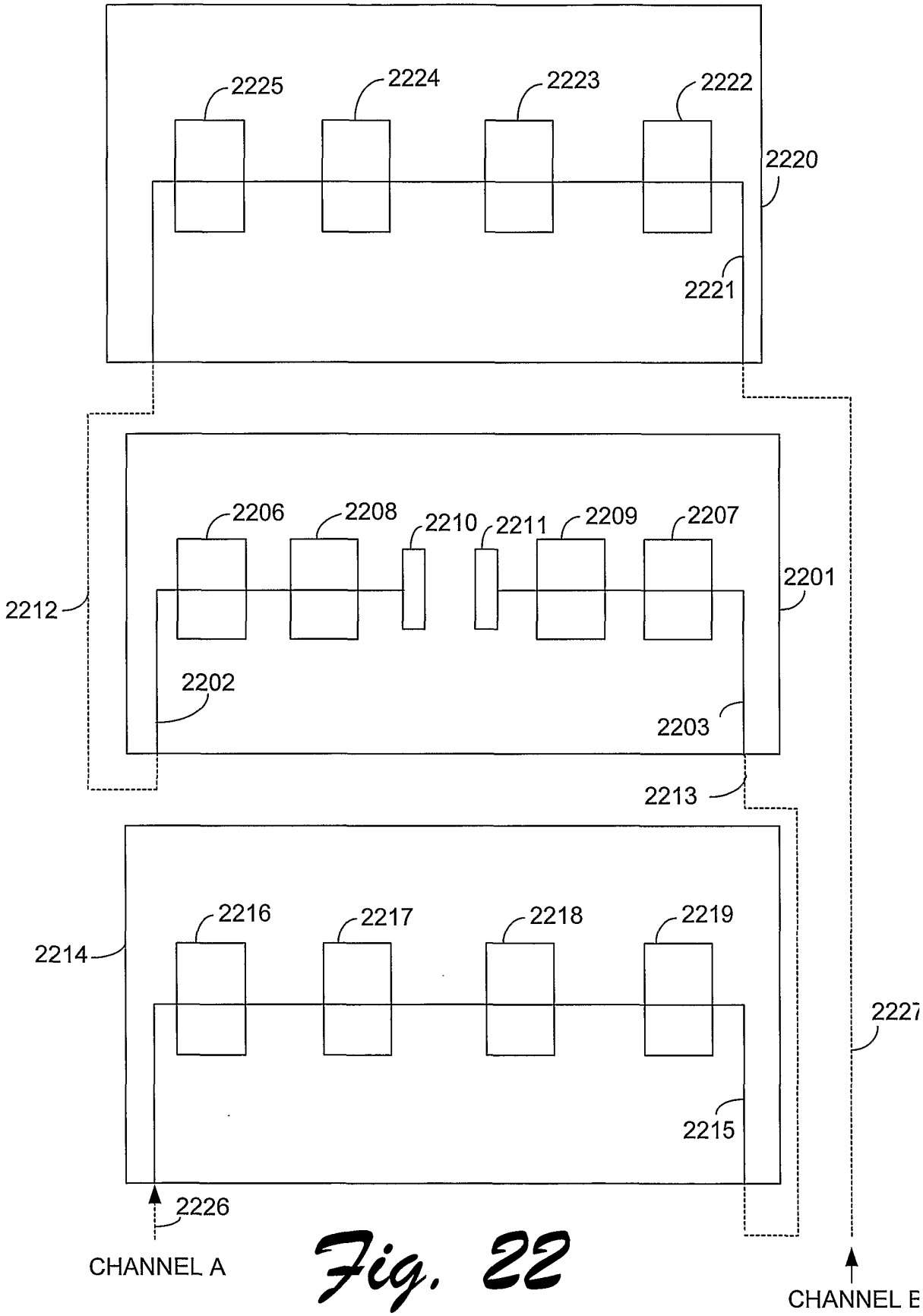
2225
2224
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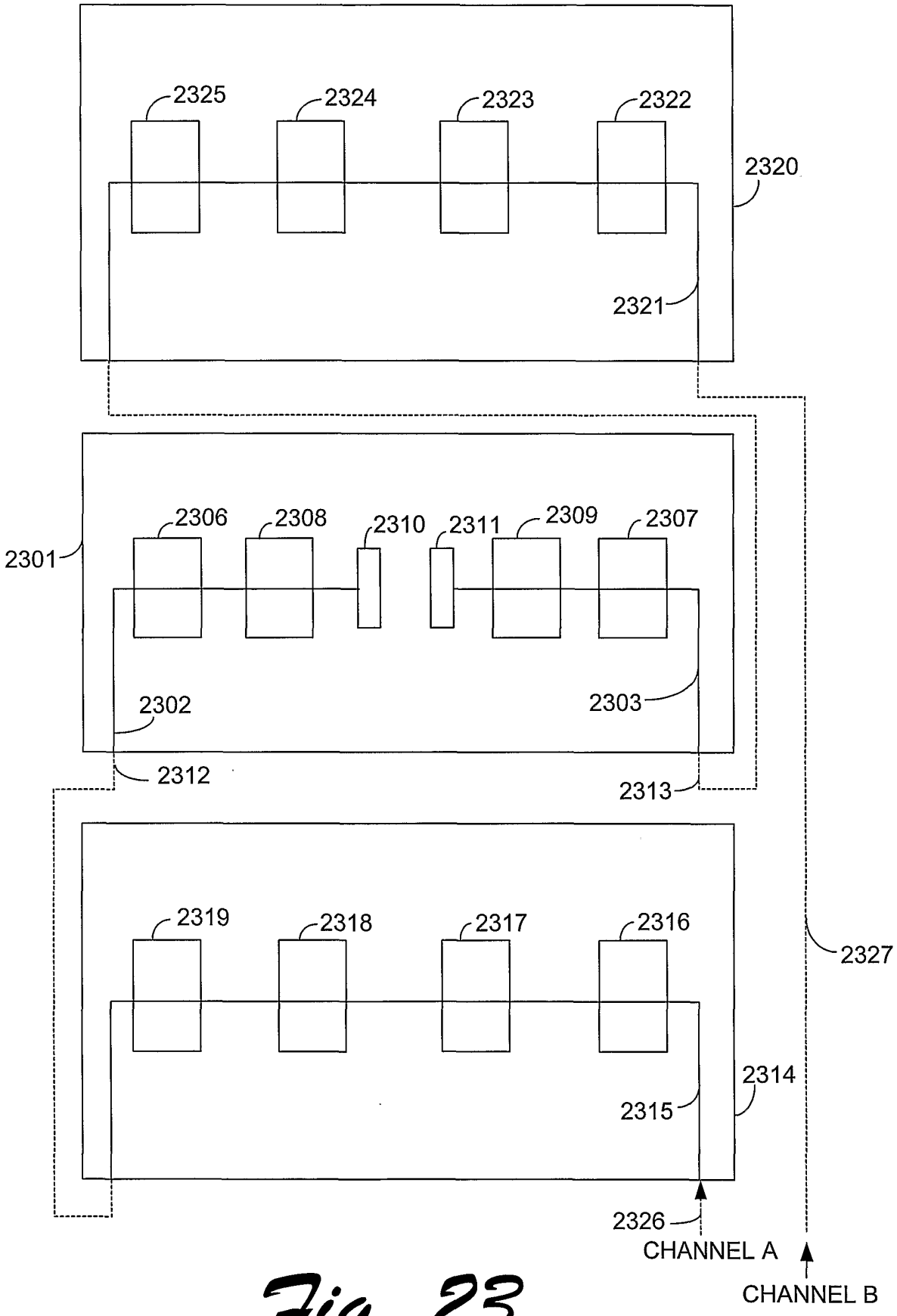
Fig. 22


2325
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CHANNEL A
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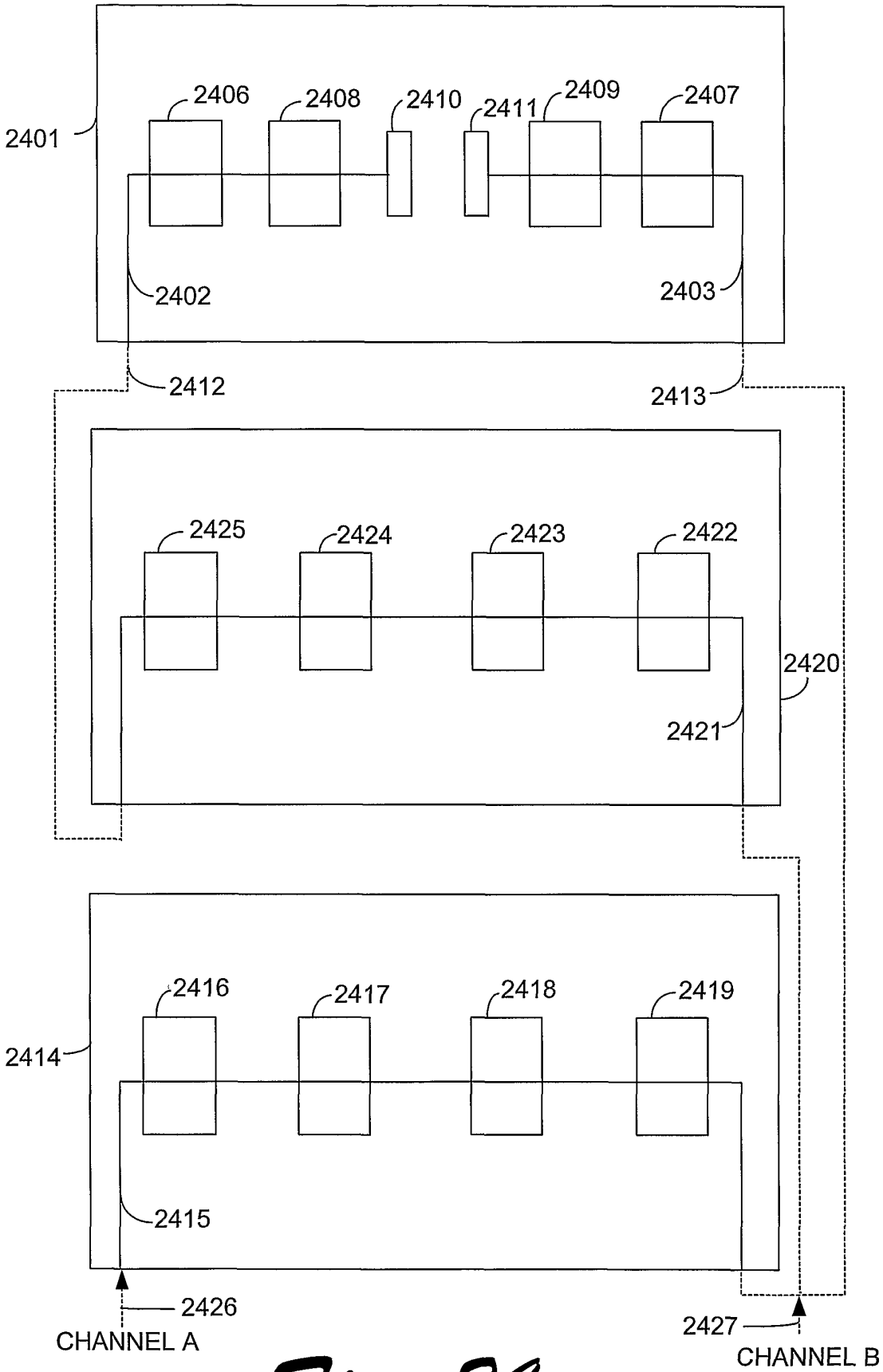
Fig. 23


2401
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CHANNEL A
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CHANNEL B

Fig. 24

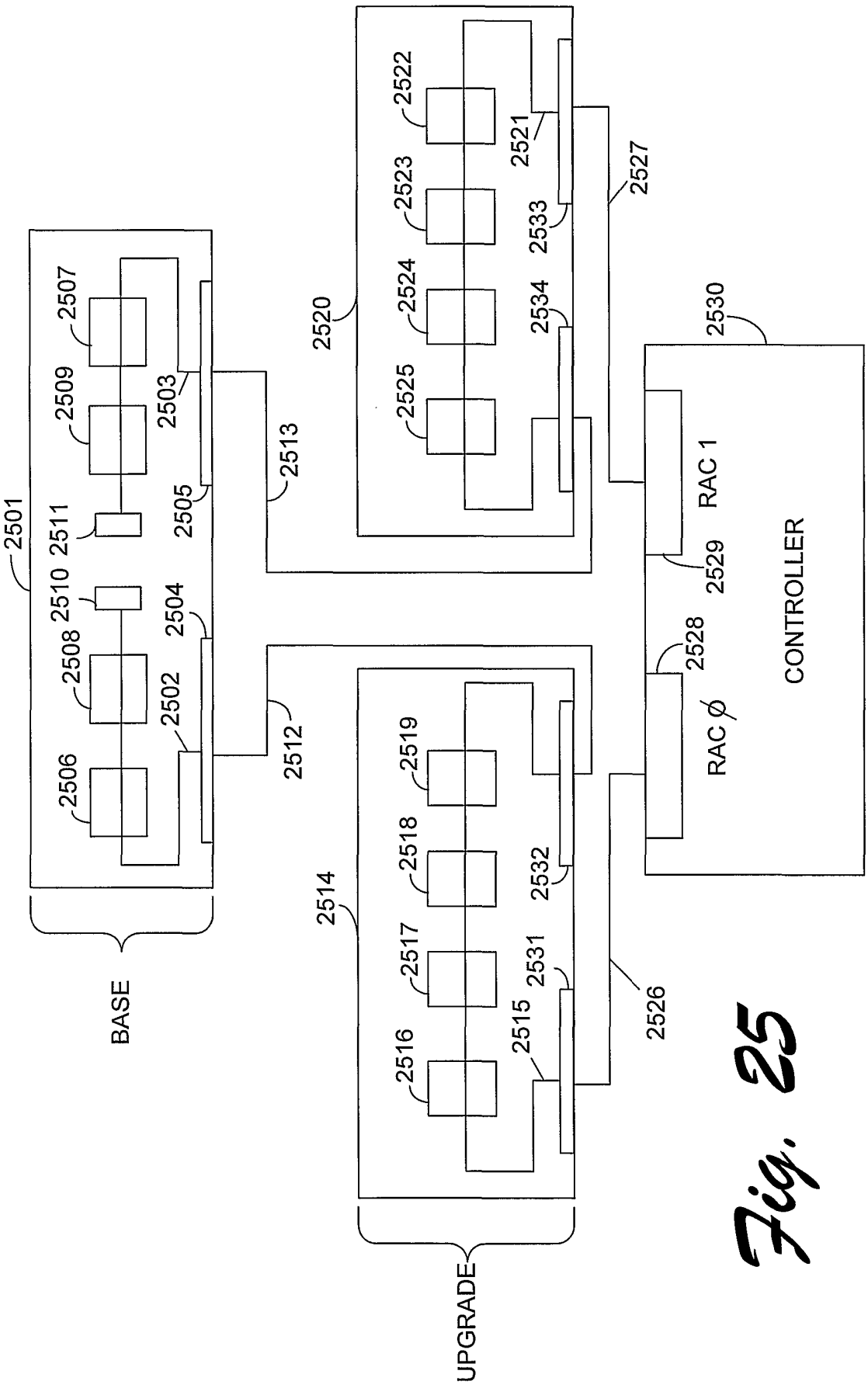
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Fig. 25

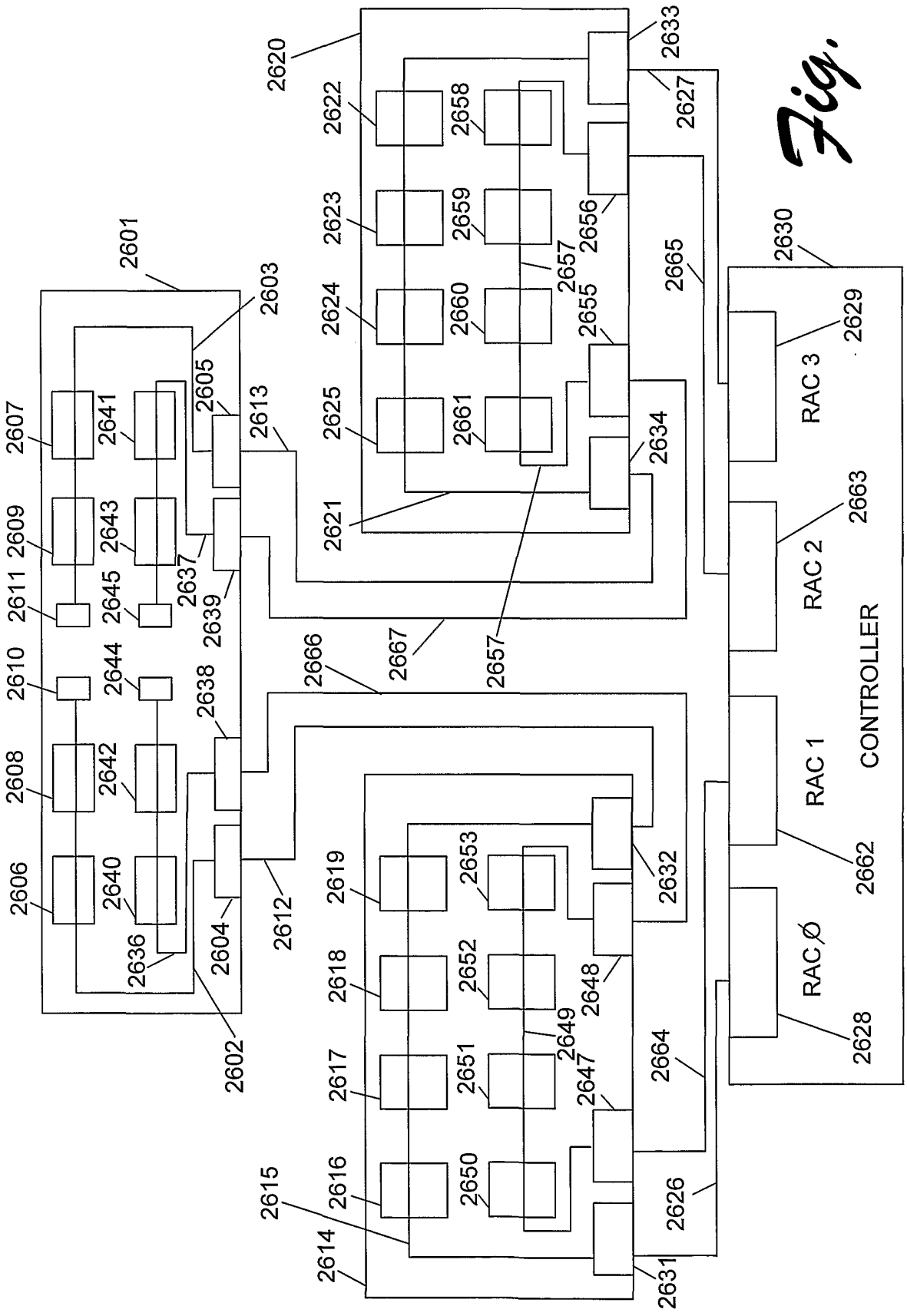
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Fig. 26

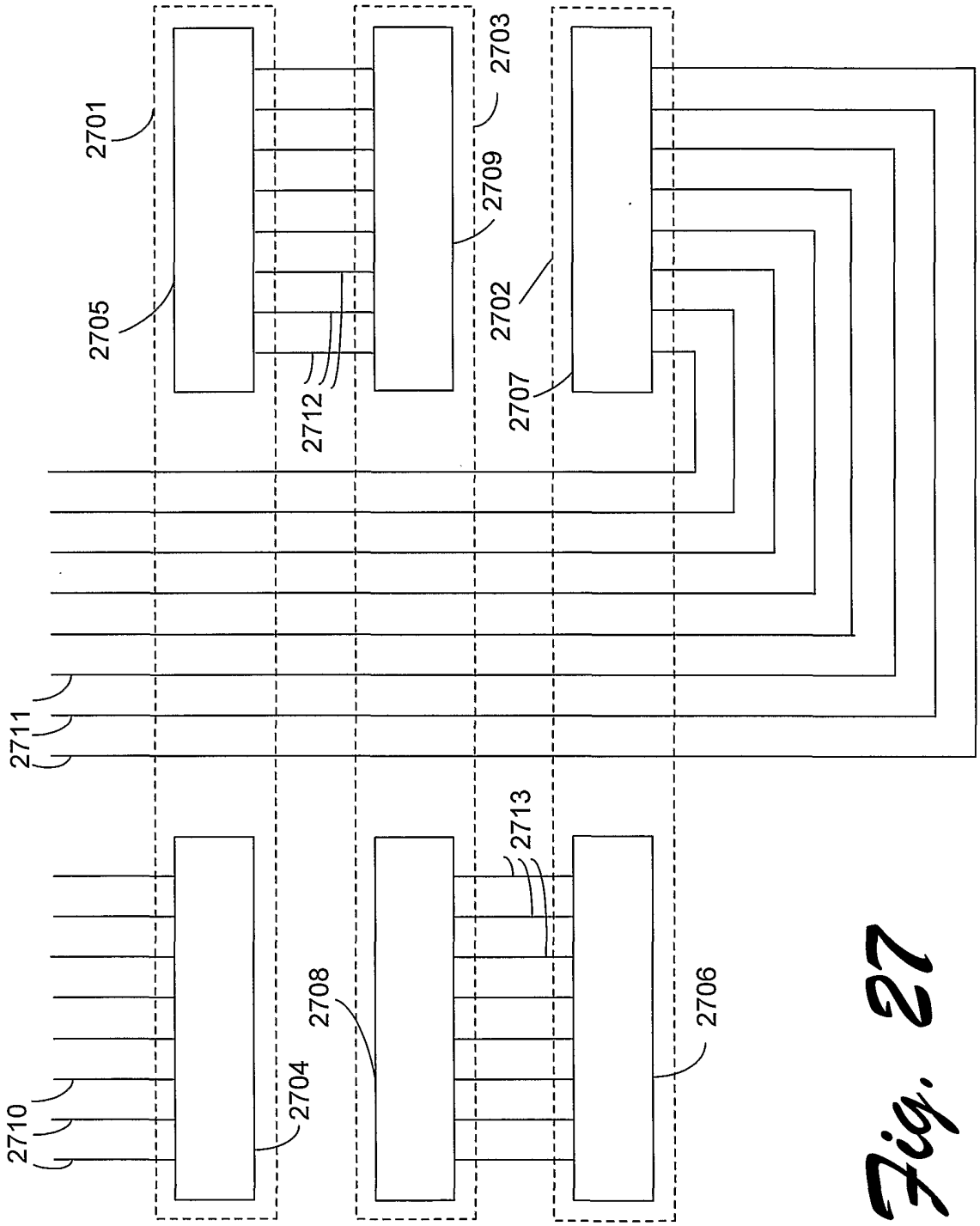
2701
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Fig. 27

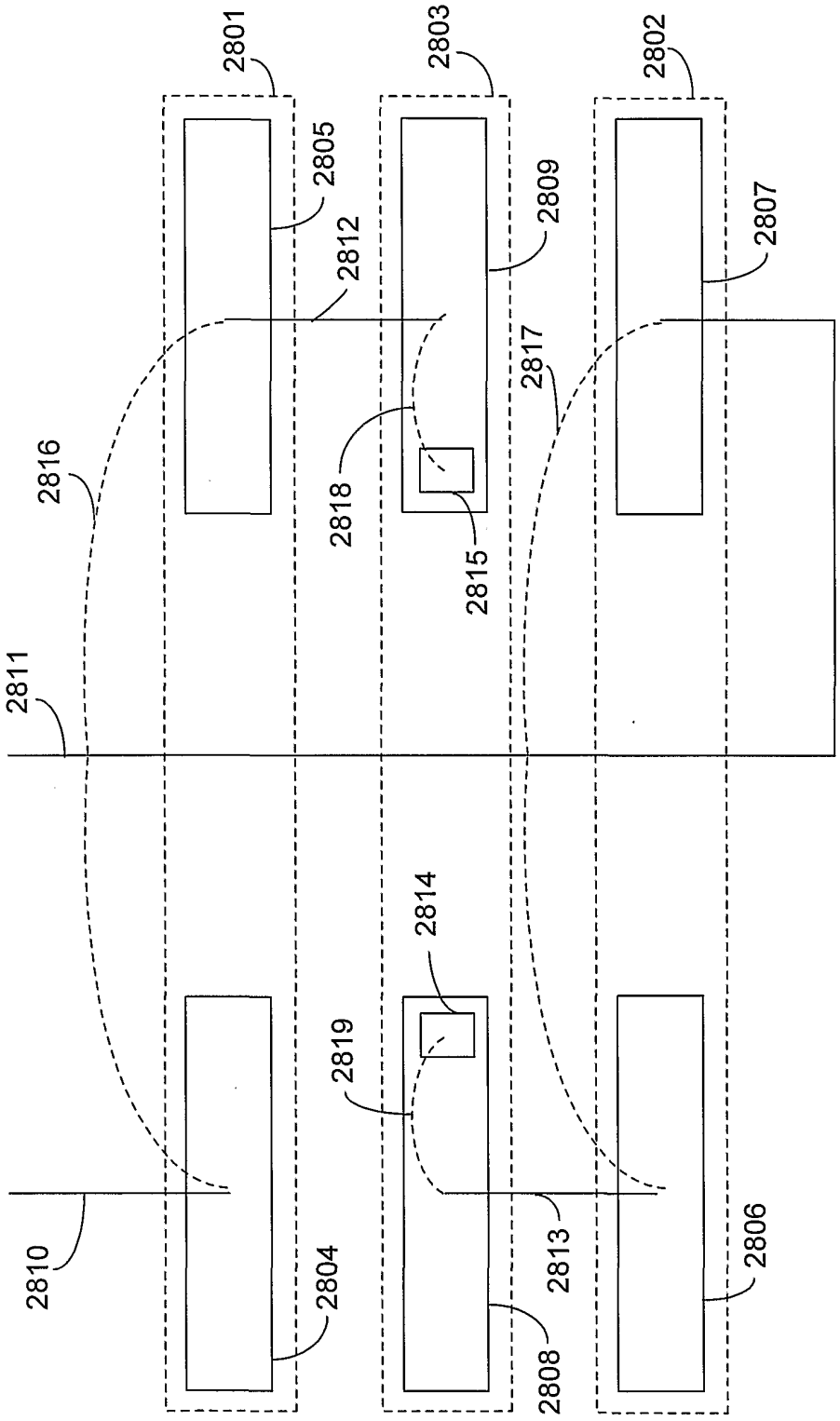
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Fig. 28

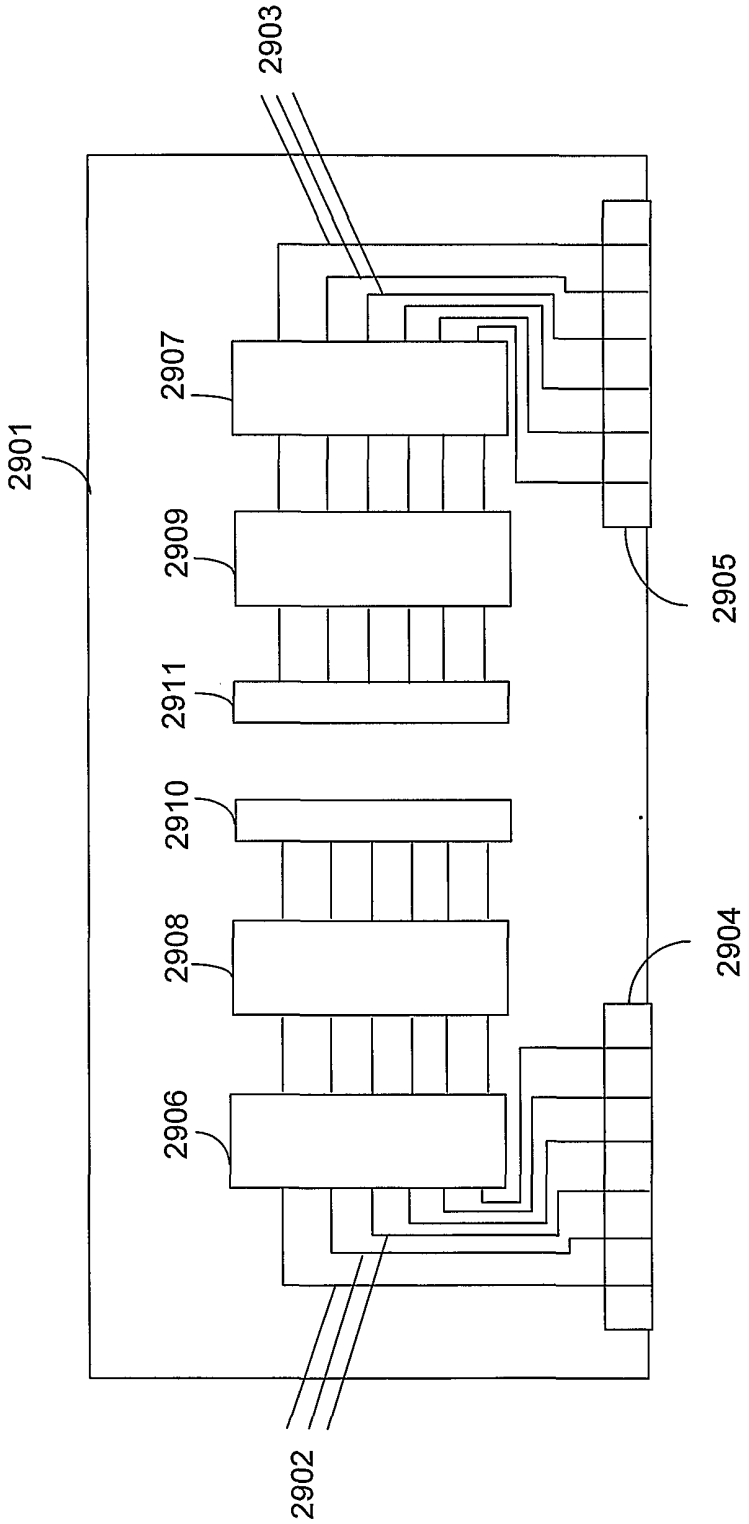


Fig. 29

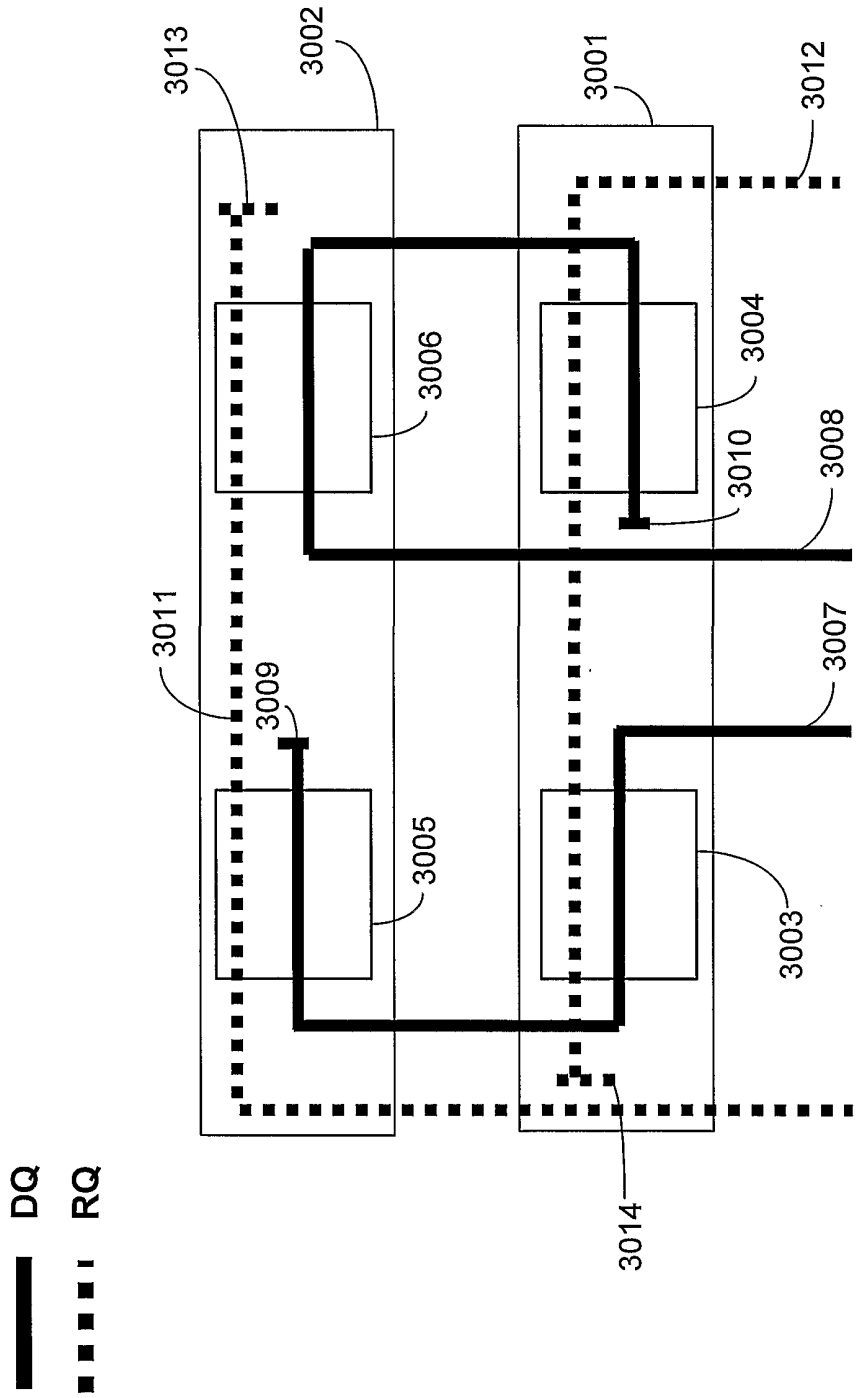

3013
3002
3001
3012
3006
3004
3010
3008
3011
3009
3007
3005
3003
3014
DQ
RQ

Fig. 30

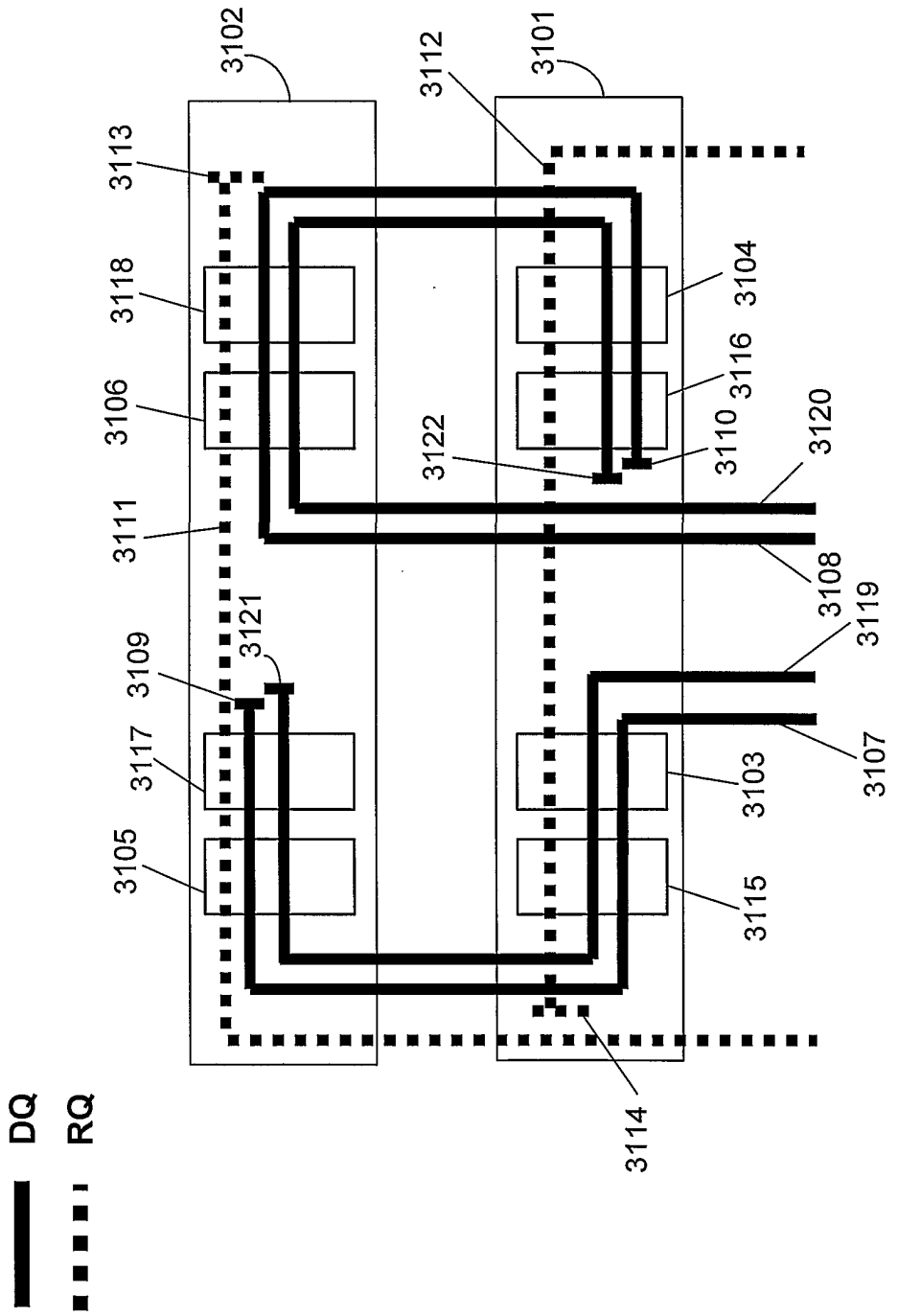

3102
3112
3101
3113
3118
3104
3106
3116
3110
3120
3122
3111
3108
3119
3121
3109
3107
3117
3103
3105
3115
3114
DQ
RQ

Fig. 31

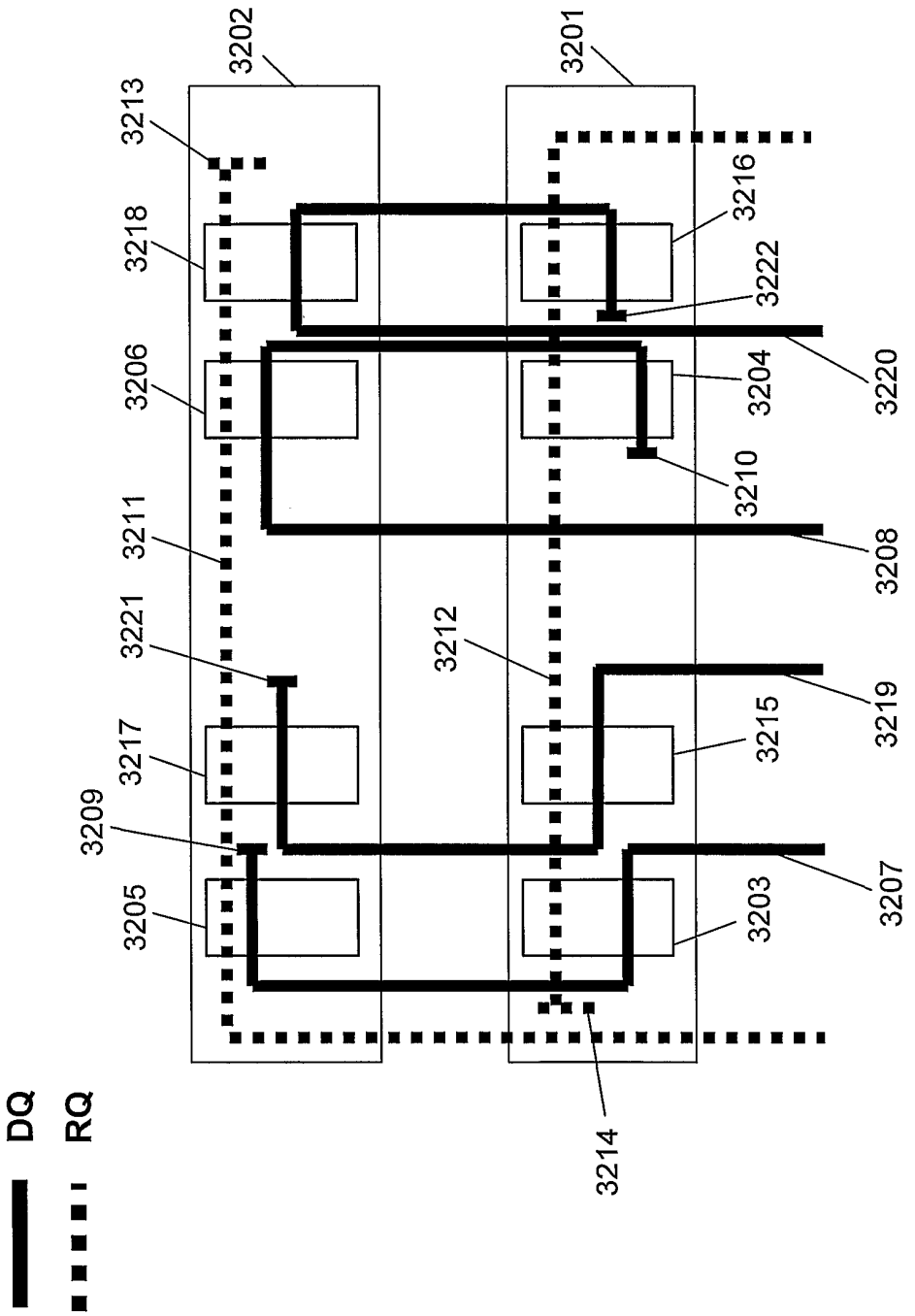

3202
3201
3213
3218
3216
3222
3206
3204
3220
3210
3211
3208
3221
3212
3219
3217
3215
3209
3207
3205
3203
3214
DQ
RQ

Fig. 32

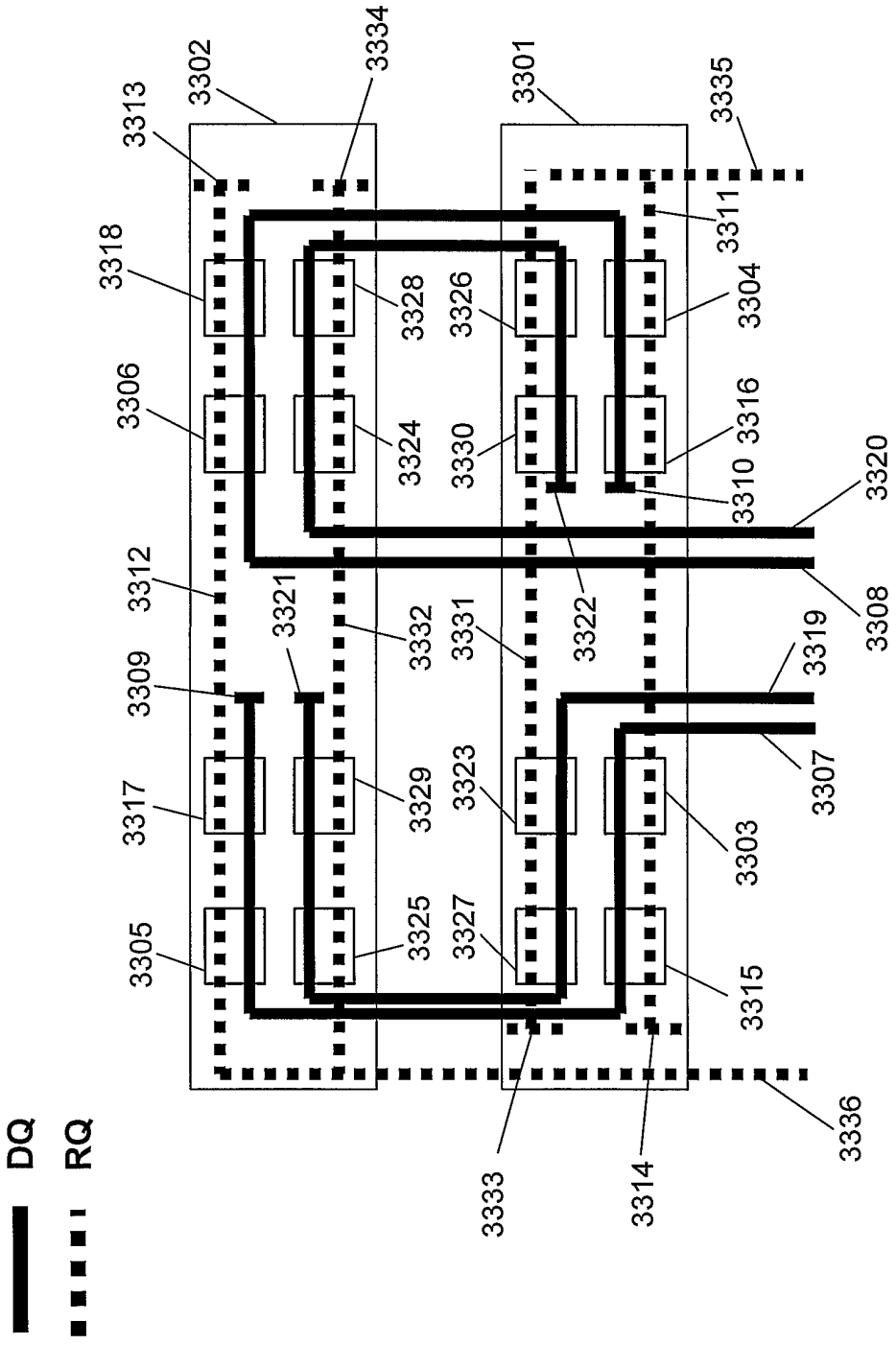
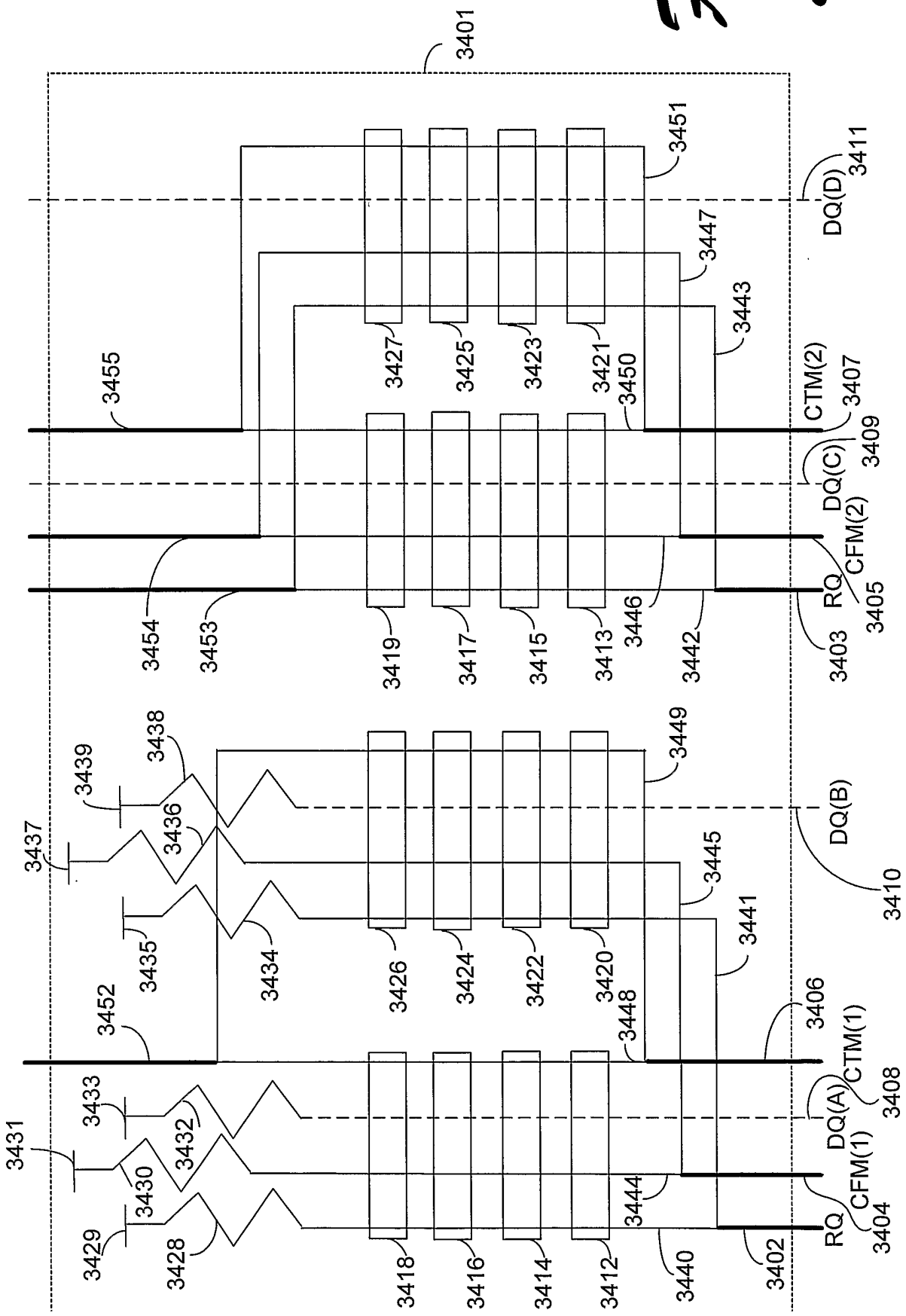

DQ
RQ
3302
3334
3301
3335
3313
3311
3318
3328
3326
3304
3306
3324
3330
3316
3310
3320
3312
3321
3332
3331
3322
3308
3319
3309
3307
3317
3329
3323
3303
3325
3327
3315
3305
3333
3314
3336

Fig. 33

Fig. 34


3401
3451
3411
DQ(D)
3447
3443
3455
3427
3425
3423
3421
3450
CTM(2)
3407
3409
DQ(C)
CFM(2)
RQ
3405
3454
3453
3419
3417
3415
3413
3446
3442
3403
3439
3438
3449
DQ(B)
3437
3436
3445
3441
3435
3434
3426
3424
3422
3420
3410
3452
3448
3406
CTM(1)
3408
3433
DQ(A)
3431
3432
CFM(1)
3430
3444
RQ
3404
3429
3428
3418
3416
3414
3412
3440
3402

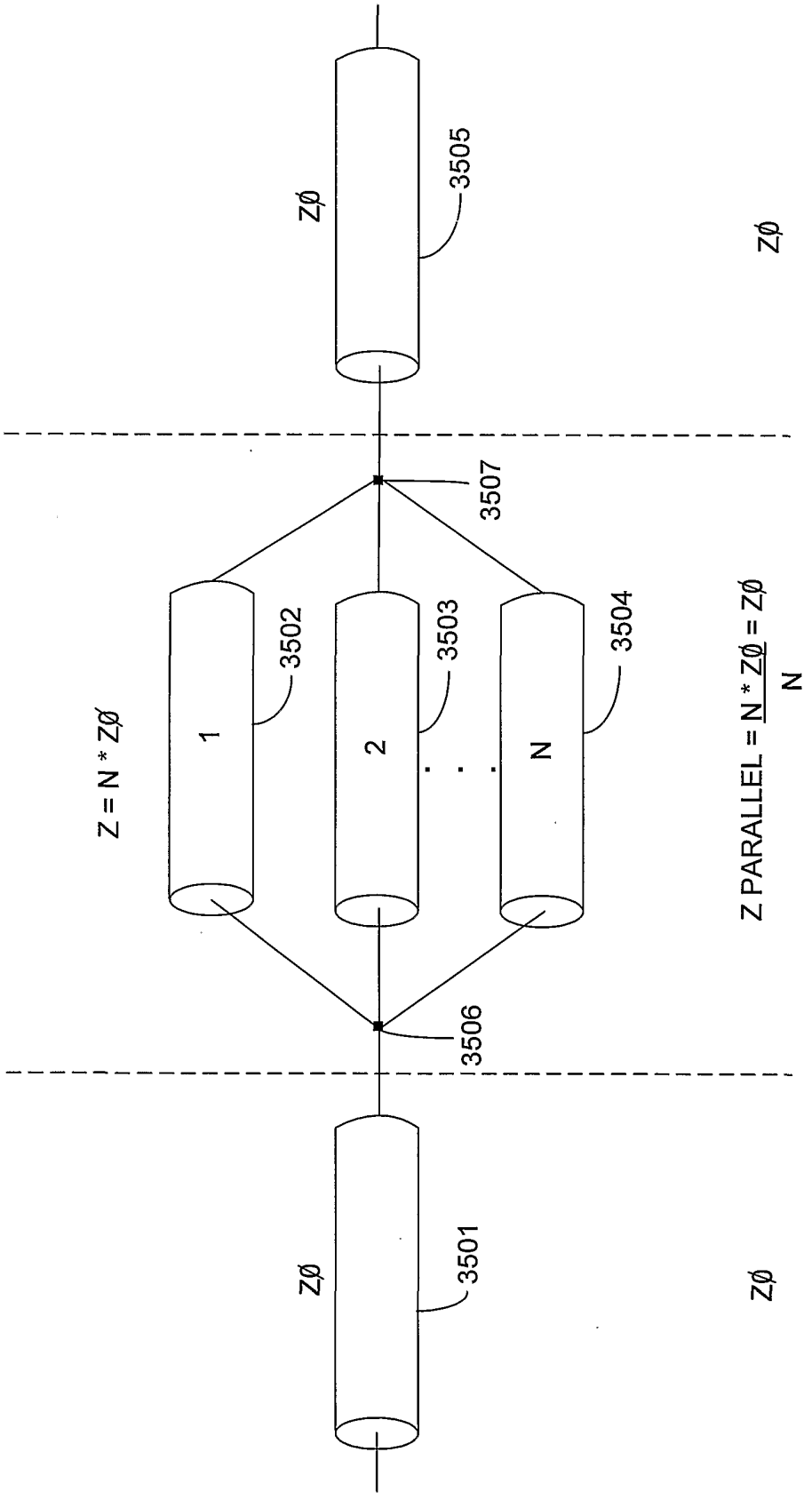

Zø
3505
Zø
3507
1
3502
2
3503
N
3504
Z = N * Zø
Z PARALLEL = N * Zø = Zø
N
3506
Zø
3501
Zø

Fig. 35

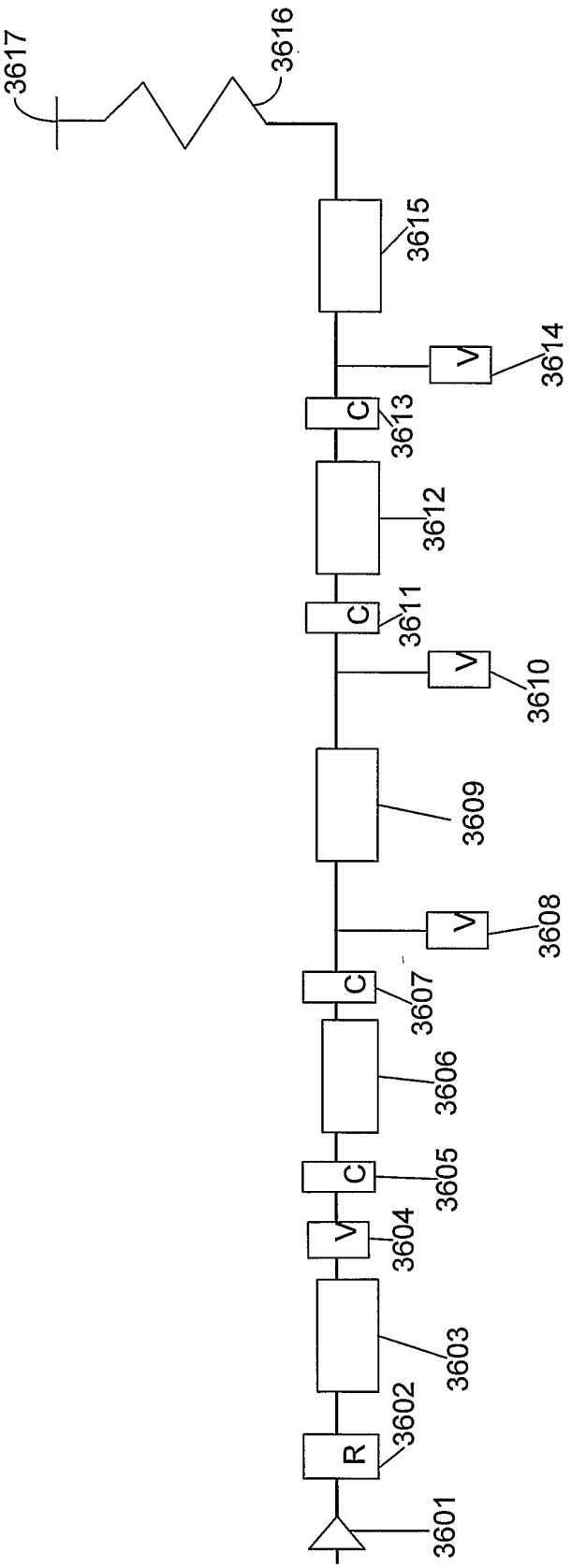

3617
3616
3615
V
3614
C
3613
3612
C
3611
V
3610
3609
V
3608
C
3607
3606
C
3605
V
3604
3603
3602
R
3601

Fig. 36

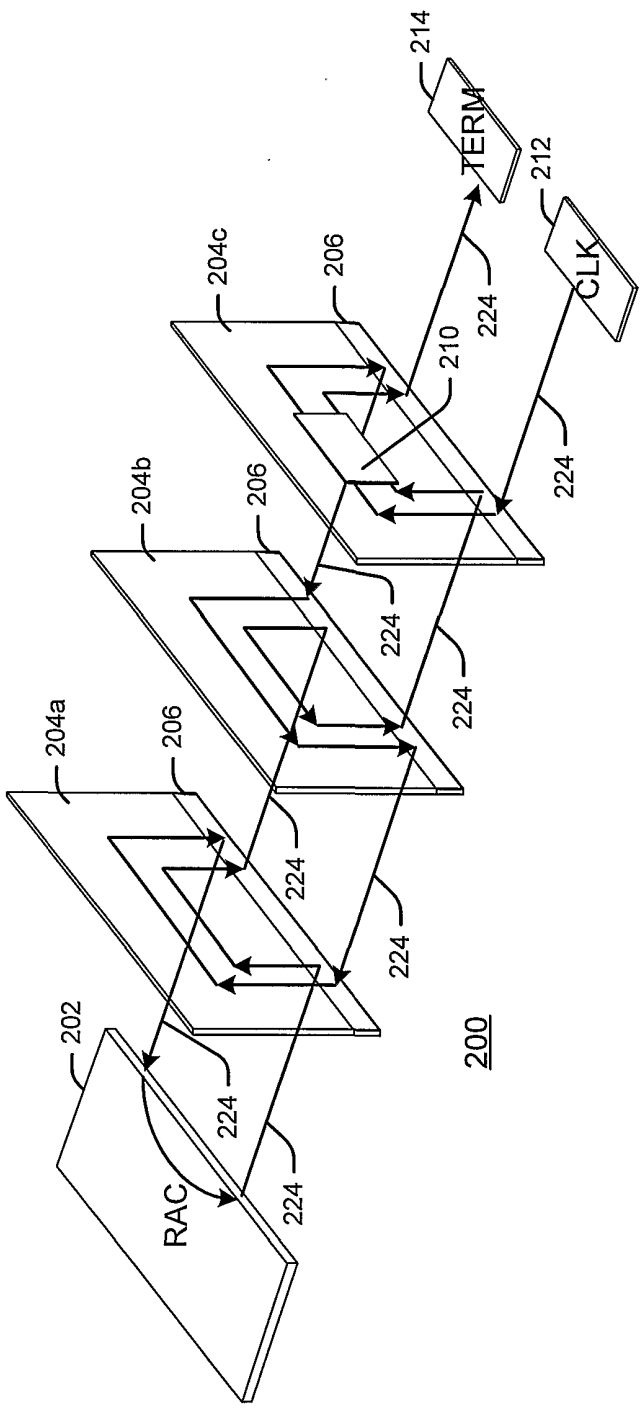

214
TERM
212
CLK
204c
206
210
224
204b
206
224
224
204a
206
224
224
202
224
RAC
224
200

Fig. 38

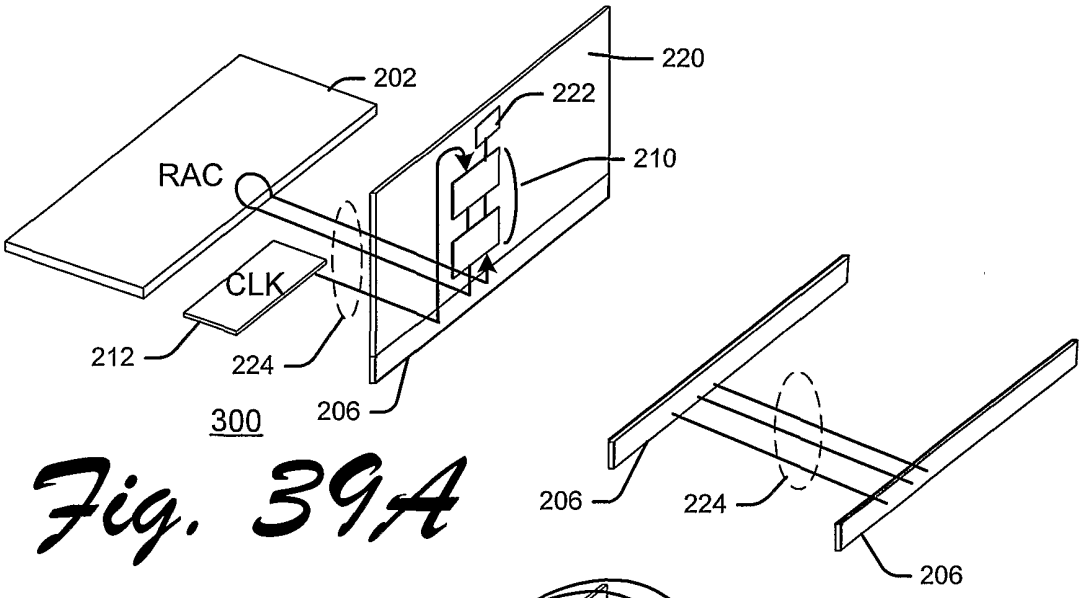


Fig. 39A

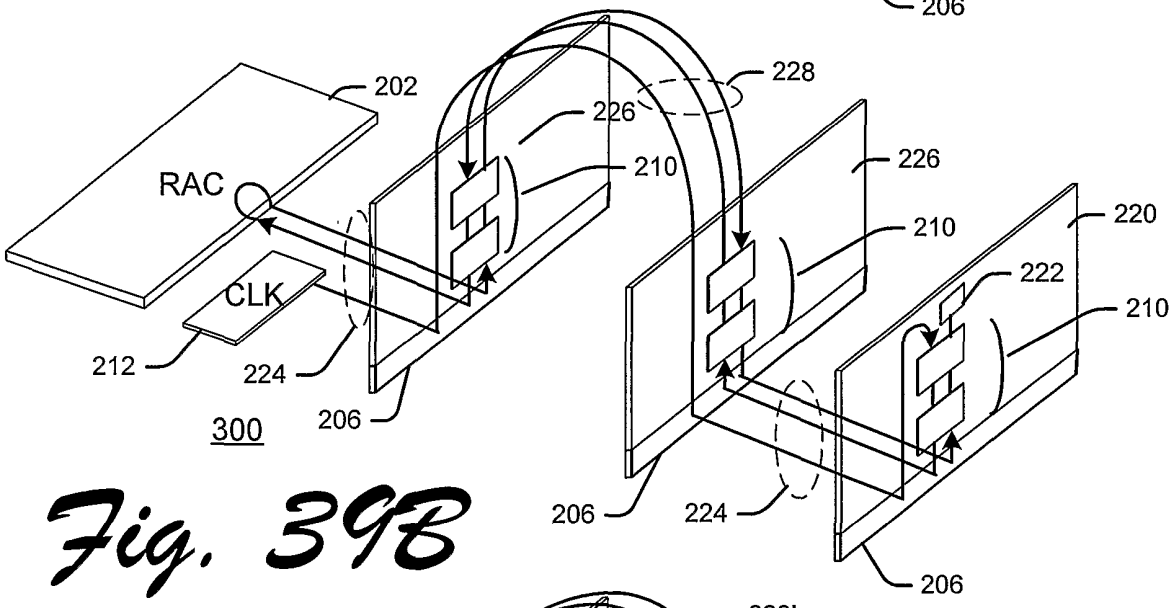


Fig. 39B

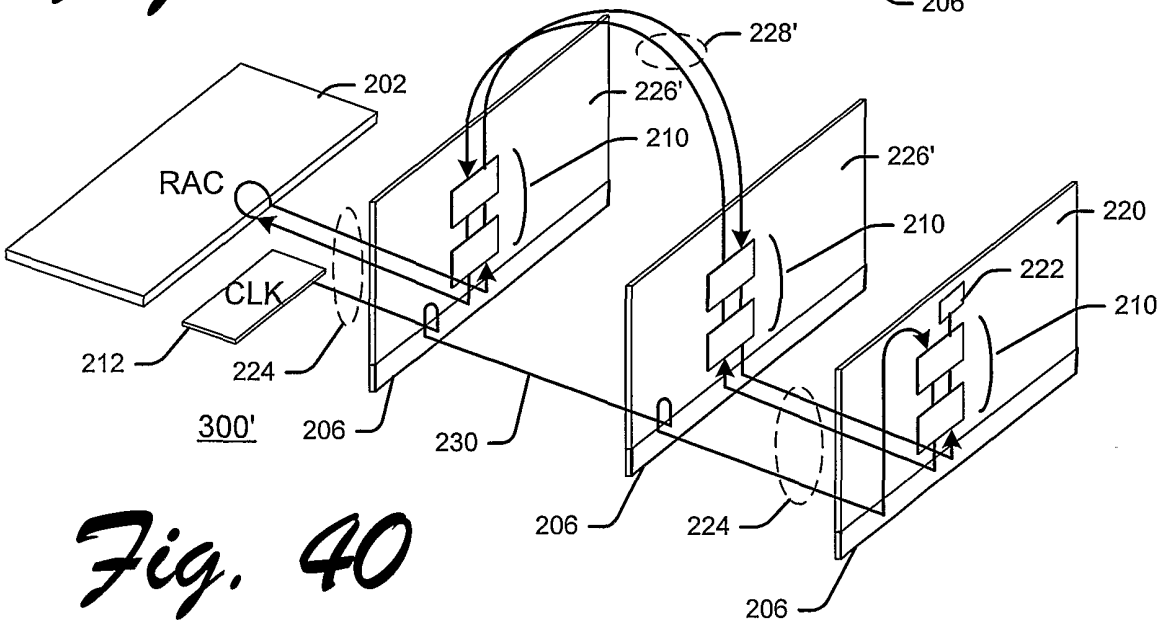


Fig. 40