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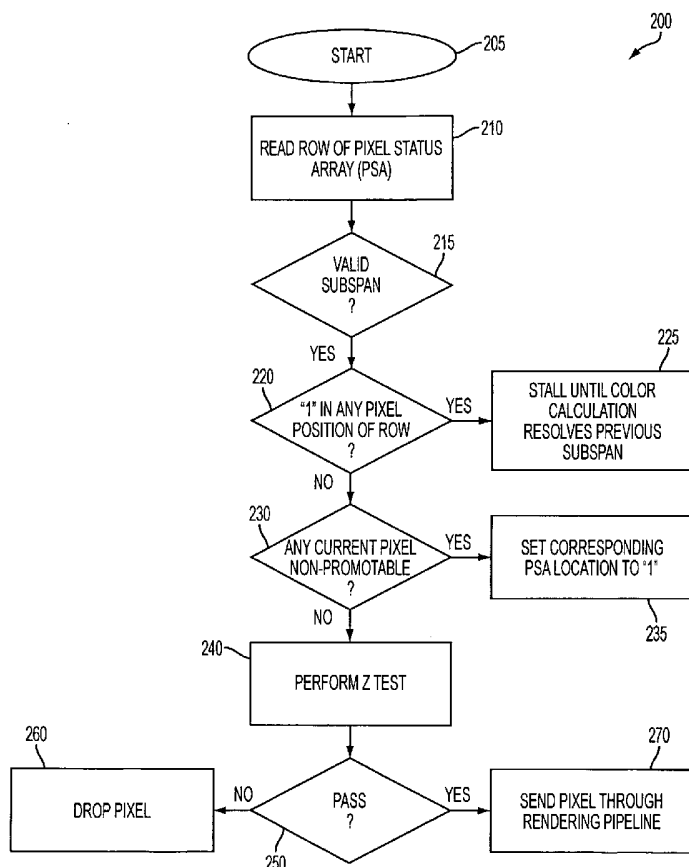
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[Continued on next page]

(54) Title: EFFICIENT Z TESTING



(57) Abstract: Z testing during computer graphics rendering is performed in a manner so as to optimize rendering. The status of a pixel as non-promotable may be tracked using a pixel status array (PSA). Each PSA row may contain bits which correspond to the non-promotable status of pixels. Each row may include five pixels, the first four of which represent the pixels in a subspan. If the row corresponds to a valid subspan, a determination may be made as to whether any pixel in the subspan is represented by a one, indicating that the pixel is non-promotable. This row corresponds to a previous subspan that has been sent down rendering pipeline. If a one is present, then the current subspan may be stalled until the pixels of the previous subspan has gone through color calculation. If, in the row that has just been read, no pixels are represented by a one, then a determination may be made as to whether any pixels in the current subspan are non-promotable. If so, then the corresponding bit in the current PSA row may be set to one. Otherwise, the Z test may be performed on each pixel of the current subspan.



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EFFICIENT Z TESTING

BACKGROUND OF THE INVENTION

[0001] Embodiments of the invention described relate to computer graphics, and in particular, to rendering.

[0002] Stated generally, computer graphics rendering is a process by which graphics instructions and data may be received and processed so that image data may be produced. This image data may then be sent to an input/output (I/O) device such as a display. Rendering creates data that may be displayed as an image.

[0003] The process of computer graphics rendering may include a number of discrete operations. For example, specific colors of an object or a background may need to be calculated. Texture may also need to be applied to a given surface. Another operation that may be performed in computer graphics rendering is the determination of whether a given object is in front of another object or background. If the foreground object is opaque, the background object may be obscured and the obscured portion of the background object may not need to be rendered. This depth analysis may generally be referred to as Z testing. In a rendered three-dimensional scene, the distance between an object or pixel and the hypothetical camera or the viewer's eye may be determined. Likewise, the comparable distance between the camera and a second, possibly obscuring object or pixel may be determined. These distances may be measured on a hypothetical Z axis, hence the term "Z testing." If the closer object is opaque, the more distant pixel or object need not be rendered.

[0004] Note, however, that Z testing may be more complicated in certain implementations. While an object may be in the foreground, for instance, the object may be translucent or transparent. In such a case, the background object may have to be rendered. Such conditions may also be programmed into a Z test.

[0005] As mentioned above, the process of Z testing may be only one of several processes that take place during rendering. Moreover, images may have to be generated, modified, and displayed in near-real time. If so, rendering processes must take place efficiently and quickly, given that computer graphics rendering often represents the processing of large amounts of data. Design issues arise, therefore, as to how best to order

these processes and how to implement them such that rendering throughput may be maximized.

BRIEF DESCRIPTIONS OF THE FIGURES

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[0006] The present invention will be described with reference to the accompanying drawings. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

10 [0007] FIG. 1 is a representation of a pixel status array, according to an embodiment of the invention.

[0008] FIG. 2 is a flow chart illustrating the process of performing Z testing, using the pixel status array, according to an embodiment of the invention.

[0009] FIG. 3 is a flow chart illustrating the process of checking and acting on the bin flag of a row in the pixel status array, according to an embodiment of the invention.

15 [0010] FIG. 4 is a block diagram showing a computer graphics renderer, according to an embodiment of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

20 [0011] The invention described herein may be embodied, for example, as a method and system for performing Z testing during computer graphics rendering, so as to optimize the efficiency of rendering throughput. For purposes of the invention, pixels may be arranged in subspans, where each subspan may be an array of two pixels by two pixels as would be presented on a computer display. Subspans may be further grouped into larger
25 sets, referred to herein as bins. Each bin may therefore represent a set of subspans, and may represent a discrete area of a scene as shown on a computer display. Some pixels may be designated as non-promotable. If a pixel is non-promotable, this means that even though the pixel may be in the foreground compared to a pixel in the background, the foreground non-promotable pixel does not necessarily obscure the background pixel. The
30 non-promotable pixel may be part of an object or a surface that is transparent or translucent, for example. The status of a pixel as non-promotable may be tracked using a data structure called a pixel status array (PSA). In an embodiment of the invention, the

pixel status array may be composed of some number of rows. Each row may contain a number of bits, each bit corresponding to the non-promotable status of a pixel. In an embodiment of the invention, each row of the PSA may include five bits, the first four of which may represent the pixels in a single subspan. If a pixel is non-promotable, the corresponding bit in the PSA may be set in the row corresponding to that pixel's subspan. A PSA may be implemented as hardware or software, or as a combination thereof.

[00012] In an embodiment of the invention, the processing of the invention may begin by reading a row of the PSA. The validity of the subspan may be determined, i.e., the process may determine whether the subspan contains at least one pixel. A

determination may be made as to whether a one occurs in any of the first four locations in the row. A one would indicate that the corresponding pixel is non-promotable. Note that this row may correspond to a previous subspan of pixels that has been sent into the rendering pipeline for purposes of color calculation and other operations. If a one is present, then the current subspan may be stalled prior to the rendering pipeline, until the pixels of the previous subspan have gone through color calculation.

[00013] If, in the row that has just been read, none of the pixels is represented by a one, then a determination may be made as to whether any pixels in the current subspan are non-promotable. If so, then the corresponding bit in the PSA row that corresponds to the current subspan may be set to 1. Otherwise, the Z test may be performed on each of the four pixels of the current subspan. In this manner, pixels that are known to be promotable may be analyzed during the Z test and potentially dropped if they are found to be obscured by another pixel. Such a dropped pixel may therefore never be forwarded for additional processing, such as color calculation. This may eliminate pixels that need not be processed.

[00014] Embodiments of the invention are now described with respect to the accompanying figures. As described above, a given pixel may be considered to be either promotable or non-promotable. The promotability or non-promotability of a given pixel may be tracked in the PSA. An exemplary PSA is illustrated in FIG. 1, according to an embodiment of the invention. The PSA may be organized as a two dimensional array. Each row of the array may correspond to a subspan of pixels. In the illustrated embodiment, each subspan contains four pixels, so that each row of the PSA includes four bits, one bit per pixel, followed by a fifth bit. The fifth bit in the row may be referred to

herein as a bin flag. The purpose of the bin flag will be described in greater detail below. Each row of the PSA is therefore five bits long in the embodiment illustrated.

[00015] An embodiment of the process of the invention is illustrated in FIG. 2. The

process may begin at block 205. In block 210, a row of the PSA is read. This row of the
5 PSA may be associated with a previous subspan of pixels that has already been forwarded
through the rendering pipeline to color calculation processing. If, in block 215, it is
determined that this subspan is valid, then the process may continue at block 220. Here, a
current subspan may be considered. Such a subspan has not yet been forwarded on to
color calculation in the rendering pipeline. In block 220, a determination may be made as
10 to whether any of the pixels in the current subspan is represented by a one. As described
above, a one would signify that the corresponding pixel is non-promotable. If a one is
present, then in block 225, this current subspan may be stalled until color calculation logic
completes resolution of the previous subspan. Otherwise, the process continues at block
230. Here, a determination may be made as to whether any of the pixels in the current
15 subspan are non-promotable. If so, then the process continues at block 235. Here, the
appropriate PSA location may be set to one. If none of the pixels in the current subspan is
non-promotable, the process continues at block 240. Here, the Z test may be performed on
pixels in the current subspan. Because all of the pixels in the current subspan are
promotable, as determined in block 230, the Z test may be performed at this point. In this
20 manner, a pixel that is obscured by a promotable pixel may be dropped without further
processing. Therefore, in block 250, a determination may be made as to whether the Z test
has been passed. If so, the tested pixel may be forwarded through the rendering pipeline
onto the color calculation logic in block 270. Otherwise, the pixel may be dropped in
block 260.

25 **[00016]** In an embodiment of the invention, a current subspan may be found to be
non-promotable, and at the same time there is no matching entry in the PSA. In this case,
Z testing may then be performed on the pixels of this subspan. If the Z test is passed, then
the corresponding PSA bit(s) may be set and the current subspan may be forwarded
through the rendering pipeline.

30 **[00017]** In an embodiment of the invention, each row of the PSA may include a bin
flag. The bin flag may be used to address size limitations on the PSA. Ideally, the PSA
would contain a row for every subspan in a scene. This is generally not practical,
particularly if the PSA is implemented in hardware. To address this problem, subspans

may be organized into bins, where each bin may be given a binary designation. Each bin may therefore be viewed as either even or odd. The designation of bins may alternate across a scene, such that if a given bin is odd, its adjacent bin may be considered even. This binary scheme may be encoded as either a zero or a one in the PSA. Hence, for a given subspan, its bin may be identified as either even or odd by the bin flag, i.e., the fifth bit in the row associated with the subspan in the exemplary PSA of FIG. 1. If, given two rows of a PSA, the respective bin flags are different, then it may be inferred that the corresponding subspans are associated with different bins. These subspans will therefore not be evaluated against each other in a Z test. There is, therefore, no point in stalling one of these subspans while the other may be processed in color calculation.

[00018] An exception to this process may occur where a current subspan is non-promotable and there is another subspan with overlapping pixels being processed further down the rendering pipeline, e.g., in the color calculation logic. In this case, the current subspan may be stalled, even though the respective bin flags may be different.

[00019] The processing of bin flags is illustrated in FIG. 3, according to an embodiment of the invention. The process begins at block 310. In block 320, a bin flag may be read. In block 330 a determination may be made as to whether the bin flag indicates a bin other than the bin of the previous subspan. If so, then processing may continue at block 333. Here, a determination may be made as to whether the current subspan is non-promotable and overlaps the previous subspan. If so, then in block 336 the current subspan may be stalled until the color calculation logic of the rendering pipeline resolves the previous subspan. If not, the process continues at block 340. Here, the current subspan may be forwarded through the rendering pipeline. If, in block 330, it is determined that the same subspan may be indicated, then processing may proceed to block 205, illustrated in FIG. 2.

[00020] The invention may be implemented in a computer graphics renderer, one example of which is illustrated in FIG. 4. Blocks 410 may be viewed as a rendering pipeline. The invention, as illustrated in FIGs. 2 and 3 may be incorporated in block 420, the intermediate Z unit. As described above, the invention may allow the dropping of a pixel without requiring additional processing if the pixel is found to be obscured, as determined by the Z test. As seen in FIG. 4, a pixel that passes the Z test may ultimately be sent through a variety of processes, and ultimately to the color calculator 430. By eliminating pixels that will not ultimately be displayed, the invention may save

considerable processing by avoiding the unnecessary color calculation for pixels that are not to be displayed.

[00021] The present invention has been described above with the aid of functional building blocks and method steps illustrating the performance of specified functions and relationships thereof. Boundaries of these functional building blocks and method steps have been arbitrarily defined herein for the convenience of the description. Alternate boundaries may be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks may be implemented by discrete components, application-specific integrated circuits, processors executing appropriate software or the like, or any combination thereof. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, and should be defined only in accordance with the following claims and their equivalents.

[00022] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail may be made therein without departing from the spirit and the scope of the invention.

WHAT IS CLAIMED IS:

1. A method comprising:
reading bin flags of two rows of a pixel status array (PSA), the rows
5 corresponding to a previous subspan and a current subspan; and
determining if the current subspan comprises a non-promotable pixel and overlaps
the previous subspan and
if so, stalling the current subspan until the previous subspan is processed by
color calculation logic of a rendering pipeline;
10 otherwise, forwarding the current subspan through the rendering pipeline.
2. The method of claim 1, wherein the subspans each comprise four pixels in a two
by two array.
- 15 3. The method of claim 2, wherein each row of the PSA represents a subspan and
comprises four bits, representing the four respective pixels of the subspan, and the bin flag
corresponding to the subspan.
4. A method comprising:
20 determining if a previous row is present in a pixel status array (PSA), the
previous row corresponding to a previous subspan,
determining if a non-promotable pixel is indicated in a current row of the
PSA;

stalling a current subspan corresponding to the current row until the previous subspan is processed by color calculation logic of a rendering pipeline, if a non-promotable pixel is indicated;

5 determining if the current subspan contains a non-promotable pixel, if no non-promotable pixels are indicated;

setting a PSA location corresponding to the non-promotable pixel of the current subspan, if the current subspan contains a non-promotable pixel; and

performing a Z test on the promotable pixels, if the current subspan contains only promotable pixels.

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5. The method of claim 4, further comprising:

forwarding the promotable pixel through the rendering pipeline, if any of the promotable pixels passes the Z test; and

dropping the promotable pixel, if the promotable pixel fails the Z test.

15

6. The method of claim 4, further comprising:

forwarding the non-promotable pixel through the rendering pipeline, if any of the non-promotable pixels passes the Z test; and

dropping the non-promotable pixel, if the non-promotable pixel fails the Z test.

20

7. The method of claim 4, wherein the Z test is performed in an intermediate Z module of the rendering pipeline.

8. The method of claim 4, wherein each subspan comprises four pixels in a two by
25 two array.

9. The method of claim 8, wherein each row of the PSA represents a subspan and comprises four bits representing the four respective pixels of the subspan.

5 10. The method of claim 4, further comprising:

setting a bit in the PSA corresponding to the non-promotable pixel; and

performing the Z test on the non-promotable pixel,

if there is no row of the PSA corresponding to the current subspan and the current subspan comprises a non-promotable pixel,

10 .

11. The method of claim 4, further comprising:

determining if the previous row represents a valid subspan if the previous row is present in a pixel status array (PSA),

15 performed before determining if a non-promotable pixel is indicated in the current row of the PSA.

12. A computer graphics renderer comprising an intermediate Z unit that performs:

executing a Z test on a promotable pixel;

20 discarding the promotable pixel if the Z test is failed; and

sending the pixel through a rendering pipeline only if the Z test is passed.

13. The computer graphics renderer of claim 12, wherein the intermediate Z unit also performs the following, before said execution:

determining if a previous row is present in a pixel status array (PSA), the previous row corresponding to a previous subspan,

determining if the previous row represents a valid subspan;

stalling a current subspan corresponding to the current row until the

5 previous subspan is processed by color calculation logic of the rendering pipeline, if a non-promotable pixel is indicated in a current row of the PSA;

determining if the current subspan contains a non-promotable pixel, if no non-promotable pixels are indicated; and

initiating the Z test on the promotable pixel if the current subspan contains

10 only a set of promotable pixels that includes the promotable pixel;

otherwise, setting a PSA location corresponding to the non-promotable pixel of the current subspan.

14. The renderer of claim 12, wherein the intermediate Z unit also performs the

15 following, before said executing step:

reading a row of a pixel status array (PSA), the row corresponding to a previous subspan; and

stalling the current subspan until the previous subspan is processed by color calculation logic of the rendering pipeline if a current subspan comprises a non-

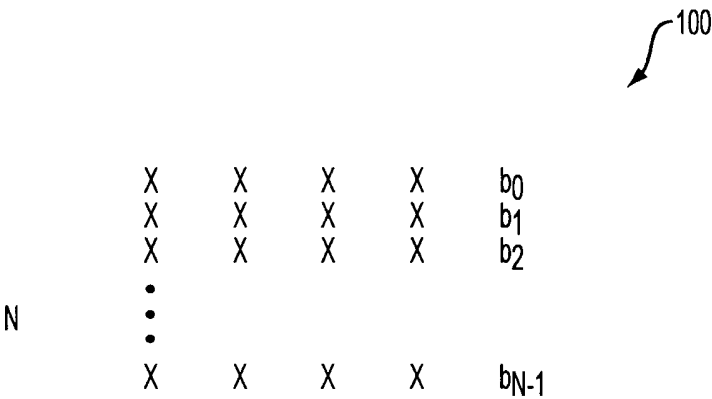
20 promotable pixel and overlaps a previous subspan;

otherwise, forwarding the current subspan through the rendering pipeline.

15. The renderer of claim 14, wherein said current and previous subspans each comprise four pixels in a two by two array.

16. The renderer of claim 14, wherein each row of the PSA corresponds to a subspan and comprises a bit for each pixel of said subspan.

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FIG. 1

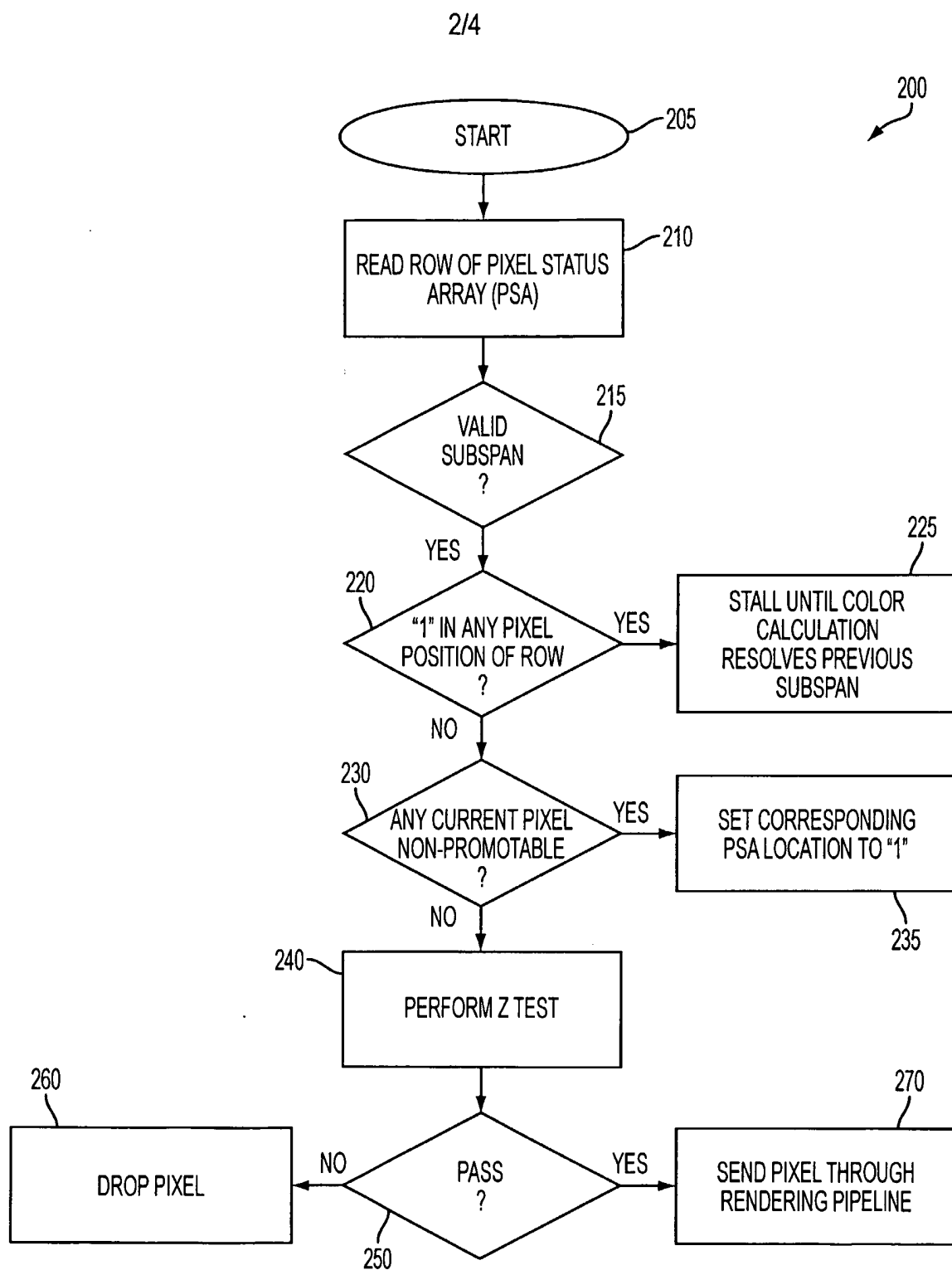


FIG. 2

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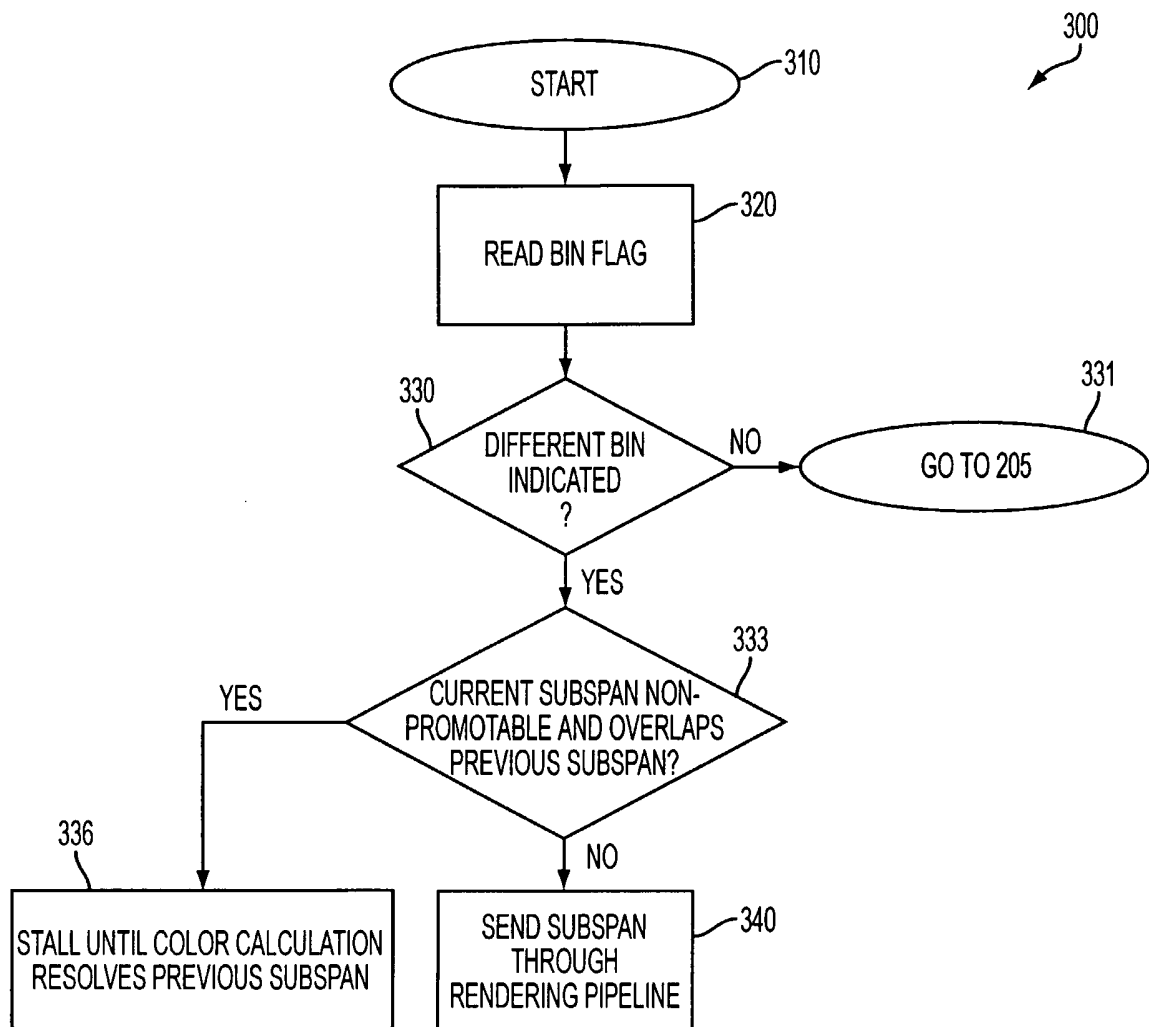


FIG. 3

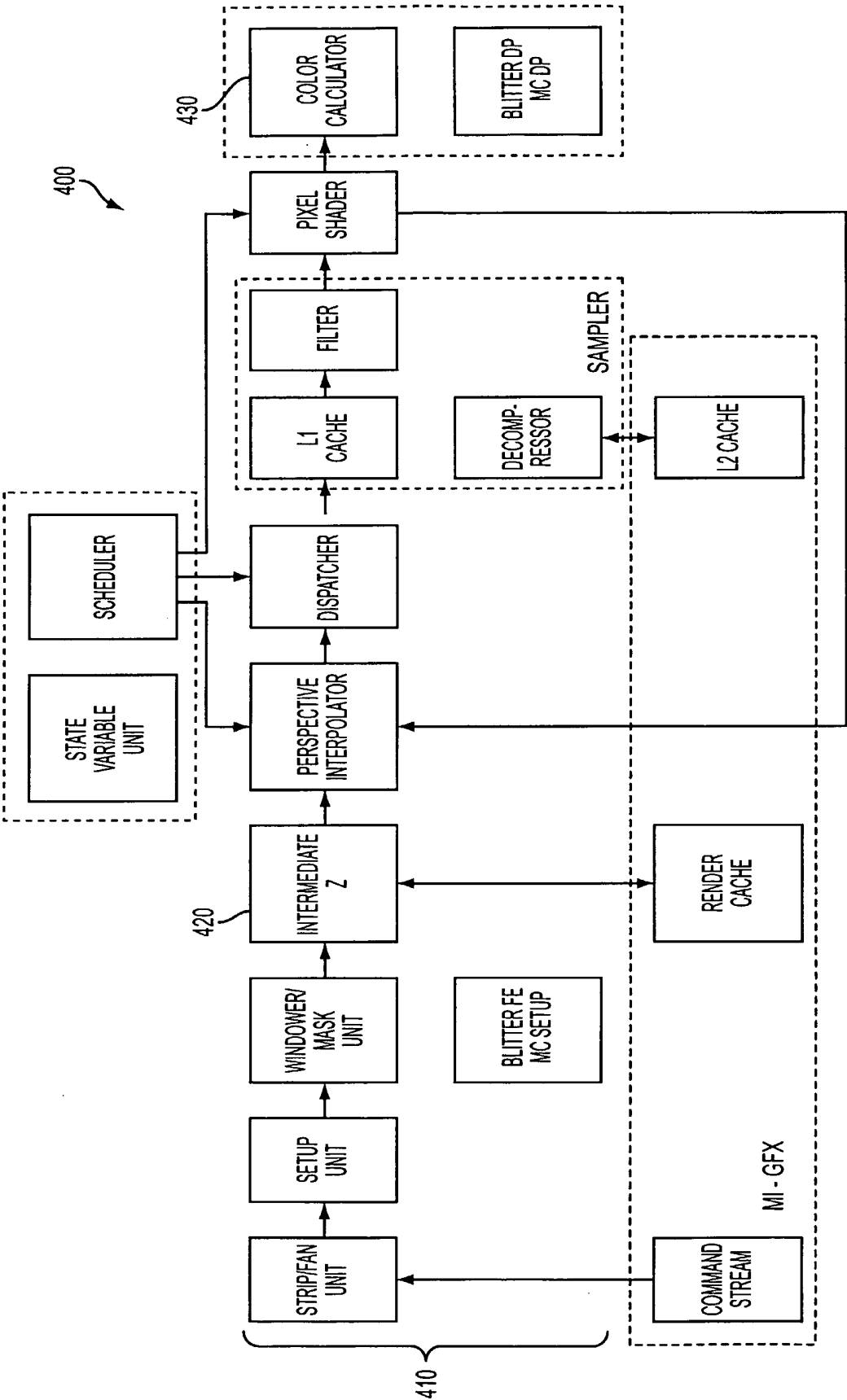


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2005/047690

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06T15/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06T

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2003/080959 A1 (MOREIN STEPHEN L) 1 May 2003 (2003-05-01) figure 4	12 1-11, 13-16
X A	US 6 271 851 B1 (HSIAO CHIEN-CHUNG ET AL) 7 August 2001 (2001-08-07) figure 2	12 1-11, 13-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2005/047690

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2003080959	A1	01-05-2003	NONE	
US 6271851	B1	07-08-2001	US 6448967 B1	10-09-2002