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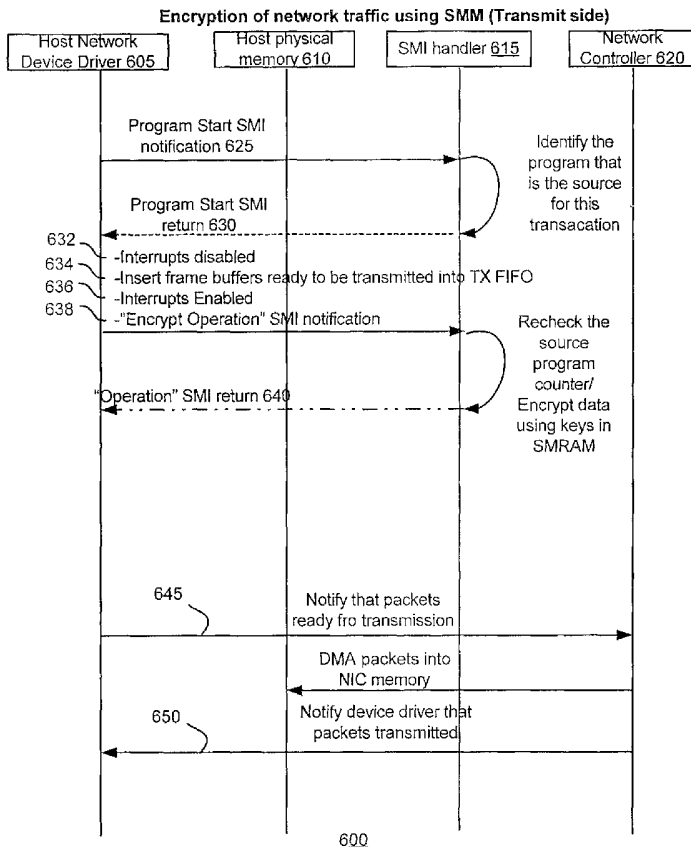
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(54) Title: SYSTEM AND METHOD FOR SECURE INTER-PLATFORM AND INTRA-PLATFORM COMMUNICATIONS



(57) Abstract: A system and method are provided to preserve the confidentiality and/or integrity of a sensitive communication from its source to its destination whether locally on the platform, between platforms, or even the same program over time.

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SYSTEM AND METHOD FOR SECURE INTER-PLATFORM AND INTRA-  
PLATFORM COMMUNICATIONS

5 TECHNICAL FIELD

[0001] Embodiments of the invention generally relate to the field of network security and, more particularly, to a system and method for inter-platform and intra-platform communications.

10 BACKGROUND

[0002] Computer networks are widely used by businesses, public institutions, and individuals. Software programs (or simply, programs) exchange information with each other via computer networks. Protecting the integrity and confidentiality of these  
15 communications is crucial in today's networked computing environment. Obviously, transmitting passwords, cryptographic keys, or other private information in clear text makes a computing system vulnerable to compromise by hostile attackers. This is because the keying material can be retrieved from memory by debuggers, malware, or other  
software components on the system which have been compromised by an attacker. The  
20 term "keying material" broadly refers to, for example, cryptographic keys, session keys, passwords, digital certificates, and/or any sensitive information.

[0003] Conventional approaches to protecting confidential information in computing systems are typically based on either virtual private networks (VPN) or specialized  
hardware. Virtual private networks can easily be circumvented or tampered with because  
25 they are implemented as application software and/or as a kernel level driver which can be violated by other software components running in a privileged mode.

[0004] Hardware solutions may include, Trusted Platform Modules (TPMs) or dedicated co-processors for implementing cryptographic functions. Trusted Platform

Modules are microchips that store, for example, cryptographic keys, passwords, and/or digital certificates. Hardware based security solutions are expensive and use separate hardware to isolate themselves from the rest of a system's hardware. Moreover, TPMs are typically connected to the chipset using a low bandwidth serial bus which makes it  
5 unsuitable for applications that require high bandwidth exchange of data such as encryption/decryption of network traffic. Hence, conventional systems lack a cost-effective, secure, and tamper-resistant method for encrypting data in software running on the host processor so that it is inline with the programs that directly interact with this data.

## 10 BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

**Figure 1** is a block diagram illustrating various communications that may be  
15 protected by embodiments of the invention.

**Figures 2A-2B** illustrate a program utilizing security operations provided by a protected region of memory, according to an embodiment of the invention.

**Figure 3A** is a flow diagram illustrating certain aspects of a method for initializing a protected region of memory (e.g., System Management Random Access Memory),  
20 according to an embodiment of the invention.

**Figures 3B-3C** are flow diagrams illustrating certain aspects of a method for secure inter-platform and intra-platform communication, according to an embodiment of the invention.

**Figure 4** is a block diagram of a framework for encrypting outbound packets,  
5 according to an embodiment of the invention.

**Figure 5** is a block diagram illustrating an embodiment of the invention that supports network security protocols at different network layers.

**Figure 6** is a transaction diagram illustrating a transaction implemented according to an embodiment of the invention.

## 10 DETAILED DESCRIPTION

[0006] A system and method are provided to preserve the confidentiality and/or integrity of a sensitive communication (and the functionality that supports the communication) from its source to its destination whether locally on the platform, between platforms, or even the same program over time. As is further described below,  
15 embodiments of the invention may be used by host resident software to implement any security processing (for example, encryption) on any data (for example, network traffic) that needs to be done in a tamper-resistant and confidential environment. Embodiments of the invention may also correctly identify and protect the source of the program requesting these services. Thus, embodiments of the invention may provide a mechanism to secure  
20 keying material within an inline (yet hidden) processor mode. As is further described below, embodiments of the invention may be used by ring-0 programs (e.g., kernel programs) to secure communications with platform components, provide unspoofable

authentication/authorization, and even verify the integrity of the program's internal state from invocation to invocation.

[0007] For ease of explanation, embodiments of the invention are disclosed with reference to the encryption of data transmitted over a network. Alternative embodiments, however, may be directed to the security processing of any data that needs to be done in a tamper-resistant and confidential environment. For example, embodiments of the invention may be directed to protecting inter-platform and/or intra-platform communication as well as inter-program and/or intra-program communication.

[0008] FIG. 1 is a block diagram illustrating various communications that may be protected by embodiments of the invention. FIG. 1 includes platforms 110 and 120. The term "platform" broadly refers to the hardware (e.g., processor), software (e.g., operating system), microcode, chipset, firmware, etc, that provide data processing. Reference number 130 illustrates inter-platform communication (e.g., between platforms 110 and 120). Platform 110 includes microcontroller sub-platform 112. The intra-platform communication between program 114 (e.g., running on the host processor) and microcontroller sub-platform 112 are illustrated by reference number 132.

[0009] Programs 114 and 116 may represent two programs executing on the host processor (not shown). The term program may refer to a kernel component (e.g., a ring-0 program) or an application program (e.g., a ring-3 program). An example of inter-program communication is the communication between programs 114 and 116 as shown by reference number 134. In an embodiment, a program (e.g., program 114) may securely store its data structures and/or states and securely access the stored data structures and/or states over time (e.g., to periodically check the integrity of its internal data structures

across context changes and/or process invocations). Reference number 136 illustrates an intra-program embodiment in which program 114 securely stores its data structures and/or states and securely accesses the stored data structures and/or states over time.

**[00010]** Embodiments of the invention may use a System Management Mode (SMM) or similar specialized processor mode to protect keying material and the cryptographic functions that utilize this keying material to encrypt/decrypt and/or validate the integrity of any data. The SMM provides a partitioned memory and context in which the keying material is protected from disclosure to other programs running on a host system. Embodiments of the invention increase the security of keying material by providing an isolated and tamper-resistant environment for key storage and processing and, thereby, increase the difficulty for an attacker to obtain the keying material through traditional attack vectors.

**[00011]** The SMM (or similar) specialized processor mode may also provide security processing for program data. The term “security processing” broadly refers to processes that enhance the security of data such as encryption, decryption, authorization, authentication, integrity checking, and the like. The SMM is a special operating mode that provides an isolated environment that is independent of the operating system. A processor enters the SMM when a System Management Interrupt (SMI) is triggered and executes code and data from a chipset protected region of main memory called System Management Random Access Memory (SMRAM) that is inaccessible to software executing in other processor operating modes.

**[00012]** For ease of reference, the SMM and similar specialized processor modes are collectively called management modes. In an embodiment, the management mode

obtains state information from the program that triggers it. In one embodiment, the program provides a saved state map or similar structure to the management mode when it invokes the management mode. The saved state map (or similar structure) provides information about processor state at the time of entering the management mode. For example, a program executing in the management mode may recover the program counter of the invoking program from the saved state map (or similar structure). In an embodiment, this provides a tamper proof way to detect the source of the call which can be traced back to the program triggering the SMI.

[00013] Since the location of the invoking program's code store can be overwritten by an attacking program, it may be desirable to verify or otherwise protect the integrity of that code store. In an embodiment, program images that are sources of SMI notifications are authenticated using a suitable hardware or software technique. Examples of mechanisms for authenticating program images include, but are not limited to, validating the image from the management mode (e.g., the SMM) or other protected system component (such as a Navassa embedded processor), and the like.

[00014] FIGs. 2A-2B illustrate an invoking program utilizing security operations provided by a protected region of memory. The illustrated embodiment may be described with reference to the SMM and System Management Random Access Memory (SMRAM). It is to be appreciated that different management modes and different protected regions of memory may be used in an alternative embodiment of the invention.

[00015] In an embodiment, SMRAM 200 includes the following data structures: Valid Program Identification (VPI) table 205; Program Identifier (ID) to Key Identifier (PIKI) mapping table 210; and Program ID to Program Counter Range (PIPC) mapping



table 215. In an alternative embodiment, SMRAM 200 may include more data structures, fewer data structures, and/or different data structures.

[00016] In an embodiment, VPI table 205 contains information on how to identify particular programs and to determine whether in-memory program images are valid. In one embodiment, the programs identified in VPI table 205 are the programs that are allowed to invoke the security operations of the SMM. In one embodiment, VPI table 205 is provisioned over a secure channel from a trusted data store 220. Alternatively, VPI table 205 may be provisioned by local trusted platform components such as an embedded management microcontroller (e.g., the Proactive/Navassa platform developed by Intel Corporation) that can provide secure remote Out-Of-Band (OOB) connections to the platform.

[00017] Table 1 describes a number of data structures that may be included in VPI table 205. In alternative embodiments, the data structures may have different names. In addition, more data structures, fewer data structures, and/or different data structures may be used in alternative embodiments of the invention.

TABLE 1

Data Structure Name	Brief Description
Program Identifier (PID)	Generic number/string that uniquely identifies a program on the machine.
Program Marker (PM)	A string of bytes used to identify the location of a program image in memory with a high probability (may be static sequence of bytes compiled into the program). This sequence should mark the start of the program's image in memory.
Program Size (PS)	Bounds the program's image size in memory (how large the image is starting at the PM).

Program Hash Value (PHV)	Specifies the Secure Hash Algorithm 1 (SHA1) or Message Digest (MD5) hash value that is computed over the program image using the Program Hash Key (PHK). The program image in memory should compute the same PHV if it has not been modified from its expected form.
Program Hash Key (PHK)	Key used to calculate the PHV for a particular program image.

[00018] In an embodiment, PIKI table 210 contains protected key values and the key identifiers used to identify the key values. In one embodiment, PIKI table 210 associates particular keying material with a particular program (e.g., via the PID). In an  
 5 embodiment, administrator 225 provisions PIKI table 210 via out-of-band provisioning process 230.

[00019] Table 2 describes a number of data structures that may be included in PIKI table 210. In alternative embodiments, the data structures may have different names. In addition, more data structures, fewer data structures, and/or different data structures may  
 10 be used in alternative embodiments of the invention.

TABLE 2

Data Structure Name	Brief Description
Program Identifier (PID) 216	Generic number/string that uniquely identifies a program on the machine.
Key ID (KID) 214	Key identifier used by programs to communicate to the SMM component which key should be used for its operation.
Key Length (KL) 213	Length of a particular key stored in SMRAM identified by KID.
Key Value (KV) 212	The actual key value, stored in SMRAM protected memory, identified by a KID.

[00020] In an embodiment, PIPC table 215 is created by an SMM component (or other trusted agent) such as a security process. PIPC table 215 may be used to compute the location in host memory of a particular program and to track the program's status. Table 3 describes a number of data structures that may be included in PIPC table 215. In alternative embodiments, the data structures may have different names. In addition, more data structures, fewer data structures, and/or different data structures may be used in alternative embodiments of the invention.

TABLE 3

Data Structure Name	Brief Description
Program Counter Base (PCB) 222	Program start location, should correspond to the memory address where the PM was actually found in host memory.
Program Counter Limit (PCL) 224	Program end location, should correspond to the PCB + PS.
Program Identifier (PID)	Generic number/string that uniquely identifies a program on the machine.
Program Start Notification Completed (PSN) 218	Used to record whether the Program Start Notification was properly called by a particular valid program. It is cleared on a Program End Notification.

10 [00021] FIG 2B illustrates program memory 235 according to an embodiment of the invention. The term "program memory" refers to a region of memory (e.g., Random Access Memory (RAM)) that is accessible to a program executing on a host processor. In one embodiment, SMRAM 200 and program memory 235 may both be part of a host processor's main memory. In an alternative embodiment, SMRAM 200 may be  
15 implemented in a region of memory other than the host processor's main memory.

[00022] In an embodiment, a program communicates with SMM components (e.g., the security programs stored in the SMM), at least in part, through Program Data Table (PDT) 240. SMM components may access PDT 240 because the SMM is a highly privileged processor mode that can access program memory 235 (as well as the operating system's memory). PDT 240 may specify particular security operations 245 to be performed on program data. In addition, PDT 240 may specify the location of the program data. For example, in the illustrated embodiment data buffer pointer (DBP) 250 points to data buffer 260 and integrity buffer pointer (IBP) 258 points to integrity buffer 265. In addition, PDT 240 may identify the keying material to be used to process the program data via key identifier 268. For example, key identifier 268 may identify a key stored in SMRAM 200 that may be used to process data stored, for example, in data buffer 260.

[00023] Table 4 describes a number of data structures that may be included in PDT 240. In alternative embodiments, the data structures may have different names. In addition, more data structures, fewer data structures, and/or different data structures may be used in alternative embodiments of the invention.

TABLE 4

Data Structure Name	Brief Description
Operation Request (OpR) 245	Identifies the particular security operation (e.g., integrity check, encrypt, decrypt, etc.) the program wishes the SMM to apply to its selected data buffers.
Data Buffer Length (DBL)	Identifies the length of a program's data buffer.
Data Buffer Pointer (DBP) 250	Pointer to the program's actual data buffer used by SMM as input for requested operations.
Data Mask Pointer (DMP) 252	Pointer to mask buffer that indicates which

	bits in data buffer 260 the SMM operations should skip.
Integrity Buffer Length (IBL) 255	Length of the integrity buffer allocated by the program.
Integrity Buffer Pointer (IBP) 258	Pointer to program's buffer holding integrity information such as a Hash Method Authentication Code (HMAC).
Error Code (EC) 272	Value returned by the SMM when a particular operation fails. It may specify the reason for the failure or indicate NONE if there is no failure.

[00024] Since PDT 240 "lives" in a vulnerable memory region, in an embodiment, the integrity of this data structure, as well as the integrity of the data buffers (e.g., data buffer 260 and/or integrity buffer 265) needs to be assured. One mechanism for assuring the validity of the data in these structures is to ensure that only the valid program that owns these data structures is allowed to manipulate these data structures. In one embodiment, this mechanism is implemented by the program bounding all valid modifications to PDT 240 between program start and program end notifications to the SMM component. In this way, the SMM component can track which program is running before PDT 240 is modified.

[00025] Program start notification 270 notifies an SMM component that a program is going to invoke a security operation provided by the SMM component. In an embodiment, program start notification 270 is issued by the program or device driver as soon as it is invoked and before it starts modifying internal data structures of PDT 240. In one embodiment, program start notification 270 is an SMI notification. In an embodiment, a program start notification handler (not shown) may receive program start notification 270. The handler may verify the program image and record the source of the

caller in PIPC table 215 by, for example, setting Program Start Notification (PSN) indicator 218 to TRUE for the table entry if the program counter is in the proper range and the program's image in this range remains unmodified. Immediately after the PSN handler returns, the program/driver may setup its internal data structures and configure PDT table 240 which may be used as input for the Operation Notification handler (not shown). The program/driver may disable interrupts when doing this to avoid context switches (that can cause malicious code to execute) and thereby prevent malicious code from changing the program's data or state prior to the Operation Notification.

[00026] An "operation notification" refers to a request by a program/driver for an SMM component to provide a security operation (e.g., to provide secure data and/or to process program data). In an embodiment, the operation notification may be implemented with an SMI notification. In one embodiment, the SMI notification may be issued by the program or device driver only after an SMI Program Start Notification 270 completed successfully. In an embodiment, the SMI handler for this notification will recover the invoker's program counter from, for example, the Saved State Map (SSM) and find the entry in PIPC table 215 where the recovered program counter is in the range between PCB 222 and PCL 224. If a matching range is found in PIPC table 215, the SMI handler may then verify that the PSN value 218 for that PIPC entry is set to TRUE, meaning Program Start Notification 270 was properly invoked previously by the same program. If PSN value 218 is TRUE, the handler may then read data from PDT 240 that was setup by the program prior to this notification and apply the operation requests 245 specified there for the provided Key IDs 268.

[00027] In an embodiment, operation request 245 specifies a security operation for an SMM component. The security operation may include obtaining confidential data and/or may include invoking a security process for program data. Examples of security processes include, and are not limited to, an encrypt operation, a decrypt operation, and/or  
5 an integrity check of encrypted and/or decrypted data.

[00028] In an embodiment, an encrypt operation may cause a handler (e.g., an SMI handler) to execute a selected encryption algorithm on the buffer (e.g., data buffer 260) referenced by the PDT entry's DBP 250 skipping those regions masked by the mask buffer referenced by DMP 252. In an embodiment, the encrypt code uses the keys stored in  
10 SMRAM corresponding to the selected key ID 268. On SMM return, the data buffers 260 will be encrypted and ready to communicate securely. In an embodiment, the keying material is not divulged to the invoking program. Rather, the management mode uses the correct keying material (e.g., as identified by key ID 268) on behalf of the invoking program (e.g., if the program image of the invoking program has been verified in  
15 memory).

[00029] In an embodiment, an integrity check operation may cause a handler to execute a selected integrity checking algorithm on, for example, integrity buffer 265 as referenced by Integrity Buffer Pointer (IBP) 258. In an embodiment, the handler may skip regions of buffer 265 that are specified by Data Mask Pointer (DMP) 252. The integrity  
20 checking algorithm may be based, at least in part, on the associated session key identified by key id 268. In one embodiment, the results of the integrity checking algorithm are provided in a Hash Method Authentication Code (HMAC) that is stored in integrity buffer

265. Examples of integrity checking algorithms include, but are not limited to, Secure Hash Algorithm 1 (SHA1) or Message Digest 5 (MD5).

[00030] In an embodiment, a decrypt operation may cause an SMI handler to execute a decryption algorithm on one or more buffers referenced by DBP 250, skipping  
5 DMP 252 masked regions. In an embodiment, the SMM decrypt code (not shown) may use the keys stored in SMRAM 200 corresponding to Key ID 268. On SMM return, the buffers referenced by DBP 250 are decrypted and ready to be read or an error code Error Code (EC) 272 is set for the appropriate entry in PDT 240.

[00031] In a similar fashion to the decrypt operation, the integrity of the data buffer  
10 referenced by DBP 250 may be validated by the SMM code. The integrity check may be based, at least in part, on an HMAC provided in the integrity buffer referenced by IBP 258 and the associated session key value for the Key ID 268 found in SMRAM 200. The success or failure of the integrity check can then be communicated back to the program that invoked the SMI through the PDT error code EC 272 for the corresponding PDT  
15 entry.

[00032] In an embodiment, private keys (e.g., for public/private cryptographic operations) can be protected by the SMM. In one embodiment, an SMM component may provide public/private operations such as generating public/private key pairs. In an  
20 embodiment, an SMM operation performs Diffie-Hellman exchange using protected private keys. The SMM operation may encrypt data with a private key identified by key ID 268. Similarly, an SMM operation may decrypt data with a private key identified by key ID 268.



[00033] In an embodiment, Program End Notification 275 may be issued by the program or device driver to denote the end of the program segment's use of the SMM facilities prior to the program's return to its caller. In an embodiment, Program End Notification 275 is an SMI notification. The handler (e.g., SMI handler) for this notification resets the PIPC table 215's PSN value from TRUE to FALSE for the entry matching the SSM recovered program counter. In one embodiment, the SMM module will no longer act on future Operation Notifications from this program until Program Start Notification 270 is again properly initiated from the valid program image. This effectively locks out other malicious programs from attempting to circumvent the SMM module for this program ID by modifying the program's data structures and then simply jumping into the instruction just prior to the valid program's code that invokes the SMI Operation Notification. By bounding all Operation Notifications between Program Start Notification 270 and Program End Notification 275, the program writer can be assured that all program segments between Notification 270 and Notification 275 have been executed before an Operation Notification initiated from the program's valid image will be allowed.

[00034] Turning now to FIGs. 3A-3C, the particular methods associated with embodiments of the invention are described in terms of computer software and hardware with reference to a flowchart. The methods to be performed by a computing device may constitute state machines or computer programs made up of computer-executable instructions. The computer-executable instructions may be written in a computer programming language or may be embodied in firmware logic. If written in a programming language conforming to a recognized standard, such instructions can be executed on a variety of hardware platforms and for interface to a variety of operating systems. In addition, embodiments of the invention are not described with reference to

any particular programming language. It will be appreciated that a variety of programming languages may be used to implement embodiments of the invention as described herein. Furthermore, it is common in the art to speak of software, in one form or another (e.g., program, procedure, process, application, etc.), as taking an action or  
5 causing a result. Such expressions are merely a shorthand way of saying that execution of the software by a computing device causes the device to perform an action or produce a result.

[00035] FIGs. 3A-3C are flow diagrams illustrating selected aspects of a method for secure inter-platform and intra-platform communications, according to an embodiment of  
10 invention. The method described in FIGs. 3A-3C may be implemented with the data structures described with reference to FIGs. 2A-2B. In an alternative embodiment, the method described in FIGs. 3A-3C may be implemented with different data structures.

[00036] FIG. 3A is a flow diagram illustrating certain aspects of a method for initializing a protected region of memory (e.g., SMRAM 200, shown in FIG. 2A),  
15 according to an embodiment of the invention. Referring to process block 305, a VPI table (e.g., VPI table 205, shown in FIG. 2A) is populated with program identification information. In one embodiment, the VPI table is populated via a secure out-of-band channel. Referring to process block 310, a PIKI table (e.g., PIKI table 210, shown in FIG. 2A) is populated with confidential information such as key values (e.g., key values 212,  
20 shown in FIG. 2A) and corresponding key identifiers (e.g., key IDs 214, shown in FIG. 2A) associated with program identifiers (e.g., program IDs 216, shown in FIG. 2A).

[00037] Referring to process block 315, an SMM module (or other trusted agent) searches program memory (e.g., program memory 235, shown in FIG. 2B) for programs

corresponding to the program IDs provisioned in process block 310. Referring to process block 320, the SMM module sets a Program Counter Base (PCB) (e.g., PCB 222, shown in FIG. 2A) and a Program Counter Limit (PCL) (e.g., PCL 224, shown in FIG. 2A) for the associated program ID of each found program.

5       **[00038]** FIGs. 3B-3C are a flow diagram illustrating certain aspects of a method for secure inter-platform and intra-platform communication, according to an embodiment of the invention. Referring to process block 325, a Program Start Notification (e.g., Program Start Notification 270, shown in FIG. 2B) triggers the SMM. An SMM module recovers the program counter from, for example, a saved state map at process block 330. Referring  
10 to process block 335, the SMM module searches a PIPC table for an entry corresponding to the program that sent the program start notification. In an embodiment, if an entry is found, the SMM module checks to see whether the recovered program counter is between the PCB and the PCL at process block 340. Checking to see whether the recovered program counter is between the PCB and the PCL helps to ensure that the program start  
15 notification was actually sent by the program and not by malicious software. In some embodiments, the SMM module re-verifies that the invoking program image matches an entry in the VPI table (e.g., by calculating a hash value and comparing the calculated hash value to a predetermined hash value stored in the VPI table) as shown by process block 345.

20       **[00039]** Referring to process block 350, a program start notification flag is set to true and control is returned to the invoking program. In an embodiment, the invoking program is now allowed to modify the data in a program data table (PDT) (e.g., PDT 240, shown in FIG. 2B). The program updates buffer locations (e.g., via DBP 250 and IBP

258, shown in FIG. 2B) and provides appropriate key identifiers (e.g., key identifiers 268, shown in FIG. 2B) at process block 355. The program completes buffer related tasks (e.g., allocation of the buffers, etc.) at process block 360. Referring to process block 365, the program triggers an operation notification (e.g., an SMI notification) and control returns to  
5 the SMM.

[00040] Referring to process block 370, an SMM module recovers the program counter from the saved state map (SSM). The SMM module searches the PIPC table for an entry corresponding to the invoking program at 375. Referring to process block 376, the SMM module determines whether the recovered program counter is between the PCB  
10 and the PCL as recorded in the entry of the PIPC table that corresponds to the invoking program. In one embodiment, there may be multiple allowed ranges for the PCB and the PCL. In such an embodiment, the SMM module may determine whether the program counter is within one of the multiple allowed ranges for the PCB and the PCL. Referring to process block 378, the SMM module determines whether the program start notification  
15 flag in the invoking program's PIPC table entry is set to true. In an embodiment, if either of the conditions checked in process blocks 376 or 378 are not true, then the SMM module sets the appropriate error code (e.g., error code 272, shown in FIG. 2B) and returns control to the invoking program as shown at 380. Referring to process block 382, the SMM  
20 module performs an operation as specified by an operation request (e.g., operation request 245, shown in FIG. 2B). The operation may be performed on data that is in a data buffer as referenced by a data buffer pointer (e.g., DPB 250, shown in FIG. 2B). The SMM module may use a key value (e.g., a key value 212, shown in FIG. 2A) for a corresponding program ID and key ID to process the data. In an embodiment, the SMM module skips

masked areas as specified by a data mask buffer (e.g., data mask buffer 256, shown in FIG. 2B).

[00041] If the operation is successful, the SMM module may set an error code to NONE and return control to the invoking program at process block 384. Referring to  
5 process block 386, the program may send a program end notification to prevent the program data table from being modified by an unauthorized program. An SMM module recovers the program counter for the invoking program at process block 388. The SMM module searches the PIPC table for an entry corresponding to the invoking program at  
10 390. In an embodiment, the SMM module determines whether the program counter for the invoking program is between the PCB and the PCL at process block 392. The program start notification flag is set to false at process block 394 and control is returned to the invoking program at 396. In an embodiment, the program data table cannot be modified while the program start notification flag is set to false.

[00042] FIG. 4 is a block diagram of framework 400 for encrypting outbound  
15 packets, according to an embodiment of the invention. For the purposes of illustrating an embodiment of the invention, FIG. 4 refers to the transmit queue of framework 400. It is to be appreciated that the operation described with reference to the outbound queue shown in FIG. 4 may also apply to the inbound queue on the receive side of platform 400 (not shown).

20 [00043] The illustrated embodiment of Framework 400 includes processor 405, physical memory 410, Input/Output (I/O) controller hub 415, and Media Access Control (MAC) device 420. Processor 405 may include a microprocessor, microcontroller, field programmable gate array (FPGA), application specific integrated circuit (ASIC), central

processing unit (CPU), programmable logic device (PLD), and similar devices that access instructions from system storage (e.g., memory 410), decode them, and execute those instructions by performing arithmetic and logical operations.

[00044] Physical memory 410 may include a wide variety of memory devices including read-only memory (ROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), random access memory (RAM), non-volatile random access memory (NVRAM), cache memory, flash memory, and other memory devices. In an embodiment, Physical memory 410 includes SMRAM 425 and driver memory 430. In one embodiment, SMRAM 425 and driver memory 430 are two regions of the same memory device. In an alternative embodiment, SMRAM 425 and driver memory 430 are implemented on separate memory devices.

[00045] In one embodiment, I/O Controller Hub (ICH) 415 may provide an interface between framework 400 and peripheral I/O devices as well as between framework 400 and MAC device 420, which may provide an interface to an external network (not shown).

[00046] In an embodiment, framework 400 transmits packets as described below. A network device driver (not shown) generates an SMI Program Start Notification as shown by reference number 435. An SMI handler recovers the program counter of the device driver and compares the recovered program counter to a range of allowable program counter values stored in PIPC table 440. In an embodiment, the device driver's address is retrieved from the recovered program counter.

[00047] The network device driver sets up buffer(s) 445 for transmission (e.g., with interrupts disabled) at 450. After the buffer(s) 445 are set up, the network device driver causes an SMI Operation Notification specifying Operation Requests of “encrypt” and/or “integrity generation” notification types as shown by reference number 455. An SMI handler records the physical addresses of frames deposited in buffer(s) 445 that are ready for transmission. In an embodiment, a DBP in a PDT specifies the physical addresses of buffer(s) 445.

[00048] In an embodiment, the SMI handler runs encrypt code 460 and/or integrity generation code on, for example, buffer(s) 445 holding the data that is ready to be sent. In an embodiment, buffer(s) 445 are encrypted in place and/or integrity HMAC is generated in a buffer referenced by an integrity buffer pointer of a PDT (not shown) and control is returned to the network device driver. In an embodiment, the device driver uses direct memory access to send the frames stored buffer(s) 445 to MAC device 420. Reference number 465 illustrates the buffered data being sent to MAC device 420 via direct memory access. MAC device 420 sends a transmit complete signal to processor 405 after transmitting the data it received from buffer(s) 445. In an embodiment, the device driver triggers an SMI program end notification after the transmission is complete.

[00049] As shown in FIG. 4 (e.g., in reference numbers 435, 450, and 455), embodiments of the invention may provide intra-platform communication as well as inter-platform communication. One example of intra-platform communication is the exchange of authenticated heartbeat messages between security software on the host and a firmware security agent on an embedded management processor on the platform (Proactive/Navassa) to establish the presence of the security components.

[00050] Regular heartbeat communication establishes the presence of the security agents on the platform. This communication is sensitive and, in an embodiment, it may be protected against spoofing. This communication may be over any medium, for example, via direct memory access, or over a dedicated management bus. In an embodiment, (as  
5 described above) an integrity check and/or an encrypt operation may be applied to the heartbeat message in a tamper-resistant and confidential environment. An embedded management processor may set up the keys so that it can verify the heartbeat messages. In an embodiment, the keys used are not divulged to the security software whose presence is established by the heartbeat. The end-points communicating in this case may be the host  
10 software and management software on the embedded management controller. The same concept can be used for sensitive inter-program communication or for integrity preservation of data for a single program (this single program is both the source and destination of the data exchange). In one embodiment, a random nonce may be used in conjunction with the key to prevent replay attacks in an alternate embodiment.

15 [00051] As shown in FIG. 4 (e.g., in reference numbers 435 and 452), embodiments of the invention may provide intra-program communication as well as inter-program communication. In an embodiment, the program may be a kernel component (e.g., a ring-0 program). In one embodiment, the program may be an application (e.g., a ring-3 program). In an embodiment in which the program is an application, the protected  
20 communications may be referred to as inter-process and/or intra-process communications. For example, in an embodiment, a program may secure its own data and state over time, from invocation to invocation, so that no other program can modify its data or state unbeknownst to the program that owns the data or state.



[00052] In such an embodiment, the “legitimate” program may use the SMM protected keys to hide and reveal data by encrypting and decrypting the data so that only the same (or other) legitimate program(s) can access the data. In an alternative embodiment, the program can use the SMM protected keys to verify the integrity of its state, from invocation to invocation, by calculating an HMAC for the internal program state when the program is invoked to assure that the data is unchanged since the previous invocation. Prior to the program’s return, the program may issue an SMI to generate a new HMAC for its internal state or other data to be verified at the time of the next invocation. Alternatively, the program can create a hash value or running checksum for its internal data structures and simply use the SMM component to sign or otherwise protect the integrity of the program generated hash/checksum of its own data structures. In such an embodiment, the program will calculate the hash/checksum of its internal data structures prior to the SMI Program End Notification and after the SMI Program Start Notification. Operation Notifications may be used to check the integrity of this hash/checksum prior to its use, and new integrity HMACs may be generated again after the program has finished manipulating its data structures and updated its hash/checksum. In an embodiment, errors in integrity validation are reported to the calling program via error codes in the PDT (e.g., PDT 240, shown in FIG. 2B).

[00053] FIG. 5 is a block diagram of framework 500 illustrating an embodiment of the invention that supports network security protocols at different layers. In an embodiment, framework 500 may support network layer security (e.g., Internet Protocol Security (IPSEC)), Transport Layer Security (TLS), and/or application layer security.

[00054] In one embodiment, network driver 510 "tags" the frame descriptors received from (and/or transmitted to) various network layer protocols 522-526 with additional meta-data (e.g., 532, 534, and 536). These tags are also pre-provisioned in SMRAM (along with the keys) and used by the SMI handlers to decide, for example, which encryption algorithm to use, which keys to use, and what layers to encrypt. In an embodiment, the upper protocol layers (e.g., protocol layers 522-526) are also source verified when calling into network driver 510 to prevent an attacker from injecting frames into secured sessions.

[00055] FIG. 6 is a transaction diagram illustrating transaction 600 implemented according to an embodiment of the invention. Transaction 600 includes host network device driver 605, host physical memory 610, SMI handler 615, and network controller 620. In an embodiment, device driver 605 causes program start SMI notification 625 to be sent to SMI handler 615. SMI handler 615 may identify device driver 605 as the program that is the source for the transaction via, for example, a saved state map (not shown). SMI handler returns control to device driver 605 at reference number 630.

[00056] In an embodiment, device driver 605 may disable interrupts to protect against context switching during transaction 600 as shown by 632. Device driver 605 may then insert frame buffers that are ready to be transmitted into a transmit First In First Out (FIFO) queue (queue not shown) as shown by 634. In one embodiment, the interrupts are enabled when the FIFO queue is loaded as shown by 636. Device driver 605 may then send an encrypt operation SMI notification to SMI handler 615 as shown by 638.

[00057] SMI handler 615 may recheck the source program counter to confirm that it corresponds to device driver 605. In an embodiment, SMI handler 615 encrypts data that

is specified in, for example, a program data table for device driver 605 using key material that is stored in SMRAM. SMI handler 615 may then return control to device driver 605 via operation SMI return 640. Device driver 605 may then notify network controller 620 that the packets are ready for transmission as shown by reference number 645. Network  
5 controller 620 may use, for example, direct memory access to send the packets to the network interface card memory in host physical memory 610. In an embodiment, network controller 620 notifies device driver 605 that the packets were transmitted at 650.

[00058] Elements of embodiments of the present invention may also be provided as a machine-accessible medium for storing the machine-executable instructions. A  
10 machine-accessible medium includes any mechanism that provides (e.g., stores and/or transmits) information in a form accessible by a machine (e.g., a computer, a network device, a personal digital assistant, a manufacturing tool, any device with a set of one or more processors, etc.). For example, a machine-accessible medium includes  
15 recordable/non-recordable media (e.g., read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices, etc.), as well as electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

[00059] It should be appreciated that reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or  
20 characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be appreciated that two or more references to “an embodiment” or “one embodiment” or “an alternative embodiment” in various portions of this specification are not necessarily all

referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

[00060] Similarly, it should be appreciated that in the foregoing description of embodiments of the invention, various features are sometimes grouped together in a single  
5 embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed subject matter requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single  
10 foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

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## CLAIMS

What is claimed is:

1. A method comprising:  
invoking a management mode with an operation notification from a software  
5 program executing in a program memory of a host system, the management mode having a  
protected region of memory that is inaccessible to a host operating system, wherein the  
host operating system temporarily relinquishes control of the host system to the  
management mode; and  
providing a security operation from the protected region of memory to the software  
10 program executing in the program memory, if the management mode is invoked.
2. The method of claim 1, further comprising:  
invoking the management mode with a start notification, the start notification to  
indicate that the software program is executing in program memory; and  
setting a start indicator in the protected region of memory to show that the software  
15 program is executing in program memory.
3. The method of claim 2, wherein providing the security operation from the  
protected region of memory to the software program executing in the program memory  
further comprises:  
providing the security operation from the protected region of memory to the  
20 software program executing in the program memory, if the start indicator is set.
4. The method of claim 2, further comprising:  
verifying that the software program provided the start notification.

5. The method of claim 4, wherein verifying that the software program provided the start notification comprises:
- obtaining a program counter value of the software program, responsive to receiving the start notification; and
- 5 comparing the program counter value to an allowed range of program counter values.
6. The method of claim 4, further comprising:
- verifying the integrity of the software program.
7. The method of claim 6, wherein verifying the integrity of the software program
- 10 comprises:
- computing a hash value of at least a portion of an image of the software program;
  - and
  - comparing the computed hash value to a predetermined hash value to determine whether the software program is modified.
- 15 8. The method of claim 1, wherein the software program is a kernel program.
9. The method of claim 8, wherein the kernel program is a device driver.
10. The method of claim 1, wherein providing the security operation from the protected region of memory to the software program executing in the program memory
- 20 comprises: accessing data stored in the protected region of memory for the software program.

11. The method of claim 10, wherein accessing data stored in the protected region of memory for the software program comprises:

accessing keying material for the software program, wherein the keying material is stored in the protected region of memory.

5 12. The method of claim 11, wherein accessing keying material for the software program comprises accessing at least one of:

an encryption key for a cryptographic operation; and  
a session key for an integrity check operation.

13. The method of claim 1, wherein providing the security operation from the  
10 protected region of memory to the software program executing in the program memory comprises:

providing security processing for data of the software program.

14. The method of claim 13, wherein the data of the software program comprises at least one of:

15 state information of the software program;  
transmit buffer data to be transmitted to a second software program executing on the same processor as the software program;  
transmit buffer data to be transmitted to a second software program executing on another processor of the host system; and  
20 transmit buffer data to be transmitted to a second software program executing on another host system.

15. The method of claim 13, wherein providing the security processing for data of the software program comprises at least one of:

encrypting the data;  
decrypting the data;  
checking the integrity of the data; and  
adding integrity information to the data.

5

16. The method of claim 15, wherein checking the integrity of the data comprises:  
computing a hash value of the data; and  
comparing the computed hash value to a predetermined hash value.

17. The method of claim 1, further comprising:

10 initializing the security operation over a secure channel.

18. The method of claim 17, wherein initializing the security operation over the secure channel comprises:

storing one or more program identifiers in the protected region of memory,  
wherein each program identifier is to identify a software program that is authorized to  
15 invoke the management mode; and

storing keying material in the protected region of memory, the keying material to  
be accessed by a software program identified by at least one of the one or more program  
identifiers.

19. An apparatus comprising:

20 a host processor to execute instructions of a software program, the software  
program having instructions to invoke a security operation resident in a secure memory,  
wherein a host operating system temporarily relinquishes control of a host system to the  
security operation, responsive to an invocation from the software program;



a program memory to store data of the software program communicatively coupled to the host processor; and

the secure memory not visible to the host operating system, communicatively coupled to the program memory, the secure memory to provide the security operation to  
5 process the data of the software program.

20. The apparatus of claim 19, wherein the software program is a network device driver and the program memory is a transmit buffer to store transmit data.

21. The apparatus of claim 20, wherein the security operation is at least one of:  
encrypting the transmit data; and  
10 checking the integrity of the transmit data.

22. The apparatus of claim 20, further comprising:  
a network interface communicatively coupled with the program memory to receive the transmit data from the program memory and to send the transmit data to another host system over a network.

15 23. An article of manufacture comprising:  
an electronically accessible medium providing instructions that, when executed by an apparatus, cause the apparatus to  
invoke a management mode with an operation notification from a software program executing in a program memory of a host system, the management mode having a  
20 protected region of memory that is inaccessible to a host operating system, wherein the host operating system temporarily relinquishes control of the host system to the management mode; and

provide a security operation from the protected region of memory to the software program executing in the program memory, if the management mode is invoked.

24. The article of manufacture of claim 23, wherein the electronically accessible medium provides further instructions that, when executed by the apparatus, cause the apparatus to:

invoke the management mode with a start notification, the start notification to indicate that the software program is executing in program memory; and

set a start indicator in the protected region of memory to show that the software program is executing in program memory.

25. The article of manufacture of claim 24, wherein the instructions that, when executed by the apparatus, cause the apparatus to provide the security operation from the protected region of memory to the software program executing in the program memory cause the apparatus to:

provide the security operation from the protected region of memory to the software program executing in the program memory, if the start indicator is set.

26. The article of manufacture of claim 24, wherein the electronically accessible medium provides further instructions that, when executed by the apparatus, cause the apparatus to:

verify that the software program provided the start notification.

27. The article of manufacture of claim 26, wherein the instructions that, when executed by the apparatus, cause the apparatus to verify that the software program provided the start notification cause the apparatus to:

obtain a program counter value of the software program, responsive to receiving the start notification; and

compare the program counter value to an allowed range of program counter values.

28. The article of manufacture of claim 26, wherein the electronically accessible  
5 medium provides further instructions that, when executed by the apparatus, cause the apparatus to:

verify the integrity of the software program.

29. The article of manufacture of claim 28, wherein the instructions that, when  
executed by the apparatus, cause the apparatus to verify the integrity of the software  
10 program cause the apparatus to:

compute a hash value of at least a portion of an image of the software program;

and

compare the computed hash value to a predetermined hash value to determine  
whether the software program is modified.

15 30. The article of manufacture of claim 23, wherein the instructions that, when  
executed by the apparatus, cause the apparatus to provide the security operation from the  
protected region of memory to the software program executing in the program memory  
cause the apparatus to:

20 access keying material for the software program, wherein the keying material is  
stored in the protected region of memory.

31. The article of manufacture of claim 23, wherein the instructions that, when  
executed by the apparatus, cause the apparatus to provide the security operation from the

protected region of memory to the software program executing in the program memory  
cause the apparatus to:

provide security processing for data of the software program.

32. The article of manufacture of claim 31, wherein the instructions that, when  
5 executed by the apparatus, cause the apparatus to provide security processing for data of  
the software program cause the apparatus to perform at least one of:

encrypt the data;

decrypt the data; and

check the integrity of the data.

10 33. The article of manufacture of claim 23, wherein the electronically accessible  
medium provides further instructions that, when executed by the apparatus, cause the  
apparatus to:

initialize the security operation over a secure channel.

34. The article of manufacture of claim 33, wherein the instructions that, when  
15 executed by the apparatus, cause the apparatus to provide security processing for data of  
the software program cause the apparatus to:

store one or more program identifiers in the protected region of memory, wherein  
each program identifier is to identify a software program that is authorized to invoke the  
management mode; and

20 store keying material in the protected region of memory, the keying material to be  
accessed by a software program identified by at least one of the one or more program  
identifiers.

35. A system comprising:

a host processor to execute instructions of a software program, the software program having instructions to invoke a security operation resident in a secure memory, wherein a host operating system temporarily relinquishes control of a host system to the security operation, responsive to an invocation from the software program;

5 a synchronous dynamic random access memory (SDRAM) device to store data of the software program communicatively coupled to the host processor; and

the secure memory not visible to the host operating system, communicatively coupled to the SDRAM device, the secure memory to provide the security operation to process the data of the software program.

10 36. The apparatus of claim 35, wherein the software program is a network device driver and the program memory is a transmit buffer to store transmit data.

37. The apparatus of claim 36, wherein the security operation is at least one of:  
encrypting the transmit data; and  
checking the integrity of the transmit data.

15 38. The system of claim 36, further comprising:  
a network interface communicatively coupled with the SDRAM device to receive the transmit data from the program memory and to send the transmit data to another host system over a network.

20

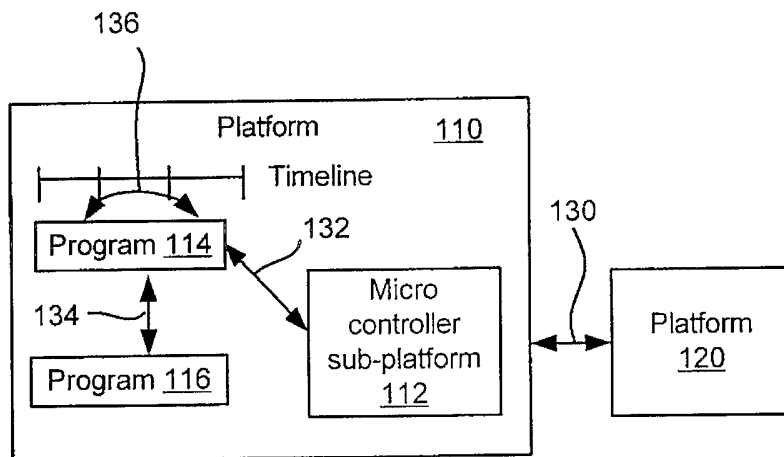
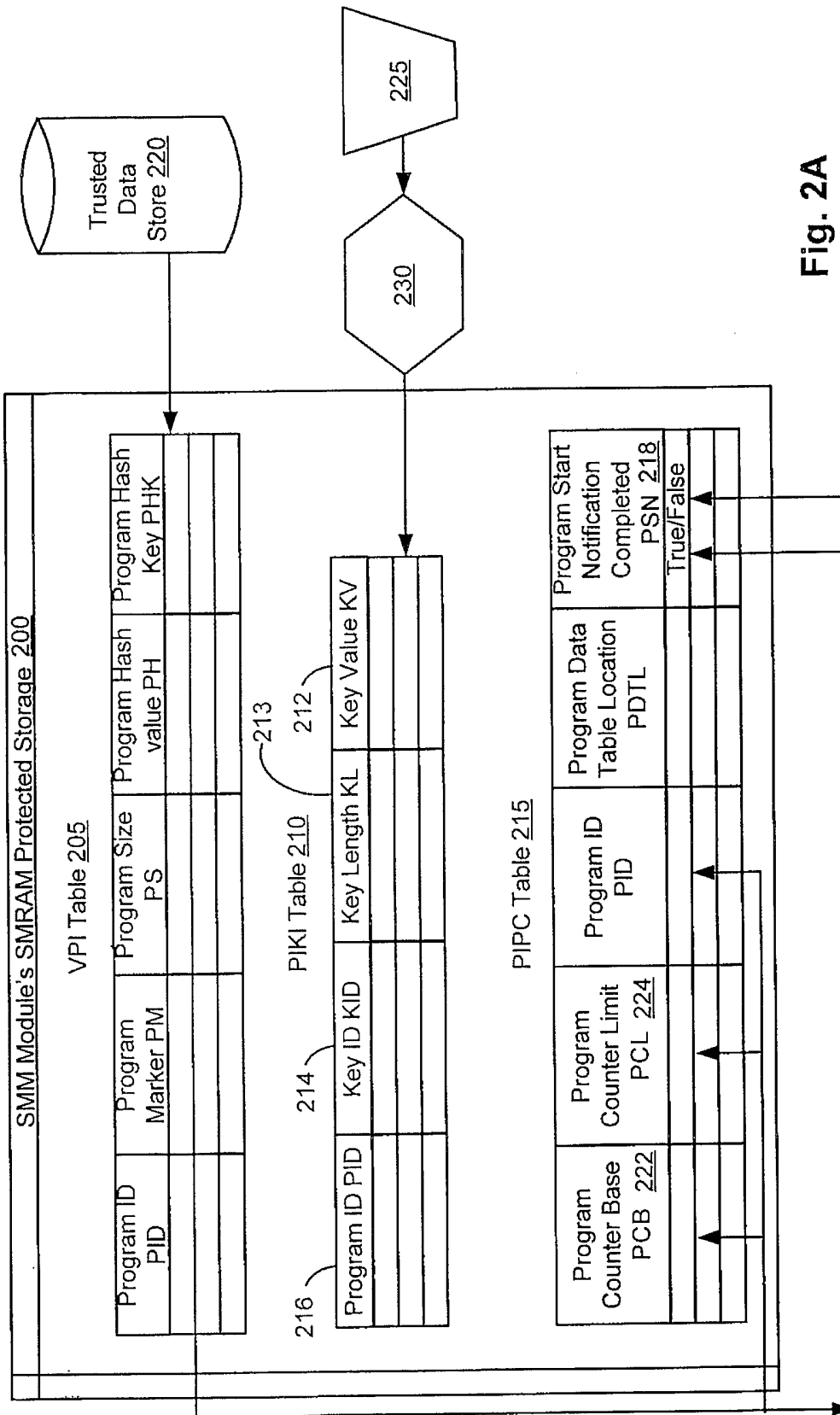


Fig. 1







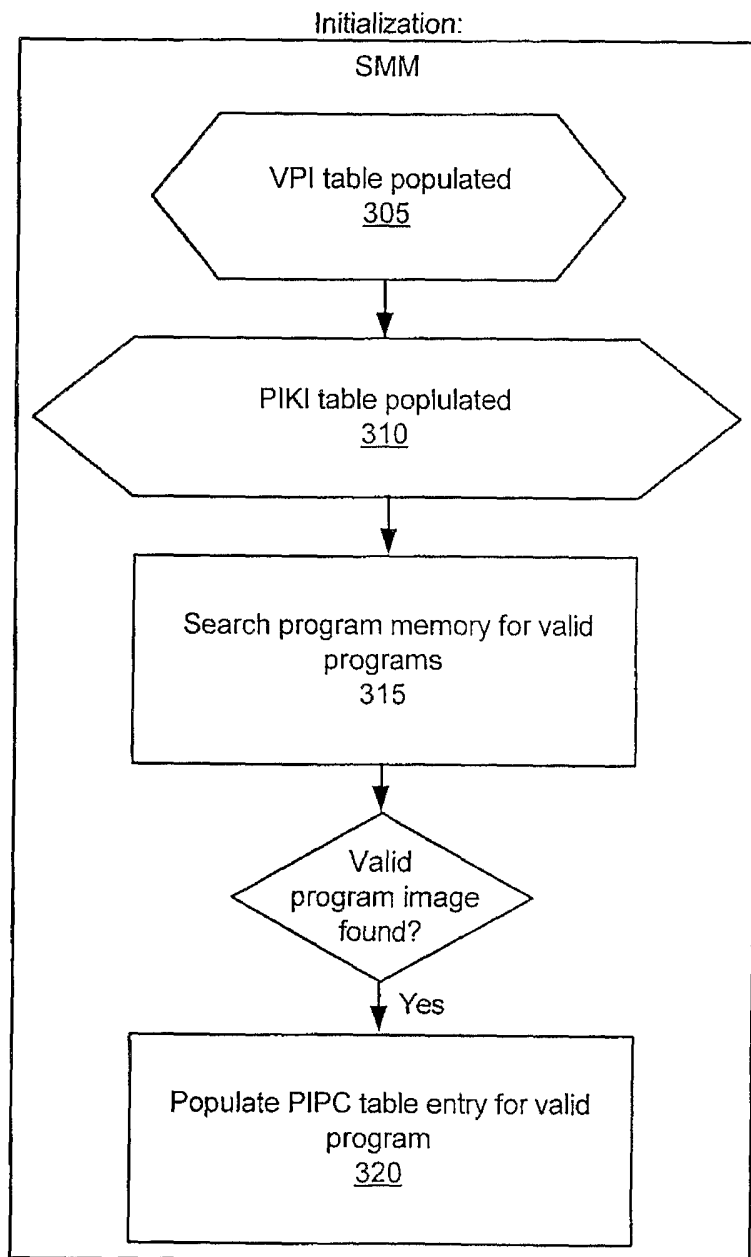


Fig. 3A

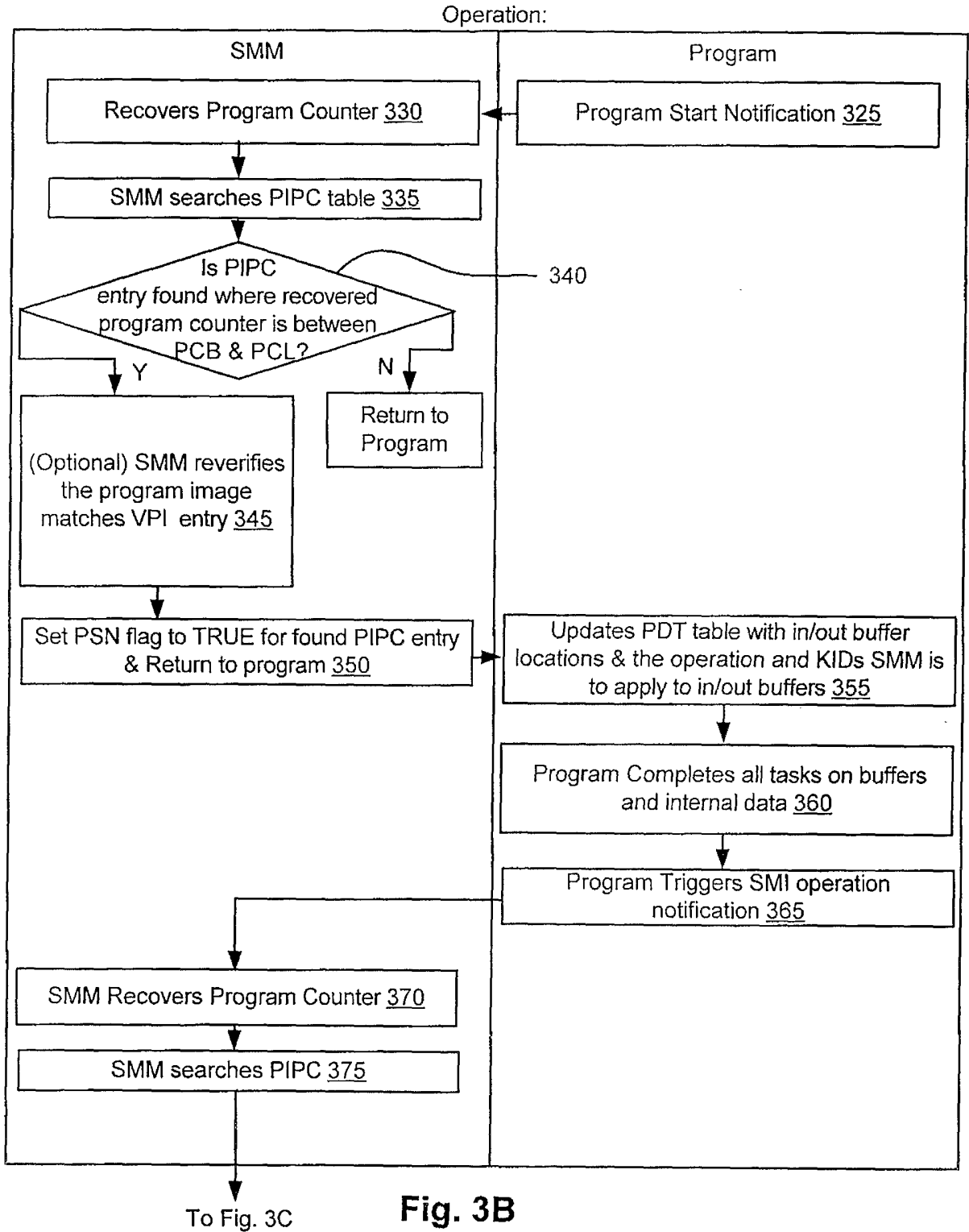


Fig. 3B

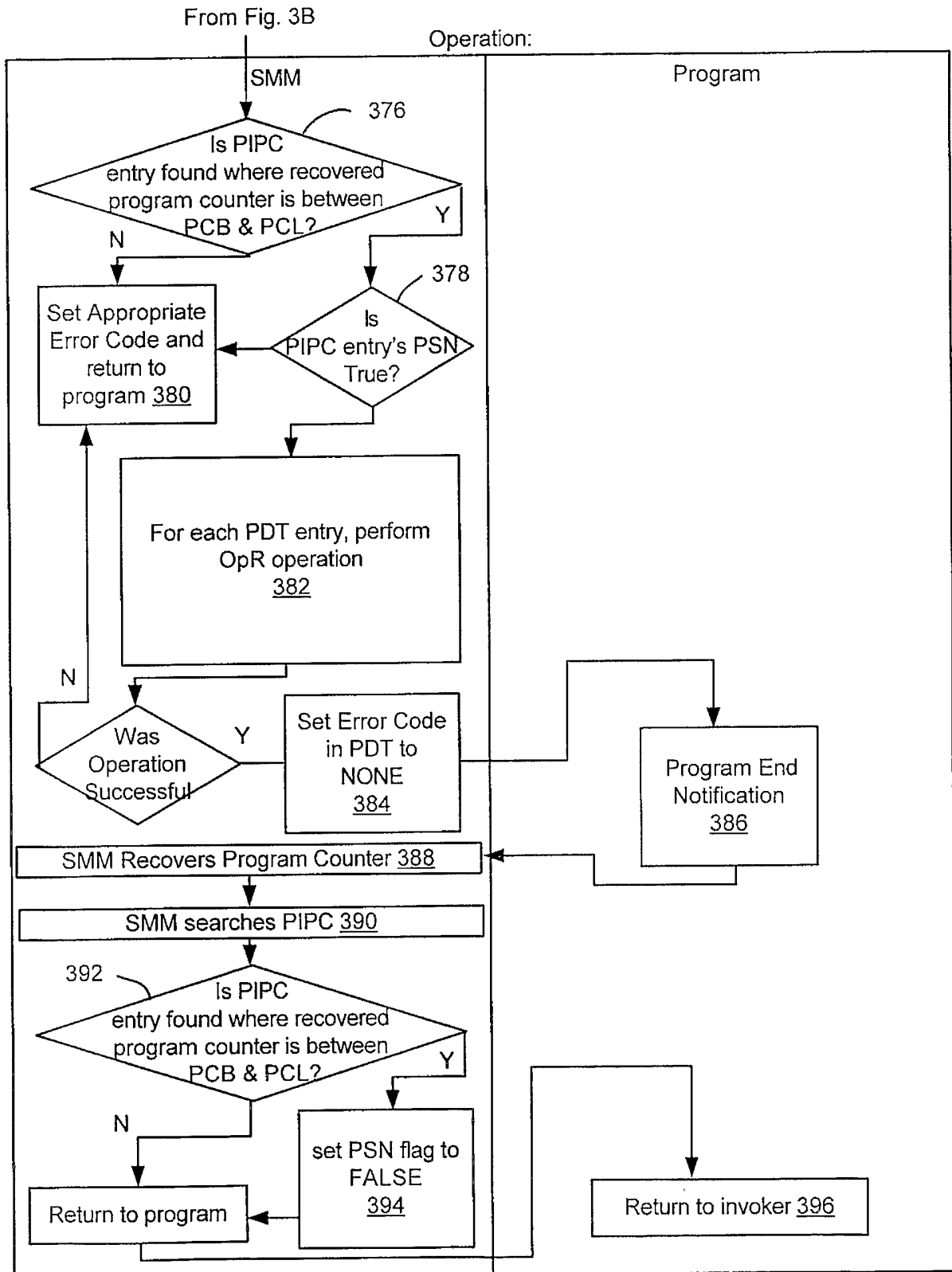


Fig. 3C

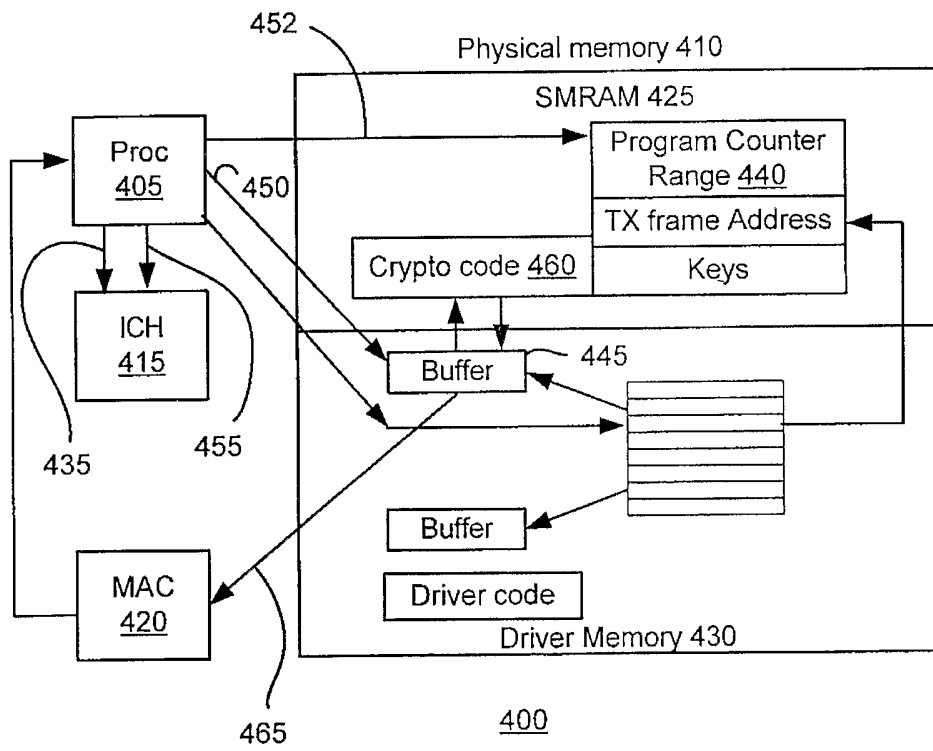
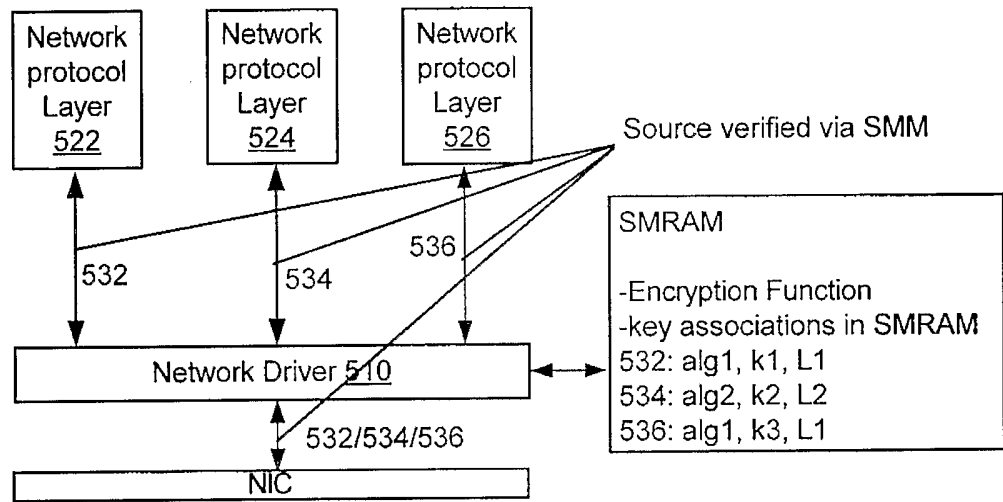
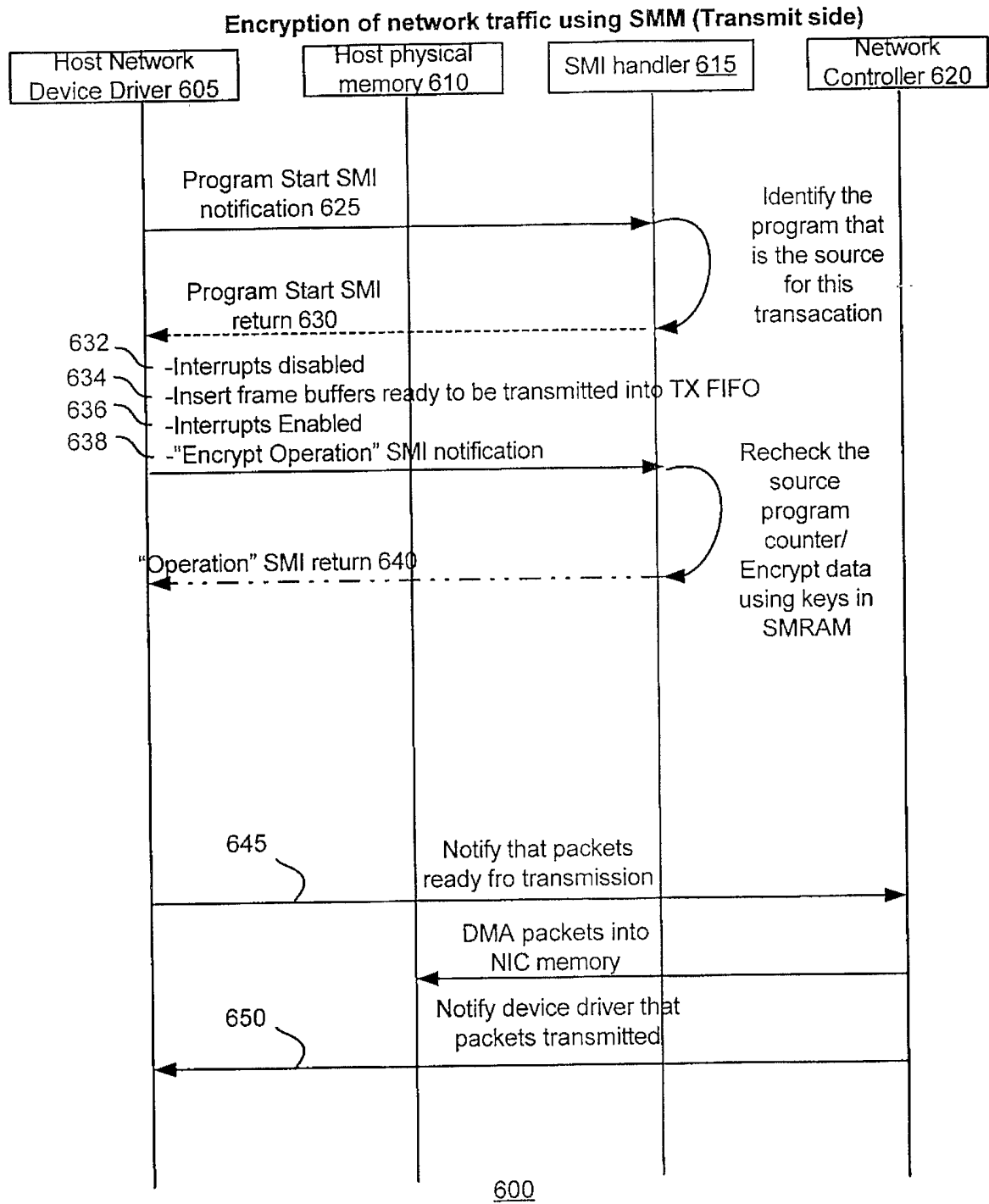


Fig. 4



500

Fig. 5



**Fig. 6**

**INTERNATIONAL SEARCH REPORT**

International Application No  
PCT/US2005/022577

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> G06F1/00				
According to International Patent Classification (IPC) or to both national classification and IPC				
<b>B. FIELDS SEARCHED</b>				
Minimum documentation searched (classification system followed by classification symbols) G06F H04L				
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched				
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal				
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>				
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.		
X	US 2003/229794 A1 (SUTTON JAMES A ET AL) 11 December 2003 (2003-12-11)  paragraph '0005! paragraph '0018! - paragraph '0019! paragraph '0021! - paragraph '0022! paragraph '0028! - paragraph '0029! paragraph '0031!  ----- -/--	1, 2, 8, 10, 13, 23, 24, 30, 31, 33, 35		
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.				
<input checked="" type="checkbox"/> Patent family members are listed in annex.				
° Special categories of cited documents :				
<table style="width:100%; border: none;"> <tr> <td style="width:50%; border: none; vertical-align: top;"> <ul style="list-style-type: none"> <li>*A* document defining the general state of the art which is not considered to be of particular relevance</li> <li>*E* earlier document but published on or after the international filing date</li> <li>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</li> <li>*O* document referring to an oral disclosure, use, exhibition or other means</li> <li>*P* document published prior to the international filing date but later than the priority date claimed</li> </ul> </td> <td style="width:50%; border: none; vertical-align: top;"> <ul style="list-style-type: none"> <li>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</li> <li>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</li> <li>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</li> <li>*Z* document member of the same patent family</li> </ul> </td> </tr> </table>			<ul style="list-style-type: none"> <li>*A* document defining the general state of the art which is not considered to be of particular relevance</li> <li>*E* earlier document but published on or after the international filing date</li> <li>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</li> <li>*O* document referring to an oral disclosure, use, exhibition or other means</li> <li>*P* document published prior to the international filing date but later than the priority date claimed</li> </ul>	<ul style="list-style-type: none"> <li>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</li> <li>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</li> <li>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</li> <li>*Z* document member of the same patent family</li> </ul>
<ul style="list-style-type: none"> <li>*A* document defining the general state of the art which is not considered to be of particular relevance</li> <li>*E* earlier document but published on or after the international filing date</li> <li>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</li> <li>*O* document referring to an oral disclosure, use, exhibition or other means</li> <li>*P* document published prior to the international filing date but later than the priority date claimed</li> </ul>	<ul style="list-style-type: none"> <li>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</li> <li>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</li> <li>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</li> <li>*Z* document member of the same patent family</li> </ul>			
Date of the actual completion of the international search  10 November 2005		Date of mailing of the international search report  24/11/2005		
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer  Chabot, P		

## INTERNATIONAL SEARCH REPORT

International Application No

PCT/US2005/022577

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>US 2004/039924 A1 (BALDWIN ROBERT W ET AL) 26 February 2004 (2004-02-26)</p> <p>abstract paragraph '0018! paragraph '0034! paragraph '0043! paragraph '0067! paragraph '0073! paragraph '0090! paragraph '0094!</p>	<p>1,2,4,6, 7,10-13, 15,16, 19,23, 24,26, 28-30,35</p>
X	<p>WO 01/42874 A (PHOENIX TECHNOLOGIES INC) 14 June 2001 (2001-06-14)</p> <p>page 1, line 1 - line 16 page 2, line 12 - line 25 page 3, line 5 - line 12 page 4, line 4 - line 17 page 5, line 12 - line 17</p>	<p>1-4,19, 23,24, 27,35</p>
A	<p>US 5 944 821 A (ANGELO ET AL) 31 August 1999 (1999-08-31) abstract</p>	<p>1-38</p>
A	<p>US 6 105 137 A (GRAUNKE ET AL) 15 August 2000 (2000-08-15) column 4, line 13 - line 16</p>	<p>5,27</p>
A	<p>US 2003/005272 A1 (NALAWADI RAJEEV K ET AL) 2 January 2003 (2003-01-02) paragraph '0009!</p>	<p>2,4,24, 26</p>
A	<p>US 6 658 515 B1 (LARSON MARK A ET AL) 2 December 2003 (2003-12-02) column 6, line 39 - line 52</p>	<p>14</p>



## INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US2005/022577

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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			CN 1675623	A 28-09-2005
			EP 1512074	A2 09-03-2005
			JP 2005529401	T 29-09-2005
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