(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 April 2004 (22.04.2004)

PCT

(10) International Publication Number
WO 2004/034428 A2

(51) International Patent Classification[7]: H01L

(21) International Application Number:
PCT/US2003/031362

(22) International Filing Date: 2 October 2003 (02.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/416,503	4 October 2002 (04.10.2002)	US
60/417,217	8 October 2002 (08.10.2002)	US
60/446,758	11 February 2003 (11.02.2003)	US
10/677,069	1 October 2003 (01.10.2003)	US

(71) Applicant: **INTERNATIONAL RECTIFIER CORPORATION** [US/US]; 233 Kansas Street, El Segundo, CA 90245 (US).

(72) Inventor: **STANDING, Martin**; 19 Barden Park Road, Tonbridge, Kent TN9 1XD (GB).

(74) Agents: **WEINER, Samuel, H.** et al.; Ostrolenk, Faber, Gerb & Soffen, LLP, 1180 Avenue of the Americas, New York, NY 10036 (US).

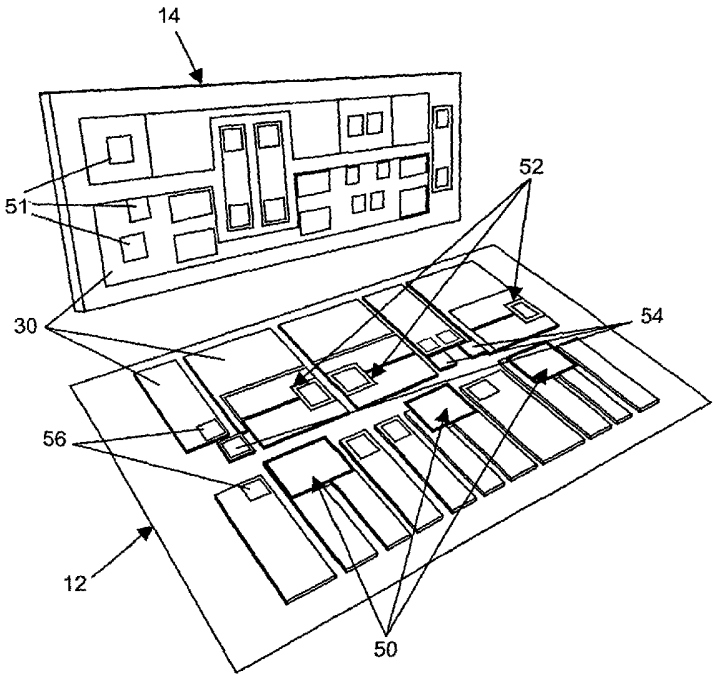
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE PACKAGE



(57) Abstract: A semiconductor package that includes two circuit boards and at least one semiconductor device which is disposed between the two circuit boards and connected to external connectors disposed on at least one of the circuit boards.

WO 2004/034428 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SEMICONDUCTOR DEVICE PACKAGE

RELATED APPLICATIONS

[0001] The application is based on and claims benefit of United States Provisional Application No. 60/416,503, filed on October 4, 2002, entitled Multiple Phase Inverter Modules for High Density Power Applications, United States Provisional Application No. 60/417,217, filed on October 8, 2002, entitled Multiple Phase Inverter Modules For High Density High Power Applications and United States Provisional Application No. 60/446,758, filed February 11, 2003, entitled Intelligent Multiphase Modules, to which claims of priority are hereby made.

BACKGROUND OF THE INVENTION

[0002] To integrate a semiconductor component into an electronic circuit, the component must be packaged. Figure 1 shows the cross-section of a typical, multi-chip package 5, which includes substrate 6, semiconductor components 7, and molded housing 8. It should be noted that semiconductor components are interconnected inside the package and to external connectors (not shown) by connectors such as bond wires 9A and in some cases conductive clips, e.g. 9B.

[0003] Such connectors add to the overall resistance and inductance of the package, and cause undesirable effects such as ringing.

[0004] Furthermore, if the package contains heat generating components, in a conventional package such as package 5, a heatsink (not shown) may be thermally coupled to substrate 6 to dissipate the generated heat. The size of the heatsink typically depends on the amount of heat generated. Thus, a large amount of heat would require a larger heatsink. Therefore, heat generation has a bearing on the size of the package.

SUMMARY OF THE INVENTION

[0005] It is an object of the present invention to provide a package for a semiconductor device or a plurality of semiconductor devices.

[0006] A semiconductor package according to the present invention includes a first circuit board, a second circuit board, and at least one semiconductor device disposed between the two circuit boards. In the preferred embodiment of the present invention the circuit boards are the thermally conductive variety such as insulated metal substrate or double bonded copper. When thermally conductive circuit boards are used double-sided cooling may be achieved. As a result, heat dissipation may be divided between two surfaces and instead of one large heatsink for dissipating heat from one surface, which is the prior art solution, two smaller heatsinks may be used, thereby reducing the overall size of the package.

[0007] According to one aspect of the invention, at least one of the circuit boards includes external connectors for external connection to other components. Each electrical connector is a portion of a conductive track on the circuit board which also includes at least one conductive pad that is electrically connected to an electrical contact of the at least one semiconductor device.

[0008] According to another embodiment of the present invention, a semiconductor package may include a plurality of semiconductor devices which are interconnected inside the package to form one a or a plurality of circuits. For example, a package according to the present invention may include a plurality of power switching devices for forming half-bridges or converter circuits.

[0009] It has been determined, through experiments, that a semiconductor die in a package according to the present invention exhibits 26% less thermal resistance at its electrical contacts than a die in a conventional package. It has also been found that a die in a package according to the present invention operates at a lower temperature than a die in a conventional package. Experiments have shown, for example, that under identical load conditions the steady state temperatures measured at the outer surface of a circuit board in a

package according to the present invention is 75° C while the temperature at a similar position for a conventional package is 82°C.

[0010] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 shows a cross-sectional view of a semiconductor package according to the prior art;

[0012] Figure 2 shows the top plan view of a semiconductor package according to the first embodiment of the present invention;

[0013] Figure 3 shows the circuit diagram for the components disposed within a package according to the first embodiment of the present invention;

[0014] Figure 4 shows a top plan view of a circuit board used in a package according to the present invention;

[0015] Figure 5 shows a top plan view of another circuit board used in a package according to the present invention;

[0016] Figure 6 shows a top plan view of the circuit board shown by Figure 4 which includes a plurality of semiconductor switching devices;

[0017] Figure 7 shows a cross-sectional view of a package according to the present invention taken along line 7-7 in Figure 2 viewed in the direction of the arrows;

[0018] Figure 8 shows a side view of a package according to the present invention which has a heatsink mounted on one side thereof;

[0019] Figures 9A-9B illustrate the processing steps taken for the manufacture of a package according to the present invention;

[0020] Figure 10 shows a top plan view of a package according to the second embodiment of the present invention;

[0021] Figure 11 shows a top plan view of a package according to the third embodiment of the present invention;

[0022] Figure 12 shows a package according to the third embodiment of the present invention as integrated with a circuit board;

[0023] Figure 13 shows a top plan view of a circuit board adapted for integration with a package according to the first embodiment of the present invention;

[0024] Figure 14 shows a side view of a circuit board as integrated with a package according to the first embodiment of the present invention;

[0025] Figure 15 shows a side view of a motor integrated with a circuit board that includes an integral package according to the present invention;

[0026] Figure 16 shows a circuit diagram for a three-phase buck converter; and

[0027] Figure 17 illustrates a package according to the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE FIGURES

[0028] Referring to Figure 2, semiconductor package 10 according to the first embodiment of the present invention includes first circuit board 12, and second circuit board 14 which is assembled over first circuit board 12. According to an aspect of the present invention, circuit boards 12, 14 are of the thermally conductive variety such as insulated metal substrate (IMS), or double-bonded copper (DBC). Such circuit boards include a thermally conductive, but electrically insulating body which can have conductive patterns formed over at least one of its surfaces. In the first embodiment of the present invention, first circuit board 12 includes a plurality of external connectors 16 which serve as input and output connectors to the elements disposed between first circuit board 12 and second circuit board 14 as will be described later.

[0029] Referring next to Figure 3, semiconductor package 10 according to the first embodiment of the present invention includes a plurality of power MOSFETs T_1, T_2, T_3, T_4, T_5, T_6 which are interconnected to form three parallel-

connected half-bridge circuits, each for driving a respective phase of a three-phase motor.

[0030] As is well known in the art, each half-bridge circuit includes a high side MOSFET, T_3, T_2, T_1 and a low side MOSFET T_4, T_5, T_6. When power MOSFETs are used to form half-bridge circuits, the source contact of the high side MOSFET, e.g. T_1, is series connected to the drain contact of the low side MOSFET e.g. T_6, while the drain contact of the high side MOSFET is connected to the input power V_+ and the source contact of the low side MOSFET is connected to the ground G. Referring to Figure 3, in the first embodiment of the present invention MOSFET T_3, forms a half-bridge with MOSFET T_4, MOSFET T_2 forms a half-bridge with MOSFET T_5, and MOSFET T_1 forms a half-bridge with MOSFET T_6. As is well known the output of each half-bridge circuit A, B, C is taken from the connection point of its high side MOSFET to its respective low side MOSFET as shown by Figure 3. To operate each MOSFET T_1, T_2, T_3, T_4, T_5, T_6, a gate signal is sent by a control circuit (not shown) through a respective gate connection G_1, G_2, G_3, G_4, G_5, G_6. It should be understood that the present invention is not restricted to the circuit shown by Figure 3, and that other circuits formed with other devices may be packaged according to the principles of the present invention.

[0031] According to an aspect of the present invention a circuit, such as the one shown by Figure 3, is implemented without the use of wirebonds or the like. Specifically, referring now to Figure 4, first circuit board 12 includes a plurality of source conductive pads 18_{T1}, 18_{T2}, 18_{T3} for receiving source contacts of high side MOSFETS T_1, T_2, T_3, respectively, and drain conductive pads 20_{T6}, 20_{T5}, 20_{T4} for receiving the drain contacts of low side MOSFETs T_6, T_5, T_4, respectively. Each conductive pad is an area on a conductive track which has been exposed through an opening in a solder passivation layer formed on the conductive track. The conductive track is itself disposed on the thermally conductive body of a circuit board 12, 14. Specifically, each conductive track is a layer of conductive material, such as copper or aluminum, which is patterned to

a desired configuration. Conductive tracks are covered with solder passivation material, and openings are formed in the solder passivation material to expose portions of the conductive tracks to serve as conductive pads.

[0032] Source conductive pad 18_{T1} is connected electrically through a conductive trace 22 on circuit board 12 to conductive pad 20_{T6}, and then connected to external connector 16_A through another conductive trace 22 on circuit board 12. Each conductive trace 22 is essentially a portion of the conductive track which electrically connects conductive pads together or to an external connection. Specifically, for example, as will be shown, source conductive pad 18_{T1}, drain conductive pad 20_{T2}, and traces 22, and external connector 16_A form a conductive track that provides an output connection for the half-bridge circuit that is formed by MOSFETs T_1 and T_6.

[0033] Now continuing with the description of the first embodiment, conductive pads 18_{T2}, and 18_{T3} are similarly connected to conductive pads 20_{T5} and 20_{T4} and then to external connectors 16_B and 16_C in a similar manner. As a result, source contacts of high side MOSFETs T_1, T_2, T_3 are electrically connected to drain contacts of respective low side MOSFETs T_6, T_5, T_4 and then connected to external connectors 16_A, 16_B, 16_C, which serve as output connections for each half-bridge circuit without using any wirebonds.

[0034] First circuit board 12 also includes gate conductive pads 24_{T1}, 24_{T2}, 24_{T3} each for receiving a respective gate contact of high side MOSFETs T_1, T_2, T_3. Gate conductive pad 24_{T1} is connected via a trace 22 to external connector 16_{G1}, which serves as the gate connection for receiving a gate signal for high side MOSFET T_1. Similarly, gate pads 24_{T2} and 24_{T3} are connected to output connectors 16_{G2} and 16_{G3} respectively via traces 22. Connectors 16_{G2}, 16_{G3} serve as gate connections for high side MOSFETs T_2, T_3.

[0035] Referring now to Figure 5, second circuit board 14 includes drain conductive pads 20_{T1}, 20_{T2}, 20_{T3} for receiving drain contacts of high side MOSFETs T_1, T_2, T_3. Second circuit board 14 also includes interconnect conductive pads 28_{V+} and $28_{Vground}$. Drain conductive pads 20_{T1}, 20_{T2}, 20_{T3} are

formed on the same conductive trace as interconnect conductive pads 28_{V+}. Interconnect pads 28_{V+} are electrically connectable to interconnect pad 29_{V+} on first circuit board 12, which is electrically connected to external connector 16_{V+} via a trace 22. As a result drain contacts of high side MOSFET T_1, T_2, T_3 will be connected electrically to external connector 16_{V+}. External connector 16_{V+} in the first embodiment of the present invention serves as the connection to the input power V_+, when second circuit board 14 is disposed over first circuit board 12.

[0036] Second circuit board 14 also includes gate conductive pads 24_{T4}, 24_{T5}, 24_{T6} for receiving gate contacts of low side MOSFETs T_4, T_5, T_6. Each gate conductive pad 24_{T4}, 24_{T5}, 24_{T6} is electrically connected to gate interconnect pads 28_{G4}, 28_{G5}, 28_{G6} via a respective trace 22. Each gate interconnect pad 28_{G4}, 28_{G5}, 28_{G6} is then connected to a corresponding gate interconnect pad 29_{G4}, 29_{G5}, 29_{G6} on first circuit board 12, and thereby electrically connected via a respective trace 22 to a corresponding gate connector 16_{G4}, 16_{G5}, 16_{G6}.

[0037] Also disposed on second circuit board 14 are source conductive pads 18_{T4}, 18_{T5}, 18_{T6}, and ground interconnect pads 28_{ground}. Source conductive pads 18_{T4}, 18_{T5}, 18_{T6} and ground interconnect pads 28_{ground} are formed on a common conductive track and, therefore, are electrically connected together. Ground interconnect pads 28_{ground} on second circuit board 14 are connected to corresponding ground interconnect pads 29_{ground} on first circuit board 12, which are in turn connected via a common trace 32 to external ground connector 16_{ground}. As a result, source contacts of low side MOSFETs T_4, T_5, T_6 are connectable to a ground connection via external connector 16_{ground}.

[0038] Referring now to Figures 6 and 7, source contact, e.g. ST_1, of each high side MOSFET T_1, T_2, T_3 is electrically connected to a corresponding source conductive pad 18_{T1}, 18_{T2}, 18_{T3}, and each gate contact, e.g. GT_1, of each high side MOSFET T_1, T_2, T_3 is electrically connected to a corresponding gate conductive pad 24_{T1}, 24_{T2}, 24_{T3}. Also, each drain contact, e.g. DT_6, of each low side MOSFET T_4, T_5, T_6 is electrically connected to its corresponding drain conductive pad, e.g. 20_{T6}, on first circuit board 12. Electrical connection in each

case is made by a layer of conductive adhesive 33 such as solder or conductive epoxy. It should be noted that source contact and the gate contact of each MOSFET are exposed through a solder passivation 19 (shown by crossing lines in Figure 6) layer which prevents the solder (or any other conductive adhesive) from shorting the gate contact to the source contact.

[0039] Referring now specifically to Figure 7, second circuit board 14 is assembled opposite first circuit board 12 such that drain contact, e.g. DT_1 of each high side MOSFET T_1, T_2, T_3 is electrically connected via a layer of conductive adhesive 33 to its corresponding drain conductive pad, e.g. 20_{T1}, on second circuit board 14. Similarly, source contact, e.g. ST_6, of each low side MOSFET T_4, T_5, T_6 is electrically connected via a layer of conductive adhesive 33 to its corresponding source conductive pad, e.g. $18T_6$ on second circuit board 14, and gate contact, e.g. GT_6, of each low side MOSFET, T_4, T_5, T_6, is electrically connected to its corresponding gate conductive pad, e.g. 24_{T6}, via a layer of conductive adhesive 33.

[0040] Also shown in Figure 7, is interconnect 35 which electrically connects ground conductive pad 29_{ground} on first circuit board 12 to ground conductive pad 28_{ground} on second circuit board 14. Interconnect 35 is connected to each conductive pad via a layer of conductive adhesive 33. Interconnect 35 may be any conductive body such as a copper slug.

[0041] Figure 7 shows that low side MOSFET T_6, high side MOSFET T_1 and interconnect 35 are connected between first circuit board 12 and second circuit board 14. The remaining high side MOSFETs T_2, T_3 and low side MOSFETs T_4, T_5 are connected in the same manner as that of high side MOSFET T_1 and low side MOSFET T_6. Furthermore, interconnects are used to connect internal gate conductive pads 28_{G4}, 28_{G5}, 28_{G6} to internal conductive pads 29_{G4}, 29_{G5}, 29_{G6}, and internal conductive pads 28_{V+} to conductive pads 29_{V+} in the same manner as described for interconnect 35 above.

[0042] Referring now to Figure 8, once second circuit board 14 is assembled over first circuit board 12, an epoxy underfilling 37 is provided in the spaces

between first circuit board 12 and second circuit board 14. The purpose of epoxy underfilling 37 is to protect MOSFETs from environmental conditions such as moisture. As shown by Figure 8, a heatsink 40 may be thermally coupled to second circuit board 14 to assist in heat dissipation. Heatsink 40 may also be coupled to first circuit board 12 without deviating from the present invention

[0043] According to an aspect of the present invention, each circuit board 12, 14 may receive a heatsink to effect double-sided cooling. Advantageously, because of double-sided cooling, smaller heatsinks can be used (instead of one large heatsink) thereby reducing the overall size of the package.

[0044] Referring now to Figures 9A-9D, semiconductor package 10 according to the present invention is manufactured according to the following process. First, solder paste (shown by slanted lines) or some other conductive adhesive is printed on the conductive pads on first circuit board 12. Next, as illustrated by Figure 9B, high side MOSFETs T_1, T_2, T_3 and low side MOSFETs T_4, T_5, T_6 are placed on their respective positions on first circuit board 12. Thereafter, as illustrated by Figure 9C, solder paste (shown by slanted lines) or some other conductive adhesive is printed on the conductive pads on second circuit board 14, and, as shown by Figure 9D, second circuit board 14 is placed over first circuit and then the entire structure is heated to cause the solder paste to be reflown. Thereafter, epoxy is disposed to fill the space between first circuit board 12 and second circuit board 14.

[0045] According to the preferred embodiment of the present invention, a plurality of first circuit boards 12 may be linked together to form a large panel and MOSFETs T_1, T_2, T_3, T_4, T_5, T_6 and second circuit boards 14 may be placed by a pick-and-place machine. Then, first circuit boards 12 are cut from the large panel to form individual packages after epoxy underfilling has been applied.

[0046] Referring now to Figure 10, a package according to a second embodiment of the present invention may include external connectors on more than one side.

[0047] Referring to Figure 11, a package according to the third embodiment of the present invention may include plug-type external connectors 39, which are adapted to be received in corresponding sockets, for example, in another circuit board. An example of such arrangement is shown by Figure 12, in which a package according to the third embodiment of the present invention is shown assembled onto circuit board 42 having sockets (not shown) for receiving external conductors 39.

[0048] Referring now to Figure 13, a package according to the first embodiment of the present invention may be integrated with another circuit board by having external connectors 16 electrically connected to corresponding lands. Specifically, Figure 13 shows circuit board 44 having a plurality of conductive lands 45 for receiving external connectors 16 of a package according to the first embodiment of the present invention. Figure 14 illustrates the assembly of package 10 according to the present invention onto circuit board 44. Circuit board 44 may include other components 47, which may be operatively connected to the components within package 10. Components 47, may be, for example, circuit elements for controlling the MOSFETs in package 10.

[0049] Referring to Figure 15, according to an aspect of the present invention, a circuit board including a package according to the present invention may be adapted for mounting, and mounted to the body of a device, thereby forming, for example, a device having an integral control mechanism. Specifically, for example, circuit board 44 containing package 10, which includes three-half bridge circuits, may include a control circuitry for driving each half-bridge circuit, and mounted on the body of a three-phase motor 50. Each phase of motor 50 may then be operatively connected to the output connectors of package 10, thereby forming a motor package with an integral drive circuitry.

[0050] A package according to the present invention is not restricted to half-bridge circuits. Referring for example to Figures 16 and 17, a package according to the fourth embodiment of the present invention may be configured to include the power components for a three-phase synchronous buck converter as shown by

Figure 16. As is well known, a synchronous buck converter includes two series connected power switching elements, such as power MOSFETs, one of which is referred to as a control MOSFET 50, and the other as a synchronous MOSFET 52. Also, as is well known, a schottky diode 54 is connected between the source and the drain of the synchronous MOSFET 52. A three-phase synchronous buck converter is essentially three synchronous buck converters connected together.

[0051] Referring specifically to Figure 17, a package according to the fourth embodiment includes first circuit board 12, second circuit board 14, control MOSFETs 50, synchronous MOSFETs 52, and schottky diodes 54. According to the present invention, circuit boards 12, 14 include conductive pads 51 formed on selected areas of conductive tracks 30 on each circuit board for electrical connections to, for example, electrical contacts of MOSFETs 50, 52, and schottky diodes 54, as well as conductive pads for receiving interconnects 56 for internal connection of the elements within the package. Similar to the first embodiment, a package according to the fourth embodiment may be manufactured by first placing the power components on first circuit board 12 as described earlier, printing solder paste (or some other conductive adhesive) on conductive pads of second circuit board 14, placing second circuit board 14 over first circuit board 12 and then reflowing the solder paste. Thereafter, the space between circuit boards 12, 14 may be filled with epoxy 37.

[0052] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a first circuit board including at least one conductive pad disposed on a major surface thereof;

a second circuit board including at least one conductive pad on a major surface thereof; and

a semiconductor die including a first electrical contact on a first major surface thereof and a second electrical contact on a second major surface thereof;

wherein said semiconductor die is disposed between said at least one conductive pad on said first circuit board and said at least one conductive pad on said second circuit board, and said first electrical contact is electrically connected to said at least one conductive pad on said first circuit board and said second electrical contact is electrically connected to said at least one conductive pad on said second circuit board.

2. A semiconductor package according to claim 1, further comprising terminals electrically connected to said first electrical contact and said second electrical contact of said semiconductor die, said terminals being disposed on at least one of said substrates.

3. A semiconductor package according to claim 1, wherein each of said circuit board is an insulated metal substrate.

4. A semiconductor package according to claim 1, wherein said semiconductor die is a switching power semiconductor device which includes a control terminal, said control terminal being disposed on one of said first major surface of said die and said second major surface of said die and electrically connected to a conductive pad on one of said circuit boards, and electrically connected to a terminal disposed on one of said circuit boards.

5. A semiconductor package according to claim 1, wherein said semiconductor die is one of a MOSFET and an IGBT.

6. A semiconductor package according to claim 1, wherein said first electrical contact and said second electrical contact of said semiconductor die are connected to respective conductive pads via respective layers of a conductive adhesive.

7. A semiconductor package according to claim 6, wherein said conductive adhesive is one of solder and conductive epoxy.

8. A semiconductor package according to claim 1, further comprising an epoxy underfilling disposed between said circuit boards.

9. A semiconductor package according to claim 1, further comprising a heatsink disposed on one of said circuit boards.

10. A semiconductor package according to claim 1, further comprising at least one heatsink disposed on each of said circuit boards.

11. A semiconductor package comprising:

a first thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a second thermally conductive substrate including a plurality of conductive pads disposed on a first major surface thereof;

a plurality of power semiconductor devices each including a first power contact on a first major surface thereof, a second power contact and a control contact on a second opposing major surface thereof;

wherein said plurality of power semiconductor devices are disposed between said first major surface of said first thermally conductive substrate and said first major surface of said second thermally conductive substrate, wherein each one of said contacts of said power semiconductor devices is electrically connected to a respective one of said plurality of conductive pads, and wherein said conductive pads on said thermally conductive substrate are interconnected to form part of a circuit.

12. A semiconductor package according to claim 11, further comprising output terminals connected to said power semiconductor devices through said conductive pads and disposed on at least one of said substrates.

13. A semiconductor package according to claim 11, wherein said thermally conductive substrate are insulated metal substrates.

14. A semiconductor package according to claim 11, wherein said power semiconductor devices are one of power MOSFETs and IGBTs.

15. A semiconductor package according to claim 11, wherein said power semiconductor devices are connected to said conductive pads via a conductive adhesive layer.

16. A semiconductor package according to claim 15, wherein said conductive adhesive is one of solder and conductive epoxy.

17. A semiconductor package according to claim 11, wherein said power semiconductor devices are connected in a half-bridge configuration.

18. A semiconductor package according to claim 11, wherein said power semiconductor device are connected to form a plurality of half-bridge configurations.

19. A semiconductor package according to claim 11, further comprising a control device for controlling the operation of said power semiconductor devices.

20. A semiconductor package according to claim 11, further comprising epoxy filling spaces between said first and second thermally conductive substrates.

21. A semiconductor package according to claim 11, further comprising at least one heatsink in thermal contact with one of said thermally conductive substrates.

22. A semiconductor package according to claim 11, further comprising a heatsink in thermal contact with each one of said conductive substrates.

23. A method for manufacturing a semiconductor package comprising:

providing a first circuit board having at least one conductive pad disposed on a first major surface thereof;

printing a paste of a conductive adhesive on said conductive pad;

placing a semiconductor device on said conductive adhesive;

providing a second circuit board having at least one conductive pad disposed on a first major surface thereof;

printing a paste of a conductive adhesive on said conductive pad on said second circuit board;

placing said second circuit board over said semiconductor device such that said conductive adhesive on said second circuit board is in contact with said semiconductor device; and

applying heat to reflow said conductive adhesive.

24. A method according to claim 23, wherein said conductive adhesive is one of solder and conductive epoxy.

25. A method according to claim 23, further comprising filling spaces between said circuit boards with epoxy.

26. A method according to claim 23, wherein said circuit boards are insulated metal substrates.

27. A method according to claim 23, wherein each placing step is carried out by a pick-and-place method.

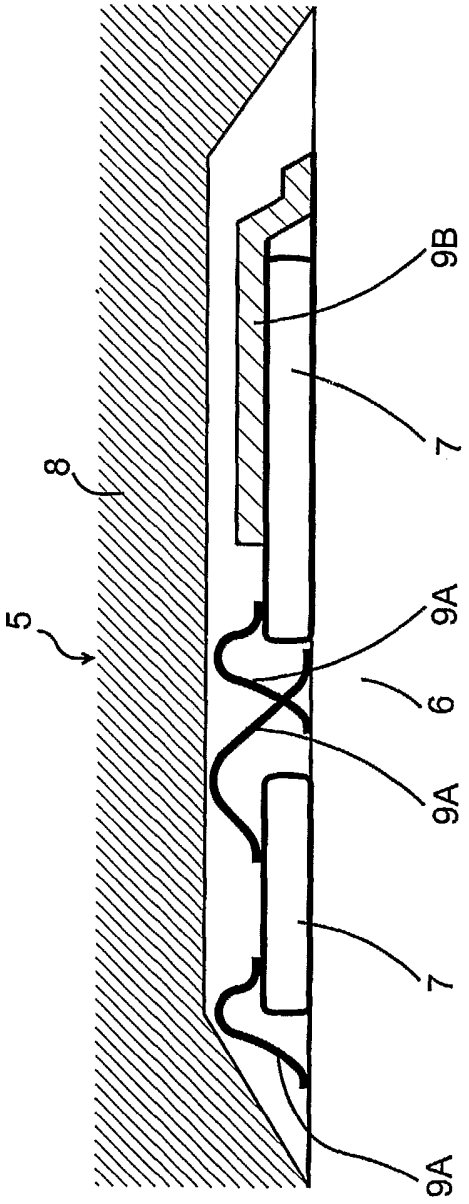


Figure 1
(Prior Art)

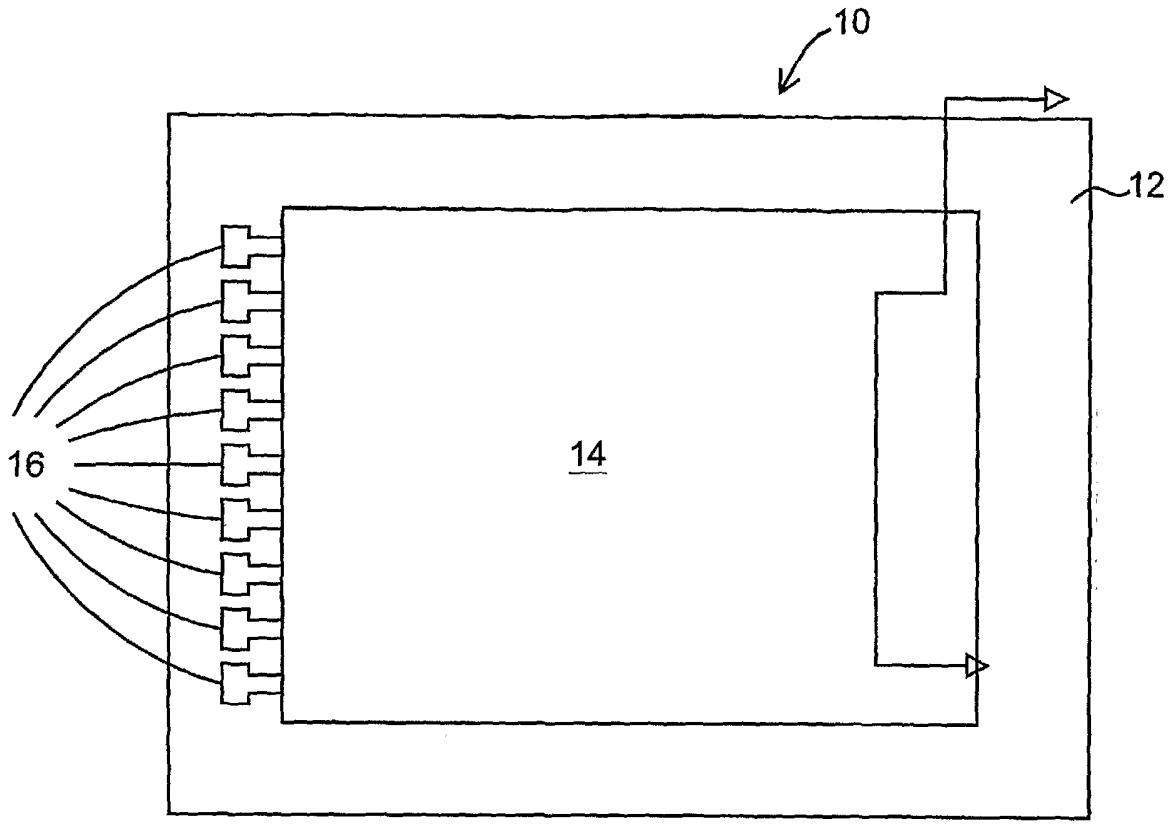


Figure 2

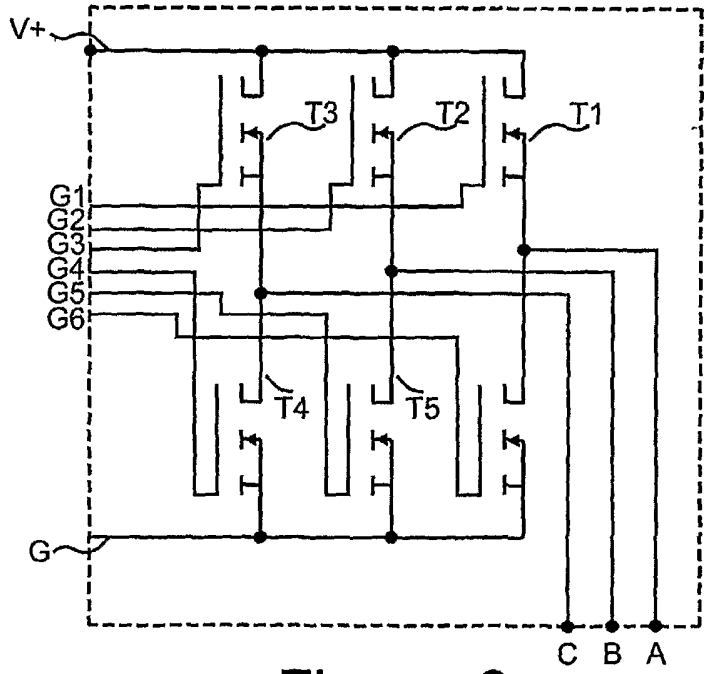


Figure 3

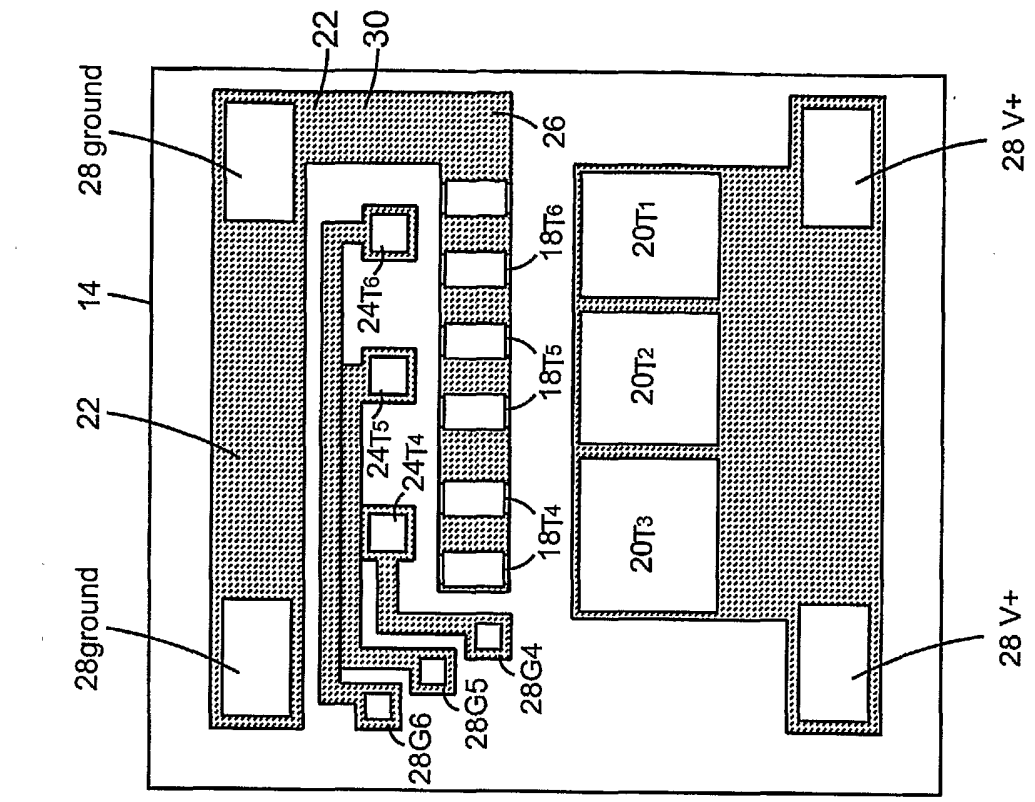


Figure 5

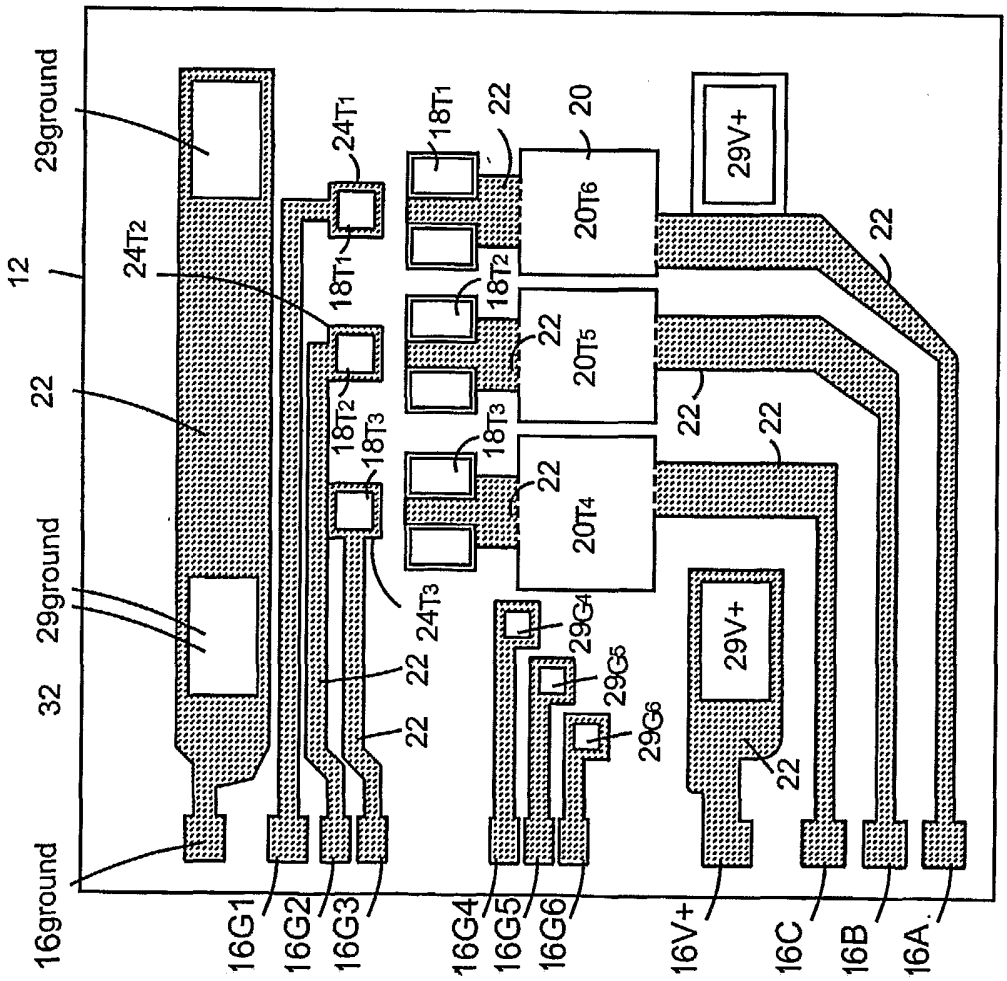


Figure 4

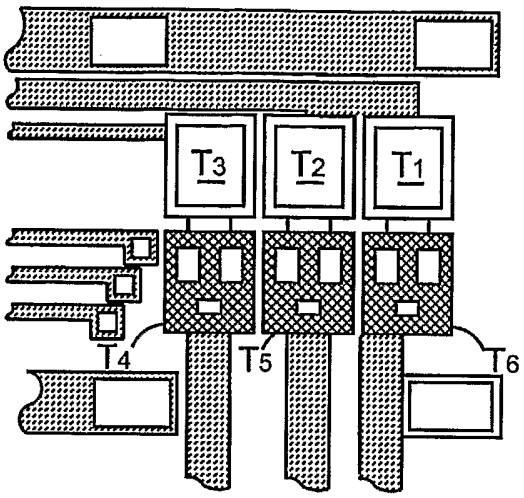


Figure 6

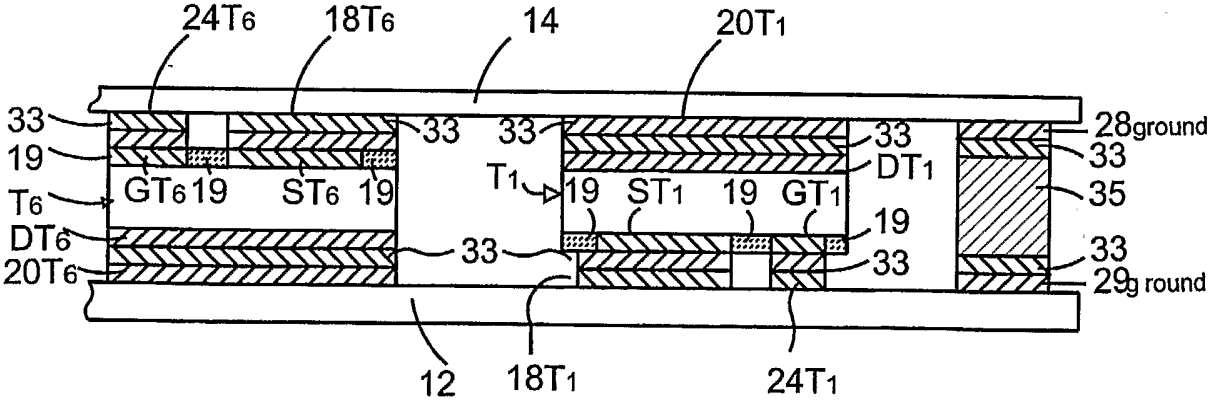


Figure 7

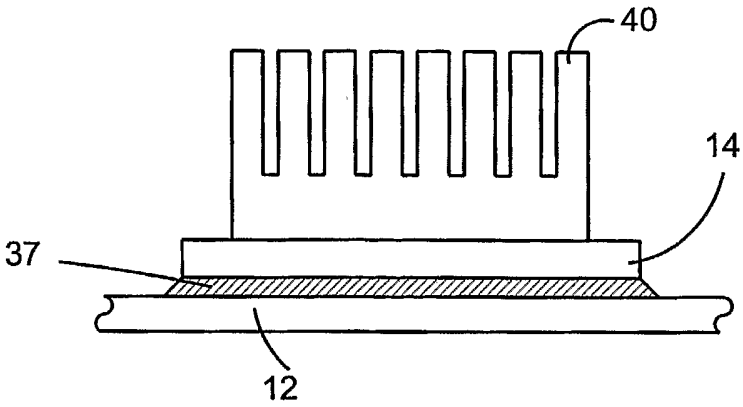


Figure 8

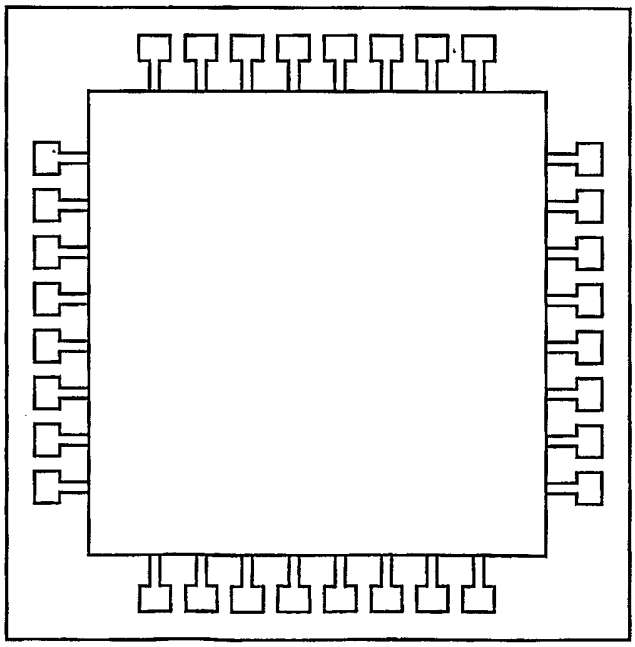


Figure 10

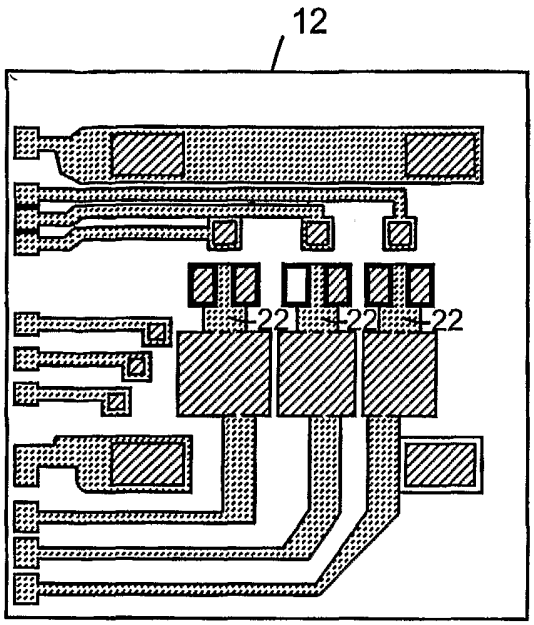


Figure 9A

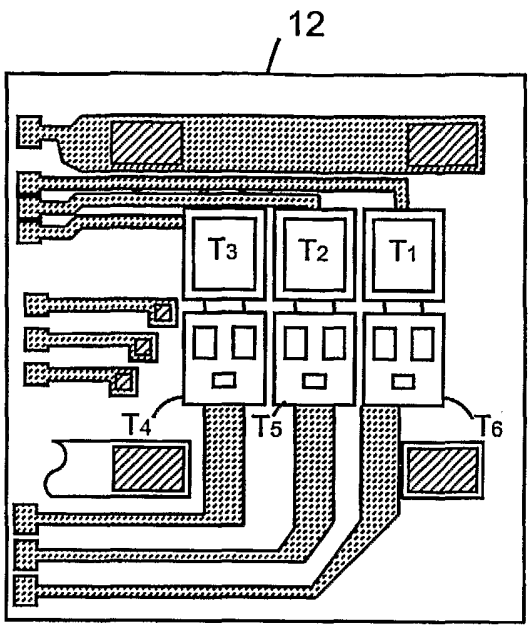


Figure 9B

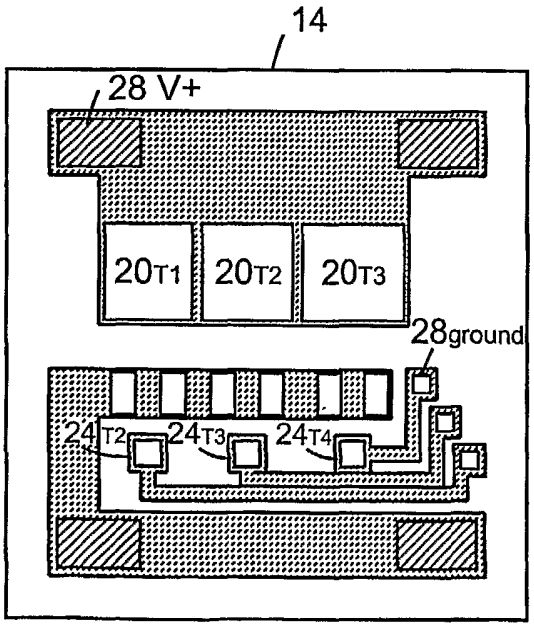


Figure 9C

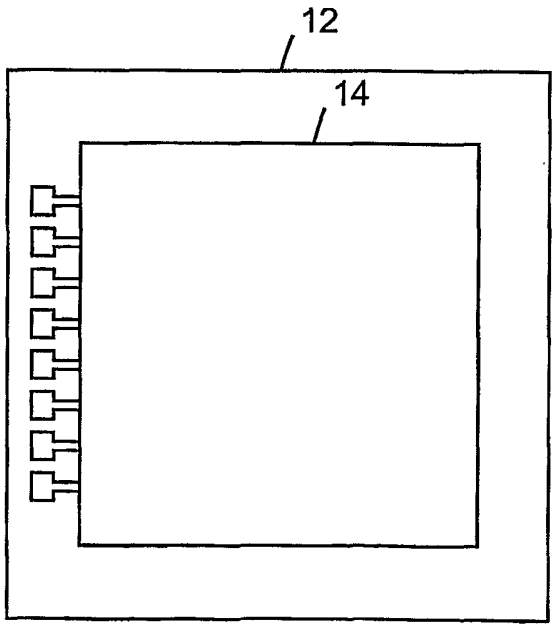


Figure 9D

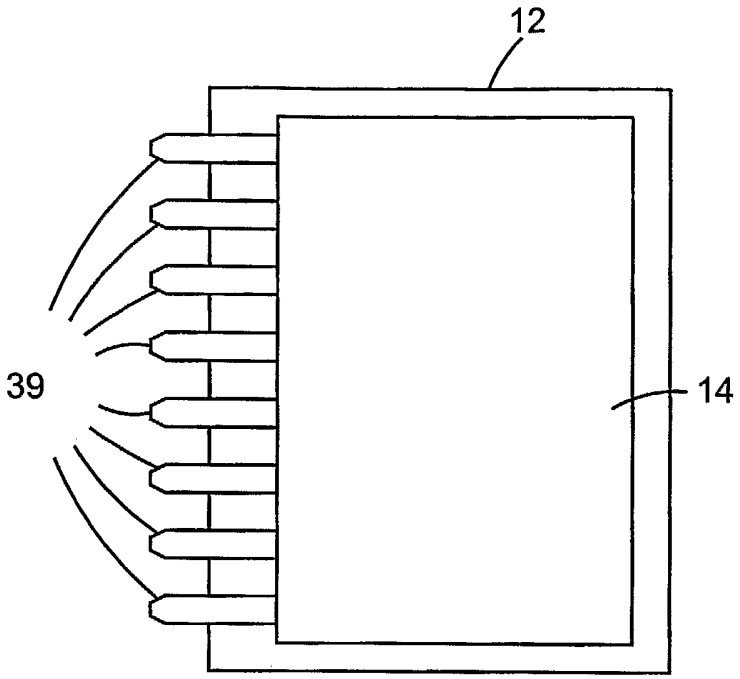


Figure 11

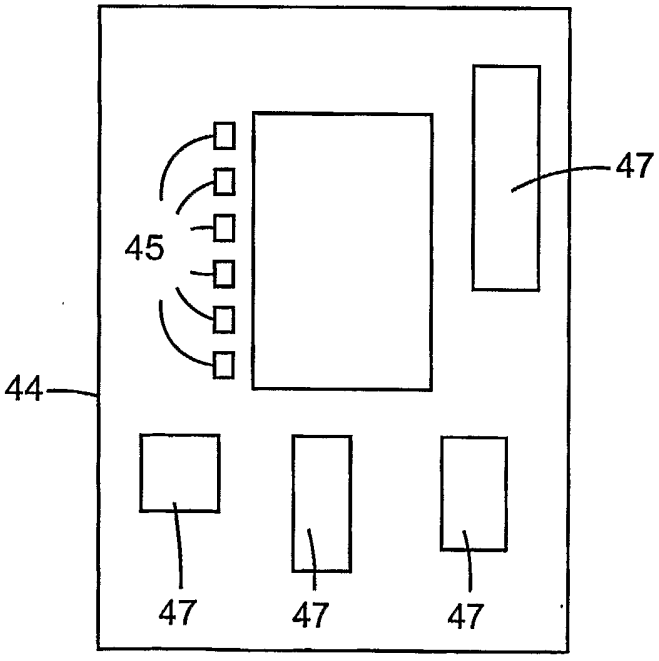


Figure 13

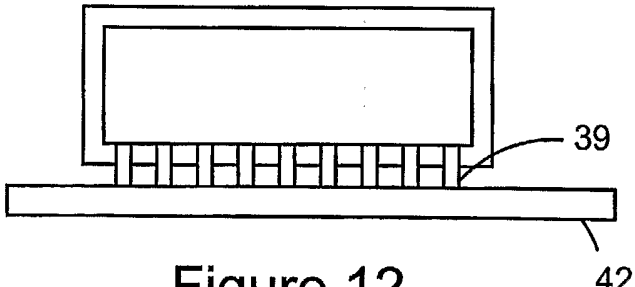


Figure 12

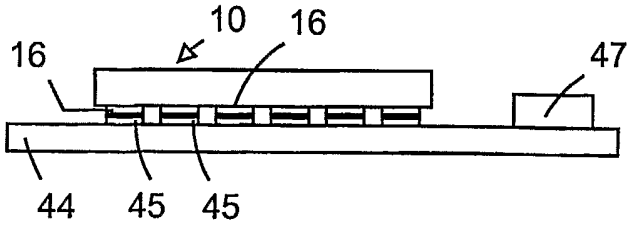


Figure 14

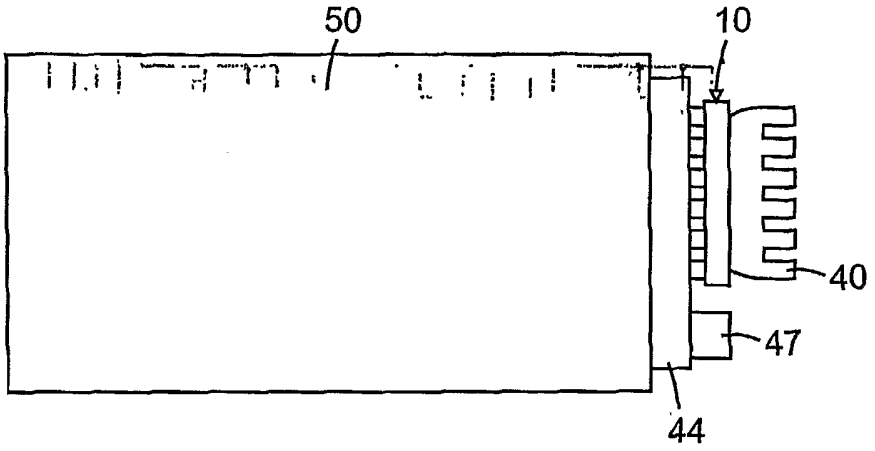


Figure 15

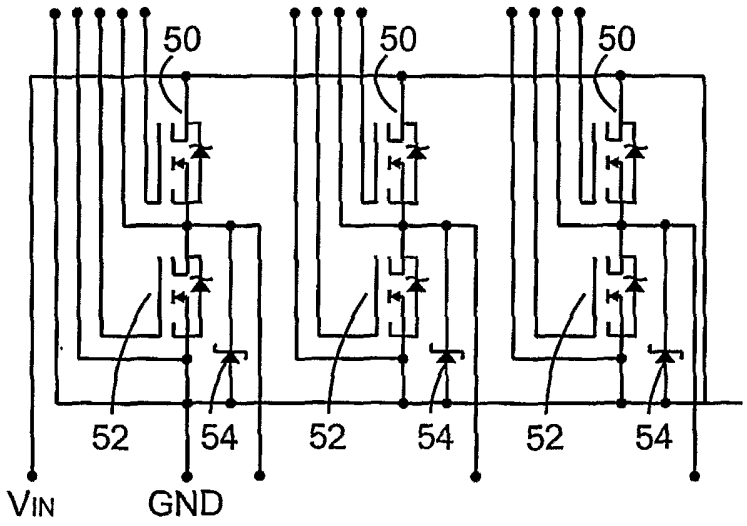


Figure 16

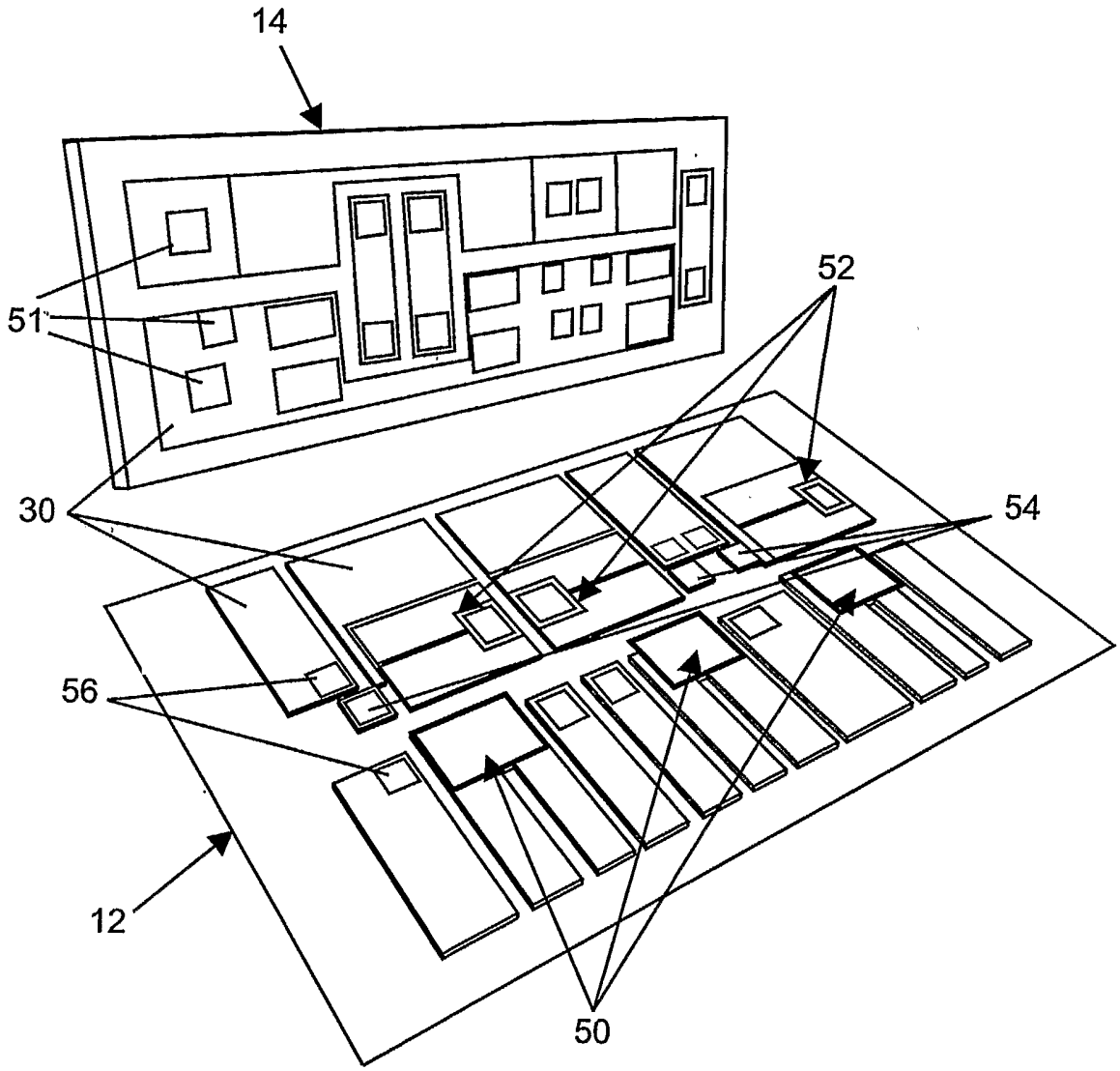


Figure 17