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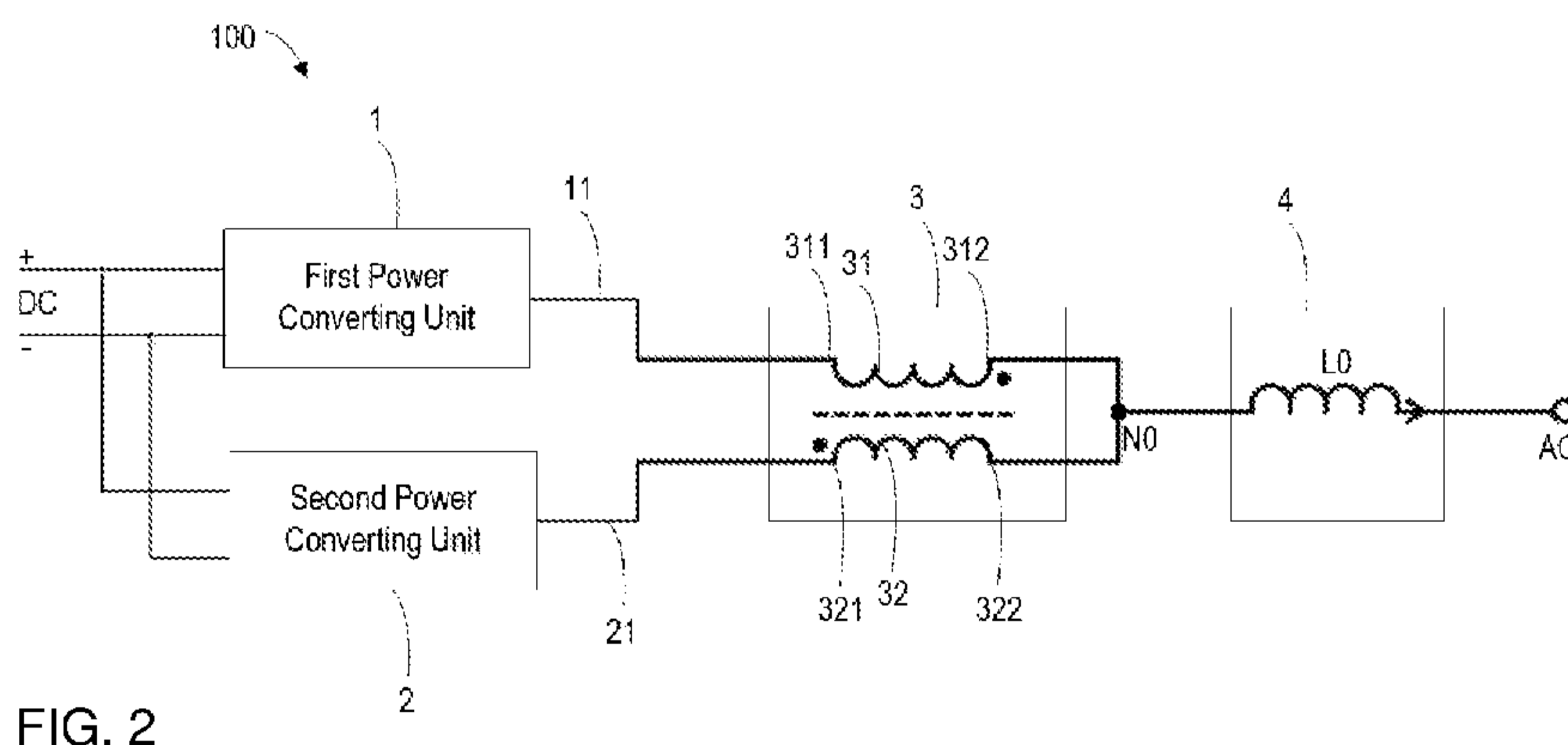
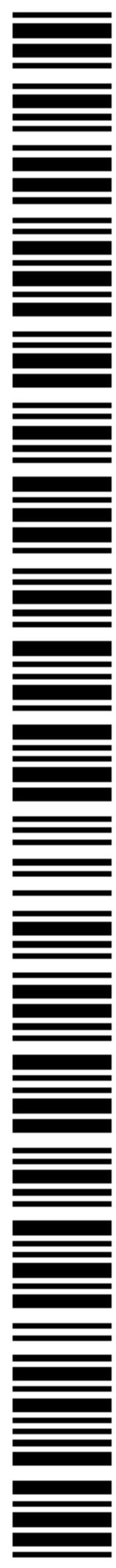


FIG. 2

(57) Abstract: A multi-level power convertor and a method for a multi-level power convertor. The multi-level power convertor (100) comprises a DC port; an AC port; a first power converting unit (1) coupled to the DC port and comprising a first AC terminal (11) adapted to provide a first plurality of voltage levels; a second power converting unit (2) coupled to the DC port and comprising a second AC terminal (21) adapted to provide a second plurality of voltage levels of the same number as the first plurality of voltage levels, wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels; a coupling inductor (3) comprising first and second windings (31, 32) with the same number of turns, wherein the first winding (31) comprises a first end (311) coupled to the first AC terminal (11) and a second end (312), the second winding (32) comprises a third end (321) coupled to the second AC terminal (21) and a fourth end (322), and the second end (312) of the first winding (31) and the third end (321) of the second winding (32) are namesake ends of the first and second windings (31, 32); and an inductive filtering unit (4) arranged between the AC port and the second and fourth ends (312, 322) of the first and second windings (31, 32).



MULTI-LEVEL POWER CONVERTOR AND METHOD FOR MULTI-LEVEL POWER CONVERTOR

5 FIELD

[0001] Embodiments of present disclosure generally relate to the field of power convertors, and more particularly, to a multi-level power convertor and a method for a multi-level power convertor.

10 BACKGROUND

[0002] Currently, multi-level power converters are widely used in various fields, which can effectively decrease the switching frequency and improve the output waveform quality.

[0003] Fig. 1 illustrates a schematic circuit diagram of a conventional multi-level power convertor 100. As shown in Fig. 1, the multi-level power convertor 100 includes a DC port and an AC port. The DC port includes DC terminals DC+ and DC-. Capacitors C1 and C2 are connected in series between the DC terminals DC+ and DC-. Switching semiconductor devices S1, S2, S3, and S4 are connected in series between the DC terminals DC+ and DC-. The switching semiconductor devices S1, S2, S3, and S4 are line frequency switches. A node N1 between the capacitors C1 and C2 is connected to a node N2 between the switching semiconductor devices S2 and S3. A first branch including switching semiconductor devices S5, S6, S17, and S18 is connected in series between a node N3 and an inductor L. A second branch including switching semiconductor devices S7, S8, S19, and S20 are connected in series between a node N4 and the inductor L. The switching semiconductor devices S5, S6, S17, S18, S7, S8, S19, and S20 are high frequency switches. Capacitors C3, C5, and C7 are connected between the first and second branches respectively. The switching semiconductor devices S1, S2, S3, S4, S5, S6, S17, S18, S7, S8, S19, and S20 may be switched on and off under control of respective driving signals. With the above arrangement, the multi-level power convertor 100 may output nine voltage levels at the AC port.

[0004] When the multi-level power convertor 100 operates, the capacitors C3, C5, and C7 may be connected in series via respective ones of the switching semiconductor devices S5, S6, S17, S18, S7, S8, S19, and S20. In a steady state of the multi-level power convertor 100, the voltages across the capacitors C3, C5, and C7 are stable. However, in
5 a dynamic state of the multi-level power convertor 100, the voltages across the capacitors C3, C5, and C7 may be out of control. For example, the voltage of the capacitor C3, C5, or C7 may become relatively high. In this event, the corresponding switching semiconductor devices S5, S6, S17, S18, S7, S8, S19, or S20 may be susceptible to be damaged. Hence, the performance and reliability of the multi-level power convertor 100
10 would be adversely affected.

[0005] Thus, there is need for a solution for improving the performance and reliability of the multi-level power convertor.

SUMMARY

15 [0006] In view of the foregoing problems, various example embodiments of the present disclosure provide a multi-level power convertor and a method for a multi-level power convertor so as to improve the performance and reliability of the multi-level power convertor.

[0007] In a first aspect of the present disclosure, example embodiments of the present
20 disclosure provide a multi-level power convertor. The multi-level power convertor comprises a DC port; an AC port; a first power converting unit coupled to the DC port and comprising a first AC terminal adapted to provide a first plurality of voltage levels; a second power converting unit coupled to the DC port and comprising a second AC terminal adapted to provide a second plurality of voltage levels of the same number as the
25 first plurality of voltage levels, wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels; a coupling inductor comprising first and second windings with the same number of turns, wherein the first winding comprises a first end coupled to the first AC terminal and a second end, the second winding comprises a third end coupled to the second AC terminal and a fourth
30 end, and the second end of the first winding and the third end of the second winding are

namesake ends of the first and second windings; and an inductive filtering unit arranged between the AC port and the second and fourth ends of the first and second windings.

[0008] In some embodiments, the second and fourth ends of the first and second windings are coupled to a common node, and the inductive filtering unit comprises an inductor arranged between the common node and the AC port.

[0009] In some embodiments, the inductive filtering unit comprises: a first inductor arranged between the second end of the first winding and the AC port; and a second inductor arranged between the fourth end of second winding and the AC port.

[0010] In some embodiments, the inductive filtering unit comprises an additional coupling inductor comprising third and fourth windings, the third winding is arranged between the second end of the first winding and the AC port, the fourth winding is arranged between the fourth end of second winding and the AC port, and namesake ends of the third and fourth windings are connected to the AC port.

[0011] In some embodiments, each of the first and second AC terminals provides five voltage levels, and the AC port provides nine voltage levels.

[0012] In some embodiments, the DC port comprises first and second DC terminals, and the first power converting unit comprises: first and second capacitors connected in series between the first and second DC terminals; first, second, third, and fourth switching semiconductor devices connected in series between the first and second DC terminals, wherein a first node between the first and second capacitors is connected to a second node between the second and third switching semiconductor devices; fifth and sixth switching semiconductor devices connected in series between a third node and the first AC terminal, the third node being between the first and second switching semiconductor devices; seventh and eighth switching semiconductor devices connected in series between a fourth node and the first AC terminal, the fourth node being between the third and fourth switching semiconductor devices; and a third capacitor connected between a fifth node and a sixth node, the fifth node being between the fifth and sixth switching semiconductor devices, and the sixth node being between the seventh and eighth switching semiconductor devices.

[0013] In some embodiments, the second power converting unit comprises: the first and second capacitors shared with the first power converting unit; the first, second, third, and fourth switching semiconductor devices shared with the first power converting unit; ninth and tenth switching semiconductor devices connected in series between the third node and the second AC terminal; eleventh and twelfth switching semiconductor devices connected in series between the fourth node and the second AC terminal; and a fourth capacitor connected between a seventh node and a eighth node, the seventh node being between the ninth and tenth switching semiconductor devices, and the eighth node being between the eleventh and twelfth switching semiconductor devices.

10 [0014] In some embodiments, the second power converting unit comprises: the first and second capacitors shared with the first power converting unit; thirteenth, fourteenth, fifteenth, and sixteenth switching semiconductor devices connected in series between the first and second DC terminals, wherein a ninth node between the fourteenth and fifteenth switching semiconductor devices is connected to the first node; ninth and tenth switching semiconductor devices connected in series between the a tenth node and the second AC terminal, the tenth node being between the thirteenth and fourteenth switching semiconductor devices; eleventh and twelfth switching semiconductor devices connected in series between an eleventh node and the second AC terminal, the eleventh node being between the fifteenth and sixteenth switching semiconductor devices; and a fourth capacitor connected between a seventh node and a eighth node, the seventh node being between the ninth and tenth switching semiconductor devices, and the eighth node being between the eleventh and twelfth switching semiconductor devices.

[0015] In some embodiments, each of the first and second AC terminals provides nine voltage levels, and the AC port provides seventeen voltage levels.

25 [0016] In some embodiments, the multi-level power convertor operates as an inverter when the DC port is used as an input and the AC port is used as an output, and the multi-level power convertor operates as a rectifier when the AC port is used as an input and the DC port is used as an output.

[0017] In a second aspect of the present disclosure, example embodiments of the present disclosure provide a method for a multi-level power convertor. The multi-level

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power convertor comprises a DC port; an AC port; a first power converting unit coupled to the DC port and comprising a first AC terminal; a second power converting unit coupled to the DC port and comprising a second AC terminal; a coupling inductor comprising first and second windings with the same number of turns, wherein the first
5 winding comprises a first end coupled to the first AC terminal and a second end, the second winding comprises a third end coupled to the second AC terminal and a fourth end, and the second end of the first winding and the third end of the second winding are namesake ends of the first and second windings; and an inductive filtering unit arranged between the AC port and the second and fourth ends of the first and second windings.

10 The method comprises providing a first plurality of voltage levels to the first end of the first winding from the first AC terminal; providing a second plurality of voltage levels of the same number as the first plurality of voltage levels to the third end of the second winding from the second AC terminal, wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels; and
15 outputting a third plurality of voltage levels via the second end of the first winding and the fourth end of the second winding, wherein the number of the third plurality of voltage levels equals to the sum of the number of the first plurality of voltage levels and the number of the second plurality of voltage levels minus one.

[0018] In some embodiments, the second and fourth ends of the first and second
20 windings are coupled to a common node, and wherein the inductive filtering unit comprises an inductor arranged between the common node and the AC port.

[0019] In some embodiments, the inductive filtering unit comprises: a first inductor arranged between the second end of the first winding and the AC port; and a second inductor arranged between the fourth end of second winding and the AC port.

25 [0020] In some embodiments, the inductive filtering unit comprises an additional coupling inductor comprising third and fourth windings, the third winding is arranged between the second end of the first winding and the AC port, the fourth winding is arranged between the fourth end of second winding and the AC port, and namesake ends of the third and fourth windings are connected to the AC port.

30 [0021] According to various embodiments of the present disclosure, the first plurality

of voltage levels and the second plurality of voltage levels may be combined by the coupling inductor into a third plurality of voltage levels; the number of the third plurality of voltage levels is larger than the number of the first plurality of voltage levels and the number of the second plurality of voltage levels respectively. In this way, the multi-level power convertor in accordance with embodiments of the present disclosure may generate the same number of voltage levels as the conventional multi-level power convertor through using less capacitor, reducing the risk of voltage imbalance among the capacitors in the multi-level power convertor and thereby avoiding the damage of the switching semiconductor devices in the multi-level power convertor. Hence, the performance and reliability of the multi-level power convertor may be improved.

DESCRIPTION OF DRAWINGS

[0022] Through the following detailed descriptions with reference to the accompanying drawings, the above and other objectives, features and advantages of the example embodiments disclosed herein will become more comprehensible. In the drawings, several example embodiments disclosed herein will be illustrated in an example and in a non-limiting manner, wherein:

[0023] Fig. 1 illustrates a schematic circuit diagram of a conventional multi-level power convertor;

[0024] Fig. 2 illustrates a block diagram of a multi-level power convertor in accordance with an embodiment of the present disclosure;

[0025] Fig. 3 illustrates an example arrangement of a coupling inductor and an inductive filtering unit in accordance with an embodiment of the present disclosure;

[0026] Fig. 4 illustrates an example arrangement of the coupling inductor and the inductive filtering unit in accordance with another embodiment of the present disclosure;

[0027] Fig. 5 illustrates an example arrangement of the coupling inductor and the inductive filtering unit in accordance with yet another embodiment of the present disclosure;

[0028] Fig. 6 illustrates a schematic circuit diagram of a multi-level power convertor

in accordance with an embodiment of the present disclosure;

[0029] Fig. 7 illustrates a schematic circuit diagram of a multi-level power convertor in accordance with another embodiment of the present disclosure;

[0030] Fig. 8 illustrates a schematic circuit diagram of a three-phase power converting
5 circuit in accordance with an embodiment of the present disclosure;

[0031] Fig. 9 illustrates a schematic circuit diagram of a multi-level power convertor in accordance with another embodiment of the present disclosure; and

[0032] Fig. 10 illustrates a schematic circuit diagram of a multi-level power convertor in accordance with yet another embodiment of the present disclosure.

10 [0033] Throughout the drawings, the same or similar reference symbols are used to indicate the same or similar elements.

DETAILED DESCRIPTION OF EMBODIEMENTS

[0034] Principles of the present disclosure will now be described with reference to
15 several example embodiments shown in the drawings. Though example embodiments of the present disclosure are illustrated in the drawings, it is to be understood that the embodiments are described only to facilitate those skilled in the art in better understanding and thereby achieving the present disclosure, rather than to limit the scope of the disclosure in any manner.

20 [0035] The term “comprises” or “includes” and its variants are to be read as open terms that mean “includes, but is not limited to.” The term “or” is to be read as “and/or” unless the context clearly indicates otherwise. The term “based on” is to be read as “based at least in part on.” The term “being operable to” is to mean a function, an action, a motion or a state can be achieved by an operation induced by a user or an external
25 mechanism. The term “one embodiment” and “an embodiment” are to be read as “at least one embodiment.” The term “another embodiment” is to be read as “at least one other embodiment.” The terms “first,” “second,” and the like may refer to different or same objects. Other definitions, explicit and implicit, may be included below. A definition of a term is consistent throughout the description unless the context clearly

indicates otherwise.

[0036] Unless specified or limited otherwise, the terms “mounted,” “connected,” “supported,” and “coupled” and variations thereof are used broadly and encompass direct and indirect mountings, connections, supports, and couplings. Furthermore, “connected” and “coupled” are not restricted to physical or mechanical connections or couplings. In the description below, like reference numerals and labels are used to describe the same, similar or corresponding parts in the figures. Other definitions, explicit and implicit, may be included below.

[0037] As discussed above, the performance and reliability of the conventional multi-level power convertor may be adversely affected due to the use of multiple capacitors. According to embodiments of the present disclosure, to improve the performance and reliability of the multi-level power convertor, the first plurality of voltage levels and the second plurality of voltage levels having a phase shift of 90 degree may be combined by the coupling inductor, such that the multi-level power convertor in accordance with embodiments of the present disclosure may generate the same number of voltage levels as the conventional multi-level power convertor through using less capacitor. The above idea may be implemented in various manners, as will be described in detail in the following paragraphs.

[0038] Hereinafter, the principles of the present disclosure will be described in detail with reference to Figs. 2-10. Referring to Fig. 2 first, Fig. 2 illustrates a block diagram of a multi-level power convertor 100 in accordance with an embodiment of the present disclosure. As shown in Fig. 2, the multi-level power convertor 100 generally includes a DC port, an AC port, a first power converting unit 1, a second power converting unit 2, a coupling inductor 3, and an inductive filtering unit 4. The multi-level power convertor 100 may be a bidirectional power convertor. The multi-level power convertor 100 may operate as an inverter when the DC port is used as an input and the AC port is used as an output. Instead, the multi-level power convertor 100 may operate as a rectifier when the AC port is used as an input and the DC port is used as an output.

[0039] The DC port includes first and second DC terminals DC+, DC-. The first power converting unit 1 and the second power converting unit 2 are coupled to the DC

port respectively. The first power converting unit 1 includes a first AC terminal 11 for providing a first plurality of voltage levels. The second power converting unit 2 includes a second AC terminal 21 for providing a second plurality of voltage levels. The number of the second plurality of voltage levels is the same as the number of the first plurality of voltage levels. The first and second power converting units 1 and 2 have the same switching cycle. In addition, the second plurality of voltage levels are phase-shifted by 90 degree, i.e., a quarter of the switching cycle of the first and second power converting units 1 and 2, with respect to the first plurality of voltage levels.

[0040] The coupling inductor 3 includes first and second windings 31, 32 with the same number of turns. The first winding 31 includes a first end 311 coupled to the first AC terminal 11 and a second end 312. The second winding 32 includes a third end 321 coupled to the second AC terminal 21 and a fourth end 322. The second end 312 of the first winding 31 and the third end 321 of the second winding 32 are namesake ends of the first and second windings 31, 32. With such an arrangement, the first and second winding 31, 32 may induce voltages of the same magnitude and opposite directions.

[0041] The first plurality of voltage levels and the second plurality of voltage levels having a phase shift of 90 degree may be combined by the coupling inductor into a third plurality of voltage levels. The number of the third plurality of voltage levels would equal to the sum of the number of the first plurality of voltage levels and the number of the second plurality of voltage levels minus one. If both the number of the first plurality of voltage levels and the second plurality of voltage levels are five, the number of the third plurality of voltage levels would be nine. If both the number of the first plurality of voltage levels and the second plurality of voltage levels are nine, the number of the third plurality of voltage levels would be seventeen.

[0042] The inductive filtering unit 4 is arranged between the AC port and the coupling inductor 3 so as to filter the third plurality of voltage levels provided by the coupling inductor 3. The coupling inductor 3 and the inductive filtering unit 4 may have various arrangements, which will be described in detail hereinafter with reference to Figs. 3-5.

[0043] In an embodiment, as shown in Fig. 3, the second and fourth ends 312, 322 of the first and second windings 31, 32 are coupled to a common node N0. The inductive

filtering unit 4 includes an inductor L0 arranged between the common node N0 and the AC port.

[0044] In another embodiment, as shown in Fig. 4, the inductive filtering unit 4 includes a first inductor L1 and a second inductor L2. The first inductor L1 is arranged
5 between the second end 312 of the first winding 31 and the AC port. The second inductor L2 is arranged between the fourth end 322 of second winding 32 and the AC port.

[0045] In yet another embodiment, as shown in Fig. 5, the inductive filtering unit 4 includes an additional coupling inductor consisting of third and fourth windings 41, 42. The third winding 41 is arranged between the second end 312 of the first winding 31 and
10 the AC port. The fourth winding 42 is arranged between the fourth end 322 of second winding 32 and the AC port. Namesake ends of the third and fourth windings 41, 42 are connected to the AC port.

[0046] Fig. 6 illustrates a schematic circuit diagram of a multi-level power convertor 100 in accordance with an embodiment of the present disclosure. As shown in Fig. 6, the
15 coupling inductor 3 and the inductive filtering unit 4 have the same construction and arrangement as those described with reference to Figs. 2 and 3. It is to be understood the coupling inductor 3 and the inductive filtering unit 4 may have other constructions and arrangements, for example those as described above with reference to Figs. 4 and 5. The scope of the present disclosure is not intended to be limited in this respect.

[0047] In an embodiment, as shown in Fig. 6, the first power converting unit 1 includes capacitors C1, C2, and C3 and switching semiconductor devices S1, S2, S3, S4, S5, S6, S7, and S8. The capacitors C1 and C2 are connected in series between the first and second DC terminals DC+, DC-. The switching semiconductor devices S1, S2, S3, and S4 are line frequency switches. The switching semiconductor devices S1, S2, S3, and S4 are connected in series between the first and second DC terminals DC+, DC-. A
25 first node N1 between the capacitors C1 and C2 is connected to a second node N2 between the switching semiconductor devices S2 and S3. The node N1 may be used as a reference voltage point of the AC port. The switching semiconductor devices S5, S6, S7, and S8 are high frequency switches and have the same switching cycle. The switching
30 semiconductor devices S5 and S6 are connected in series between a third node N3 and the

first AC terminal 11. The third node N3 is between the switching semiconductor devices S1 and S2. The switching semiconductor devices S7 and S8 are connected in series between a fourth node N4 and the first AC terminal 11. The fourth node N4 is between the switching semiconductor devices S3 and S4. The third capacitor C3 is connected
5 between a fifth node N5 and a sixth node N6. The fifth node N5 is between the switching semiconductor devices S5 and S6. The sixth node N6 is between the switching semiconductor devices S7 and S8.

[0048] The switching semiconductor devices S5 and S7 are complementary switches. That is, when the switching semiconductor device S5 is switched on, the switching
10 semiconductor device S7 is switched off, vice versa. Similarly, the switching semiconductor devices S6 and S8 are complementary switches. A driving signal of the switching semiconductor device S5 may lag a half of the switching cycle than that of the switching semiconductor device S6.

[0049] In an embodiment, as shown in Fig. 6, the second power converting unit 2
15 includes capacitors C1, C2, and C4 and switching semiconductor devices S1, S2, S3, S4, S9, S10, S11, and S12. The capacitors C1 and C2 and the switching semiconductor devices S1, S2, S3 and S4 are shared by the first power converting unit 1 and the second power converting unit 2. The switching semiconductor devices S9, S10, S11, and S12 are high frequency switches and have the same switching cycle as the switching
20 semiconductor devices S5, S6, S7, and S8. The switching semiconductor devices S9 and S10 are connected in series between the third node N3 and the second AC terminal 21. The switching semiconductor devices S11 and S12 are connected in series between the fourth node N4 and the second AC terminal 21. The fourth capacitor C4 is connected between a seventh node N7 and an eighth node N8. The seventh node N7 is between the
25 switching semiconductor devices S9 and S10. The eighth node N8 is between the switching semiconductor devices S11, S12.

[0050] The switching semiconductor devices S9 and S10 are complementary switches. Similarly, the switching semiconductor devices S11 and S12 are complementary switches. A driving signal of the switching semiconductor device S9 may lag a half of the
30 switching cycle than that of the switching semiconductor device S10. Driving signals of

the switching semiconductor devices S5, S6, S7, and S8 and driving signals of the switching semiconductor devices S9, S10, S11, and S12 have a phase difference of 90 degree, i.e., a quarter of the switching cycle of these switching semiconductor devices. Thus, there is a phase shift of 90 degree between the second plurality of voltage levels and the first plurality of voltage levels.

[0051] With the above arrangement, each of the first and second power converting units 1, 2 may provide five voltage levels at the respective AC terminals 11, 21. Accordingly, the coupling inductor 3 may provide nine voltage levels at the second end 312 of the first winding 31 and the fourth end 322 of the second winding 32. In comparison with the conventional multi-level power convertor 100 as shown in Fig. 1, the multi-level power convertor 100 as shown in Fig. 6 may provide the same number of voltage levels through using less capacitor, reducing the risk of voltage imbalance among the capacitors in the multi-level power convertor 100 and thereby avoiding the damage of the switching semiconductor devices in the multi-level power convertor 100.

[0052] Fig. 7 illustrates a schematic circuit diagram of a multi-level power convertor 100 in accordance with another embodiment of the present disclosure. The construction of the multi-level power convertor 100 as shown in Fig. 7 is similar to that of the multi-level power convertor 100 as shown in Fig. 6. The difference between the multi-level power convertors 100 as shown in Figs. 6 and 7 lies in the construction of the second power converting units 2.

[0053] As shown in Fig. 7, the second power converting unit 2 includes capacitors C1, C2, and C4 and switching semiconductor devices S13, S14, S15, S16, S9, S10, S11, and S12. The switching semiconductor devices S13, S14, S15, and S16 are line frequency switches. The switching semiconductor devices S9, S10, S11, and S12 are high frequency switches. The capacitors C1 and C2 are shared by the first power converting unit 1 and the second power converting unit 2. The switching semiconductor devices S13, S14, S15, and S16 are connected in series between the first and second DC terminals DC+, DC-. A ninth node N9 between the switching semiconductor devices S14 and S15 is connected to the first node N1. The switching semiconductor devices S9 and S10 are connected in series between a tenth node N10 and the second AC terminal 21. The tenth

node N10 is between the switching semiconductor devices S13 and S14. The switching semiconductor devices S11 and S12 are connected in series between an eleventh node N11 and the second AC terminal 21. The eleventh node N11 is between the switching semiconductor devices S15 and S16. The fourth capacitor C4 is connected between a seventh node N7 and an eighth node N8. The seventh node N7 is between the switching semiconductor devices S9 and S10. The eighth node N8 is between the switching semiconductor devices S11 and S12.

[0054] With the above arrangements, the operation of the multi-level power convertor 100 as shown in Fig. 7 is similar to that of the multi-level power convertor 100 as shown in Fig. 6.

[0055] Each of the multi-level power convertors 100 as described with reference to Figs. 2-7 is a single-phase circuit. However, in other embodiments, each of the multi-level power convertors 100 may be used to form a three-phase circuit. Fig. 8 illustrates a schematic circuit diagram of a three-phase power converting circuit 200 in accordance with an embodiment of the present disclosure. As shown in Fig. 8, the three-phase power converting circuit 200 includes three phases L11, L22, and L33. Each of the phases L11, L22, and L33 includes the multi-level power convertor 100 as described above with reference to Fig. 6. In other embodiments, each of the phases L11, L22, and L33 may include the multi-level power convertor 100 according to other embodiments.

[0056] Fig. 9 illustrates a schematic circuit diagram of a multi-level power convertor 100 in accordance with another embodiment of the present disclosure. The construction of the multi-level power convertor 100 as shown in Fig. 9 is similar to that of the multi-level power convertor 100 as shown in Fig. 6. The difference between the multi-level power convertors 100 as shown in Figs. 9 and 6 lies in the construction of the first and second power converting units 1, 2. As shown in Fig. 9, the first power converting unit 1 further includes switching semiconductor devices S17, S18, S19, and S20 and capacitors C5 and C7. Similarly, the second power converting unit 2 further includes switching semiconductor devices S21, S22, S23, and S24 and capacitors C6 and C8. With such an arrangement, each of the first and second power converting units 1, 2 may provide nine voltage levels at the respective AC terminals 11 and 12. Then, the coupling inductor 3

may output seventeen voltage levels.

[0057] Fig. 10 illustrates a schematic circuit diagram of a multi-level power convertor 100 in accordance with yet another embodiment of the present disclosure. The construction of the multi-level power convertor 100 as shown in Fig. 10 is similar to that of the multi-level power convertor 100 as shown in Fig. 7. The difference between the multi-level power convertors 100 as shown in Figs. 10 and 7 lies in the constructions of the first and second power converting units 1, 2. As shown in Fig. 10, the first power converting unit 1 further includes switching semiconductor devices S17, S18, S19, and S20 and capacitors C5 and C7. Similarly, the second power converting unit 2 further includes switching semiconductor devices S21, S22, S23, and S24 and capacitors C6 and C8. With such an arrangement, each of the first and second power converting units 1, 2 may provide nine voltage levels at the respective AC terminals 11 and 12. Then, the coupling inductor 3 may output seventeen voltage levels.

[0058] In embodiments according to the present disclosure, the switching semiconductor devices in the first and second power converting units 1, 2 may be of various types, for example MOSFET, IGBT and the like. The scope of the present disclosure is not intended to be limited in this respect.

[0059] In some embodiments, a method for the multi-level power convertor 100 as described above is provided. The method includes providing a first plurality of voltage levels to the first end 311 of the first winding 31 from the first AC terminal 11; providing a second plurality of voltage levels of the same number as the first plurality of voltage levels to the third end 321 of the second winding 32 from the second AC terminal 21, wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels; and outputting a third plurality of voltage levels via the second end 312 of the first winding 31 and the fourth end 322 of the second winding 32, wherein the number of the third plurality of voltage levels equals to the sum of the number of the first plurality of voltage levels and the number of the second plurality of voltage levels minus one.

[0060] According to various embodiments of the present disclosure, the first plurality of voltage levels and the second plurality of voltage levels having a phase shift of 90

degree may be combined by the coupling inductor 3 into a third plurality of voltage levels; the number of the third plurality of voltage levels equals to the sum of the number of the first plurality of voltage levels and the number of the second plurality of voltage levels minus one. In this way, the multi-level power convertor 100 in accordance with
5 embodiments of the present disclosure may generate the same number of voltage levels as the conventional multi-level power convertor through using less capacitor, reducing the risk of voltage imbalance among the capacitors in the multi-level power convertor 100 and thereby avoiding the damage of the switching semiconductor devices in the multi-level power convertor 100. Hence, the performance and reliability of the multi-level
10 power convertor 100 may be improved.

[0061] While several inventive embodiments have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the function and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or
15 modifications is deemed to be within the scope of the inventive embodiments described herein. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the inventive teachings is/are used.
20 Those skilled in the art will recognize, or be able to ascertain using no more than routine experimentation, many equivalents to the specific inventive embodiments described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described
25 and claimed. Inventive embodiments of the present disclosure are directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the inventive scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A multi-level power convertor (100) comprising:

a DC port;

5 an AC port;

a first power converting unit (1) coupled to the DC port and comprising a first AC terminal (11) adapted to provide a first plurality of voltage levels;

a second power converting unit (2) coupled to the DC port and comprising a second AC terminal (21) adapted to provide a second plurality of voltage levels of the same number as the first plurality of voltage levels, wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels;

a coupling inductor (3) comprising first and second windings (31, 32) with the same number of turns, wherein the first winding (31) comprises a first end (311) coupled to the first AC terminal (11) and a second end (312), the second winding (32) comprises a third end (321) coupled to the second AC terminal (21) and a fourth end (322), and the second end (312) of the first winding (31) and the third end (321) of the second winding (32) are namesake ends of the first and second windings (31, 32); and

an inductive filtering unit (4) arranged between the AC port and the second and fourth ends (312, 322) of the first and second windings (31, 32).

2. The multi-level power convertor (100) according to claim 1, wherein the second and fourth ends (312, 322) of the first and second windings (31, 32) are coupled to a common node (N0), and wherein the inductive filtering unit (4) comprises an inductor (L0) arranged between the common node (N0) and the AC port.

3. The multi-level power convertor (100) according to claim 1, wherein the inductive filtering unit (4) comprises:

a first inductor (L1) arranged between the second end (312) of the first winding (31) and the AC port; and

a second inductor (L2) arranged between the fourth end (322) of second winding

(32) and the AC port.

4. The multi-level power convertor (100) according to claim 1, wherein the inductive filtering unit (4) comprises an additional coupling inductor comprising third
5 and fourth windings (41, 42),

wherein the third winding (41) is arranged between the second end (312) of the first winding (31) and the AC port,

wherein the fourth winding (42) is arranged between the fourth end (322) of second winding (32) and the AC port, and

10 wherein namesake ends of the third and fourth windings (41, 42) are connected to the AC port.

5. The multi-level power convertor (100) according to claim 1, wherein each of the first and second AC terminals (11, 21) provides five voltage levels, and the AC port
15 provides nine voltage levels.

6. The multi-level power convertor (100) according to claim 1, wherein the DC port comprises first and second DC terminals (DC+, DC-), and wherein the first power converting unit (1) comprises:

20 first and second capacitors (C1, C2) connected in series between the first and second DC terminals (DC+, DC-);

first, second, third, and fourth switching semiconductor devices (S1, S2, S3, S4) connected in series between the first and second DC terminals (DC+, DC-), wherein a first node (N1) between the first and second capacitors (C1, C2) is connected to a second
25 node (N2) between the second and third switching semiconductor devices (S2, S3);

fifth and sixth switching semiconductor devices (S5, S6) connected in series between a third node (N3) and the first AC terminal (11), the third node (N3) being between the first and second switching semiconductor devices (S1, S2);

30 seventh and eighth switching semiconductor devices (S7, S8) connected in series between a fourth node (N4) and the first AC terminal (11), the fourth node (N4) being between the third and fourth switching semiconductor devices (S3, S4); and

a third capacitor (C3) connected between a fifth node (N5) and a sixth node (N6), the fifth node (N5) being between the fifth and sixth switching semiconductor devices (S5, S6), and the sixth node (N6) being between the seventh and eighth switching semiconductor devices (S7, S8).

5

7. The multi-level power convertor (100) according to claim 6, wherein the second power converting unit (2) comprises:

the first and second capacitors (C1, C2) shared with the first power converting unit (1);

10 the first, second, third, and fourth switching semiconductor devices (S1, S2, S3, S4) shared with the first power converting unit (1);

ninth and tenth switching semiconductor devices (S9, S10) connected in series between the third node (N3) and the second AC terminal (21);

15 eleventh and twelfth switching semiconductor devices (S11, S12) connected in series between the fourth node (N4) and the second AC terminal (21); and

a fourth capacitor (C4) connected between a seventh node (N7) and a eighth node (N8), the seventh node (N7) being between the ninth and tenth switching semiconductor devices (S9, S10), and the eighth node (N8) being between the eleventh and twelfth switching semiconductor devices (S11, S12).

20

8. The multi-level power convertor (100) according to claim 6, wherein the second power converting unit (2) comprises:

the first and second capacitors (C1, C2) shared with the first power converting unit (1);

25 thirteenth, fourteenth, fifteenth, and sixteenth switching semiconductor devices (S13, S14, S15, S16) connected in series between the first and second DC terminals (DC+, DC-), wherein a ninth node (N9) between the fourteenth and fifteenth switching semiconductor devices (S14, S15) is connected to the first node (N1);

30 ninth and tenth switching semiconductor devices (S9, S10) connected in series between the a tenth node (N10) and the second AC terminal (21), the tenth node (N10) being between the thirteenth and fourteenth switching semiconductor devices (S13, S14);

eleventh and twelfth switching semiconductor devices (S11, S12) connected in series between an eleventh node (N11) and the second AC terminal (21), the eleventh node (N11) being between the fifteenth and sixteenth switching semiconductor devices (S15, S16); and

5 a fourth capacitor (C4) connected between a seventh node (N7) and a eighth node (N8), the seventh node (N7) being between the ninth and tenth switching semiconductor devices (S9, S10), and the eighth node (N8) being between the eleventh and twelfth switching semiconductor devices (S11, S12).

10 9. The multi-level power convertor (100) according to claim 1, wherein each of the first and second AC terminals (11, 21) provides nine voltage levels, and the AC port provides seventeen voltage levels.

15 10. The multi-level power convertor (100) according to claim 1, wherein the multi-level power convertor (100) operates as an inverter when the DC port is used as an input and the AC port is used as an output, and

wherein the multi-level power convertor (100) operates as a rectifier when the AC port is used as an input and the DC port is used as an output.

20 11. A method for a multi-level power convertor (100), the multi-level power convertor (100) comprising a DC port; an AC port; a first power converting unit (1) coupled to the DC port and comprising a first AC terminal (11); a second power converting unit (2) coupled to the DC port and comprising a second AC terminal (21); a coupling inductor (3) comprising first and second windings (31, 32) with the same
25 number of turns, wherein the first winding (31) comprises a first end (311) coupled to the first AC terminal (11) and a second end (312), the second winding (32) comprises a third end (321) coupled to the second AC terminal (21) and a fourth end (322), and the second end (312) of the first winding (31) and the third end (321) of the second winding (32) are namesake ends of the first and second windings (31, 32); and an inductive filtering unit (4)
30 arranged between the AC port and the second and fourth ends (312, 322) of the first and second windings (31, 32),

the method comprising:

providing a first plurality of voltage levels to the first end (311) of the first winding (31) from the first AC terminal (11);

5 providing a second plurality of voltage levels of the same number as the first plurality of voltage levels to the third end (321) of the second winding (32) from the second AC terminal (21), wherein the second plurality of voltage levels are phase-shifted by 90 degree with respect to the first plurality of voltage levels; and

10 outputting a third plurality of voltage levels via the second end (312) of the first winding (31) and the fourth end (322) of the second winding (32), wherein the number of the third plurality of voltage levels equals to the sum of the number of the first plurality of voltage levels and the number of the second plurality of voltage levels minus one.

12. The method according to claim 11, wherein the second and fourth ends (312, 322) of the first and second windings (31, 32) are coupled to a common node (N0), and
15 wherein the inductive filtering unit (4) comprises an inductor (L0) arranged between the common node (N0) and the AC port.

13. The method according to claim 11, wherein the inductive filtering unit (4) comprises:

20 a first inductor (L1) arranged between the second end (312) of the first winding (31) and the AC port; and

a second inductor (L2) arranged between the fourth end (322) of second winding (32) and the AC port.

25 14. The method according to claim 11, wherein the inductive filtering unit (4) comprises an additional coupling inductor comprising third and fourth windings (41, 42),

wherein the third winding (41) is arranged between the second end (312) of the first winding (31) and the AC port,

30 wherein the fourth winding (42) is arranged between the fourth end (322) of second winding (32) and the AC port, and

wherein namesake ends of the third and fourth windings (41, 42) are connected to

the AC port.

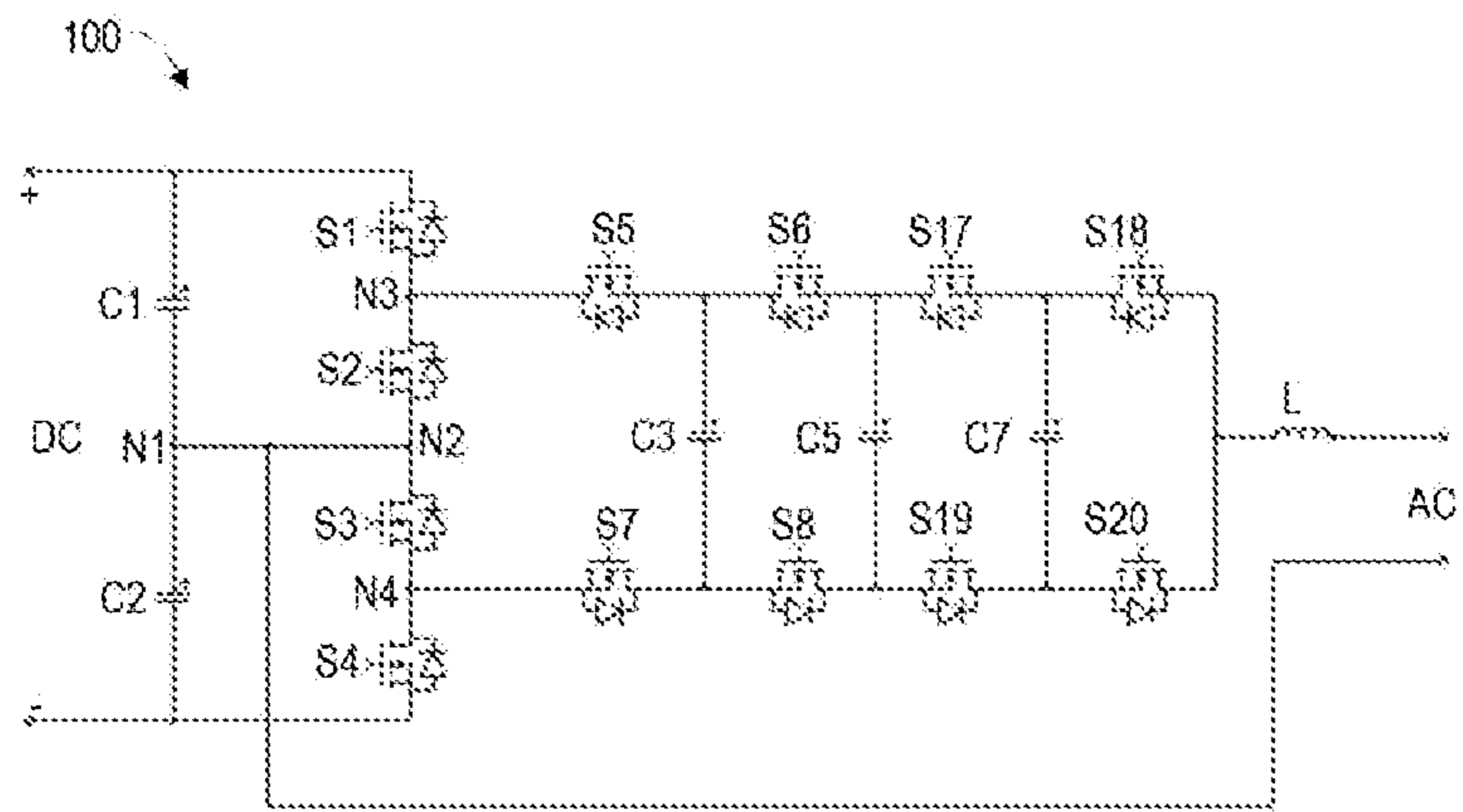


FIG. 1

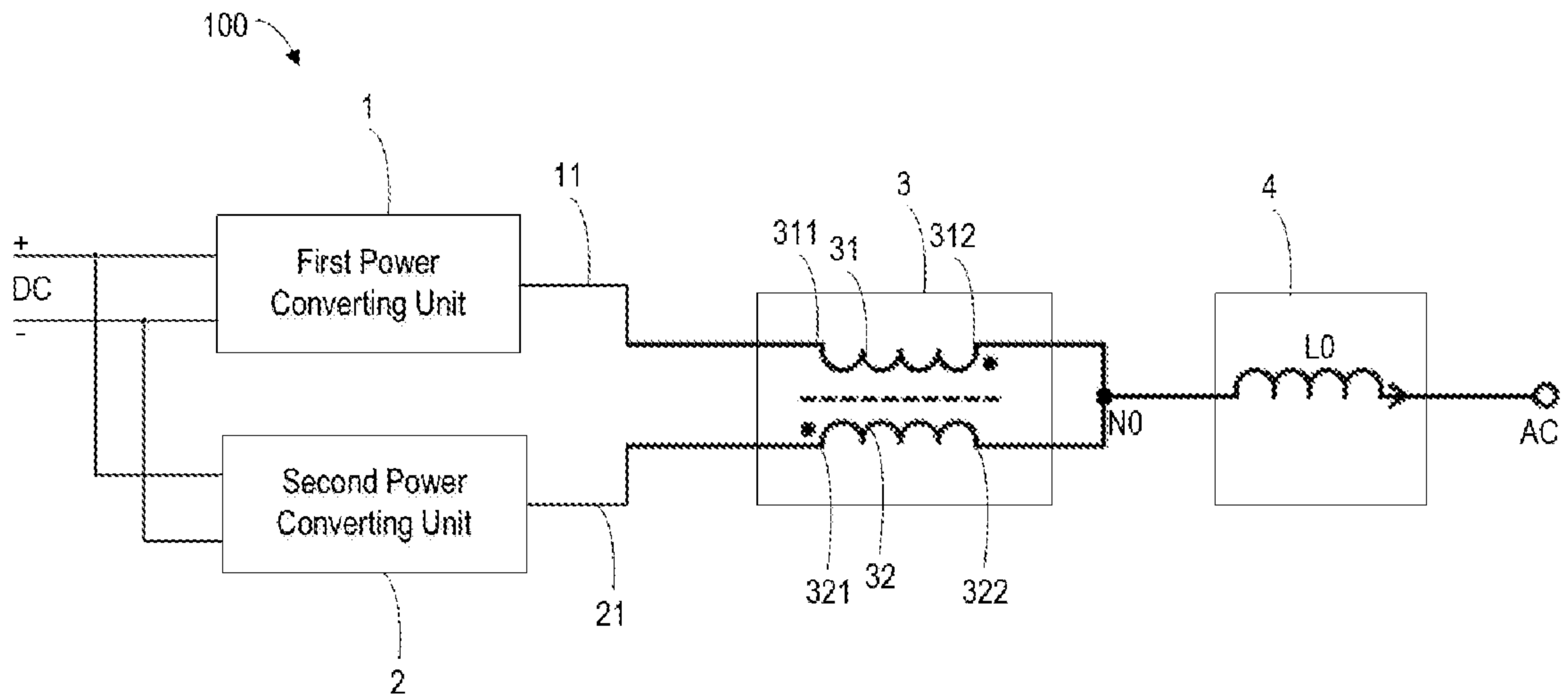


FIG. 2

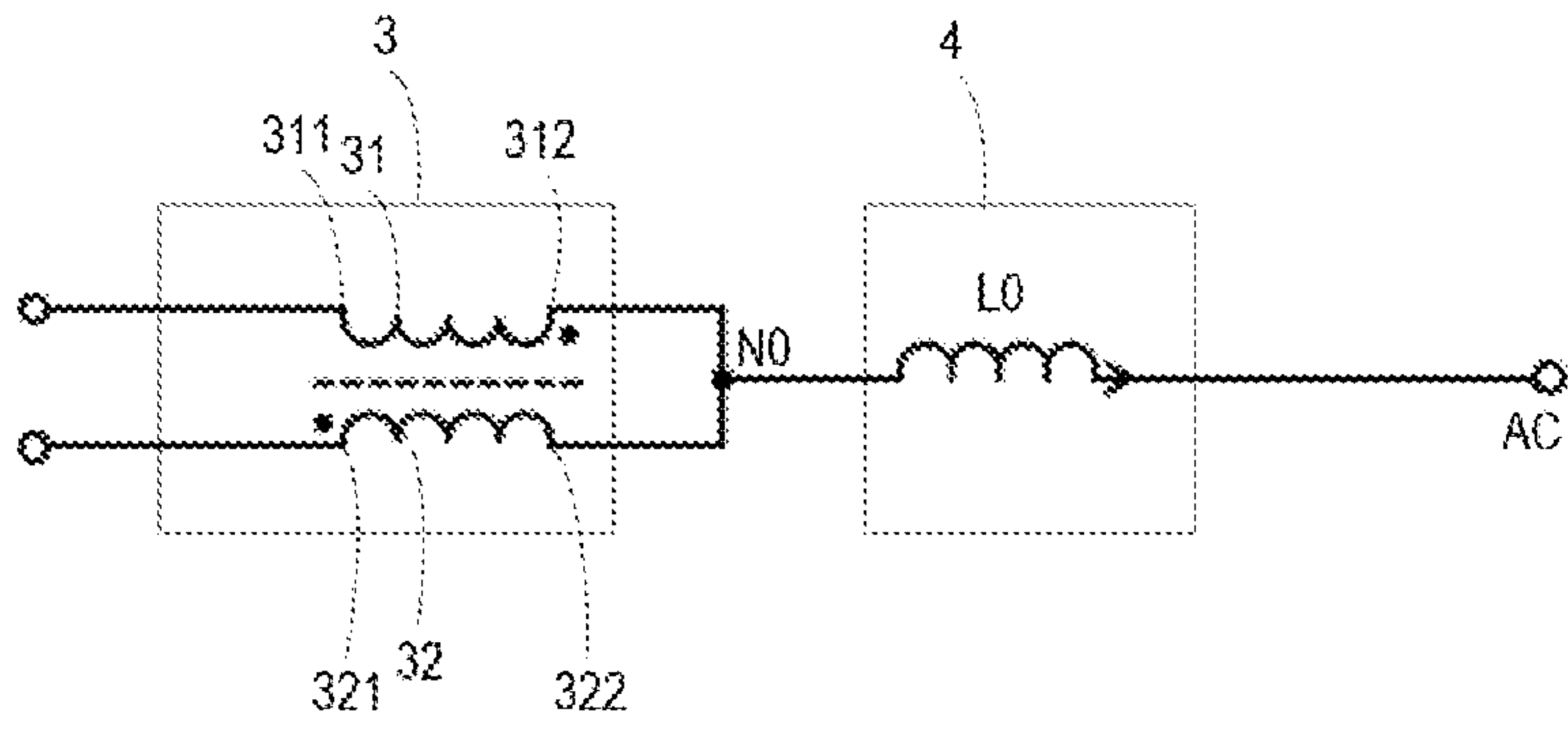


FIG. 3

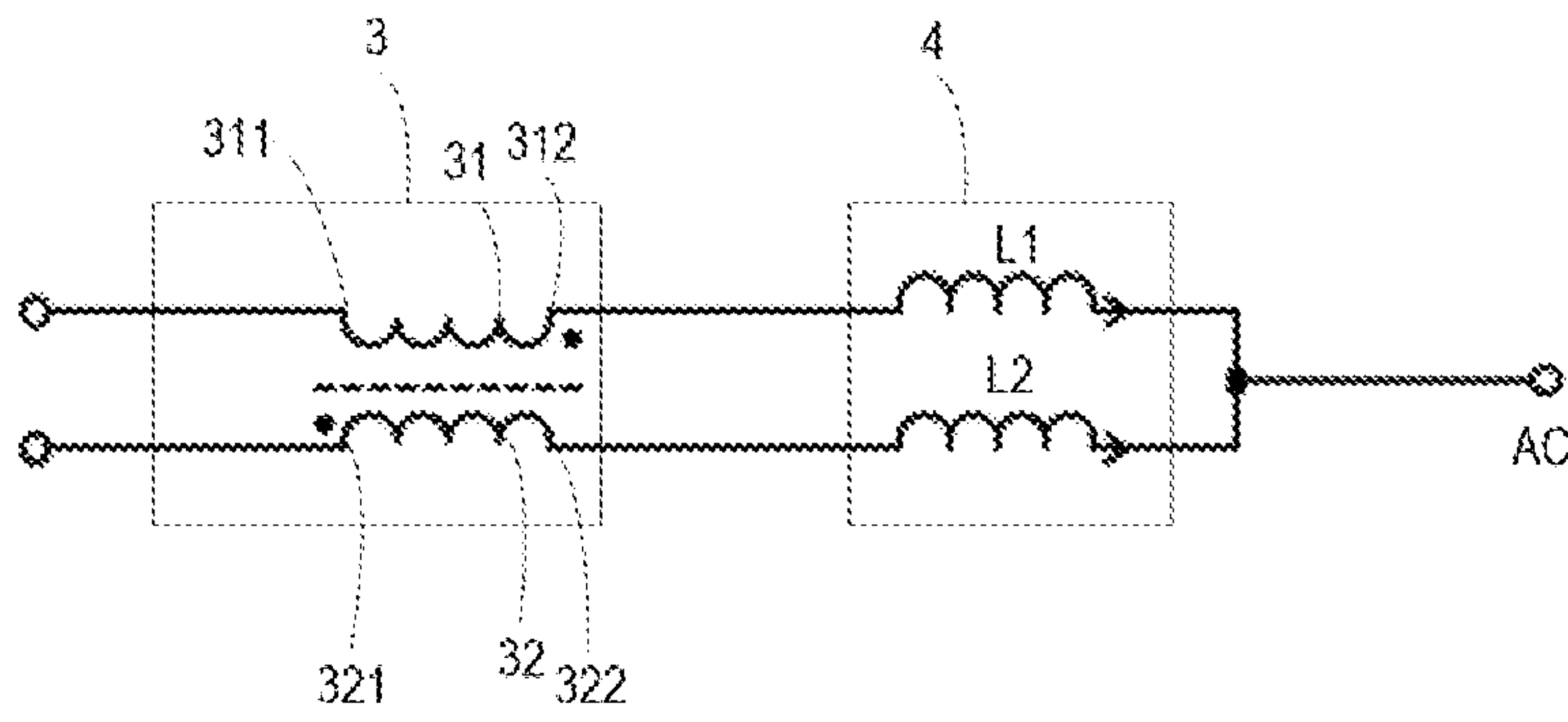


FIG. 4

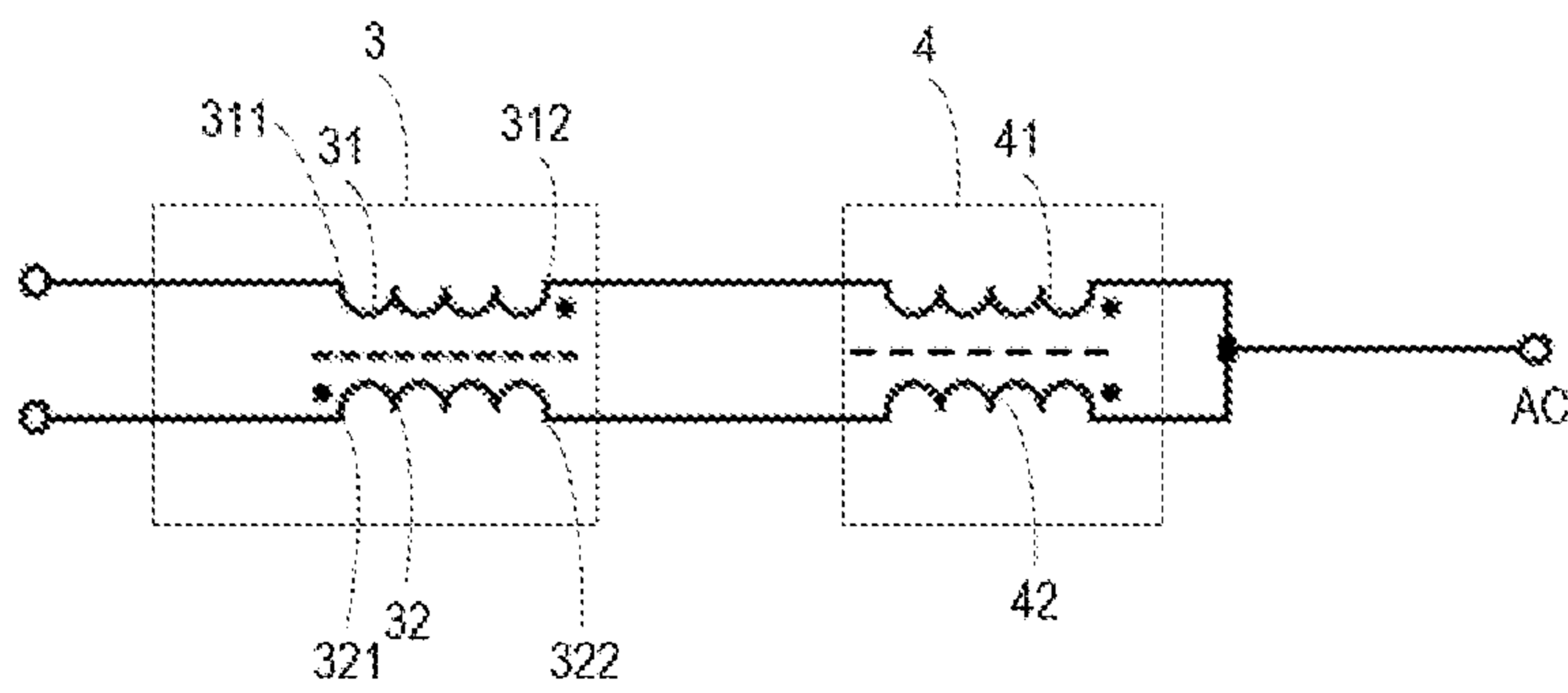


FIG. 5

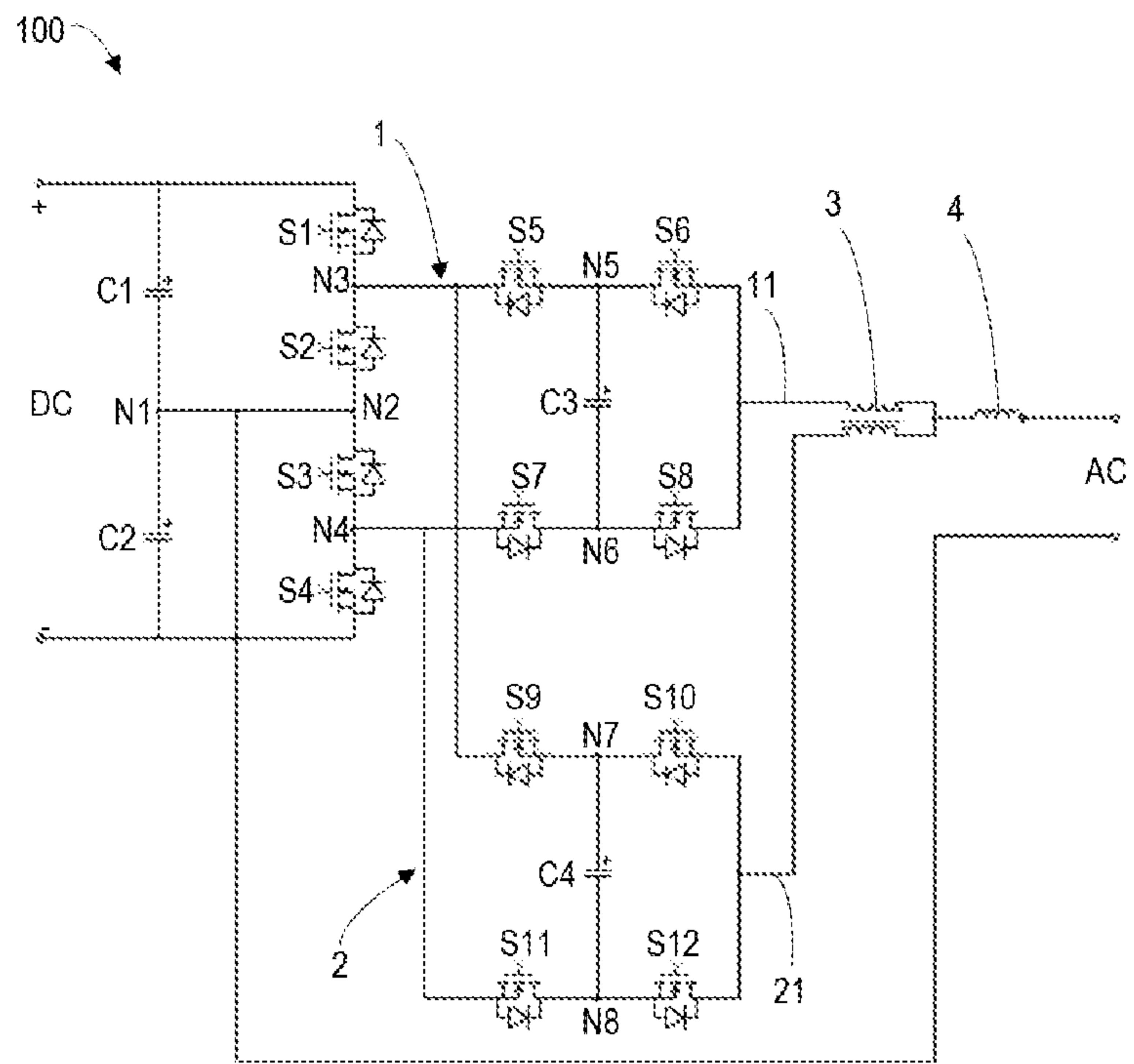


FIG. 6

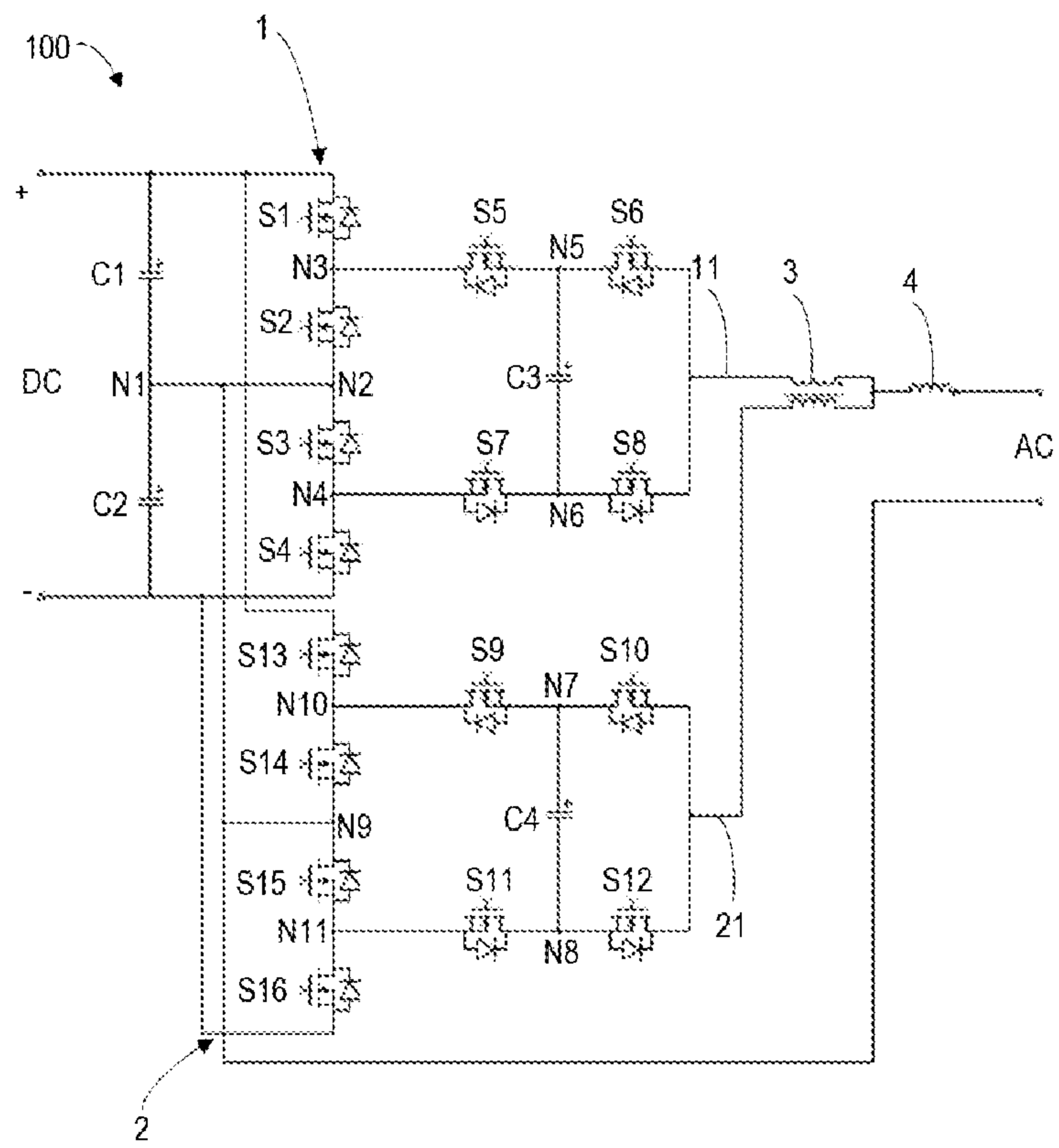


FIG. 7

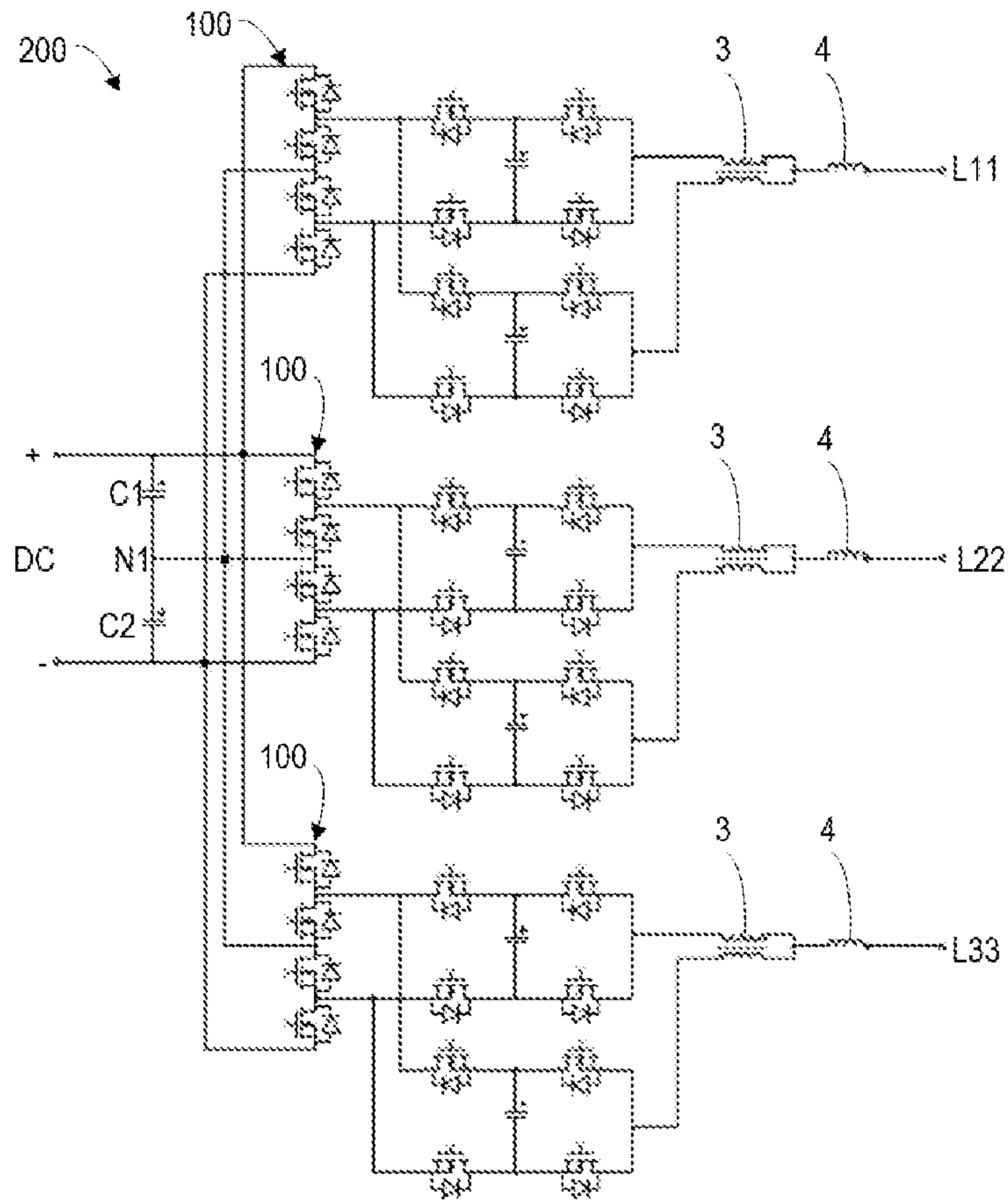


FIG. 8

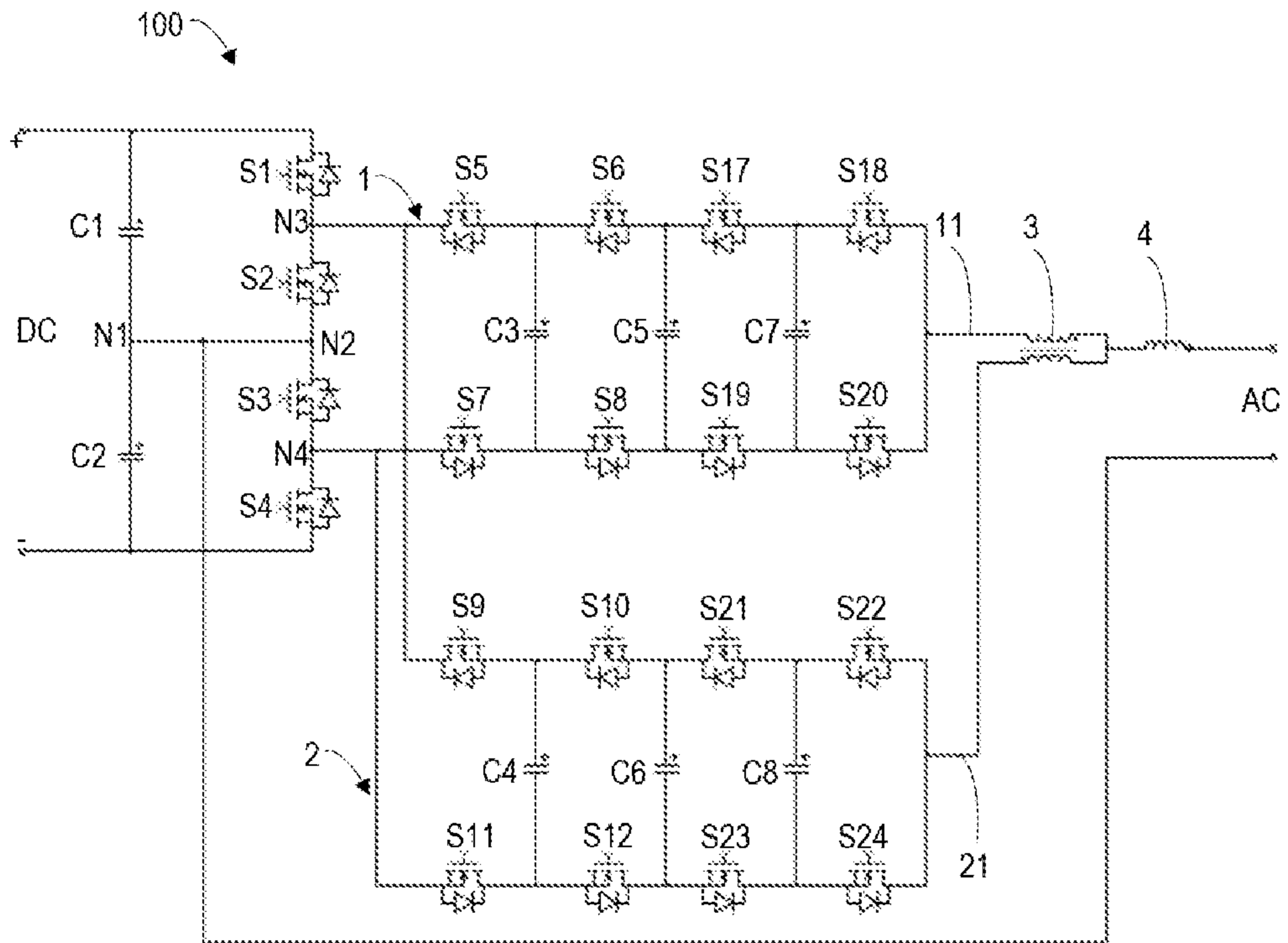


FIG. 9

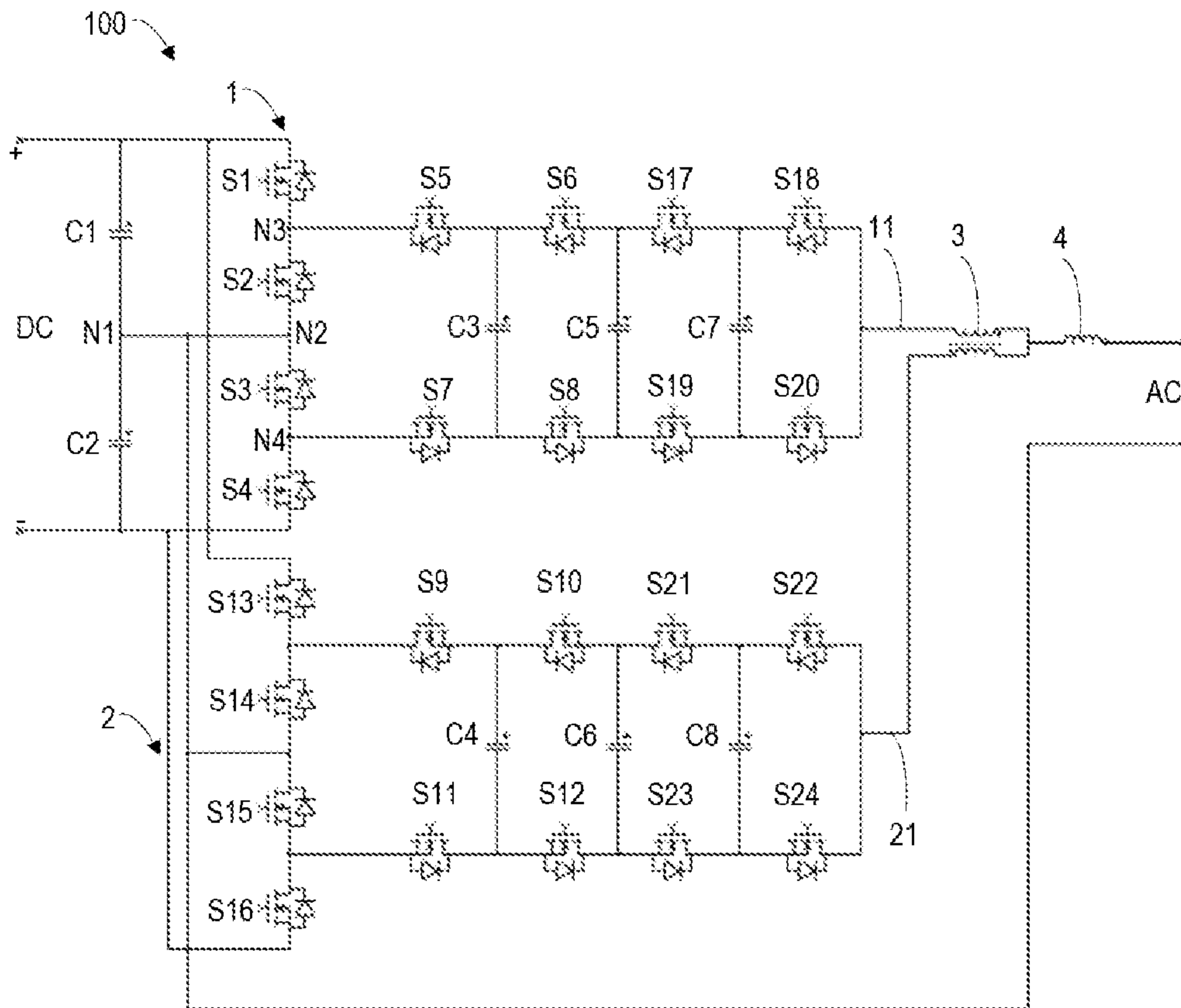


FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/117102

A. CLASSIFICATION OF SUBJECT MATTER H02M 7/483(2007.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H02M Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) WPI, EPODOC, CNPAT, CNKI: multi, level, power, convertor?, converter?, phase, shift+, coupling, inductor?, 3 1w level?, 5 1w level?, 7 1w level?, 9 1w level?, filter+		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 103346690 A (HUAWEI TECHNOLOGIES CO., LTD.) 09 October 2013 (2013-10-09) description, paragraphs [0039]-[0061], and figure 1	1-5, 9-14
Y	CN 103346690 A (HUAWEI TECHNOLOGIES CO., LTD.) 09 October 2013 (2013-10-09) description, paragraphs [0039]-[0061], and figure 1	6-8
Y	CN 108809133 A (NAVAL UNIVERSITY ENG. PLA) 13 November 2018 (2018-11-13) description, paragraph [0042], and figures 1-2	6-8
X	CN 103368427 A (EMERSON NETWORK POWER CO., LTD.) 23 October 2013 (2013-10-23) description, paragraphs [0024]-[0050], and figures 1-7	1-4, 10-14
A	CN 102882409 A (CHINESE ACAD. SCI. ELECTRICAL ENG. INST.) 16 January 2013 (2013-01-16) the whole document	1-14
A	KR 20160027408 A (KYUNGPOOK NAT. UNIV. IND. ACAD.) 10 March 2016 (2016-03-10) the whole document	1-14
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
<p>* Special categories of cited documents:</p> <p>“A” document defining the general state of the art which is not considered to be of particular relevance</p> <p>“E” earlier application or patent but published on or after the international filing date</p> <p>“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>“O” document referring to an oral disclosure, use, exhibition or other means</p> <p>“P” document published prior to the international filing date but later than the priority date claimed</p> <p>“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>“&” document member of the same patent family</p>		
Date of the actual completion of the international search 27 July 2020		Date of mailing of the international search report 12 August 2020
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088 China Facsimile No. (86-10)62019451		Authorized officer FANG,Lei Telephone No. 86-(10)-53961493

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No. PCT/CN2019/117102

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	103346690	A	09 October 2013	WO	2015000291	A1	08 January 2015
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				US	9385632	B2	05 July 2016
				CN	103346690	B	30 March 2016
				US	2015085541	A1	26 March 2015
				EP	2942863	A1	11 November 2015

CN	108809133	A	13 November 2018	None			

CN	103368427	A	23 October 2013	None			

CN	102882409	A	16 January 2013	None			

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