United States Patent [19]

Koeller et al.

[11] **3,823,359**

[45] **July 9, 1974**

[54] **INHIBIT AND RESET CIRCUIT**

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[73] Assignee: **The National Cash Register Company,** Dayton, Ohio

[22] Filed: **Mar. 7, 1973**

[21] Appl. No.: **338,673**

[52] **U.S. Cl.** **321/11,** 321/47

[51] **Int. Cl.** **H02m 1/18**

[58] **Field of Search** 321/11–14, 321/47

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Primary Examiner—William M. Shoop, Jr.

Attorney, Agent, or Firm—J. T. Cavender; Albert L. Sessler, Jr.; Edward Dugas

[57] **ABSTRACT**

The circuit of the present invention is used in conjunction with a peripheral machine power supply to control the connection of the peripheral machine to the trunk line of a computer processing unit such that the peripheral machine does not load the trunk line unnaturally during power "on" and "off" transitions. Means are provided for sensing the AC power supplied to the peripheral machine and for providing a signal indicative of the presence or absence of AC power. A delay means receives the provided signal and delays the provided signal for a period of time sufficient to allow the peripheral machine's power supply to reach operating level and for a minimal time in anticipation of the machine's power supply dropping out of its operating level. Means responsive to the delayed signal connects or disconnects the peripheral machine from the trunk line when power operating levels are reached or not reached, respectively.

10 Claims, 11 Drawing Figures

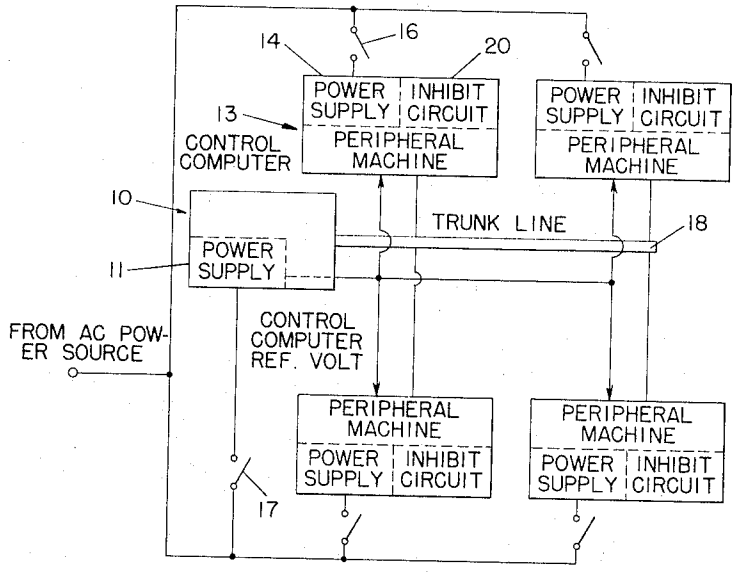


FIG. 1

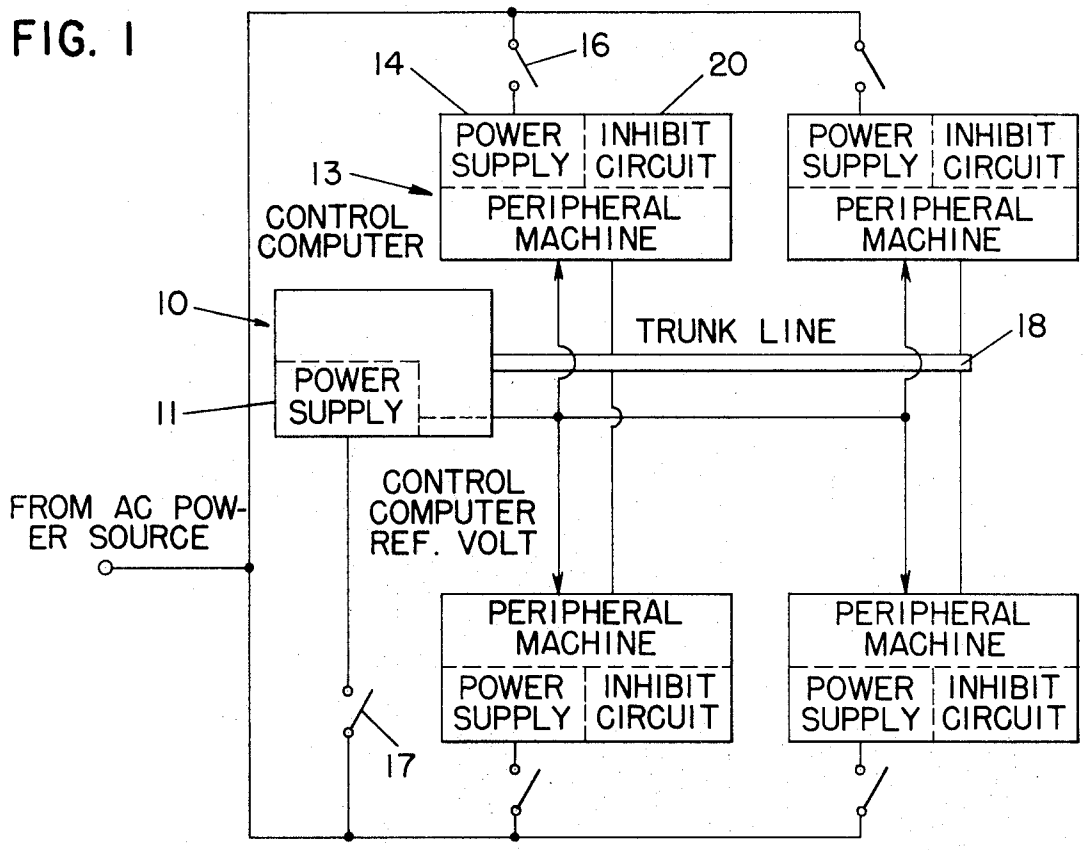


FIG. 3A

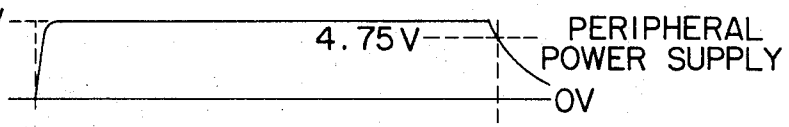


FIG. 3B

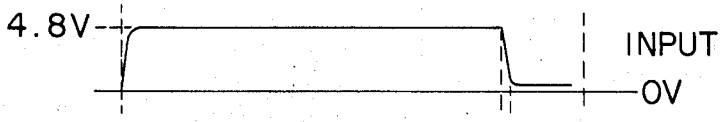


FIG. 3C

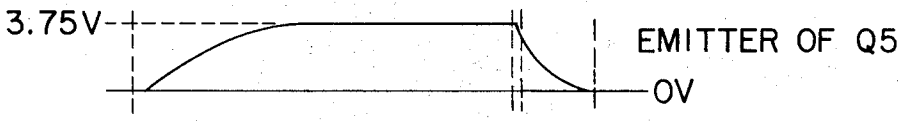


FIG. 3D

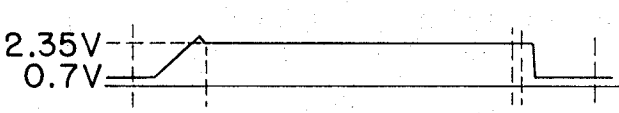


FIG. 3E

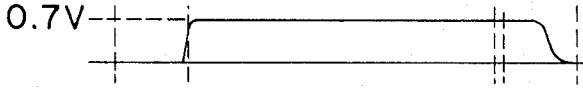


FIG. 3F

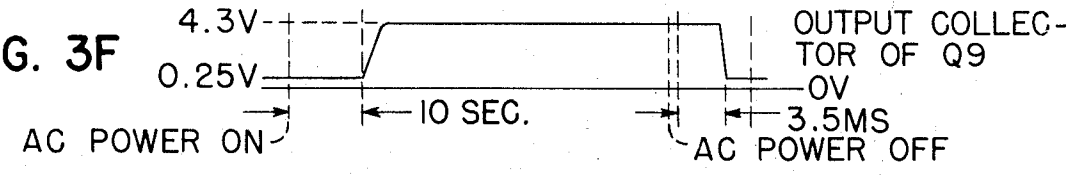


FIG. 2A

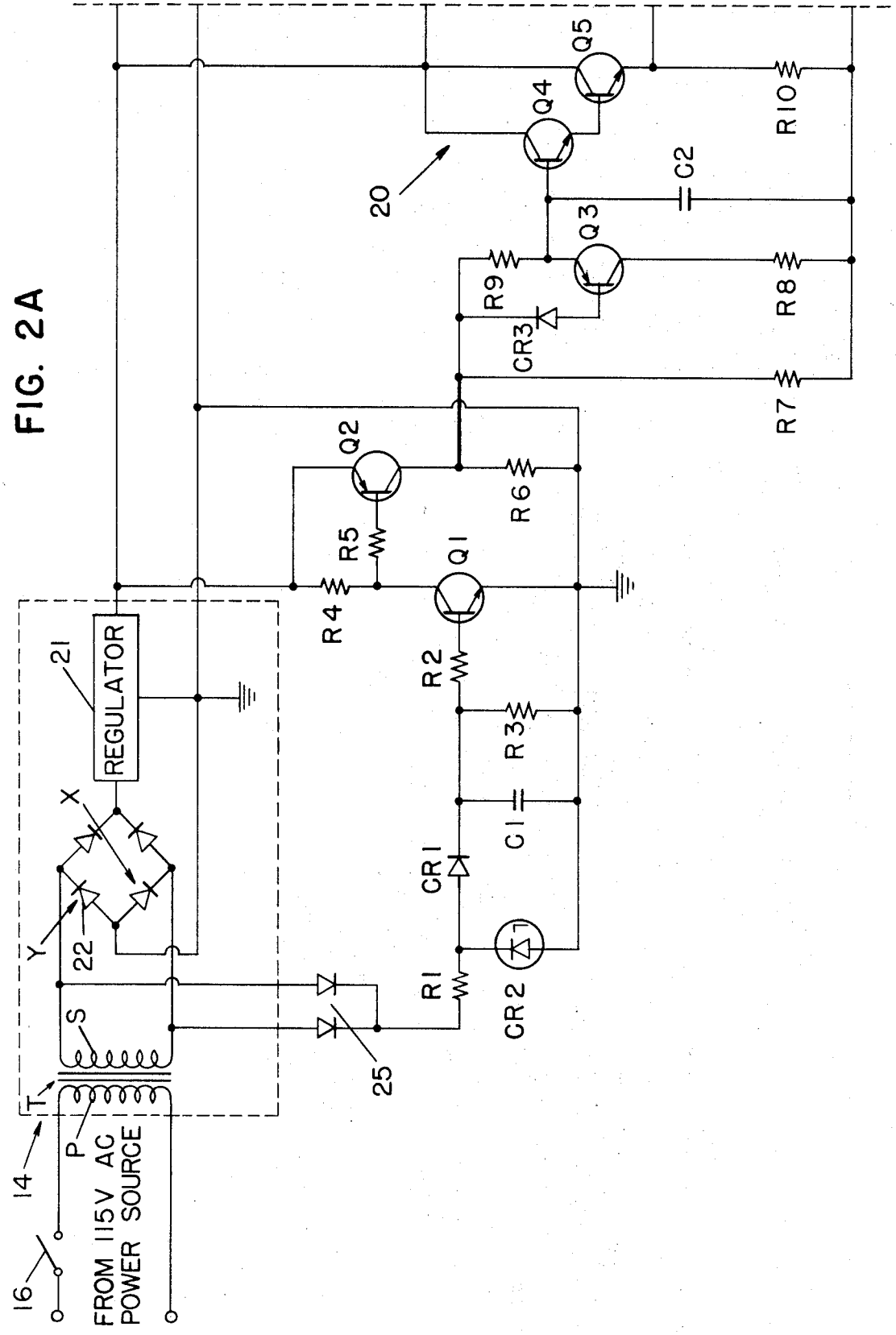

Q5
Q4
R10
20
C2
Q3
R9
R8
CR3
R7
Q2
R6
R5
Q1
R4
R2
21
REGULATOR
R3
X
C1
CR1
Y
22
CR2
R1
S
25
T
P
14
16
FROM 115V AC
POWER SOURCE

FIG. 2B

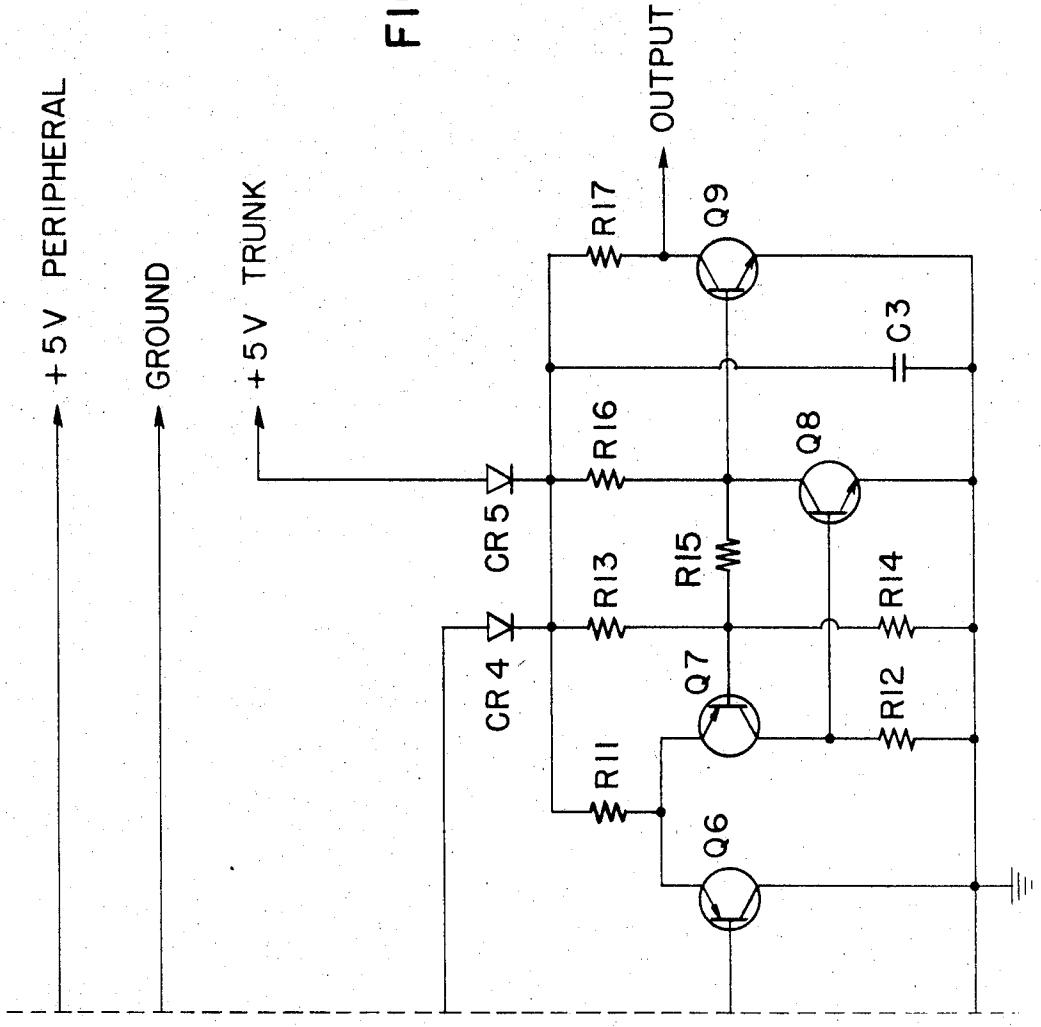

+5V PERIPHERAL
GROUND
+5V TRUNK
OUTPUT
R17
Q9
C3
R16
Q8
CR5
R15
R13
R14
CR4
Q7
R12
R11
Q6

FIG. 4

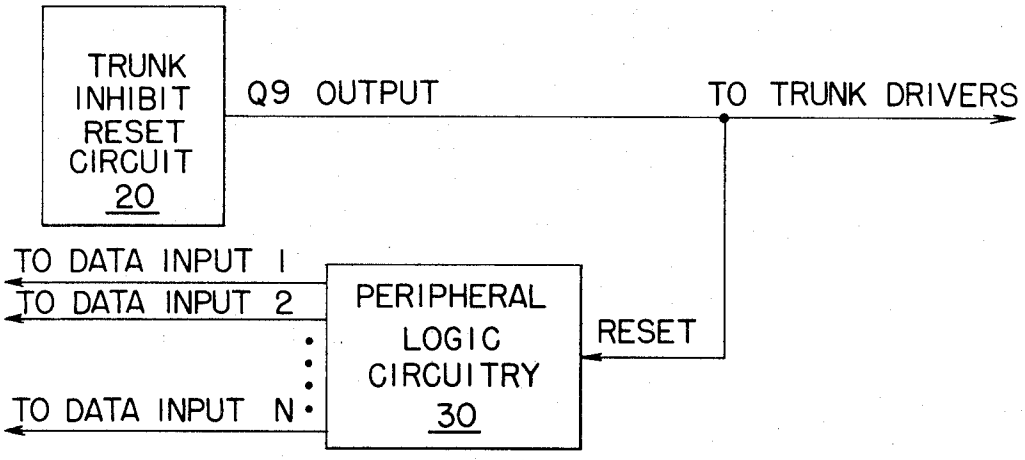
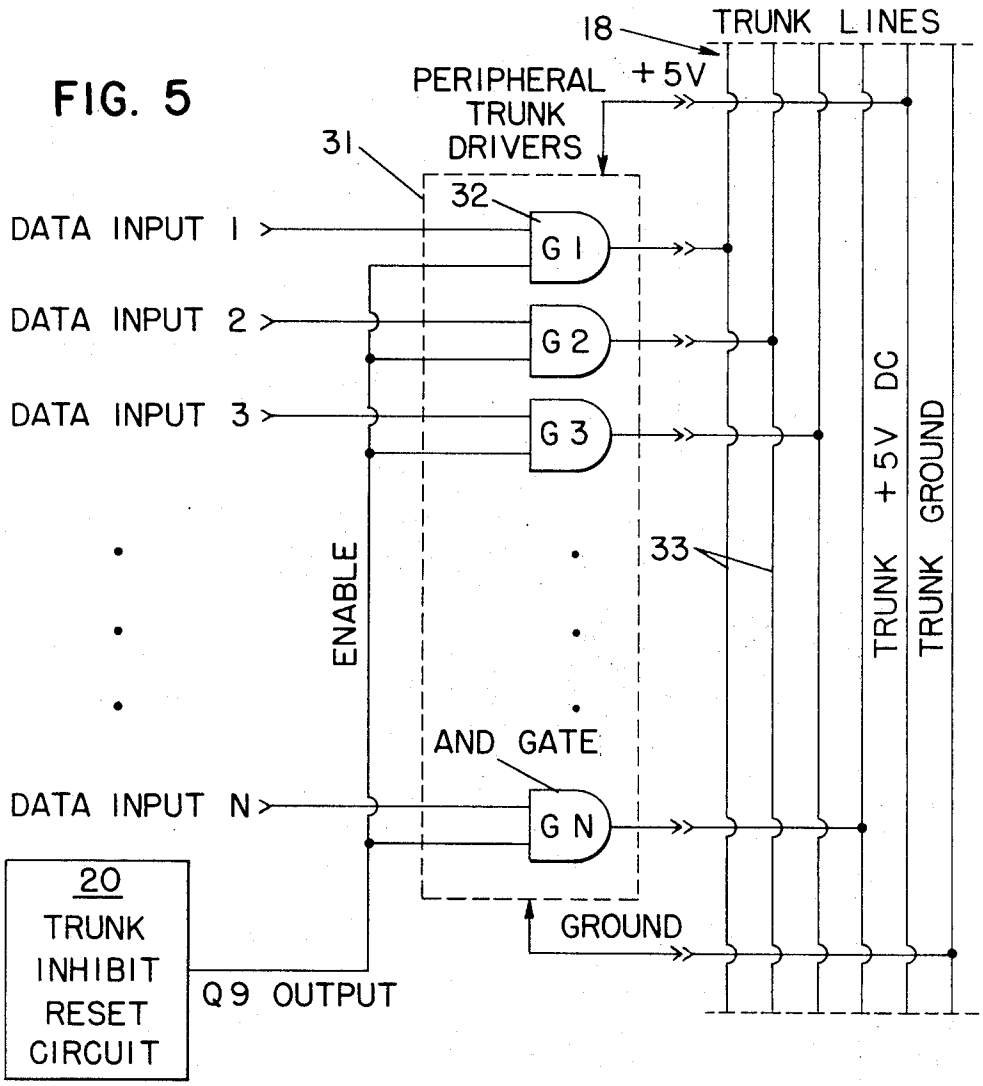

TRUNK
INHIBIT
RESET
CIRCUIT
20
Q9 OUTPUT
TO TRUNK DRIVERS
TO DATA INPUT 1
TO DATA INPUT 2
TO DATA INPUT N
PERIPHERAL
LOGIC
CIRCUITRY
30
RESET

FIG. 5


18
TRUNK LINES
PERIPHERAL
TRUNK
DRIVERS
+5V
31
32
DATA INPUT 1
DATA INPUT 2
DATA INPUT 3
G 1
G 2
G 3
ENABLE
33
TRUNK +5V DC
TRUNK GROUND
AND GATE
DATA INPUT N
G N
GROUND
20
TRUNK
INHIBIT
RESET
CIRCUIT
Q9 OUTPUT

INHIBIT AND RESET CIRCUIT

BACKGROUND OF THE INVENTION

A computer processing unit which operates in conjunction with peripheral machines through a common trunk line is often loaded by the peripheral machines when the peripheral machines are in a transition to a power off or a power on condition. In addition, a peripheral machine having an abnormally low power supply voltage will not function correctly when attached to the common trunk line and, therefore, it should be disconnected as quickly as possible in order to prevent degradation of the trunk signals.

Ideally, when AC power is applied to a peripheral machine its power supply voltage instantly reaches its designed voltage level and in a like manner when AC power is removed the power supply voltage should drop immediately to a zero value. In actuality, due to various factors, such as R.C. time constants, the voltage level of the peripheral machine's power supply takes time before reaching its design value. In a like manner, when AC power is removed, the peripheral power supply voltage takes time to reach a zero value. During these transition times, performance of the peripheral machine will be below tolerable design levels. It therefore would be highly desirable to have a system for quickly sensing the absence of AC power and/or a low voltage level and for disconnecting the peripheral machine quickly from the communication trunk upon the occurrence of either event. The present system is directed to a solution of this problem.

SUMMARY OF THE INVENTION

The present invention is directed to a circuit for connecting and disconnecting a peripheral machine from a computer processing unit when the peripheral machine is in the transition of an AC power "on" or "off" condition or a condition which limits the operating voltage of the machine to a limit below acceptable operating values. The circuit is comprised of a means for sensing the AC power applied to the peripheral machine and for supplying a sense signal indicative of the presence or absence of AC power. The time response of the sensing means is substantially less than the time response of the power supply of the peripheral machine. A delay means receiving the sense signal provides a delay for a period of time sufficient to allow the peripheral supply voltage to reach its operating level. A means responsive to the absence of the sensed signal disables the delay means. Means are also provided for connecting and disconnecting the peripheral machine to the trunk line of the computer processing unit in accordance with the sensed signal.

Accordingly, it is an object of the present invention to provide an improved peripheral trunk inhibit, reset, circuit.

It is another object of the present invention to provide an improved circuit for disconnecting a peripheral machine from a common turnk line when the peripheral machine's power supply output falls below a tolerable level.

It is a further object of the present invention to provide an improved circuit for automatically connecting and disconnecting a peripheral machine from a common trunk in accordance with preselected tolerance levels of machine performance.

These and further objects of the present invention will become more apparent and better understood when taken in conjunction with the following description and drawings throughout which like characters indicate like parts, and which drawings form a part of this application.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a system wherein the present invention finds particular utility;

FIGS. **2**A and **2**B, taken together, are a schematic diagram of the preferred embodiment of the present invention;

FIGS. **3**A to **3**F illustrates waveforms taken at selected locations on the preferred embodiment shown in FIGS. **2**A and **2**B;

FIG. **4** illustrates in block diagram form the circuit of the present invention operating in conjunction with the peripheral machine's logic circuitry; and

FIG. **5** illustrates in partial block diagram form the circuit of the present invention connected to activate peripheral machine drivers.

DESCRIPTION OF THE PREFERRED EMBODIMENT OF THE INVENTION

Referring to FIG. **1,** a computer processing unit **10** is connectable to a plurality of peripheral machines **13** by means of a common trunk line **18.**

Peripheral machines, such as card readers, punches, paper tape readers, line printers, storage discs and the like are not generally used each time the computer processor is used. In addition, the speed at which the peripheral machine operates is much slower as compared to the speed of the computer processor. It is, therefore, more practical to connect the peripheral machine to a trunk line and address the machine only when needed.

Each peripheral machine is connected to a source of AC power (not shown) through a switch **16.** The computer processing unit **10** is also connected to the AC power source through switch **17.**

The computer processing unit **10** contains a power supply **11** which provides the required power to operate the processor but, in addition, the power supply **11** also provides a reference potential, which may be either AC or DC to the individual peripheral machine power supplies **14.** For simplicity, FIG. **1** illustrates all electrical wiring in a single line notation when in fact more than one line is used to transfer power and signals between the computer processor and the peripheral machines.

In FIGS. **2**A and **2**B the power supply **14,** used in one peripheral machine, is shown connected in combination to its associated inhibit reset circuit **20.** Each of the peripheral machines contains an identical inhibit circuit **20.** AC power is supplied to the primary winding P of power transformer T, through switch **16.**

The secondary winding S, is connected to a full wave bridge rectifier **22** to provide an output voltage, of approximately 9 VDC, to a regulator **21,** which regulator filters and limits the DC output voltage to a +5V level. This output voltage is the primary peripheral supply voltage. A pair of diodes **25** are connected to the secondary winding S to form in conjunction with diodes X and Y of bridge rectifier **22** a full wave rectifier for providing a DC sense signal which signal is directly dependent on the presence of an AC signal on the secondary

winding S; that is, there is no substantial time delay between the existence of the AC signal and the full wave rectified DC signal at the juncture of diodes **25.**

A charging path for a capacitor C1 is formed through the series path of resistor R1 and diode CR1. Resistor R1 connects the juncture of the cathodes of diodes **25** to the anode of diode CR1. Connected in parallel across diode CR1 and capacitor C1 is a zener diode CR2, which diode functions to limit the voltage appearing across its terminals to a predesigned value. Resistor R3 connected in parallel across capacitor C1 provides a discharge path for capacitor C1. The base of transistor Q1 is connected to the juncture of resistor R3 and diode CR1 and capacitor C1 by a base biasing resistor R2. The collector of Q1 is connected to the peripheral supply voltage by a load resistor R4. The emitter of Q1 is connected to a reference point, ground. In operation, when AC power is supplied to power supply **14,** capacitor C1 begins to charge, quickly raising the voltage on the base of Q1. The peripheral supply regulator **21,** as is the case with all filtered and regulated supplies, contains a time delay due to the use of filter capacitors and the load. Capacitor C1 is chosen to provide a time delay substantially less than the delay caused by regulator **21.** The voltage on the collector of Q1 will, therefore, rise more slowly than the voltage on its base. Transistor Q1 is saturated on as the +5V peripheral supply voltage rises. The output of transistor Q2, which is taken from its collector, follows the rise in the +5V peripheral supply as its emitter is connected directly to the peripheral supply while its base is connected through resistors R4 and R5 to the peripheral supply. The collector of the transistor Q2 is connected by a resistor R6 to the reference potential, shown as ground.

When AC power is turned off, the voltage on the base of Q1 drops much faster than the +5V supply voltage. Transistor Q1, therefore, turns off quickly. With Q1 turned off, Q2 also quickly turns off. In the preferred embodiment Q1 and Q2 are turned off (output of Q2 goes to zero) before the +5V supply drops below +4.75V. The output signal from Q2 is therefore used as the provided sense signal, because it falls in a minimum time in anticipation of the machine's power supply voltage dropping and rises only after the power supply voltage has achieved its operating level.

FIG. 3A illustrates the rise and fall times of the +5V peripheral power supply for the conditions of AC power on and off. The output of Q2 is shown in FIG. 3B. The output of Q2 (appearing across R6) goes to zero almost immediately when AC power is turned off.

The junction of R6 and the collector of Q2 is connected to resistor R7 which in turn is connected to ground and to resistor R9 which in turn is connected to the emitter of transistor Q3, capacitor C2, and the base of transistor Q4. Diode CR3 is connected at its anode to the base of transistor Q3, and at its cathode to the junction of the collector of Q2 and resistor R6. Resistor R8 connects the collector of transistor Q3 to ground. Resistor R9 and capacitor C2 form a timing circuit which delays the sense signal for a selected period of time. When the output from Q2 is high (positive potential), C2 is charged through R9. When the output from Q2 is low (zero potential), Q3 is turned "on" and provides a low impedance path for C2 to discharge. Transistor Q3 therefore acts as a switch to discharge C2 effectively removing the delayed portion of the sensed signal.

A Darlington emitter follower buffer stage comprised of transistors Q4 and Q5 is connected to receive the potential on capacitor C2 and to provide a non-inverting output which is proportional to the received potential on the base of Q4. The high input impedance of the Darlington emitter follower minimizes the leakage of charge through the state and therefore provides impedance isolation.

The collectors of Q4 and Q5 are connected to the +5V peripheral supply. The emitter of Q5 is connected to ground through resistor R10, and to the base of Q6. Transistors Q6 and Q7 along with resistors R11 and R12 form an emitter coupled differential amplifier means with the signal present on the collector of transistor Q7 providing the base drive for transistor Q8. Resistor R11 is connected to the +5V peripheral supply by diode CR4. Resistors R13 and R14 are serially connected between ground and the +5V peripheral supply. The +5V trunk supply, from the computer processing unit, is connected by diode CR5 to resistor R16. The +5 volt trunk supply is connected to the circuits formed by transistors Q6 through Q9 in order to provide power to these circuits even though the peripheral machine's power supply is off. The states of these circuits maintain the proper bias and states for the trunk system. The +5 volt peripheral supply is also connected to these circuits to enable the peripheral machine in which the present inhibit resist circuit is used, to function when in an off line mode (physically disconnected from the trunk) particularly if the output signal from Q9 is used internally in the peripheral machine as a power up reset signal. Further discussion of the reset function appears in the description associated with FIG. 4. The junction of R13 and R14 is connected to the base of transistor Q7, and also to the base of transistor Q9 through resistors R15. The collector of transistor Q8 is connected to the cathodes of diodes CR4 and CR5 through resistor R16. The emitter of transistor Q8 is connected directly to ground. When the collector of transistor Q7 is high, Q8 is saturated "on" effectively connecting resistor R15 in parallel across resistor R14.

The collector of transistor Q9 is connected through resistor R17 to the cathode of diode CR5, with the collector being the output of the circuit. The emitter of transistor Q9 is connected to ground. Capacitor C3 is connected between the cathode of diode CR5 and ground to eliminate high frequency noise components from the trunk supply voltage. The voltage at the base of transistor Q7 establishes a threshold reference for transistor Q6. The threshold reference established when transistor Q8 is saturated and transistor Q9 is turned off is normally 1.78V. When transistor Q8 is off and transistor Q9 is "on", the threshold reference voltage rises to 1.9 volts. Transistors Q8 and Q9 therefor form a switching means for connecting and disconnecting the inhibit and reset circuit to the peripheral machine.

Feedback from the collector of transistor Q8 to the base of transistor Q7 generates a leval shift in the threshold reference as a function of the input.

In FIG. 3C, the waveform present on the emitter of Q5 is shown. The leading edge of the waveform is slow in rising to the level of 3.75V due to the charging time of capacitor C2. The trailing edge of the waveform is

fast in falling to the lower threshold level due to the short discharging time of capacitor C2.

FIG. 3D illustrates the waveform present on the emitters transistors Q6 and Q7. Transistor Q6 turns off approximately 10 seconds after the AC power is applied to the peripheral power supply. The waveform present on the base of Q8 is shown in FIG. 3E. Transistor Q8 squares up the leading and trailing edges of the waveform from Q5 so as to provide a more defined switching transistor level for transistor Q9. The output of the transistor circuit taken at the collector of Q9 is shown in FIG. 3F. The lag time to an on state after application of AC power is approximately 10 seconds. Turn off time after removal of AC power is approximately 3.5 milli seconds.

Referring to FIG. 4, the peripheral logic circuitry 30 is contained in the peripheral machine 13. The output of the trunk inhibit reset circuit 20 taken from the collector of transistor Q9 is fed, as a reset signal, to the peripheral logic circuitry 30. The outputs of circuitry 30 appear on the 1 to N lines as data inputs to the trunk line. When the reset signal from circuit 20 is at a ground potential it acts as a resetting function to all critical logic memory elements in the peripheral machine such that when the reset signal is removed (goes high) the peripheral machine will start operation in a predictable manner.

Transmission of the data input signals from the logic circuitry to the trunk lines is controlled by means of a plurality of AND gates. FIG. 5 illustrates one arrangement for gating the data signals to the trunk line under the control of the trunk inhibit reset circuit 20. The trunk line 18 is comprised of a plurality of conductors 33 which are connectable to one or more peripheral machines Each peripheral machine contains a trunk driver means 31 comprised of a plurality of gates 32. Each gate operates to connect one data input line to a particular trunk conductor under the control of the enable signal from transistor Q9. Any number of gates may be used with the number being dependent on the number of data signals to be connected. The gates are therefore labeled G1 to GN to indicate a selectable number which is dependent upon system usage.

When the output at transistor Q9 is of a positive level, the trunk drivers, G1 to GN, are enabled so that the data input signals, 1 to N, may be transmitted along the trunk lines. When the output of transistor Q9 is at a ground potential, the drivers are disabled, that is, the driver outputs are off and appear as essentially infinite impedance loads to the trunk line conductors. The trunk drivers receive their power directly from the trunk +5 volt supply.

While there has been disclosed what is considered to be the preferred embodiment of the invention, it will be manifest that many changes and modifications may be made therein without departing from the essential spirit of the invention. It is intended, therefore, in the annexed claims, to cover all such changes and modifications which fall within the true scope of the invention.

What is claimed is:

1. An inhibit and reset circuit for effectively connecting and disconnecting a peripheral machine from the trunk line of a computer processing unit when the peripheral machine unnaturally loads the trunk line, comprising in combination:

a. a peripheral machine power supply means for converting applied AC power into DC power;

b. means for sensing the applied AC power and for providing a sense signal, the level of which is indicative of the presence or absence of the applied AC power;

c. delay means for receiving said sense signal and for delaying the rise time of said sense signal for a selected period of time;

d. switch means responsive to said sense signal connected to said delay means for removing the delayed portion of said sense signal in the absence of AC power;

e. amplifier means for receiving and amplifying an impedance isolated sense signal;

f. buffer means for receiving the sense signal from said delay means and transmitting said signal to the amplifier means, and for providing impedance isolation between said switch means and said amplifier means;

g. switching means for receiving the amplified sense signal from said amplifier means and for connecting and disconnecting said peripheral machine to said trunk line in response to the level of the amplified sense signal, so as to connect said peripheral machine to said trunk line after AC power is applied to the peripheral machine power supply means for said selected period of time and to disconnect said peripheral machine from said trunk line immediately after AC power is removed from said power supply means.

2. The inhibit and reset circuit according to claim 1 wherein said amplifier and switching means are connected to receive DC power from said peripheral machine power supply and from said trunk line.

3. The inhibit and reset circuit according to claim 1 wherein said delay means is comprised of a resistor and a capacitor connected in series between said sensing means and a reference potential point, said sense signal being fed to said buffer means from the juncture point of said resistor and said capacitor.

4. The inhibit and reset circuit according to claim 1 wherein said switch means is connected across said capacitor so as to discharge said capacitor when said sense signal indicates an absence of AC power.

5. The inhibit and reset circuit according to claim 1 wherein said buffer means is a Darlington emitter follower stage.

6. An inhibit and reset circuit for effectively connecting and disconnecting a peripheral machine from the trunk line of a computer processing unit when the peripheral machine unnaturally loads the trunk line, comprising in combination:

a. a peripheral power supply means for converting applied AC power into DC power;

b. means for sensing the applied AC power and for providing a DC signal, when AC power is sensed;

c. delay means for receiving said DC signal and for delaying the rise time of said DC signal for a selected period of time;

d. switch means responsive to said DC signal for terminating the delayed DC signal from said delay means;

e. amplifier means for receiving and amplifying an impedance isolated delayed DC signal;

f. buffer means for receiving said delayed DC signal and transmitting said signal to the amplifier means, and for providing impedance isolation between said switch means and said amplifier means; and

g. means for receiving the amplified signal from said amplifier means and for connecting said peripheral machine to said trunk line in response to the amplified DC signal from said amplifier means, and for disconnecting said peripheral machine from said trunk line in the absence of an amplified DC signal

7. The inhibit and reset circuit according to claim **6** wherein said amplifier and switching means are connected to receive power from said peripheral machine's power supply and from said trunk line.

8. The inhibit and reset circuit according to claim **6** wherein said delay means is comprised of a resistor and a capacitor connected in series between said means for sensing and a reference potential point, said DC signal being fed to said buffer means from the juncture point of said resistor and said capacitor.

9. The inhibit and reset circuit according to claim **6** wherein said switch means is connected across said capacitor so as to discharge said capacitor when said DC signal indicates an absence of AC power.

10. The inhibit and reset circuit according to claim **6** wherein said buffer means is a Darlington emitter follower stage.

* * * * *