(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
29 June 2017 (29.06.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/112159 A1

(51) International Patent Classification:
H01L 25/065 (2006.01) *H05K 1/02* (2006.01)
H01L 23/522 (2006.01) *H01Q 1/52* (2006.01)
H01L 23/66 (2006.01)

(21) International Application Number:
PCT/US2016/062436

(22) International Filing Date:
17 November 2016 (17.11.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/979,185 22 December 2015 (22.12.2015) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 14/979,185 (CON)
Filed on 22 December 2015 (22.12.2015)

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) **Title**: WIRELESS IN-CHIP AND CHIP TO CHIP COMMUNICATION

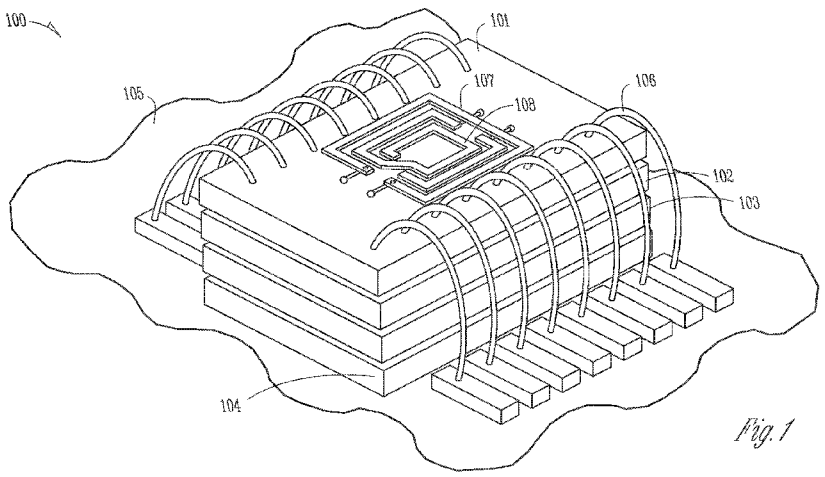


Fig. 1

(57) **Abstract**: Apparatus and methods are provided for wireless communications between integrated circuits or integrated circuit dies of an electronic system. In an example, an apparatus can include a first integrated circuit die including a plurality of integrated circuit devices, a second integrated circuit die including a second plurality of integrated circuit devices, and a conductor device configured to wirelessly receive a signal from the first integrated circuit die, to conduct the signal from a first end of an electrical conductor of the conductor device to a second end of the electrical conductor, and to wirelessly transmit the signal to the second integrated circuit die from the second end of the electrical conductor.

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WIRELESS IN-CHIP AND CHIP TO CHIP COMMUNICATION

[0001] This application claims the benefit of priority to U.S. Patent Application Serial No. 14/979,185, filed December 22, 2015, which is incorporated herein by reference in its entirety.

Technical Field

[0002] The disclosure herein relates generally to wireless communication and more particularly to inter and intra communications wireless communications.

Background

[0003] Electronics continue to be developed that are smaller yet more powerful computationally and functionally. Opportunities and challenges continue to arise that push the creative enterprise of electronic designers to provide small powerful electronic products that provide desired user functionality in a convenient package. Signal distribution can significantly impact integrated circuit and integrated circuit system design, especially as such circuits and system continue to physically shrink.

Brief Description of the Drawings

[0004] In the drawings, which are not necessarily drawn to scale, like numerals may describe similar components in different views. Like numerals having different letter suffixes may represent different instances of similar components. Some embodiments are illustrated by way of example, and not limitation, in the figures of the accompanying drawings in which:

[0005] FIG. 1 illustrates a stacked chip system with an existing wireless chip-to-chip communication concept.

[0006] FIG. 2 illustrates generally an example system for wireless inter-chip communications.

[0007] FIG. 3 illustrates generally an example system for wireless inter-chip communications.

[0008] FIG. 4 illustrates generally an example system for wireless intra-chip communications.

[0009] FIG. 5 illustrates generally a flowchart of an example method of operating an example apparatus according various examples of the present subject matter.

Detailed Description

[0010] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

[0011] Multiple chip circuits, meaning electronic packages that include more than one active die, have become a trend and look to continue being a platform for the future. Considerable design resources can be expended in stacking chips especially in designing connections using through silicon vias (TSVs). Side by side and opossum configurations can provide options for TSVs, however, the number of possible external connections per square millimeter as well as the number of possible traces per millimeter is limited due to limited design rules of substrates and boards as the die and accompanying package shrink. Design of side by side packages desire that the connection physical signal connections between be position as much as possible in the area between the two dies. One constraint that can interfere with this desire is area for electrostatic discharge (ESD) protection which is often used with solder interconnects. In Opossum stacking configurations, the area for connections and the routing capability on the die can be limited due to the opossum (daughter) die, mounted on the mother die.

[0012] The present inventors have recognized an elegant interconnect system that does not require ESD structures, does not consume much area per

connection on the package exterior and can provide better signal performance. In certain examples, the system can reduce the physical traces or interconnects between chips, as well as, between areas of a single chip while still exchanging the information that would have been communicated over such trances of interconnects.

[0013] FIG. 1 illustrates a stacked chip system 100 with an existing wireless chip-to-chip communication concept. The stacked chip system can include a plurality of chips 101, 102, 103, 104, stacked on each other and mounted on a printed circuit board 105. In some examples, connections to the printed circuit board 105 can include solder connection to the bottom chip 104 and wire bond connections 106 to exposed terminal of the top chip 101 or one of the other chips 102, 103 having exposed terminals. Flat loop antennas 107, 108 can be mounted on at least two of the chips. A pair of loop antennas 107, 108 mounted on a chip 101 can include an antenna 107 for transmission and an antenna 108 for reception. When the chips 101, 102, 103, 104 are stacked, the antennas 107, 108 over lay antennas (not shown) mounted on another chip of the stack such that signals can be exchanged between the chips. Such a system works well for stacked chips that have a size commensurate with the size required for the loop antennas. However, for side-by-side and opossum chip configurations, such a system can be impractical because the size constraints, and distance and orientation limitations of the antennas required to provide robust communications.

[0014] FIG. 2 illustrates generally an example system 200 for wireless inter-chip communications. In certain examples, the system can include a substrate such as a semiconductor or silicon-based substrate, a printed circuit board (PCB) 205 or another chip, a first integrated circuit package 201 and a second integrated circuit package 202. In certain examples, the first and second integrated circuit packages 201, 202 can physically connect to traces of the substrate or PCB 205 for example via solder balls 208 or wire bonds. In an example, a signal can be transferred wirelessly from the first integrated circuit package 201 to a trace 209 of the PCB 205. The signal can be conducted through the trace 209 of the PCB 205 to another point. At the other point, the signal can

be wirelessly transferred to the second integrated circuit package 202 using a pair of couplers 210. In certain examples, this wireless transfer of the signal can be achieved by the use of couplers 210, 211, 212, 213 that include coils or inductive lines. In certain examples, the trace 209 of the PCB can be directly coupled to a first coupler 211 at one end and a second coupler 212 at the other end. Such a system does not use ESD protection as such protection is typically used for solder trace connections to compensate or reduce line parasitic associated with the physically coupled wire media. In addition, a system according the present subject matter does not use additional amplifiers to drive the trace 209. Robust conduction over long trace runs can be accomplished using thicker or broader traces 209 of the PCB 205. In certain example, the couplers 211, 212 of the substrate or PCB 205 and the traces 209 can be referred to as a conductive device.

[0015] Transferring signals between chips as illustrated in FIG. 2 can significantly reduce package size as the number of external connections can be reduced and chip spacing can be more compact in some examples because of the reduction in trace routing real estate between the chips that can result from the decrease in external connections of each chip or integrated circuit package 201, 202. In some examples, the reduction in traces resulting from the reduction in external package connections can also result in a less complex PCB 205 such that the PCB 205 can be reduced in size, number of layers, and number of interlayer connections. In certain examples, more efficient use of the PCB can result from using areas under each of the first integrated circuit package 201 and the second integrated circuit package 202 for traces.

[0016] FIG. 3 illustrates generally an example system 300 for wireless inter-chip communications. In certain examples, the system 300 can include a substrate 305 such as a printed circuit board (PCB) or another chip, a first integrated circuit package 301, a second integrated circuit package 302, and a third integrated circuit package 303. In certain examples, the first and second integrated circuit packages 301, 302 can physically connect to traces of the substrate 305 for example via solder balls 308 or wire bonds. As illustrated, the third integrated circuit package 303 can be mounted to and underneath the first

integrated circuit package 301 such that the third integrated circuit package 303 is positioned between the first integrated circuit package 301 and the substrate 305. Such a mounting arrangement can be referred to as an opossum mount of the third integrated circuit package 303 to the first integrated circuit package 301. In such a mounting arrangement, the first integrated circuit package 301 can sometimes be referred to as a "mother chip" and the third integrated circuit package 303 can sometimes be referred to as a "daughter chip". In some designs, an opossum mount is disregarded the daughter chip consumes a significant amount of external connection area of the mother chip.

[0017] In certain examples, a signal can be transferred wirelessly from the third integrated circuit package 303 to a trace 309 of the substrate 305 using a first pair of couplers 310, 311, for example. The signal can be conducted through the trace 309 of the substrate 305 to another point. At the other point, the signal can be wirelessly transferred to the second integrated circuit package 302 using a second pair of couplers 312, 313. In certain examples, this wireless transfer of the signal can be achieved by the use of couplers 310, 311, 312, 313 that include coils or inductive lines. In certain examples, the trace 309 of the substrate 305 can be directly coupled to a first coupler 311 at one end and a second coupler 312 at the other end. Such a system does not use ESD protection as such protection is typically used for solder trace connections to compensate or reduce line parasitic associated with the physically coupled wire media. In addition, a system according the present subject matter does not use additional amplifiers to drive the trace 309. Robust conduction over long trace runs can be accomplished using thicker or broader traces of the substrate 305.

[0018] Transferring signals between chips as illustrated in FIG. 3 can significantly reduce package size as the number of external connections can be reduced and chip spacing can be more compact in some examples because of the reduction in trace routing real estate between the chips that can result from the decrease in external connections of each chip or integrated circuit package 301, 302. In some examples, the reduction in traces resulting from the reduction in external package connections can also result in a less complex PCB or substrate 305 such that the PCB or substrate 305 can be reduced in size, number of layers,

and number of interlayer connections. In certain examples, more efficient use of the PCB can result from using areas under each of the first and third integrated circuit packages 301, 303 and the second integrated circuit package 302 for traces.

[0019] FIG. 4 illustrates generally an example system 400 for wireless intra-chip communications. In certain examples, the system 400 can include a substrate 405 such as a printed circuit board (PCB) or another chip and a first integrated circuit package 401. In certain examples, the first integrated circuit package 401 can physically connect to traces of the substrate 405 for example via solder balls 408 or wire bonds. As illustrated, an optional second integrated circuit package 403 can be mounted to and underneath the first integrated circuit package 401 such that the second integrated circuit package 403 is positioned between the first integrated circuit package 401 and the substrate 405.

[0020] In certain examples, a signal can be transferred wirelessly from a first location 421 of the first integrated circuit package 401 to a trace 409 of the substrate 305. The signal can be conducted through the trace 409 of the substrate 405 to a second location 422 of the first integrated circuit package 401 and vice versa. At the first location 421, the signal can be wirelessly transferred between the first integrated circuit package 401 and the trace 409 using a first pair of couplers 410, 411. At the second location 422, the signal can be wirelessly transferred between the first integrated circuit package 401 and the trace 409 using a second pair of couplers 412, 413. In certain examples, this wireless transfer of the signal can be achieved by the use of couplers 410, 411, 412, 413 that include coils or inductive lines. In certain examples, the trace 409 of the substrate 405 can be directly coupled to a first coupler 411 at one end of the trace 409 and a second coupler 412 at the other end of the trace 409. Such a system does not use ESD protection as such protection is typically used for solder trace connections to compensate or reduce line parasitic associated with the physically coupled wire media. In addition, a system according the present subject matter does not use additional amplifiers to drive the trace 409. Robust conduction over long trace runs can be accomplished using thicker or broader traces of the substrate 405. Transferring signals between areas of the first

integrated circuit package 401 as illustrated in FIG. 4 can significantly reduce package size as the number of routings internal to the first integrated circuit package 401 can be reduced. In certain examples, including those of FIGS. 2-4, the substrate 205, 305, 405 can optionally include connections, such as solder balls 230, 330, 430, for electrically mounting to other components of a system.

[0021] In certain examples, pairs of couplers can be separated by an air gap. In some examples, first underfill 423 or a paste, such as a non-conductive paste, can be used to physically couple a pair of couplers 410, 411. In certain examples, underfill 423, 424 or paste material can be selected to enhance wireless coupling of the pairs of couplers 410, 411, 412, 413. In some examples, the underfill 423 or paste material can be applied to encapsulate the couplers 410, 411. In some examples, the underfill 424 or paste material can be sized and shaped to couple to a surface of each coupler of the pair of couplers 412, 413.

[0022] It is understood that other integrated circuit arrangement can realize benefits of the present subject matter. Such arrangements include those discussed and shown above as well as, but not limited to, providing a hybrid wireless/wired communication link between stacked integrated circuit devices, between mother and daughter integrated circuits, between mother and other side-by-side mounted integrated circuits, between different location of a daughter integrated circuit, between a first mother integrated circuit die and a second daughter integrated circuit die mounted to second mother integrated circuit die, etc. In certain examples, including the examples, of FIGS. 1-4, the hybrid wireless/wired signal system does not require ESD structures for the connections, the system has lower parasitics, and the chips and the substrate can have less routing layers.

[0023] FIG. 5 illustrates generally a flowchart of an example method 500 of operating an example apparatus according various examples of the present subject matter. At 501, a first coil can be electrically excited to provide or transmit a first wireless signal. The coil can be coupled to a first integrated circuit die. In certain examples, the coil, or inductor, can be coupled to a transmitter, receiver, transceiver or combination thereof of the first integrated circuit die. At 503, a second coil can wirelessly receive the first wireless signal

such as by inductive coupling, electromagnetic coupling, or combinations thereof to provide a second signal. At 505, the second signal can be electrically conducted via a wire, a conductive wire, a conductive trace of combination thereof directly to a third coil. For example, the second and third coil can be directly electrically coupled using a wire-type medium. At 507, the second signal can electrically excite the third coil to provide a second wireless signal. At 509, a fourth coil can wirelessly receive the second wireless signal such as by inductive coupling, electromagnetic coupling, or combinations thereof. The fourth coil can be coupled to a second integrated circuit die or a location of the first integrated circuit die remote from the location of the first coil. In certain examples, the fourth coil can be coupled to a second transmitter, receiver or transceiver and information can be passed between the first and second integrated circuit dies using the wireless link. Such signal communication can eliminate some external terminations of an integrated circuit system or some internal routings of an integrated circuit die such that smaller integrated packages can be realized as well as les complicated integrated circuit routing and less complicated printed circuit boards.

[0024] In the examples discussed above, routing signals wirelessly to the substrate can free up die space for additional circuitry or can reduce the overall size of a die. In some examples, routing signals wirelessly to the substrate can result in a less complex die as some signal routing and associated processing can be eliminated especially some cost intensive multi-layer interconnect redistribution processes.

Additional Examples and Notes

[0025] In Example 1, an apparatus can include a first integrated circuit die including a plurality of integrated circuit devices, a second integrated circuit die including a second plurality of integrated circuit devices, and a conductor device configured to wirelessly receive a signal from the first integrated circuit die, to conduct the signal from a first end of an electrical conductor of the conductor device to a second end of the electrical conductor, and to wirelessly

transmit the signal to the second integrated circuit die from the second end of the electrical conductor.

[0026] In Example 2, the first integrated circuit die of Example 1 optionally includes a first coil configured to inductively couple with a second coil at the first end of the conductive device.

[0027] In Example 3, the apparatus of any one or more of Examples 1-2 optionally includes a non-conductive material positioned between the first coil and the second coil, the non-conductive material configured to enhance mutual inductance between the first coil and the second coil compared to an air gap between the first coil and the second coil.

[0028] In Example 4, the second integrated circuit device of any one or more of Examples 1-3 optionally includes a third coil configured to inductively couple with a fourth coil at the second end of the conductive device.

[0029] In Example 5, the apparatus of any one or more of Examples 1-2 optionally includes a non-conductive material positioned between the third coil and the fourth coil, the non-conductive material configured to enhance mutual inductance between the third coil and the fourth coil compared to an air gap between the third coil and the fourth coil.

[0030] In Example 6, the first integrated circuit die and the second integrated circuit die of any one or more of Examples 1-5 optionally are the same die.

[0031] In Example 7, a printed circuit board optionally includes the conductive device of any one or more of Examples 1-6.

[0032] In Example 8, the conductive device of any one or more of Examples 1-7 optionally includes a trace of the printed circuit board.

[0033] In Example 9, the first integrated circuit die of any one or more of Examples 1-8 optionally includes a mother integrated circuit die, and the second integrated circuit die of any one or more of Examples 1-8 optionally includes a daughter integrated circuit die, the daughter integrated circuit die coupled to the mother integrated circuit die.

[0034] In Example 10, the first integrated circuit die of any one or more of Examples 1-9 optionally includes a daughter integrated circuit die, the daughter integrated circuit die coupled to a mother integrated circuit die.

[0035] In Example 11, the daughter integrated circuit die of any one or more of Examples 1-10 optionally is coupled face-up with the mother integrated circuit die.

[0036] In Example 12, the second integrated circuit die of any one or more of Examples 1-11 optionally is the mother integrated circuit die.

[0037] In Example 13, the apparatus of any one or more of Examples 1-12 optionally includes a semiconductor substrate that includes an electrically conductive portion of the conductor device.

[0038] In Example 14, a method can include electrically exciting a first coil coupled to a first integrated circuit die to provide a first wireless signal, receiving the first wireless signal at a second coil to provide a second signal, electrically conducting the second signal via a wire trace directly to a third coil, electrically exciting the third coil using the second signal to provide a second wireless signal, and wireless receiving the second wireless signal at a fourth coil, the fourth coil coupled to a second integrated circuit die.

[0039] In Example 15, the conducting the second signal of any one or more of Examples 1-14 optionally includes conducting the second signal via wire trace of a printed circuit board.

[0040] In Example 16, the second integrated circuit die of any one or more of Examples 1-15 optionally includes an area of the first integrated circuit die remote from a location of the first coil.

[0041] In Example 17, the first integrated circuit die of any one or more of Examples 1-16 optionally includes a daughter integrated circuit die, the daughter integrated circuit die coupled to a mother integrated circuit die.

[0042] In Example 18, the daughter integrated circuit die of any one or more of Examples 1-17 optionally is coupled face-up with the mother integrated circuit die.

[0043] In Example 19, the second integrated circuit die of any one or more of Examples 1-18 optionally is the mother integrated circuit die.

[0044] In Example 20, the first integrated circuit die includes of any one or more of Examples 1-19 optionally a mother integrated circuit die, and the second integrated circuit die of any one or more of Examples 1-19 optionally includes a daughter integrated circuit die,

[0045] In Example 21, the conducting the second signal of any one or more of Examples 1-20 optionally includes conducting the second signal via wire trace of a semiconductor substrate.

[0046] Each of these non-limiting examples can stand on its own, or can be combined with one or more of the other examples in any permutation or combination.

[0047] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the invention can be practiced. These embodiments are also referred to herein as "examples." Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[0048] In this document, the terms "a" or "an" are used, as is common in patent documents, to include one or more than one, independent of any other instances or usages of "at least one" or "one or more." In this document, the term "or" is used to refer to a nonexclusive or, such that "A or B" includes "A but not B," "B but not A," and "A and B," unless otherwise indicated. In this document, the terms "including" and "in which" are used as the plain-English equivalents of the respective terms "comprising" and "wherein." Also, in the following claims, the terms "including" and "comprising" are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the

terms "first," "second," and "third," etc. are used merely as labels, and are not intended to impose numerical requirements on their objects.

[0049] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description. The Abstract is provided to comply with 37 C.F.R. §1.72(b), to allow the reader to quickly ascertain the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather, inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are legally entitled.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a first integrated circuit die including a plurality of integrated circuit devices;

a second integrated circuit die including a second plurality of integrated circuit devices; and

a conductor device configured to wirelessly receive a signal from the first integrated circuit die, to conduct the signal from a first end of an electrical conductor of the conductor device to a second end of the electrical conductor, and to wirelessly transmit the signal to the second integrated circuit die from the second end of the electrical conductor.

2. The apparatus of claim 1, wherein the first integrated circuit die includes a first coil configured to inductively couple with a second coil at the first end of the conductive device.

3. The apparatus of claim 2, including a non-conductive material positioned between the first coil and the second coil, the non-conductive material configured to enhance mutual inductance between the first coil and the second coil compared to an air gap between the first coil and the second coil.

4. The apparatus of claim 2, wherein the second integrated circuit device includes a third coil configured to inductively couple with a fourth coil at the second end of the conductive device.

5. The apparatus of claim 4, including a non-conductive material positioned between the third coil and the fourth coil, the non-conductive material configured to enhance mutual inductance between the third coil and the fourth coil compared to an air gap between the third coil and the fourth coil.

6. The apparatus of claim 1, wherein the first integrated circuit die and the second integrated circuit die are the same die.

7. The apparatus of claim 1, wherein a printed circuit board includes the conductive device.

8. The apparatus of claim 7, wherein the conductive device includes a trace of the printed circuit board.

9. The apparatus of claim 1, wherein the first integrated circuit die includes a mother integrated circuit die, and the second integrated circuit die includes a daughter integrated circuit die, the daughter integrated circuit die coupled to the mother integrated circuit die.

10. The apparatus of claim 1, wherein the first integrated circuit die includes a daughter integrated circuit die, the daughter integrated circuit die coupled to a mother integrated circuit die.

11. The apparatus of claim 10, wherein the daughter integrated circuit die is coupled face-up with the mother integrated circuit die.

12. The apparatus of claim 10, wherein the second integrated circuit die is the mother integrated circuit die.

13. The apparatus of claim 1, including a semiconductor substrate that includes an electrically conductive portion of the conductor device.

14. A method comprising:

electrically exciting a first coil coupled to a first integrated circuit die to provide a first wireless signal;

receiving the first wireless signal at a second coil to provide a second signal;

electrically conducting the second signal via a wire trace directly to a third coil;

electrically exciting the third coil using the second signal to provide a second wireless signal; and

wireless receiving the second wireless signal at a fourth coil, the fourth coil coupled to a second integrated circuit die.

15. The method of claim 14, wherein conducting the second signal includes conducting the second signal via wire trace of a printed circuit board.

16. The method of claim 14, wherein the second integrated circuit die includes an area of the first integrated circuit die remote from a location of the first coil.

17. The method of claim 14, wherein the first integrated circuit die includes a daughter integrated circuit die, the daughter integrated circuit die coupled to a mother integrated circuit die.

18. The method of claim 17, wherein the daughter integrated circuit die is coupled face-up with the mother integrated circuit die.

19. The method of claim 17, wherein the second integrated circuit die is the mother integrated circuit die.

20. The method of claim 14, wherein the first integrated circuit die includes a mother integrated circuit die, and the second integrated circuit die includes a daughter integrated circuit die,

21. The method of claim 14, wherein conducting the second signal includes conducting the second signal via wire trace of a semiconductor substrate.

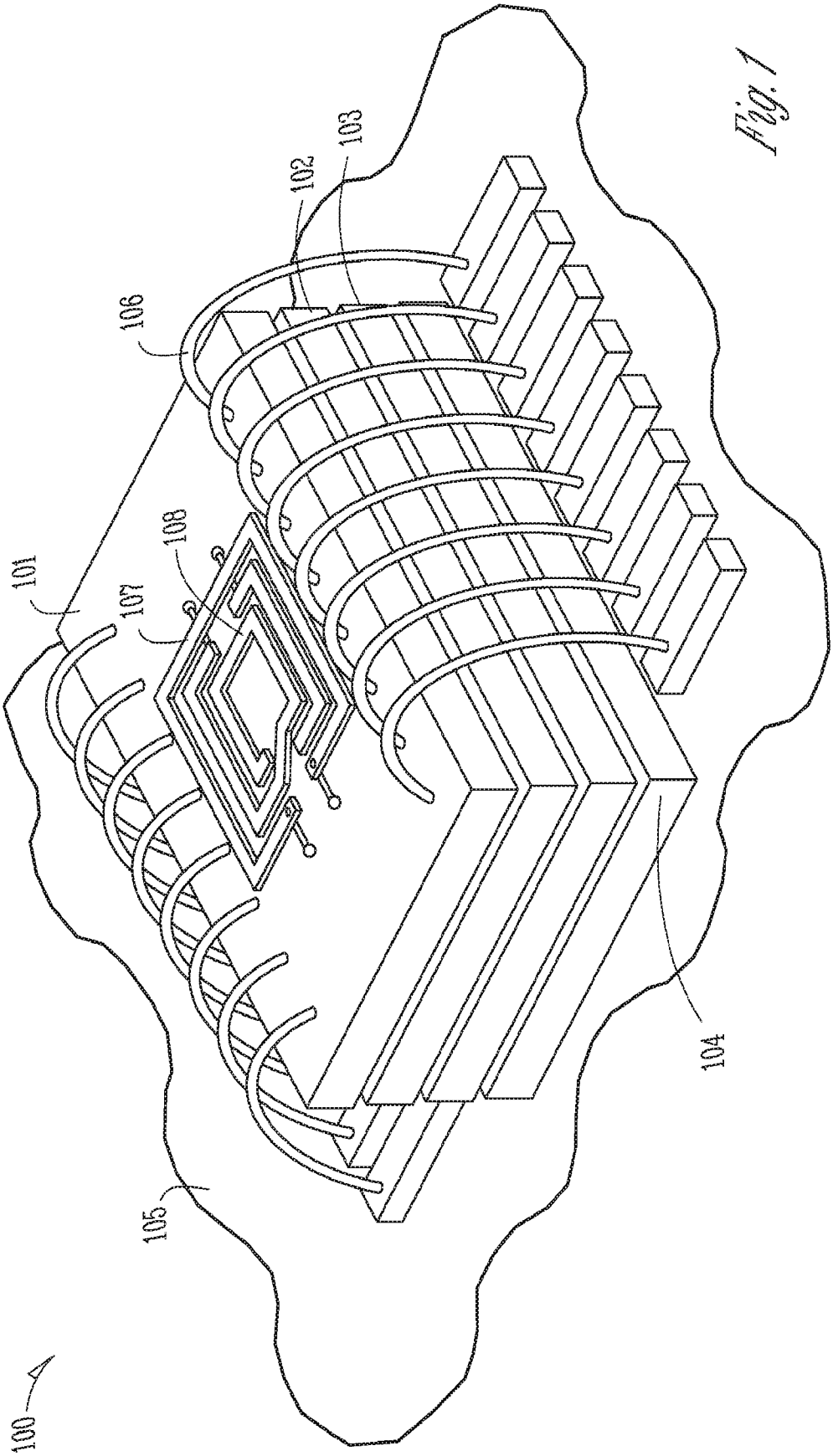


Fig. 1

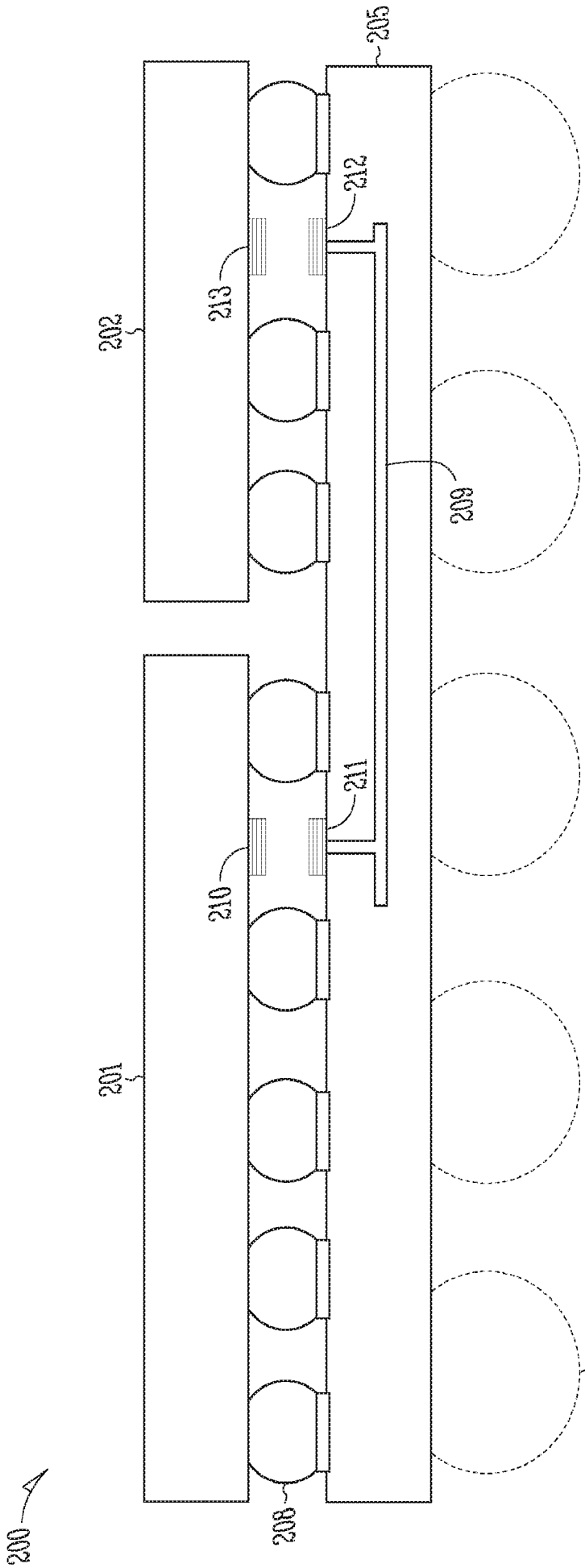


Fig. 2

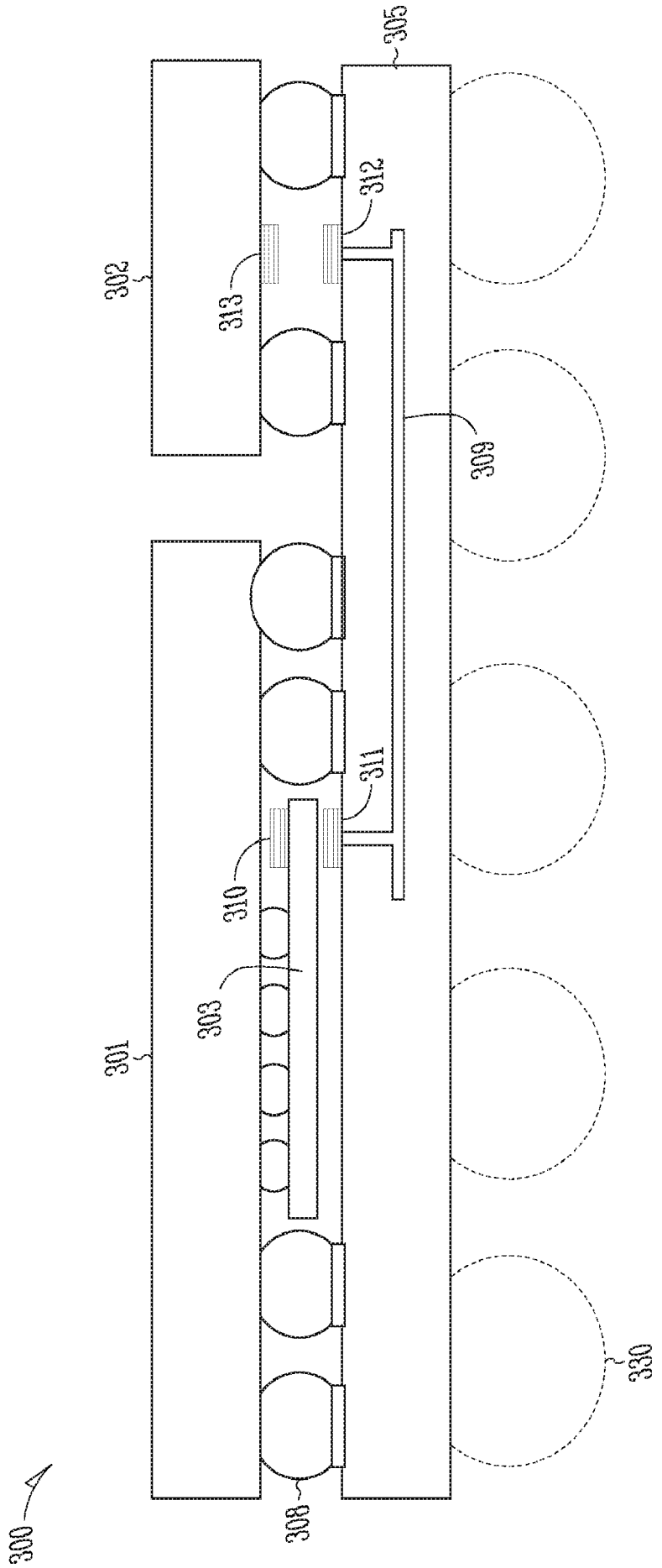


Fig. 3

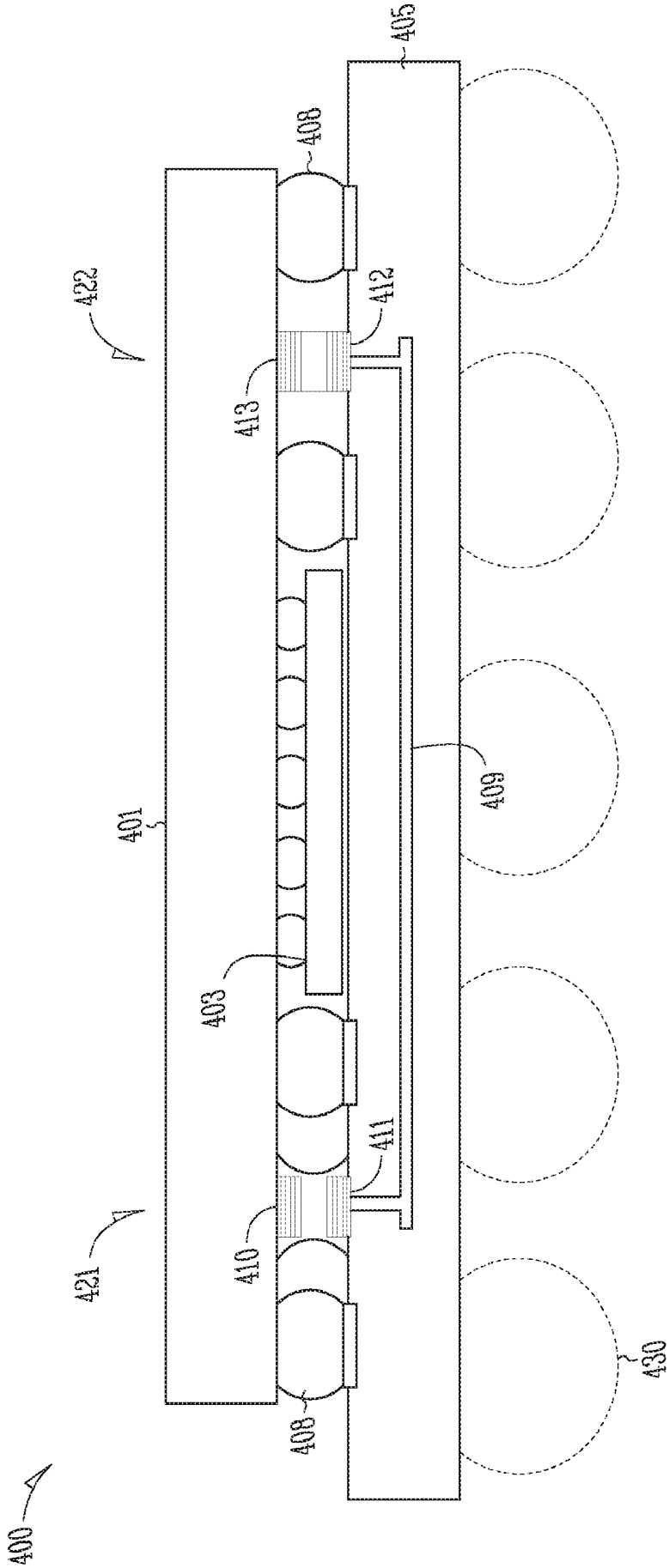


Fig. 4

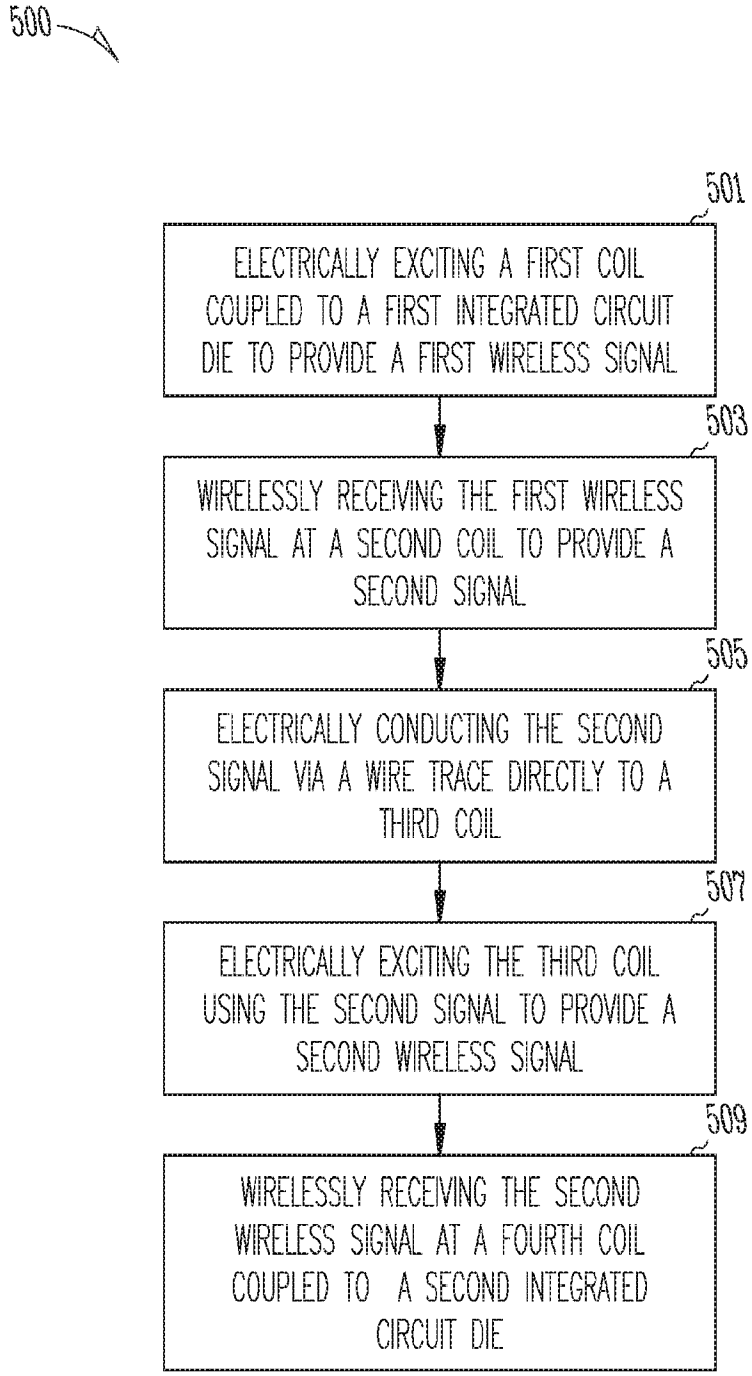

500
501
ELECTRICALLY EXCITING A FIRST COIL COUPLED TO A FIRST INTEGRATED CIRCUIT DIE TO PROVIDE A FIRST WIRELESS SIGNAL
503
WIRELESSLY RECEIVING THE FIRST WIRELESS SIGNAL AT A SECOND COIL TO PROVIDE A SECOND SIGNAL
505
ELECTRICALLY CONDUCTING THE SECOND SIGNAL VIA A WIRE TRACE DIRECTLY TO A THIRD COIL
507
ELECTRICALLY EXCITING THE THIRD COIL USING THE SECOND SIGNAL TO PROVIDE A SECOND WIRELESS SIGNAL
509
WIRELESSLY RECEIVING THE SECOND WIRELESS SIGNAL AT A FOURTH COIL COUPLED TO A SECOND INTEGRATED CIRCUIT DIE

Fig. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/062436

A. CLASSIFICATION OF SUBJECT MATTER

H01L 25/065(2006.01)i, H01L 23/522(2006.01)i, H01L 23/66(2006.01)i, H05K 1/02(2006.01)i, H01Q 1/52(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 25/065; H01L 29/00; H01L 21/768; H01L 23/48; H01L 33/00; H05K 7/00; G02B 6/12; H01L 23/522; H01L 23/66; H05K 1/02; H01Q 1/52

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: wireless, coupling, conductor, signal, coil

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0267084 A1 (CHRISTOPH BILGER et al.) 29 October 2009 See paragraph [0031], claim 13 and figure 6.	1-21
A	US 2010-0061056 A1 (DAMION SEARLS et al.) 11 March 2010 See claims 1-2, 10 and figures 1A-1C.	1-21
A	US 2013-0334707 A1 (JIAMIAO TANG et al.) 19 December 2013 See paragraphs [0012]-[0017], claims 1, 4-5 and figures 1-3.	1-21
A	US 2011-0256663 A1 (ERNEST E. HOLLIS) 20 October 2011 See paragraphs [0086]-[0088] and figures 3a-3b.	1-21
A	US 2015-0130534 A1 (INTEL CORPORATION) 14 May 2015 See paragraph [0037], claims 1-4 and figure 7.	1-21

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2017 (28.02.2017)	**28 February 2017 (28.02.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/062436

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