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(54) Title: VERTICAL DEFLECTING TILTING MICRO-MIRROR FOR A SPATIAL LIGHT MODULATOR IC AND METHOD TO FABRICATE SUCH A DEVICE

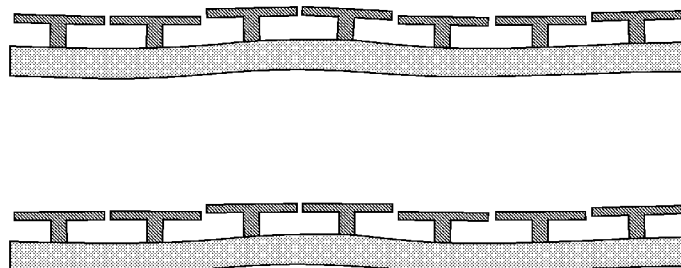


FIG. 2

(57) Abstract: The present invention relates to the replacement of optical masks by a spatial-light modulator (SLM) and a method for manufacturing said SLM. An SLM is a series or grid of mirrors on a substrate, such as silicon, used to reflect light in a predetermined manner.



Vertical deflecting tilting micro-mirror for a spatial light modulator IC and method to fabricate such a device

FIELD OF THE INVENTION

The present invention relates to the replacement of optical masks by a spatial-light modulator (SLM) and a method for manufacturing said SLM. An SLM is a series or
5 grid of mirrors on a substrate, such as silicon, used to reflect light in a predetermined manner.

BACKGROUND OF THE INVENTION

Optical Maskless Lithography (OML) is described in various documents, e.g.
10 “Optical Maskless Lithography for Fast and Low-Cost Design to Wafer”, Kars Troost, 2004, and “OML: optical maskless lithography for economic design prototyping and small-volume production”, T. Sandstrom, A. Bleeker, J.D. Hintersteiner, K. Troost, J. Freyer, K. van der Mast, PROCEEDINGS- SPIE pp.777—787 (2004). It is an alternative method for IC
15 manufacturing, avoiding the use of (more-and-more) expensive reticles for prototypes or low-volume production.

One way to do OML is by replacing the pattern that is usually in chrome on a quartz plate (fixed-pattern reticle) by a pattern created by tilting micro-mirrors. Although designed for a completely different application, such a grid of tilting mirrors will resemble a Digital Light Processing (DLP) chip as is used for e.g. projection displays. Such displays are
20 disclosed in “A MEMS-Based Projection Display”, Peter F. Van Kessel, Larry J. Hornbeck, Robert E. Meier, Michael R. Douglass, PROCEEDINGS OF THE IEEE, VOL. 86(8), pp.1687—1704 (1998). The specifications for OML, however, are much more stringent: the image created on the IC-surface consists of an interference pattern of monochromatic, coherent light reflected from the micro-mirrors. Hence, it is very sensitive to minor shifts of
25 mirror positions.

“Si:Ge: An attractive material for post-CMOS processing of MEMS”, Sherif Sedky, Microelectronic Engineering, Vol 84 (2007), 2491-2500 and “Microactuators and their technologies”, Ernst Thielicke, Ernst Obermeier, Mechatronics Vol 10 (2000) 431-455 disclose some microcomponents.

US2006077531 describes MEMS mirror arrays monolithically integrated with CMOS control electronics. The MEMS arrays include polysilicon or polysilicon-germanium components that are mechanically superior to metals used in other MEMS applications, but that require process temperatures not compatible with conventional CMOS technologies.

5 CMOS circuits used with the polysilicon or polysilicon-germanium MEMS structures use interconnect materials that can withstand the high temperatures used during MEMS fabrication. These interconnect materials include doped polysilicon, polycides, and tungsten metal.

WO2004086744 describes Micro-Electro-Mechanical Systems (MEMS)
10 actuators with hidden combs and hinges. The ability to hide the combs renders the actuators useful in digital micro-mirror devices. Comb actuators provide increased torque, which facilitates the use of stiffer, less fragile hinge structures. Also important, comb actuators do not require mechanical stops to define stable states, and thus avoid problems associated with physical contact. The actuators are infinitely variable through a range of angles.

15 US6861277 discloses a method of forming a MEMS device includes depositing a conductive material on a substructure, forming a first sacrificial layer over the conductive material, including forming a substantially planar surface of the first sacrificial layer, and forming a first element over the substantially planar surface of the first sacrificial layer, including communicating the first element with the conductive material through the
20 first sacrificial layer. In addition, the method includes forming a second sacrificial layer over the first element, including forming a substantially planar surface of the second sacrificial layer, forming a support through the second sacrificial layer to the first element after forming the second sacrificial layer, including filling the support, and forming a second element over the support and the substantially planar surface of the second sacrificial layer. As such, the
25 method further includes substantially removing the first sacrificial layer and the second sacrificial layer, thereby supporting the second element relative to the first element with the support.

US5497262 discloses an improved support post (16, 23, 25) for micro-mechanical devices (10). A via (34a) that defines the outer surface of the support post (16) is
30 etched into a spacer layer (34). An oxide layer (41) is conformally deposited over the spacer layer (34) and into the via (34a), and then etched back to the top surface of the spacer layer (34), leaving a sidewall ring (23a) on the inner surface of the via (34a). Next, a metal layer (61) is deposited over the spacer layer (34) and into the via (34a) so as to cover the sidewall ring (23a). This metal layer (61) is then etched to form a support post stem (23) inside the via

(34a). The spacer layer (34) is removed, leaving the support post stem (23) and a sidewall ring (23a) around the stem (23).

A straightforward implementation of a spatial light modulator is to put the grid of micro-mirrors (typically $8 \times 8 \mu\text{m}^2$ or smaller each) on top of a CMOS substrate for electronically controlling the mirrors. Ideally these micro-mirrors form a flat, reflecting, surface when put in the neutral position, see e.g. Fig. 1. Although modern CMOS processes, because of the Chemical Mechanical Polishing (CMP) in the back-end, are reasonably flat, there will always remain some non-flatness on the final top surface. This causes the micro-mirrors to deviate from the ideal mirror-plane. See Fig. 2.

The above devices do not provide a perfectly flat plane supporting mirrors. With only two electrodes one can not correct for this height variations in the plane.

SUMMARY OF THE INVENTION

The present invention relates to an integrated device comprising a grid of mirrors, wherein the grid comprises more than 100×100 mirrors, preferably more than 500×500 mirrors, more preferably more than 1000×1000 mirrors, even more preferably more than 2500×2500 mirrors, each mirror comprising a substantially flat surface area, and an electronic controlling unit. This device overcomes the problems mentioned above. Thereby, virtually no problems exist in using the device as a mirror, a mask or the like, obtaining a high quality projection.

One may now correct for this height variations in the plane.

Important advantages are that:

- If a bridge is provided, it is not only a point of suspension, but an electronically controlled movable suspension point;
- Each bridge comprises an additional electrode, with which the bridge may be adapted in height. The tilting of the mirror takes place by using the other two mirrors, which are also present;
- The exact form of the electrodes may be flat, but may also be provided as a comb structure.

DETAILED DESCRIPTION OF THE INVENTION

Thus, the presented invention provides a method to compensate for the non-flatness of the (CMOS-) substrate, which lies in the order of 0 to 300 nm, i.e. being extremely flat, over an area of at least 25x25 mm² for the starting material and, depending on the exact design, can result in step height differences between 0 and 250 nm over a distance of a few mm after full CMOS processing. By adding an additional degree of freedom to each individual micro-mirror, moving in the vertical direction perpendicular to the surface, the deviation from the ideal (flat) mirror-plane can be corrected, see Fig. 3. This is the major claim of the presented invention disclosure.

Also envisaged are application wherein the mirror is convex or concave, e.g. for applications wherein many mirrors are used to provide a single projection.

For this invention we describe two embodiments, both building upon the current micro-mirror architecture shown in Fig. 4. In the first implementation, see Fig. 5, the two anchor points of each micro-mirror are placed together on top of one flexible bridge. In the second implementation, see Fig. 6, each anchor-point is placed on a separate flexible bridge. These two implementation proposals are just examples, one could easily think of slightly different schemes to come to the same result.

In the current implementation the micro-mirror is tilted with an electrostatic force, by applying different voltage differences between the 2 electrodes (see Fig. 4) and the micro-mirror. In the proposed new implementations a 3rd electrode is introduced to move the flexible bridge in the vertical direction. A more practical implementation could be to integrate the 3rd electrode functionally with the 2 tilting electrodes: the voltage difference between the 2 electrodes will define the tilt-angle, while the average voltage difference between both electrodes and the mirror will define the height correction. This will eliminate the need for a separate (3rd) electrode.

The main difference between the current implementation and the first proposed new implementation is that the anchor points in this new configuration are no longer shared between neighboring mirrors. For the second proposed new implementation the anchor-points are again shared between neighboring micro-mirrors. See also Fig. 7 for more detail.

As such, a grid of mirrors, which are adjustable in height, may also be used to provide a phase-shift image, using monochromatic, phase-coherent light. Optionally as such

an extra parameter is provided to improve resolution in an Optical Maskless Lithography (OML) tool.

The present invention is further elucidated by the following Figures and examples, which are not intended to limit the scope of the invention. The person skilled in the art will understand that various embodiments may be combined.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1. Schematic top view (top) and cross section (bottom) of an ideal section of a mirror grid.

Fig. 2. Schematic cross section of a more realistic mirror grid (from Fig. 1).

Fig. 3. Schematic cross section of the same mirror grid as in Fig. 2, but this time with the mirrors placed on an additional bridge for height compensation.

Fig. 4. Schematic top-view (left) and cross section (right) of the current micro-mirror design.

Fig. 5. Schematic top-view (left) and cross section (right) of a micro-mirror design according to proposal 1.

Fig. 6. Schematic top-view (left) and cross section (right) of a micro-mirror design according to proposal 2.

Fig. 7. Schematic top-view of a 2x2 mirror grid, showing the common SiGe vias in the different schemes.

Fig. 8. Schematic processing steps. See text for details.

DETAILED DESCRIPTION OF THE DRAWINGS

Fig. 1. Schematic top view (top) and cross section (bottom) of an ideal section of a mirror grid. A perfectly flat substrate results in a perfectly flat mirror-surface in the neutral position.

Fig. 2. Schematic cross section of a more realistic mirror grid (from Fig. 1). In the neutral position (no bias), the surface of the mirrors will follow the (non-flat) profile of the substrate (top). The individual mirror may be put back in a horizontal position by applying e.g. some bias voltage. However, this may result in step-height differences between neighboring mirrors (bottom).

Fig. 3. Schematic cross section of the same mirror grid as in Fig. 2, but this time with the mirrors placed on an additional bridge for height compensation. In neutral position the mirror-surface will still follow the (non-flat) profile of the substrate (top). By applying e.g. a voltage bias to the individual mirrors, they may be put in horizontal position (middle). By applying an additional bias to the flexible bridge, the step-height difference can be compensated.

Fig. 4. Schematic top-view (left) and cross section (right) of the current micro-mirror design. The mirror is suspended between 2 anchor-points connected to the CMOS substrate. Its tilt-angle can be controlled by means of 2 electrodes on either side of the tilting axis (visible in cross section B-B').

Fig. 5. Schematic top-view (left) and cross section (right) of a micro-mirror design according to proposal 1. The mirror is suspended between 2 anchor-points connected to a bridge, which in turn is connected to the CMOS substrate. The tilt-angle can be controlled in the same manner as the original design (Fig. 4), by means of 2 electrodes on either side of the tilting axis. A 3rd electrode, located directly underneath the bridge, controls the bridge height. (all 3 electrodes are visible in both cross section B-B' and C-C').

Fig. 6. Schematic top-view (left) and cross section (right) of a micro-mirror design according to proposal 2. The mirror is suspended between 2 anchor-points, each connected to a separate bridge (shared with a neighboring mirror), which in turn is connected to the CMOS substrate. The tilt-angle can be controlled in the same manner as the original design (Fig. 4), by means of 2 electrodes on either side of the tilting axis. A 3rd and 4th electrode, located directly underneath the bridge, controls the bridge height.

Fig. 7. Schematic top-view of a 2x2 mirror grid, showing the common SiGe vias in the different schemes. Current scheme (top-left, see also Fig. 4), proposal-1 (top-right, see also Fig. 5) and proposal-2 (bottom-left, see also Fig. 6).

Fig. 8. Schematic processing steps. In Fig. 8 a schematic view is presented of a proposed processing sequence (equal for both proposed new implementations):

1. The starting material is a CMOS substrate, including all circuit elements and interconnect-levels needed to operate the chip. The first step in the micro-mirror processing is to cover the CMOS with a protective layer, make via's to the top-most interconnect-level of the CMOS circuitry, and define the electrodes.
2. Next a sacrificial layer (usually some sort of silicon-oxide) is deposited on top of the electrodes and planarized.

3. In this sacrificial layer the first via is made, which will contact the flexible bridge.

4. The flexible bridge is deposited and patterned.

5. Again a sacrificial layer, of the same material as in step 2, is deposited and planarized.

6. In this second sacrificial layer a second via is defined, which will connect the bridge with the micro-mirror.

7. On top of the second via the micro-mirror is deposited and patterned.

8. In the final step the bridge and the micro-mirror are released by selectively

10 removing the sacrificial layers from between the structures. (In case of sacrificial silicon oxide this can for instance be done with a wet hydrofluoric (HF) etch or a vapor-HF etch). The requirements of the protective coating, deposited in step 1, strongly depend on which material is used as sacrificial layer, and which etch is being used to remove it.

add I. For the present implementation, without the flexible bridges, step 2, 3, and 4
15 are skipped

add II. In order to have a full release of all the moveable structures (flexible bridges and micro-mirrors) care should be taken in the layout of these structures that all sacrificial are reachable during the final etch.

CLAIMS:

1. Integrated device comprising a grid of mirrors, wherein the grid comprises more than 100x100 mirrors, preferably more than 500x500 mirrors, more preferably more than 1000x1000 mirrors, even more preferably more than 2500x2500 mirrors, each mirror comprising a substantially flat surface area, and an electronic controlling unit.

5

2. Integrated device according to claim 1, wherein the surface area has a non-flatness of less than 300 nm relative taken over an area of 25x25 mm², preferably a non-flatness of less than 100 nm, or wherein the surface area forms a convex mirror, or wherein the surface area forms a concave mirror.

10

3. Integrated device according to claim 1 or claim 2, wherein the surface area is rectangular, hexagonal, octagonal, diamond or circular, preferably rectangular or hexagonal, more preferably square, or combinations thereof, having a surface area of 10-1000 μm².

15

4. Integrated device according to any of claims 1-3, wherein each mirror comprises one or more flexible bridges, which one or more bridges are adjustable to compensate for height differences between mirrors.

20

5. Integrated device according to any of claims 1-4, further comprising a substrate, such as a CMOS substrate, wherein each mirror comprises one or more vias, preferably SiGe vias, wherein the vias form anchor points for the mirror, each via being connected to an electrode, which electrode in operation controls the position of the via and thereby the position of the mirror.

25

6. Integrated device according to any of claims 1-5, wherein mirrors are formed from SiGe.

7. Integrated device according to any of claims 4-6, wherein each bridge comprises one or more bridge vias, wherein the bridge vias form anchor points for the bridge, the bridge via being thereby adjustable to compensate for height differences between mirrors.

5 8. Integrated device according to any of claims 4-7, wherein each bridge comprises SiGe.

9. Integrated device according to any of claims 4-8, wherein each mirror via is connected to a separate bridge or wherein each mirror via is connected to a bridge shared by
10 two or more adjacent mirrors.

10. Method for manufacturing an integrated device according to any of claims 1-9, comprising the steps of:

- providing a substrate, preferably a CMOS substrate,
- 15 - optionally protecting the substrate,
- optionally depositing a sacrificial layer, preferably a SiO₂ layer,
- forming vias in said substrate,
- forming electrodes on the vias,
- depositing a dielectric layer,
- 20 - forming vias in the dielectric layer, being connected to the electrodes, preferably being SiGe vias,
- optionally forming a bridge, preferably a SiGe bridge,
- optionally depositing a second dielectric layer,
- optionally forming vias in the second dielectric layer, being connected to the
25 bridge, preferably being SiGe vias,
- depositing a mirror, preferably a SiGe mirror,
- optionally etching the second dielectric layer, and
- etching the first dielectric layer.

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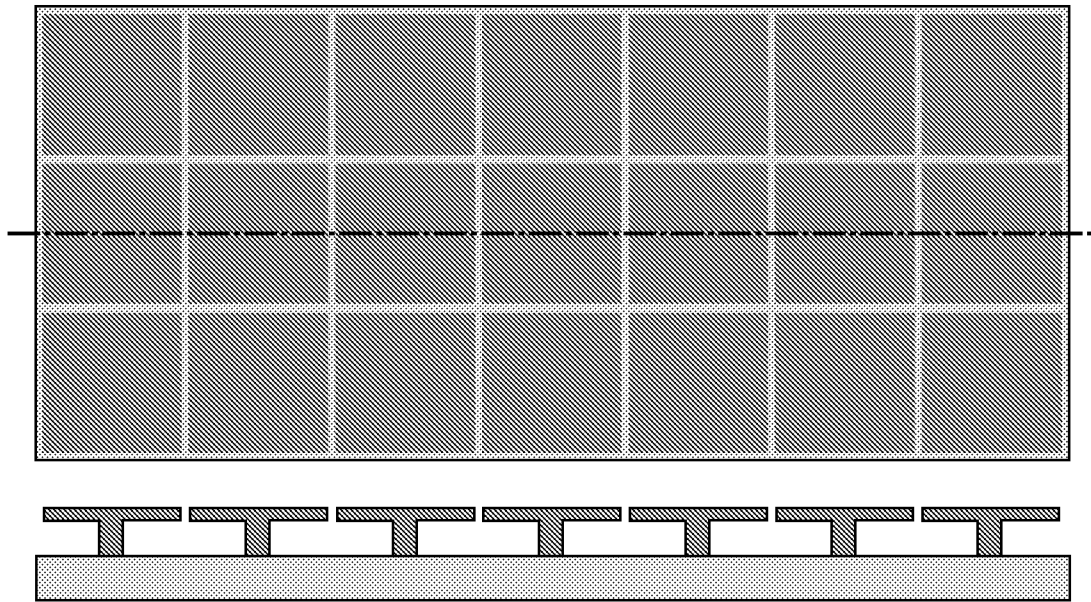


FIG. 1

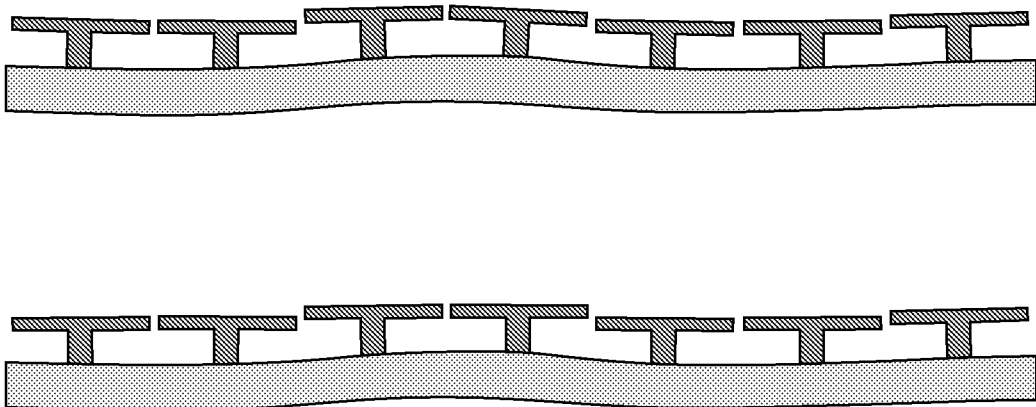


FIG. 2

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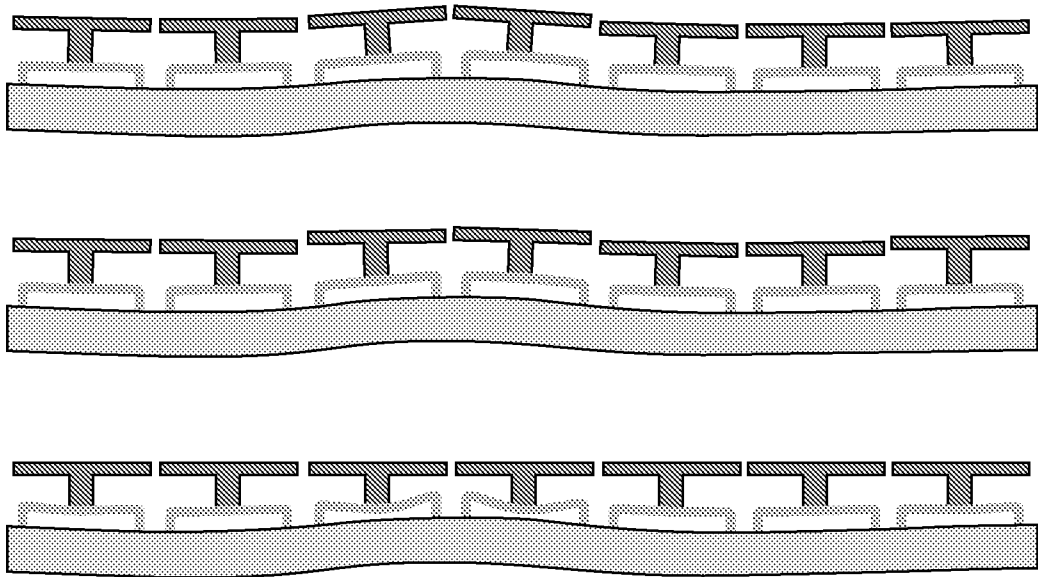


FIG. 3

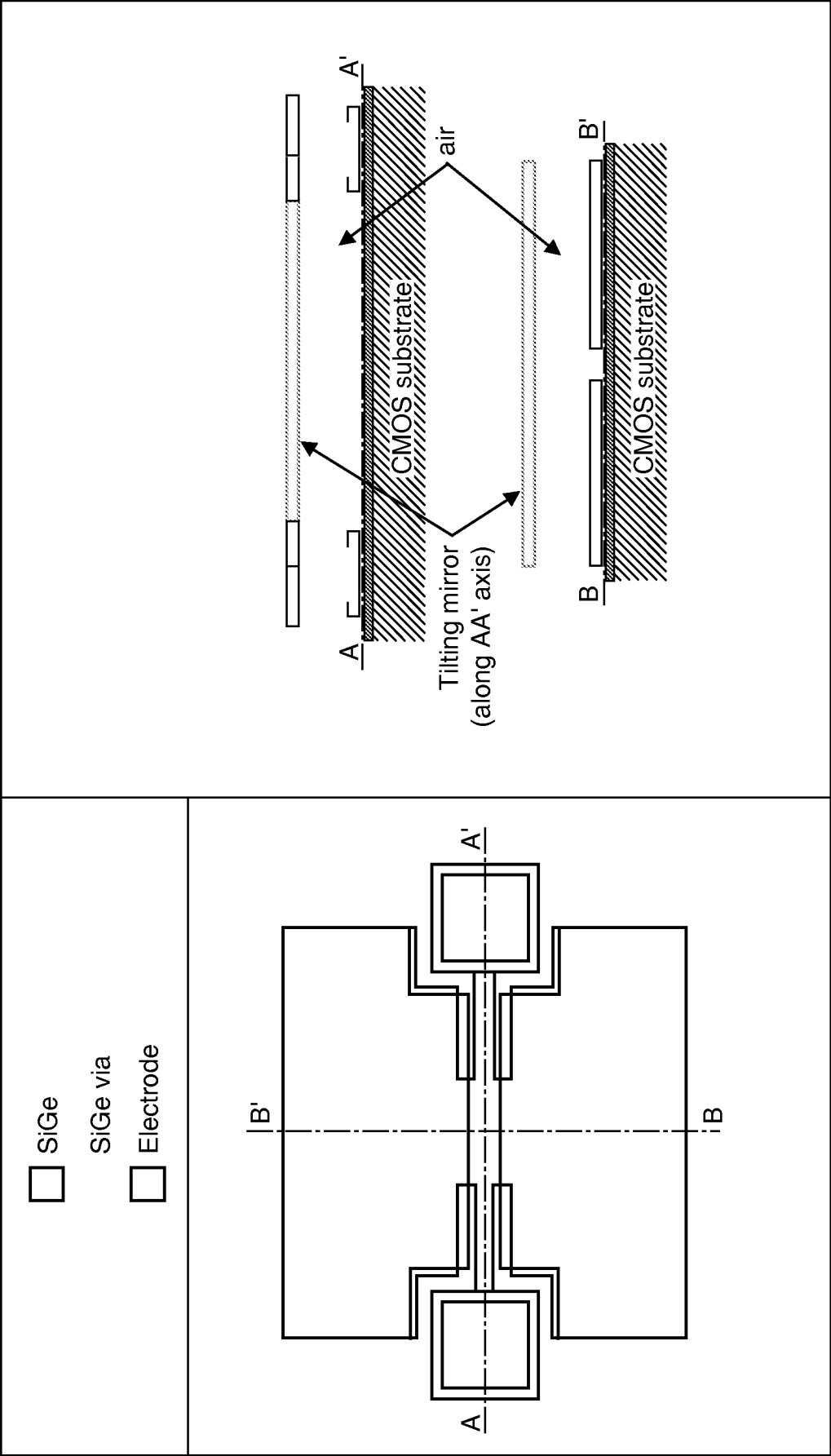


FIG. 4

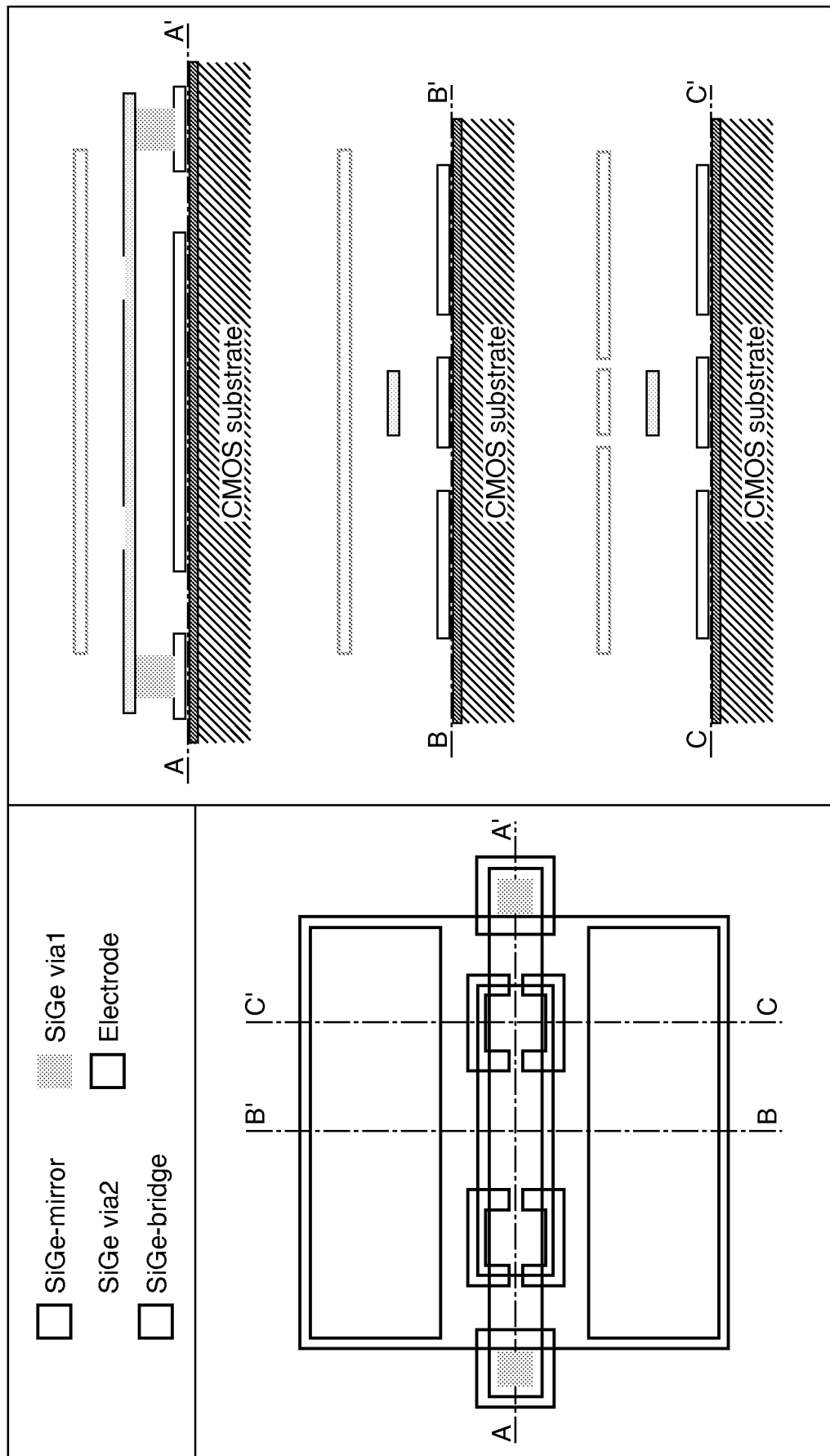


FIG. 5

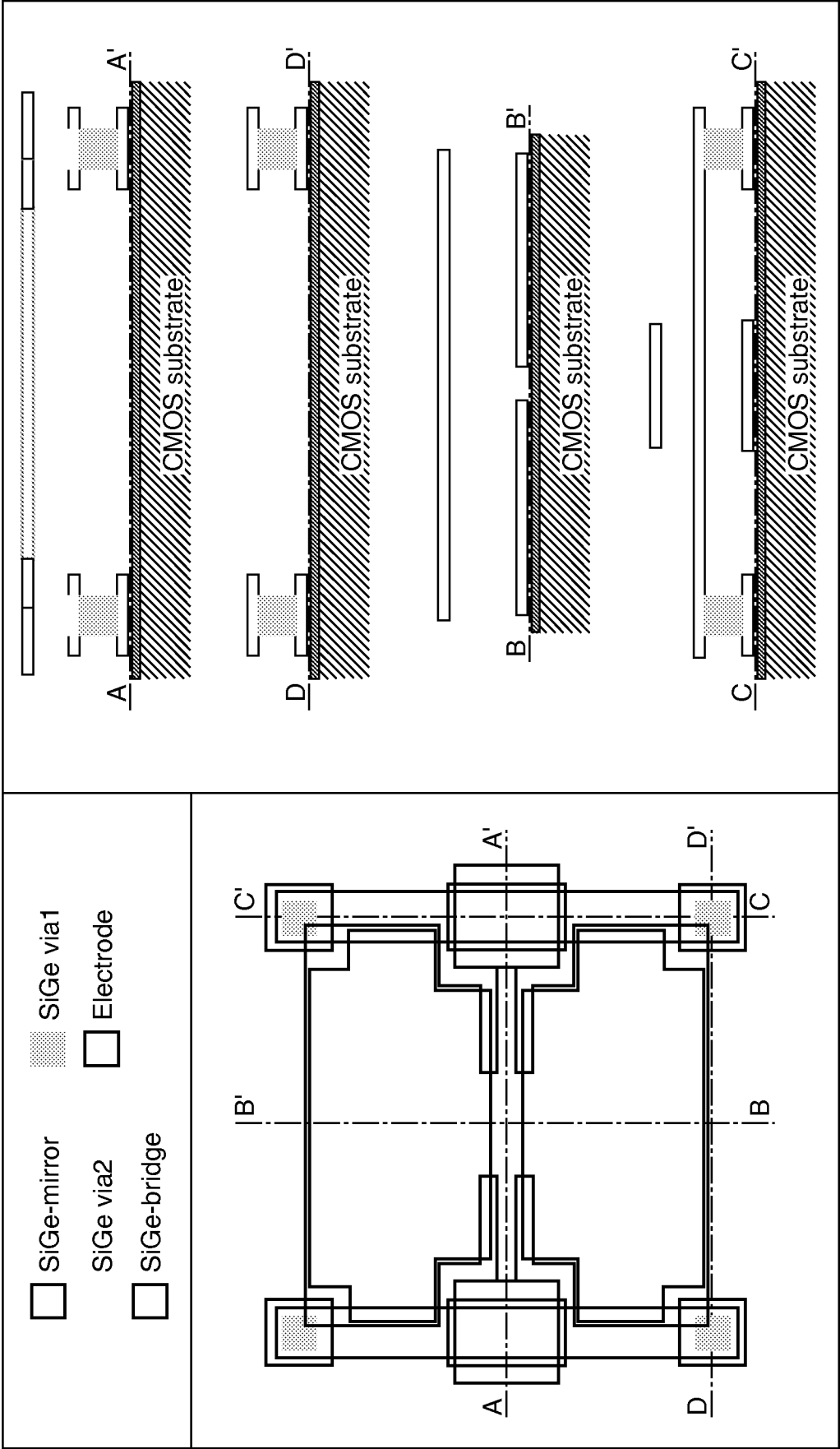


FIG. 6

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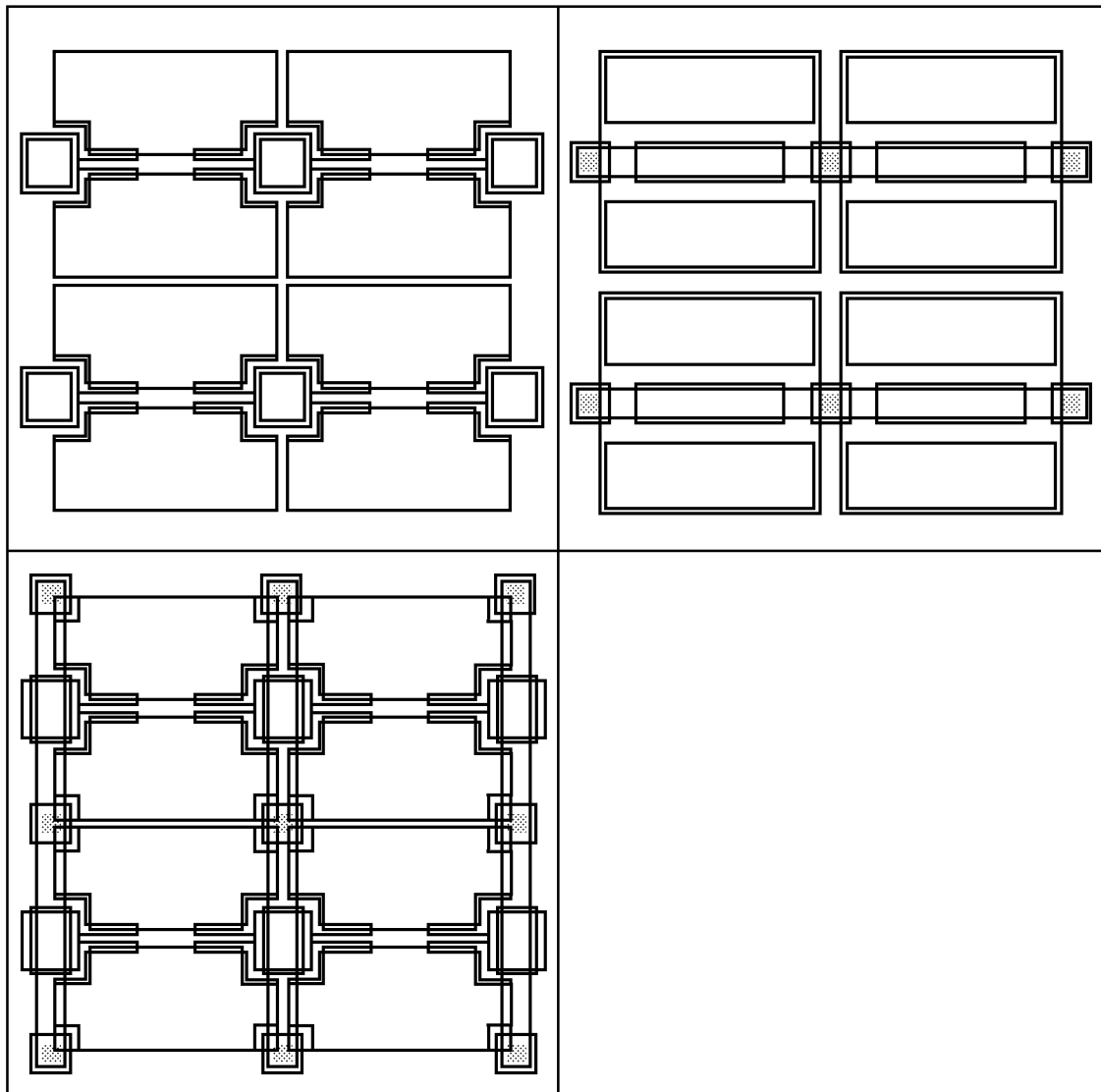


FIG. 7

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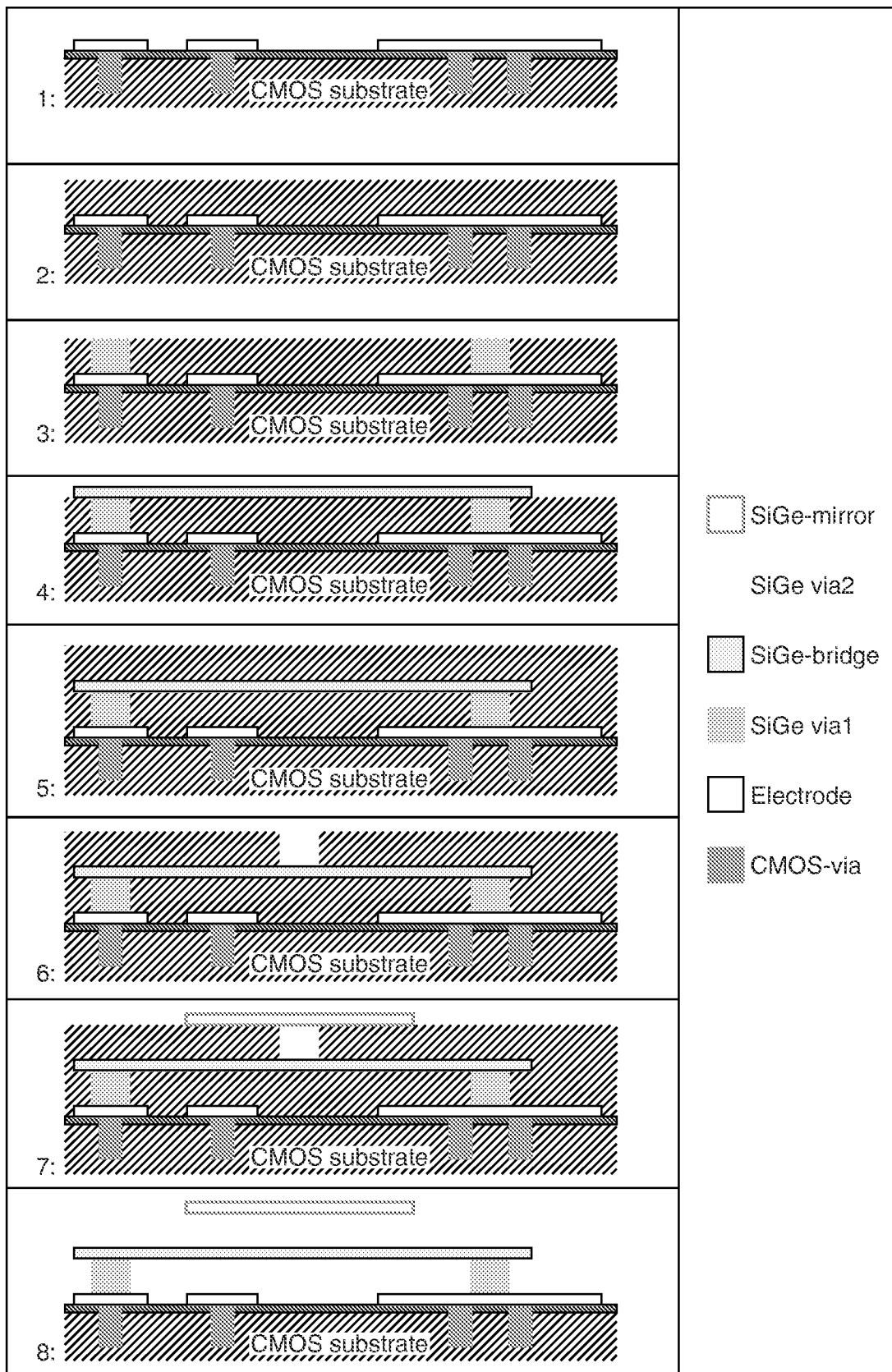


FIG. 8