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(54) **CLOCK DATA RECOVERY WITH SELECTABLE PHASE CONTROL**

TAKTRÜCKGEWINNUNGSSCHALTUNG MIT WÄHLBARER PHASENREGELUNG

RECUPERATION DE DONNEES D'HORLOGE AU MOYEN D'UNE COMMANDE DE PHASE SELECTIONNABLE

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to high speed signaling within and between integrated circuit devices.

BACKGROUND

[0002] Clock data recovery (CDR) circuits are often used in high speed signaling applications to recover clock and data signals from a signal line. Typically, transitions in an incoming signal are detected and used to generate a clock signal which is used, in turn, to sample data in the incoming signal.

[0003] Fig. 1 illustrates a prior art integrated circuit device 101 that includes a number of CDR circuits, CDR_0-CDR_{N-1}, to recover clock and data signals from lines $DATA_0$-$DATA_{N-1}$, respectively. Each CDR circuit includes a receiver 102 and a clock generator 103. The receiver 102 captures a number of samples of the incoming signal during each cycle of the recovered clock signal 104. The samples are compared with one another within a phase control circuit 107 (shown in the detail of clock generator 103 of CDR_0) to determine whether transitions in the incoming signal occur early or late relative to edges of a recovered clock signal 104. Based on the early/late determination, the phase control circuit 107 outputs a control signal to a phase adjust circuit 105 which responds by advancing or delaying (i.e., retarding) the phase of the recovered clock signal 104. Eventually, each of the CDR circuits reaches a phase locked condition in which the recovered clock signal 104 has a desired phase relationship to the incoming data signal (e.g., the recovered clock signal becomes aligned with the midpoint of the data eye), and the phase control output begins to toggle between advancing and delaying the phase of the recovered clock signal 104.

[0004] One disadvantage of the CDR arrangement in the integrated circuit 101 is that each of the signals on lines $DATA_0$-$DATA_{N-1}$ usually must undergo some minimum number of transitions per unit time (i.e., have a minimum transition density) in order for the corresponding CDR circuit to remain phase locked. Because the data content of the incoming signal may include relatively long sequences of zeroes or ones which lack such transitions, encoding, such as 8b/10b encoding, is often performed to replace the incoming data with codewords that meet the minimum transition density requirement. Because the codewords typically include more bits than the data values they replace, signal encoding tends to consume bandwidth on the signal line that could otherwise be used to transmit data. For example, in the case of 8b/10b encoding, each eight-bit data value is replaced with a 10-bit codeword, so that the encoding scheme consumes 20% of the signal line bandwidth. Other data encoding schemes also tend to consume signal line bandwidth.

SUMMARY

[0005] In various embodiments of the present invention, a select circuit is included within a clock data recovery (CDR) circuit to allow selection of either a self-generated phase control signal (i.e., a phase control circuit generated within the CDR circuit) or an externally generated phase control signal. The selected phase control signal is supplied to a phase adjust circuit within the CDR circuit to advance or retard the phase of the recovered clock signal. In one embodiment, the ability to select between self-generated and externally generated phase control enables the CDR circuit to be switched between a self-controlled CDR mode and a slave CDR mode. For a CDR circuit in the slave CDR mode, another CDR circuit (i.e., a master CDR circuit) may be used to provide the externally generated phase control signal, obviating the minimum transition density requirement of the data signal supplied to the slave-mode CDR circuit. As discussed below, multiple CDR circuits may initially be set to a self-controlled CDR mode to achieve phase lock (each CDR circuit having a respective phase offset according to the link characteristics), then all but one of the CDR circuits may be switched to a slave CDR mode in which the phase control signal from a master CDR circuit (the one CDR circuit left in self-controlled CDR mode) is used to control further phase adjustments in the slave mode CDR circuits. By this arrangement, signals input to all but one of the CDR circuits are relieved from the minimum transition density requirement. By selecting the master CDR circuit to be one in which the input data signal naturally meets the minimum transition density requirement (e.g., the input data signal is a reference clock signal), the available bandwidth on the remaining signal lines may be fully utilized. That is, no bandwidth-consuming encoding is needed to maintain phase lock in the slave mode devices.

[0006] As discussed below, providing a selection circuit to select between self-controlled CDR mode and slave CDR mode also enables the CDR circuit to be tested in a number of ways including, without limitation, phase testing and cycle testing of the CDR circuit.

[0007] These and other features and advantages of the present invention are described in the detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Fig. 1 illustrates a prior art integrated circuit device that includes multiple CDR circuits;
Fig. 2 illustrates a signaling system which includes a master-slave CDR arrangement according to one embodiment of the invention;
Fig. 3 illustrates the actions of a control device to initialize a recipient device for master-slave CDR operation;
Fig. 4 illustrates an alternative embodiment of a recipient device in which any of a number of CDR circuits may be operated as a master CDR circuit;
Fig. 5 is a block diagram of a CDR circuit according to a digital embodiment;
Fig. 6 illustrates an embodiment of a circuit that may be used within the sequence detection circuit Fig. 5 to generate an early/late indicator,
Fig. 7 illustrates a phase adjust circuit according to one embodiment;
Fig. 8 is a phase diagram of exemplary clock signals generated within the phase adjust circuit of Fig. 7;
Fig. 9 illustrates an embodiment of a configuration register that may be used within the device of Fig. 2 or the device of Fig. 4;
Fig. 10 illustrates a test system in which a test controller is used to test a device that includes a CDR circuit according to an embodiment of the present invention;
Fig. 1 1 is a flow diagram illustrating the operations of the test controller of Fig. 10 to perform a phase test on a CDR circuit;
Fig. 12 illustrates an alternative test system that can be used to determine the jitter tolerance of a CDR circuit;
Fig. 13 illustrates an embodiment of a second signal generator which includes a shift register, an exclusive orgate, and a multiplexor; and
Fig. 14 illustrates the operations of the test controller of Fig. 12 in performing a jitter tolerance test on a CDR circuit 1205.

DETAILED DESCRIPTION

Master-Slave CDR Operation

[0009] A master-slave CDR arrangement according to the preamble of Claims 1 and 8 is known from US 5 799 048.

[0010] Fig. 2 illustrates a signaling system which includes a master-slave CDR arrangement according to one embodiment of the invention. A control device 201 transmits data to a recipient device 203 by outputting signals onto N signal lines 200(0)-200(N-1), N being an integer. The signal lines 200 may be electrical or optical conductors and the signals conducted by the signal lines 200 may be generated using any number of signaling techniques including without limitation, modulating the voltage or current level of an electrical signal or modulating the intensity or other characteristics of an optical signal. The signals may represent any type of control and timing information (e.g., commands, address values, clock signals, configuration information) as well as data. All such information-carrying signals (i.e., control, timing and data signals) are referred to herein as data signals.

[0011] The recipient device 203 includes N CDR circuits 205(0)-205(N-1), each including a respective receive circuit 207(0)-207(N-1), phase control circuit 209(0)-209(N-1) and a phase adjust circuit 213(0)-213(N-1). Each receive circuit 207(0)-207(N-1) samples an incoming data signal in response to a respective recovered clock signal 210(0)-210(N-1). The samples of the incoming data signal are compared with one another in the corresponding phase control circuit 209 to determine whether the transitions in the data signal are early or late relative to the recovered clock signal 210. If the data signal transitions are determined to be early relative to the recovered clock signal 210, the recovered clock signal 210 is deemed to lag the incoming data signal and the phase control circuit 209 asserts a control signal to advance the phase of the recovered clock signal 210. Conversely, if the data signal transitions are determined to be late relative to the recovered clock signal 210, the recovered clock signal 210 is deemed to lead the incoming data signal, and the phase control signal asserts a control signal to delay (i.e., retard) the phase of the recovered clock signal 210.

[0012] Each of the select circuits 211(0)-211(N-1) is used to select between the self-generated phase control signal (i.e., the control signal generated by the corresponding phase control circuit 209(0)-209(N-1)) and an externally generated phase control signal More specifically, when a CDR select signal 212(0)-212(N-1) corresponding to one of the CDR circuits 205(0)-205(N-1) is in a first state, a self-controlled mode is selected for the CDR circuit 205 and the self-generated phase control signal is output to the phase adjust circuit 213. Conversely, when the CDR select signal 212 is in a second state, a slave mode is selected for the CDR circuit 205 and the externally generated phase control signal is output to the phase adjust circuit 213.

[0013] The phase adjust circuit 213 within each CDR circuit 205 responds to the selected phase control signal by advancing the phase of the recovered clock signal 210 if the selected phase control signal is in a phase advance state and by delaying the phase of the recovered clock signal if the selected phase control signal is in a phase delay state.

[0014] Still referring to the recipient device 203, the output of the phase control circuit 209(0) is coupled to the external CDR input of each of the select circuits 211(1)-211(N-1). Accordingly, when the CDR select signals 212(1)-212(N-1) select the slave mode, the phase control circuit 209(0) is used to control the phase of each of the recovered clock signals 210(0)-210(N-1). That is, CDR circuit 205(0) acts as a master CDR circuit and CDR circuits 205(1)-205(N-1) act as slave CDR circuits. Because the outputs of phase control circuits 209(1)-209(N-1) are not being used (i.e., when the corresponding CDR circuit 205(1)-205(N-1), the signals present on signal lines 200(1)-200(N-1) are no longer required to meet the minimum transition density in order for the CDR circuits 205(1)-205(N-1) to remain in phase lock. Also, because the phase control circuits 209(1)-209(N-1) are not being used to provide phase control, those circuits may be disabled to conserve power.

[0015] In one embodiment, the CDR select signals 212(0)-212(N-1) are output from the control device 201 directly to the external phase control inputs of the select circuits 211(0)-211(N-1). Alternatively, a configuration register 215 may be provided within the recipient device to control the state of the CDR select signals 212(0)-212(N-1). The configuration register 215 may be run-time programmed (i.e., loaded after device power-up) with a configuration value supplied by the control device 201, for example, in response to a load command issued from the control device 201 to the recipient device 203. The configuration register 215 may be designed to default to a predetermined mode upon device power up (e.g., all CDR circuits initialize to self-controlled mode). In another embodiment, each of the select circuits 211(1)-211 (N-1) may be controlled by a single CDR select signal (e.g., supplied from a configuration register, from the control device 201, or from another source) so that each of the CDR circuits 205(1)-205(N-1) is transitioned from self-controlled mode to slave mode in response to the same signal.

[0016] Fig. 3 illustrates the actions of the control device 201 to initialize the recipient device 203 for master-slave CDR operation. At block 301 the control device sets each of the CDR circuits (0 through N-1) within the recipient device to the self-controlled mode. At block 303, the control device outputs a training sequence (i.e., a test signal having a predetermined pattern such as 0, 1, 0, 1,...) onto each of the signal lines coupled to CDR circuits within the recipient device to allow the CDR circuits to attain phase lock. Note that the operations of blocks 301 and 303 may occur in any order or at the same time. After setting the CDR circuits in the recipient device to self controlled mode and initiating transmission of the training sequences, the control device delays for a predetermined time interval (as shown by block 305) to allow the CDR circuits to attain phase lock. During this time interval, the CDR circuits attain phase lock at respective phase offsets, effectively self-calibrating to compensate for timing variations between the incoming signal lines and timing variations between the CDR circuits themselves. That is, each CDR circuit may attain phase lock at a different phase offset from the other CDR circuits according to the particular characteristics of the incoming signal line and the CDR circuit itself. In some applications, the timing variations between the signal lines and the CDR circuits are relatively static so that the self-controlled mode of operation need only be selected at initial power-up. In other applications (e.g., applications in which changing temperature and/or voltage produces per-link timing offsets), it may be desirable to set the CDR circuits to self-controlled mode to compensate for timing variations either periodically or upon detection of certain conditions. For example, the CDR circuits may be set to self-controlled mode upon detecting a change in temperature or supply voltage, or upon detecting a loss of synchronization (e.g., detecting a threshold error rate in an error checking circuit within the integrated circuit device).

[0017] Still referring to block 303 of Fig. 3, rather than delay for a predetermined time, the control device may receive one or more status signals from the recipient device indicating that the CDR circuits have attained phase lock. For example, each of the CDR circuits within the recipient device may include logic circuitry to detect when the output of the phase control circuit begins to toggle between advancing and delaying the phase of the corresponding recovered clock signal and, in response, to generate a phase lock signal to indicate the phase locked condition. The phase lock signal from each of the CDR circuits may be output to the control device directly or via a status word read by the control device so that the control device may detect when all the CDR circuits within the recipient device have attained phase lock. In an alternative embodiment, the phase lock signals from each CDR circuit may be logically ANDed to generate a device level phase lock signal. The device level phase lock signal may then be output directly to the control device 201 or via a status word.

[0018] Still referring to Fig. 3, once each of the CDR circuits has attained phase lock, the control device sets CDR circuits 1 through N-1 to the slave mode (e.g., CDR circuits 205(1)-205(N-1) of Fig. 2). The recipient device is now configured for master-slave CDR operation, and signals input to the slave-mode CDR circuits are no longer required to have a minimum transition density in order for the slave-mode CDR circuits to remain in phase lock. In contrast to the prior art encoding schemes discussed above in which data words are encoded into larger codewords prior to transmission, the full bandwidth of each signal line coupled to a slave mode CDR circuit is available for data transmission.

[0019] Referring again to Fig. 2, it should be noted that the commands and/or control signals used to initialize the recipient device 203 for master-slave CDR operation may be issued by a device other than the control device 201. For

example, another device (not shown in Fig. 2) may output the CDR select signals 212 (or issue a configuration value and configuration load command) to the recipient device 203 while the device 201 outputs signals to the recipient device via signal lines 200. Also, while recipient device has been described in terms of its receive capability, numerous other circuit blocks may be included within the recipient device, including transmit circuits that transmit signals on signal lines 200 (or other signal lines) to be received by corresponding CDR circuits in the control device. For example in one embodiment, the control device and the recipient device are each SerDes (serialize/deserialize) devices that communicate via high-speed serial data streams output onto signal lines 200 (each link 200 may be bidirectional or dedicated to a given transmission direction). Deserializing circuitry within each device is used to convert the incoming serial data into parallel form for use by other circuitry within the device.

[0020] Still referring to Fig. 2, it may be known in advance that CDR circuit 205(0) is to be operated as the master CDR circuit for a given application. In that case, the select circuit 211 (0) and the signal line to carry CDR select signal 212(0) may be omitted (i.e., the output of phase control circuit 209(0) may be coupled directly to the input of phase adjust circuit 213(0)). Alternatively, the external phase control input to select circuit 211(0) may be provided for test purposes. Similarly, the select circuits 211(1)-211(N-1) may each (or any one of them) include an additional input port coupled to a test signal line for test purposes. Use of the select circuit 211 to allow CDR circuit testing is described below in further detail.

[0021] Fig. 4 illustrates an alternative embodiment of a recipient device in which any one of the CDR circuits 205(0)-205(N-1), or more than one of the CDR circuits, may be operated as a master CDR circuit. The receiver circuits 207(0)-207(N-1), phase control circuits 209(0)-209(N-1) and phase adjust circuits 213(0)-213(N-1) all operate as described above in reference to Fig. 2. The select circuits 211(0)-211(N-1) also operate as described above in reference to Fig. 2, except that the external phase control input of each select circuit is coupled to the phase control output of the select circuit of another of the CDR circuits. In the embodiment of Fig. 4, for example, the output of select circuit 211(0) is coupled to the external phase control input of select circuit 211(1), the output of select circuit 211(1) is coupled to the external phase control input of select circuit 211(2) and so forth, with the output of select circuit 211(N-1) being coupled to the external phase control input of select circuit 211(0). By this arrangement, any of the CDR circuits may be programmed (e.g., by programmable register or by assertion of the appropriate CDR select signal 412) to be a master CDR circuit. For example, by setting CDR circuit 205(1) to self-controlled mode and each of the other CDR circuits to slave mode, CDR circuit 205(1) becomes the CDR master for each of the other CDR circuits. Alternatively, two or more of the CDR circuits may be programmed to be masters of subsets of the remaining CDR circuits. For example, if there are sixteen CDR circuits 205(0)-205(15), half of the CDR circuits could be operated as a first set of master-slave CDR circuits (e.g., by setting CDR circuit 205(0) to self-controlled mode and CDR circuits CDR circuits 205(1)-205(7) to slave mode) and the other half of the CDR circuits operated as a second set of master-slave CDR circuits (e.g., by setting CDR circuit 205(8) to self-controlled mode and CDR circuits 205(9)-205(15) to slave mode). Other master-slave configurations may readily be achieved according to application requirements.

CDR Circuit

[0022] Fig. 5 is a block diagram of a CDR circuit 205 according to a digital embodiment. As shown, the phase adjust circuit 213 generates a recovered clock signal 214 having four component clock signals: data clock DC1 , data clock DC2 , edge clock EC1 and edge clock EC2. The receive circuit 207 includes four receivers which sample the incoming data signal in response to transitions in the respective component clock signals DC1, DC2, EC1 and EC2. The data signal samples captured in response to the data clocks DC1 and DC2 are input to a data deserializing circuit 503 (i.e., data deserializer) and are also output from the CDR circuit as receive data (RX DATA). The data signal samples captured in response to the edge clocks EC 1 and EC2 are input to an edge deserializer 505. In one embodiment, each of the deserializing circuits 503 and 505 is a shift register that loads data signal samples captured over an interval of R/2 clock cycles, R being an integer or a fractional value. For example, if R is five, then the data deserializer and edge deserializer would each contain ten data samples as follows:

Data Deserializer	Edge Deserializer
cycle 0: DC1 sample	cycle 0: EC1 sample
cycle 0: DC2 sample	cycle 0: EC2 sample
cycle 1: DC 1 sample	cycle 1: EC 1 sample
cycle 1: DC2 sample	cycle 1: EC2 sample
cycle 2: DC1 sample	cycle 2: EC1 sample
cycle 2: DC2 sample	cycle 2: EC2 sample
cycle 3: DC1 sample	cycle 3: EC1 sample
cycle 3: DC2 sample	cycle 3: EC2 sample

(continued)

Data Deserializer	Edge Deserializer
cycle 4: DC1 sample	cycle 4: EC1 sample
cycle 4: DC2 sample	cycle 4: EC2 sample

[0023] The outputs of the deserializing circuits are input to a detection circuit 507 which includes circuitry to generate an early/late indicator 510 for each of the R entries in the deserializing circuits 503 and 505. In one embodiment, each early/late indicator 510 includes an early signal (designated ER0 - ER(R-1) in Fig. 5) and a late signal (designated LT0-LT(R-1) in Fig. 5). As discussed below, the early signal, when asserted, indicates that a transition in the data signal occurred after a transition in one of the edge clock signals. That is, the edge clock transitioned early relative to the data signal transition. The late signal, when asserted indicates that a transition in the data signal occurred prior to a transition in one of the edge clock signals. That is, the edge clock transitioned late relative to the data signal transition. In one embodiment, both the early and late signals remain unasserted when there is no transition in the data signal.

[0024] A majority detection circuit 509 receives the R early/late indicators 510 from the detection circuit 507 and, in response, generates a phase control signal 514 according to whether a majority of the early/late indicators 510 indicate a late edge clock transition or an early edge clock transition. In the embodiment of Fig. 5, the phase control signal 514 includes an up-count component (UP) and a down-count-component (DN) which are generated as follows:

Condition	Up-Count	Down-Count
Majority of early/late indicators indicate early edge clock transition	0	1
Majority of early/late indicators indicate late edge clock transition	1	0
No majority	0	0

[0025] Still referring to Fig. 5, the phase control signal 514 is input to a first port (labeled "P1") of the select circuit 211, while the second port (labeled "P2") of the select circuit 211 is coupled to receive a phase control signal from an external source. As discussed, the select circuit 211 outputs a selected phase control signal 516 (i.e., either the phase control signal 514 or the externally generated phase control signal) according to a CDR select signal 212. The selected phase control signal 516 is supplied to the phase adjust circuit 213 which adjusts the phase of the component clock signals (i.e., DC1, DC2, EC1 and EC2) of the recovered clock signal 214 accordingly.

[0026] Fig. 6 illustrates an embodiment of an early/late circuit 601 that may be used within the detection circuit 507 of Fig. 5 to generate an early/late indicator 510. As shown in Fig. 6, the edge clock signals EC 1 and EC2 are edge aligned with transitions in an incoming data signal 603 and quadrature aligned with the data clock signals DC1 and DC2 (i.e., phase offset by $\pm$90 degrees from each of the data clock signals). By this arrangement, transitions in the data clock signals occur at the midpoint of the data eye (i.e., midway between the start and end of a valid data interval), the DC1 clock signal occurring at the midpoint of a data eye during a first half clock cycle, and the DC2 clock signal transitioning at the midpoint of a data eye during a second half clock cycle.

[0027] Exclusive OR gate 605 compares the samples of the data signal 603 captured in response to the DC1 and DC2 clock signals (referred to as DC1 and DC2 samples, respectively) to determine if the data signal 603 changed state (e.g., 0$\rightarrow$1 or 1$\rightarrow$0) in the time between the samples. In the example of Fig. 6, the data signal 603 does change state between the DC1 and DC2 samples as shown by the transition 602 between D0 and D1. Accordingly, the DC1 and DC2 samples have different values, causing logic gate 605 to assert a transition signal 606 (i.e., indicating that a transition has occurred). The EC1 and DC1 samples are compared in exclusive OR gate 607 to generate an EC-late signal 608 indicative of whether the EC1 signal transitioned before or after the data signal transition 602. If the EC1 transition trails the data signal transition, then the EC1 sample will be different from the DC1 sample and the exclusive OR gate 607 will assert the EC-late signal 608. Conversely, if the EC1 transition precedes the data signal transition, then the EC1 sample will be the same as the DC1 sample and the exclusive OR gate 607 will deassert the EC-late signal 606.

[0028] The transition signal 606 is input to each of a pair of AND logic gates 609 and 611. The EC-LATE signal 608 is also input to AND logic gate 609 and, after being inverted, to AND logic gate 611. Accordingly, if a data signal transition has occurred between the DC1 and DC2 samples, and the EC1 transition trails the data signal transition (i.e., both transition signal 606 and EC-late signal 608 are asserted), then AND logic gate 609 will assert late signal 610. Conversely, if a data signal transition has occurred between the DC1 and DC2 samples, and the EC1 transition precedes the data signal transition (i.e., transition signal 606 is asserted and EC-late signal 608 is deasserted), then AND logic gate 611 will assert the early signal 612. If the transition signal 606 is not asserted, then neither the early signal 612 nor the late signal 610 is asserted. Together the early signal 612 and the late signal 61 form the early/late indicator 510 discussed above in reference to Fig. 5.

[0029] In one embodiment, the detection circuit 507 of Fig. 5 includes R instances of the early/late circuit 601 of Fig. 6 to generate, in parallel, early/late indicators 0 through R-1. Half of the early/late circuits are coupled to the DC1, EC1 and DC2 signals as shown in Fig. 6 to generate early/late indicators for transitions in the data signal that should be aligned with EC1, while the other half of the early/late circuits are coupled to the DC2, EC2 and DC I signals (with the DC2 signal being coupled to both exclusive OR gates 605 and 607 and the DC1 signal being coupled only to exclusive OR gate 605) to generate early/late indicators for transitions in the data signal that should be aligned with EC2.

[0030] Fig. 7 illustrates a phase adjust circuit 213 according to one embodiment. As shown, a selected phase control signal 516 (including an up-count component and down-count component) is input to a phase counter 701 which, in turn, outputs a phase count 702 to a phase mixing circuit 703. The phase mixing circuit 703 includes circuitry to select, according to the phase count 702, a pair of clock signals from among eight clock signals generated by a clock generating circuit 705. In one embodiment, the clock generating circuit 705 includes four delay elements 707 each selected (or controlled) to delay a complementary pair of input clock signals by 45 degrees (one eighth of a clock cycle) such that, as shown in Fig. 8, the eight output clock signals CK0, CK1, CK2, CK3, /CK0, /CK1, /CK2 and /CK3 define eight octants within a 360 degree cycle. That is, each pair of phase-adjacent clock signals defines a 45 degree octant. (The '/' symbol is used herein to indicate inversion so that, for example, CK0 and /CK0 are complementary signals).

[0031] In one embodiment, the phase count 702 is an eight bit value with the most significant three bits being used to select one pair of octant-defining clock signals (referred to as phase vectors) and the least significant five bits being used to interpolate between vectors in equal, steps of 1.40625 degrees each (i.e., 45 degrees / (2^5)) to generate the recovered clock signal 214. Referring to Fig. 8, the DC1 component of the recovered clock signal 214 may be generated, for example, by a phase count that selects and interpolates between clock signals CK0 and CK1. The EC1, DC1 and EC2 components may be generated by interpolating every other phase vector pair using the same five-bit phase interpolation value. Thus the DC1, EC1, DC2, and EC2 clock signals may be generated as follows:

DC 1: select octant indicated by phase count interpolate bounding vectors of selected octant per phase interpolation value

EC1: select octant indicated by phase count + 2 interpolate bounding vectors of selected octant per phase interpolation value

DC2: select octant indicated by phase count + 4 interpolate bounding vectors of selected octant per phase interpolation value

EC2: select octant indicated by phase count + 6 interpolate bounding vectors of selected octant per phase interpolation value

[0032] Although the phase control circuit 209 and the phase adjust circuit 213 have been described in terms of a particular digital embodiment, the circuits may be implemented in numerous different ways. To start, the phase count (i.e., signal 702 of Fig. 7) may include more or fewer bits, with the vector selection portion of the count selecting between more or fewer than eight vector pairs, and the phase interpolation portion of the count defining more or fewer than 32 interpolation steps. Also, as shown in Fig. 6, the data clocks DC1 and DC2 are complements of one another (i.e., 180 degrees out of phase) and used to sample the incoming data signal on respective halves of a clock cycle (i.e., double data rate operation). In alternative embodiments, only one sample may be captured per clock cycle, and clock signal DC2 omitted (i.e., single data rate operation). More generally, an input data signal may be sampled at any data rate (e.g., single, double, quad, etc.) without departing from the scope of the present invention. Further, instead of a digital phase control signal (e.g., up-count/down-count signals) an analog phase control signal may be generated to control an analog phase adjust circuit such as a voltage controlled oscillator.

Configuration Register

[0033] Fig. 9 illustrates an embodiment of a configuration register 215 that may be used within the recipient device 203 of Fig. 2 or device 403 of Fig. 4. As shown in Fig. 9, the configuration register 215 may include storage for N CDR select bits, CS(0)-CS(N-1) one to drive each of the N CDR select signals. The configuration register 215. may further include storage 901 for additional configuration information that may be useful in device testing as discussed below.

CDR Circuit Testing

[0034] Fig. 10 illustrates a test system 1000 in which a test controller 1001 is used to test a device 1003 (the test device) that includes a CDR circuit 1005 according to an embodiment of the present invention. More specifically, the test controller 1001 outputs a CDR select signal 1012 to the CDR select input of a select circuit 1011 within the CDR circuit 1005 to place the CDR circuit 1005 in a slave mode. The test controller 1001 also outputs a phase control signal 1014 to the external phase control input of the select circuit 1011. The recovered clock signal 1010 is output from the

test device 1003 and received by a signal measuring device 1004 (and additionally (or alternatively) by the test controller 1001 as shown by dashed line 1016). In one embodiment, the test device 1003 is an integrated circuit and the test controller 1001 is a general purpose test device (e.g., automated test equipment (ATE)). Alternatively, the test controller 1001 may also be an integrated circuit device (e.g., to run a built in self test within a system application), or a device that is incorporated into the same integrated circuit or integrated circuit package as the test device 1003. The signal measuring device 1004 is preferably a device for illustrating a time-based voltage waveform, such as an oscilloscope, but may be any device which can capture samples the recovered clock signal 1010 may be used.

[0035] One application of the test system 1000 is to perform a phase test on the phase adjust circuit 1013 of the CDR circuit 1005. A phase test is useful, for example, for determining whether the phase adjust circuit 1013 is capable of generating clock signals whose phases are spaced evenly throughout a clock cycle. For example, if the phase adjust circuit 1013 is intended to subdividing a clock cycle into 256 phases, then a phase test may be used to determine whether the generated clock signals, in fact, represent an evenly spaced distribution of 256 phase offsets within a clock cycle.

[0036] Fig. 11 is a flow diagram illustrating the operations of the test controller 1001 of Fig. 10 to perform a phase test on the CDR circuit 1005 within test device 1003. At block 1101, the test controller configures the test device for a phase test. Referring to Fig. 10, configuring the test device for a phase test may include, for example, asserting a reset signal (as shown by the dashed arrow 1018 in Fig. 10), to reset the phase counter within the phase adjust circuit 1009, then asserting the CDR select signal 1012 to select the external phase control signal 1014 from the test controller 1001 to be the selected phase control signal.

[0037] Returning to Fig. 11, after configuring the test device for a phase test, the test controller delays for a first predetermined time interval, PT1. During time interval PT1, the test controller does not adjust the phase of the clock signal output by the phase adjust circuit (i.e., the test clock), so that the test clock oscillates at a substantially constant frequency and phase. At block 1105, the test controller asserts an up-count signal and leaves the up-count signal asserted for a second predetermined time, PT2 (block 1107). The phase adjust circuit responds to the up-count signal by repeatedly increasing the phase count until, at block 1109, the test controller deasserts the up-count signal. At block 1111, the test controller determines whether it has received a command (e.g., from a user or another control device) to exit the phase test. If not, then the operations of blocks 1103-1109 are repeated such that, during each time interval T1, the test clock is left to run at a selected phase offset, and during each time interval T2, the test clock is ramped to a next phase offset, each of the phase offsets being equally spaced in phase. By this arrangement, a phase plot such as shown on display 1006 of the signal measuring device 1004 of Fig. 10 may be captured. Each peak 1021 on the plot corresponds to a phase offset within a cycle of the test clock 1010 so that any differences in the time intervals between peaks (designated T1, T2, T3, T4, ...in display 1006) is indicative of an inaccuracy in the output of the phase adjust circuit The time interval PT2 may be selected to result in a phase increment between peaks that is as small or large as desired (or as small as can be detected by the signal measuring device 1004, or as small as the time needed to change only one phase step). Considering a phase adjust circuit capable of subdividing a test clock cycle into 256 phase offsets as an example, the time interval PT2 may be set to allow the phase counter therein to ramp by eight such that clock signals each having an incremental one of 32 different phase offsets are output during respective time intervals PT1. Each offset should be 11.25 degrees (360 degrees/32) spaced from the other and the offset times measured by the measurement device should, ideally, be (1/freq) * (32/360) seconds, where freq is the frequency of the recovered clock signal. Other ramp settings may be used to provide finer or coarser phase testing in different tests.

[0038] Returning briefly to Fig. 11, it should be noted that the signal line 1002 need not be provided to perform the phase test described in reference to Fig. 12. Accordingly, signal line 1002 may be omitted from the phase test arrangement 1000 in alternative embodiments.

[0039] Fig. 12 illustrates an alternative test system 1200 that can be used, for example, to determine the jitter tolerance of a CDR circuit 1205 within device under test 1203 (the test device). Jitter tolerance refers to the phase difference between the maximum tolerable phase offset (i.e., before reception errors begin) and the minimum tolerable phase offset of the recovered clock signal 1210. In one embodiment, the test device 1203 includes a signal generator 1223 (e.g., a pseudo-random bit sequence (PRBS) generator (typically implemented by linear feedback shift register) as shown in Fig. 12) to generate a test signal 1218. A multiplexer 1229 within the test device 1203 is responsive to a test mode signal 1217 to select the signal generator 1223 to provide an output data signal 1218 instead the circuit (or circuits) within the test device 1203 normally used to generate output data (not shown). In one embodiment, the test mode signal 1217 is asserted whenever a test mode value is stored within a device configuration register 1215 (e.g., within a storage similar to the additional configuration information portion 901 of the configuration register 215 of Fig. 9). Alternatively, the test mode signal 1217 may be supplied directly from an external device such as test controller 1201.

[0040] The test mode signal 1217 may also be coupled to switch circuits 1237 and 1238 within the test device 1203 such that, when the test mode signal 1217 is asserted, the output of transmit circuit 1227 is looped back to the input of receive circuit 1207. That is, the test device 1203 is placed in a loop-back mode with the signal generator 1223 providing the loop-back signal 1218 to the CDR circuit 1205. In alternative embodiments, the loop-back path may be made formed outside the test device 1203, for example, by a connection within the test controller 1201 or by an optical or electrical

cable coupled between the transmitter circuit 1227 and receive circuit 1207 as shown by dashed line 1241. Also, the loop-back path may be made internally within the test device without passing through the transmitter circuit 1227, or even through the multiplexer 1229. For example, the signal generator 1223 may be coupled to the input of receive circuit 1207 through switch circuit 1238.

[0041] In any case, the CDR circuit 1205 is used to recover a clock signal 1210 (the test clock) and a data signal 1220 from the loop-back signal 1218. The recovered data signal 1220 is supplied to a compare circuit 1231 which compares the recovered data signal 1220 with a twin 1224 (i.e., identical version) of the original test signal 1218 to confirm that the CDR circuit is recovering the test signal 1218 without error. In one embodiment, the compare circuit 1231 includes a second signal generator (e.g., PRBS generator 1233) to generate the twin signal 1224. A comparator 1235 within the compare circuit 1231 (e.g., implemented using an exclusive OR gate) is then used to compare the recovered data signal 1220 with the twin signal 1224 and to assert an error signal 1216 if the signals do not match.

[0042] Fig. 13 illustrates an embodiment of the second signal generator 1233 which includes a shift register 1301, an exclusive OR gate 1303, and a multiplexer 1305. The multiplexer 1301 includes a first input port coupled to an output of the exclusive OR gate 1303, and a second input port coupled to receive the recovered data signal 1220. The exclusive OR gate 1303 is coupled to selected storage elements of the shift register 1301 (storage elements six and seven in this example, though the shift register may contain more or fewer storage elements and any of the storage elements may be coupled to the exclusive OR gate in alternative embodiments) and the output of the multiplexer 1305 is coupled to the shift register 1301. Accordingly, when the first input port of the multiplexer 1305 is selected, the exclusive OR gate 1303 and the shift register 1301 form a linear feedback shift register (LFSR) which generates a pseudo random bit sequence (i.e., twin signal 1224). During an initialization interval, preferably after the CDR circuit 1205 has attained phase lock, a preload signal 1302 is asserted to cause the multiplexer 1305 to select the recovered data signal 1220 (i.e., at the second input port) to be shifted into the shift register 1301. By this arrangement, the configuration register may be preloaded with the same value that is loaded into a shift register within the signal generator 1223 of Fig. 12, effectively synchronizing the signal generator 1233 with the signal generator 1223. After the signal generators are synchronized, the preload signal 1302 is deasserted and the LFSR circuit formed by shift register 1301 and exclusive OR gate 1303 is used to predict each new bit within the recovered data signal. Any mismatch between the output of the exclusive OR gate 1303 (i.e., the predicted, twin signal 1224) and the recovered data signal 1220 may be then detected as an error by comparator 1235 of Fig. 12.

[0043] Returning to Fig. 12, in an alternative embodiment, the signal generator 1223 may be used to supply the twin signal 1224 to the compare circuit as shown by dashed line 1225, and the second signal generator 1233 omitted. In such an embodiment, it may be desirable to delay the twin signal delivered through path 1225 so that the recovered data signal 1220 and the twin signal arrive at the comparator circuit 1235 during the same clock cycle (or portion of a clock cycle).

[0044] As in the test arrangement depicted in Fig. 10, the test device 1203 may be an integrated circuit and the test controller 1201 a separate general purpose test device (e.g., automated test equipment (ATE)). Alternatively, the test controller 1201 may also be an integrated circuit device, or a device that is incorporated into the same integrated circuit or integrated circuit package as the test device 1203.

[0045] Fig. 14 illustrates the operations of the test controller 1201 of Fig. 12 in performing a jitter tolerance test on the CDR circuit 1205 within the test device 1203. At block 1401, the test controller configures the test device for a jitter tolerance test. Referring to Fig. 12, the actions involved in configuring the test device for jitter tolerance test may include, without limitation, (1) setting the test device to a test mode (e.g., by asserting a test mode signal 1217 or loading an appropriate configuration value into the configuration register 1215 to cause the test mode signal 1217 to be asserted), (2) setting the CDR select signal 1212 to select the self-controlled mode of operation for the CDR circuit 1205 (i.e., phase control signal supplied by the phase control circuit 1209), (3) delaying for a predetermined time to allow the CDR circuit 1205 to attain phase lock (or alternatively, delaying until the CDR circuit 1205 or another circuit block within the test device 1203 indicates that phase lock has been attained), and (4) after phase lock is attained, setting the CDR select signal 1212 to select the slave mode of operation (i.e., phase control signal 1214 supplied by the test controller). Referring to Fig. 13, the test controller may also assert (or configure the test device to assert) the preload signal 1302 for a predetermined time to synchronize the signal generator 1233 within the compare circuit 1231 to the signal generator 1223.

[0046] After the test device has been configured for the jitter tolerance test in block 1401, the test controller asserts a down-count signal in block 1403 for a predetermined time interval, T1. In one embodiment, the duration of time interval T1 is selected such that the phase count within the phase adjust circuit (e.g., element 1213 of Fig. 12) is decremented by one. In decision block 1405, the test controller monitors the error status of the test device (e.g., by sampling the error signal 1216 output from the test device, by reading a status value from the test device, etc.) for a predetermined time interval, T2, to determine whether the CDR circuit is still properly recovering the test signal at the new phase offset setting. In one embodiment, the duration of time interval T2 is selected to allow a statistically sufficient number of samples of the test signal to be captured by the CDR circuit (and compared with the twin signal in the compare circuit 1231) to determine whether reception errors are occurring. If no error is detected in decision block 1405, then the down-count

signal is asserted again in a repetition of block 1403 to set an incrementally more delayed phase offset for the test clock 1210, and error monitoring is performed again in block 1405. Blocks 1403 and 1405 are repeated in this manner until the phase offset of the test clock is delayed to a point at which an error is detected. When this occurs, a counter within the test controller is set to zero to mark the most delayed (i.e., minimum) phase offset at which the CDR circuit was still properly recovering data. At block 1409, the up-count signal is asserted for the predetermined time interval, T1, to select an incrementally more advanced phase of the test clock. At block 1411, the error status of the test device is evaluated in the same manner as in block 1405 to determine whether reception errors have occurred. Because the test clock has just been advanced back into the passing range of phase offsets, no error is determined in the initial pass through decision block 1411. Accordingly, at block 1413, the counter is incremented by an increment value that corresponds to the increment in the phase count value within the CDR circuit 1205 that resulted from assertion of the up-count signal in block 1409 (i.e., the counter maintained by the test controller and the counter within the phase adjust circuit of the test device are incremented in lock step). Blocks 1409, 1411 and 1413 are then repeated, incrementing the phase offset with each repetition, until a phase error is detected in decision block 1411. At this point the value of the counter within the test controller is representative of the number of increments in phase between a minimum tolerable phase offset and a maximum tolerable phase offset. That is, as shown in termination block 1415, the jitter tolerance of the CDR circuit within the test device is specified by the counter value within the test controller. Note that the actions used to perform jitter tolerance testing may be altered in numerous ways. For example, a count of the number of executions of block 1403 (i.e., a decrement count) may be maintained so that, upon detecting the minimum tolerable phase offset at block 1405, the up-count signal may be asserted for a time interval corresponding to the decrement count to return the phase offset of the test clock to its initial value. Thereafter, the phase offset of the test clock may be incremented in iterative executions of steps 1409, 1411 and 1413 to determine the maximum tolerable phase offset of the test clock. In such an embodiment, the count value incremented in block 1413 (i.e., the increment count) is indicative of the phase difference between the phase offset at phase lock and the maximum tolerable phase offset, while the decrement count is indicative of the phase difference between the phase offset at phase lock and the minimum tolerable phase offset. Accordingly, the jitter tolerance of the CDR circuit may be determined by summing the decrement count and increment count.

[0047] The phase test and jitter tolerance test described above are but two instances of numerous different tests that may be performed using embodiments of the present invention. Moreover, while the phase test and the jitter tolerance test have been described in reference to digital implementations of a CDR circuit, the tests may be carried out using analog control signals to control the phase of an analog phase adjust circuit in alternative embodiments.

[0048] Although the invention has been described with reference to specific exemplary embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

Claims

1. An integrated circuit comprising:

a first receive circuit (207) to sample an input signal in response to a first clock signal (214) thereby generating samples of the input signal;
a select circuit (211) being responsive to a select signal (212) to select from one of a first control signal (514) and a second control signal to be output as a selected control signal (516); and
a first phase adjust circuit (213) coupled to receive the selected control signal (516) from the select circuit (211), the first phase adjust circuit (213) being responsive to the selected control signal (516) to adjust the phase of the first clock signal (214);

characterized by
a control circuit (209) comparing the samples of the input signal with one another thereby generating the first control signal (514) according to a phase relationship between the input signal and the first clock signal (214); wherein the select circuit (211) being coupled to receive the first control signal (514) from the control circuit (209) and coupled to receive the second control signal.

2. The integrated circuit of claim 1, wherein
the first phase adjust circuit (213) includes circuitry to output a plurality of clock signals including the first clock signal (214);
the first receive circuit (207) captures a plurality of samples of the input signal in response to transitions of the plurality of clock signals;

the phase control circuit (209) determines, based on the plurality of samples of the input signal, whether a transition of the input signal occurs before a transition of the first clock signal (214) and whether the transition of the input signal occurs after the transition of the first clock signal (214); and
the first receive circuit (207) and the phase control circuit (209) are comprised in the control circuit (209).

3. The integrated circuit of claim 2, wherein the first control signal (514) is a digital signal having one of at least two possible states, and wherein the phase control circuit (209) includes circuitry to output the first control signal (514) in a state selected from one of a first state and a second state of the at least two possible states based, at least in part, on whether the transition of the input signal occurs before the transition of the first clock signal (214) and whether the transition of the input signal occurs after the transition of the first clock signal (214).

4. The integrated circuit of claim 1, wherein the first control signal (514) includes a first component signal (UP) that is asserted when the first clock signal (214) lags the input signal and a second component signal (DN) that is asserted when the first clock signal (214) leads the input signal.

5. The integrated circuit of claim 1, wherein the first control signal (514) is an analog signal having a voltage level indicative of the phase relationship between the input signal and the first clock signal (214).

6. The integrated circuit of claim 1, wherein the first control signal (514) is an analog signal having a current level indicative of the phase relationship between the input signal and the first clock signal (214).

7. The integrated circuit of claim 1, wherein the select circuit (211) comprises a multiplexer circuit.

8. A method of operation for an integrated circuit, the method comprising:

sampling an input signal in response to a first clock signal (214) thereby generating samples of the input signal;
selecting from one of a first control signal (514) and a second control signal to be output to a phase adjust circuit (213) as a selected control signal (516); and
adjusting, in the phase adjust circuit (213), a phase of a first clock signal (214) according to the selected control signal (516)

characterized by
comparing the samples of the input signal with one another thereby
determining a phase relationship between the input signal and the first clock signal (214); and
generating the first control signal (514) according to the phase relationship between the input signal and the first clock signal (214).

9. The method of claim 8, further comprising:

outputting a plurality of clock signals, including the first clock signal (214);
capturing a plurality of samples of the input signal in response to transitions of the plurality of clock signals; and determining the phase relationship between the input signal and the first clock signal (214), at least in part; by determining, based on the plurality of samples of the input signal, whether a transition of the input signal occurs before a transition of the first clock signal (214) and whether the transition of the input signal occurs after the transition of the first clock signal (214).

10. The method of claim 9, wherein generating the first control signal (514) comprises generating a digital control signal having one of at least two possible states based, at least in part, on whether the transition of the input signal occurs before the transition of the first clock signal (214) and whether the transition of the input signal occurs after the transition of the first clock signal (214).

11. The method of claim 8, wherein generating the first control signal (514) comprises generating a digital signal having a first and second component signals, the first component signal (UP) being asserted when the first clock signal (214) lags the input signal and the second component signal (DN) being asserted when the first clock signal (214) leads the input signal.

12. The method of claim 8 further comprising receiving the select signal (212) from a device that is external to the integrated circuit.

13. The method of claim 8 further comprising storing a mode value in a programmable register (215) within the integrated circuit, and wherein generating the selected control signal (516) comprises generating the select signal (212) according to the mode value.

14. The method of claim 8 further comprising
receiving a command to store a mode value; and
storing the mode value in a register (215) within the integrated circuit; and
wherein generating the selected control signal (516) comprises generating the select signal (212) according to the mode value.

15. An integrated circuit device comprising an integrated circuit (205) as claimed in claim 1 comprising a first CDR circuit (205 (1)) to recover clock and data signals from a first signal line (200 (1)), wherein the control circuit (209) comprises a first phase control circuit (209 (1)) to generate the first control signal,
the integrated circuit device further comprising:

a second clock data recovery (CDR) circuit (205 (0)) to recover clock and data signals from a second signal line (200 (0)), the second CDR circuit (205 (0)) including:

a second phase control circuit (209 (0)) to generate the second control signal, and
a second phase adjust circuit (213 (0)) to adjust the phase of a second recovered clock signal (210 (0)) in response to the second control signal (514).

16. The integrated circuit device of claim 15 wherein the select circuit (211 (1)) comprises a multiplexer circuit having a control input coupled to receive the select signal (212 (1)) and having respective input ports coupled to receive the first and second control signals from the first and second phase control circuits (209 (0), 209 (1)).

17. The integrated circuit device of claim 15 further comprising additional CDR circuits (205 (N-1)) each having a respective phase control circuit (209 (N-1)), select circuit and phase adjust circuit (213 (N-1)), the select circuit (211 (N-1)) of each of the additional CDR circuits (205 (N-1)) being responsive to a control input to output, as a selected control signal, from one of the second phase control signal and a phase control signal output by the phase control circuit (209 (N-1)) of the additional CDR circuit (205 (N-1)), the phase adjust circuit (213 (N-1)) of each of the additional CDR circuits (205 (N-1)) being responsive to the selected control signal output by the select circuit (211 (N-1)) for the additional CDR circuit (205 (N-1)) to adjust the phase of a respective recovered clock signal (210 (N-1)).

18. The integrated circuit device of claim 15 wherein
the first receive circuit (207 (1)) samples the input signal on the first signal line (200 (1)), and
the second CDR circuit (205 (0)) further includes a second receive circuit (207 (0)) to sample an input signal on the second signal line (200 (0)) in response to the second recovered clock signal (210 (0)).

19. The integrated circuit device of claim 1 or 15 further comprising an input to receive the select signal (212) from an external device.

20. The integrated circuit device of claim 1 or 15 further comprising a programmable register to store a mode value, the select signal (212) having from one of a first state and a second state according to the mode value, and the select circuit (211) including a circuitry to select the first control signal when the select signal (212) is in the first state and to select the second control signal when the select signal (212) is in the second state.

21. The integrated circuit device of claim 15 wherein the select circuit (211) is responsive to the select signal (212) to disable generation of the second control signal when the select signal (212) indicates that the select circuit (211) is to select the first control signal to be output as the selected control signal.

22. A method of controlling for the integrated circuit of claim 1, the method comprising:

outputting a first command to the integrated circuit to set a first clock data recovery (CDR) circuit (205 (1)) within the integrated circuit to a first mode, the first CDR circuit (205 (1)) including a select circuit (211 (1)) to select a first control signal to adjust the phase of a first clock signal (210 (1)) when the first CDR circuit (205 (1)) is in the first mode;
delaying for a first time interval; and

outputting, after the first time interval, a second command to the integrated circuit to set the first CDR circuit (205 (1)) to a second mode, the select circuit of the first CDR circuit (205 (1)) to select a second control signal when the first CDR circuit (205 (1)) is in the second mode,

characterized by
generating the second control signal in a second CDR circuit (205 (0)).

23. The method of claim 22 wherein delaying for the first time interval comprises delaying until a predetermined number of cycles of a clock signal have transpired.

24. The method of claim 22 wherein outputting the first command to the integrated circuit (205 (1)) to set the first CDR circuit to the first mode comprises outputting a command to the integrated circuit to store a mode value in a programmable register (215) within the integrated circuit, the mode value indicating the first mode.

25. The method of claim 22 wherein outputting the first command to the integrated circuit to set the first CDR circuit (205 (1)) to the first mode comprises outputting a mode signal to the integrated circuit, the mode signal being input to a select input of the select circuit (211 (1)) to select the first control signal.

26. The method of claim 22 further comprising periodically repeating the outputting the first command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

27. The method of claim 22 further comprising:

detecting a predetermined condition; and
in response to the detecting the predetermined condition, repeating the outputting the first command to the integrated circuit, delaying for the first time interval, and outputting the second command to the integrated circuit.

28. The method of claim 27 wherein the detecting the predetermined condition comprises detecting a change in temperature.

29. The method of claim 27 wherein the detecting the predetermined condition comprises detecting a change in voltage.

30. The method of claim 27 wherein the detecting the predetermined condition comprises detecting a loss of synchronization between the first clock signal (210 (1)) and a data signal received in the first CDR circuit (205 (1)).

31. A system comprising an integrated circuit (205) as claimed in claim 1, the system further comprising:

a first signal line (200 (1)) providing the input signal;
a receive device (203) coupled to the first signal line (200 (1)), the receive device (203) comprising the integrated circuit (205) as a first clock data recovery (CDR) circuit (205 (1)) to recover clock and data signals from the first signal line (200 (1)), wherein the select circuit (211 (1)) is responsive to a first mode value as the select signal (212 (1)), ; and
a control device (201) coupled to the receive device (203) to provide the first mode value thereto.

32. The system of claim 31 wherein the control device (201) is coupled to provide the first mode value to the receive device (203) via the first signal line (200 (1)).

33. The system of claim 31 further comprising at least one additional signal line (200 (0)), the at least one additional signal line (200 (0))coupled to the receive device (203) and to the control device (201), the control device (201) to provide the first mode value to the receive device (203) via the at least one additional signal line (200 (0)).

34. The system of claim 31 wherein the control device (201) to output the first mode value to the receive device (203) and then, after a first time interval, to output a second mode value as the select signal (212 (1)) to the receive device (203), the select circuit (211 (1)) being responsive to the first mode value to select the first control signal to be output as the selected control signal, the select circuit (211 (1)) being responsive to the second mode value to select the second control signal to be output as the selected control signal.

35. The system of claim 34 further comprising a second signal line (200 (0)) coupled to the receive device (203), and

wherein the receive device (203) includes a second CDR circuit (205 (0)) to recover clock and data signals from the second signal line (200 (0)), the second CDR circuit (205 (0)) including a control circuit (209) to generate the second control signal according to a phase relationship between an input signal on the second signal line (200 (0)) and a second clock signal (210 (0)).

36. The system of claim 31 wherein the receive device (203) is implemented in a first integrated circuit and the control device (201) is implemented in a second integrated circuit.

37. The system of claim 36 wherein the first and second integrated circuits are packaged in separate integrated circuit packages.

38. The system of claim 36 wherein the first and second integrated circuits are packaged in the same integrated circuit package.

39. The system of claim 31 wherein the receive device (203) and the control device (201) are implemented within a single integrated circuit.

40. A method of testing the integrated circuit of claim 1 that includes a clock data recovery (CDR) circuit (1005, 1205) and a phase control port, the method comprising:

outputting a command to the integrated circuit to set the CDR circuit (1005, 1205) to a mode of operation;
adjusting the phase of a clock signal (1010, 1210) according to a control signal (1014, 1214) being used by a phase adjust circuit (1013, 1213) within the CDR circuit (1005, 1205); and
outputting a phase control signal to the phase control port of the integrated circuit to adjust the phase of the clock signal (1010. 1210)

characterized by
selecting, in a select circuit (1011, 1211) of the CDR circuit (1005, 1205), the phase control port to source a control signal instead of a phase control circuit (1009, 1209) within the CDR circuit (1005, 1205) according the mode of operation.

41. The method of claim 40 wherein outputting the command to the integrated circuit to set the CDR circuit (1205) to the mode of operation comprises outputting a command to the integrated circuit to store a mode value in a programmable register (1215) within the integrated circuit, the mode value indicating the mode of operation.

42. The method of claim 40 wherein outputting the command to the integrated circuit to set the CDR circuit (1005, 1205) to a mode of operation comprises outputting a mode signal (1012, 1212) to the integrated circuit, the mode signal being input to a select input of the select circuit (1011, 1211) to select the phase control port to source the control signal (1014, 1214).

43. The method of testing an integrated circuit according to claim 40, wherein
outputting the phase control signal to the phase control port of the integrated circuit to adjust the phase of the clock signal (1010, 1210) comprises asserting the phase control signal at the phase control port of the integrated circuit for a first predetermined time interval, the phase adjust circuit (1013) within the CDR circuit (1005) responsive to the phase control signal to adjust the phase of the clock signal (1010);
the method further comprising:

deasserting the phase control signal for a second predetermined time interval; and
measuring the clock signal (1010) with a signal measuring device (1004) while repeating asserting a phase control signal and deasserting the phase control signal at least until the phase of the clock signal (1010) has progressed through a predetermined portion of a cycle of the clock signal (1010).

44. The method of claim 43 wherein the predetermined portion of a cycle of the clock signal (1010) is an entire cycle of the clock signal (1010).

45. The method of claim 43 wherein the phase adjust circuit (1013) responds to assertion of the control signal (1014) by advancing the phase of the clock signal (1010).

46. The method of claim 43 wherein the first predetermined time interval is selected to allow the phase adjust circuit (1013) to advance the phase of the clock signal (1010) by a predetermined phase angle.

47. The method of claim 43 wherein measuring the clock signal (1010) with a signal measuring device (1004) comprises measuring the clock signal (1010) with an oscilloscope.

48. An integrated circuit device comprising an integrated circuit as claimed in claim 1 comprising a clock data recovery (CDR) circuit (1205), the integrated circuit device further comprising:

a first signal generator (1223) to generate the input signal as a first test signal (1218); and
a compare circuit (1231) to compare samples of the first test signal (1218) to a compare signal (1224);

wherein the receive circuit (1207) has an input switchably coupled to receive the first test signal (1218) from the first signal generator (1223).

49. The integrated circuit device of claim 48 wherein the first signal generator (1223) is a linear feedback shift register and the first test signal (1218) is a pseudo random bit sequence.

50. The integrated circuit device of claim 48 further comprising a transmit circuit (1227) having an input and an output, the input of the transmit circuit switchably coupled to receive the first test signal (1218) from the first signal generator (1223), and the output of the transmit circuit switchably coupled to the input of the receive circuit (1207).

51. The integrated circuit device of claim 48 further comprising a mode control circuit (209) to store a mode value indicative of an operating mode of the integrated circuit device, the mode control circuit (209) outputting a test mode signal (1217) when the mode value is indicative of a test mode of operation, the test mode signal switching the input of the receive circuit (1207) to be coupled to receive the first test signal (1218).

52. The integrated device of claim 48 wherein the compare circuit (1231) includes a second signal generator (1233) to generate the compare signal (1224).

53. The integrated circuit device of claim 48 wherein the first signal generator (1223) and the second signal generator (1233) are designed to generate identical signals.

54. The integrated device of claim 48 wherein the first signal generator (1223) is coupled to provide the first test signal (1218) to the compare circuit (1231), the compare signal (1224) being the first test signal (1218).

55. The method of testing an integrated circuit according to claim 40, the method further comprising:

inputting a test signal (1218) to a receiver (1207) of the CDR circuit (1205);
comparing the test signal (1218) against samples of the test signal (1218) generated by the CDR circuit (1205);
asserting an error signal (1216) when the test signal (1218) does not match the samples; and
repeating comparing the test signal (1218), asserting an error signal (1216) and asserting a phase control signal to determine a maximum phase and a minimum phase of the clock signal for which the error signal (1216) is not asserted.

Patentansprüche

1. Ein integrierter Schaltkreis mit:

einer ersten Empfangsschaltung (207) zum Abtasten eines Eingangssignals in Antwort auf ein erstes Taktsignal (214), **dadurch** Generieren von Abtastungen des Eingangssignals;
einer Auswählschaltung (211), die auf ein Auswählsignal (212) zum Auswählen zwischen einem ersten Steuersignal (514) und einem zweiten Steuersignal antwortet, welches als ein ausgewähltes Steuersignal (516) auszugeben ist; und
einer ersten Phasenanpassungsschaltung (213), die zum Empfangen des ausgewählten Steuersignals (516) von der Auswählschaltung (211) gekoppelt ist, wobei die erste Phasenanpassungsschaltung (213) auf das ausgewählte Steuersignal (516) zum Anpassen der Phase des ersten Taktsignals (214) antwortet;

gekennzeichnet durch
eine Steuerschaltung (209), die die Abtastungen des Eingangssignals mit einander vergleicht, wodurch das erste Steuersignal (514) gemäß einer Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214) generiert wird; wobei die Auswählschaltung (214) zum Empfangen des ersten Steuersignals (514) von der Steuerschaltung (209) und zum Empfangen des zweiten Steuersignals gekoppelt ist.

2. Integrierter Schaltkreis nach Anspruch 1, wobei
die erste Phasenanpassungsschaltung (213) eine Schaltung zum Ausgeben einer Vielzahl von Taktsignalen aufweist, die das erste Taktsignal (214) aufweisen;
die erste Empfangsschaltung (207) eine Vielzahl von Abtastungen des Eingangssignals in Antwort auf Übergänge der Vielzahl von Taktsignalen erfasst;
die Phasensteuerschaltung (209) basierend auf der Vielzahl von Abtastungen des Eingangssignals bestimmt, ob ein Übergang des Eingangssignals vor einem Übergang des ersten Taktsignals (214) auftritt und ob der Übergang des Eingangssignals nach dem Übergang des ersten Taktsignals (214) auftritt; und
die erste Empfangsschaltung (207) und die Phasensteuerschaltung (209) in der Steuerschaltung (209) enthalten sind.

3. Integrierter Schaltkreis nach Anspruch 2, wobei das erste Steuersignal (514) ein digitales Signal mit einem von wenigstens zwei möglichen Zuständen ist, und wobei die Phasensteuerschaltung (209) eine Schaltung zum Ausgeben des ersten Steuersignals (514) in einem Zustand aufweist, der von einem eines ersten Zustandes und eines zweiten Zustandes der wenigstens zwei möglichen Zustände ausgewählt ist, basierend, wenigstens teilweise, darauf, ob der Übergang des Eingangssignals vor dem Übergang des ersten Taktsignals (214) auftritt und ob der Übergang des Eingangssignals nach dem Übergang des ersten Taktsignals (214) auftritt.

4. Integrierter Schaltkreis nach Anspruch 1, wobei das erste Steuersignal (514) ein erstes Komponentensignal (UP), das erklärt wird, wenn das erste Taktsignal (214) zu dem Eingangssignal verzögert ist, und ein zweites Komponentensignal (DN) aufweist, das erklärt wird, wenn das erste Taktsignal (214) dem Eingangssignal vorangeht.

5. Integrierter Schaltkreis nach Anspruch 1, wobei das erste Steuersignal (514) ein analoges Signal mit einem Spannungspegel ist, der die Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214) anzeigt.

6. Integrierter Schaltkreis nach Anspruch 1, wobei das erste Steuersignal (514) ein analoges Signal mit einem Strompegel ist, der die Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214) anzeigt.

7. Integrierter Schaltkreis nach Anspruch 1, wobei die Auswählschaltung (211) eine Multiplexerschaltung aufweist.

8. Betriebsverfahren für einen integrierten Schaltkreis, wobei das Verfahren aufweist:

Abtasten eines Eingangssignals in Antwort auf ein erstes Taktsignal (214), **dadurch** Generieren von Abtastungen des Eingangssignals;
Auswählen eines ersten Steuersignals (514) oder eines zweiten Steuersignals, das einer Phasenanpassungsschaltung (213) als ein ausgewähltes Steuersignal (516) auszugeben ist; und
Anpassen einer Phase eines ersten Taktsignals (214) gemäß dem ausgewählten Steuersignal (516) in der Phasenanpassungsschaltung (213)

gekennzeichnet durch
Vergleichen der Abtastungen des Eingangssignals mit einander, **dadurch**
Bestimmen einer Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214); und
Generieren des ersten Steuersignals (514) gemäß der Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214).

9. Verfahren nach Anspruch 8, ferner mit:

Ausgeben einer Vielzahl von Taktsignalen, die das erste Taktsignal (214) aufweisen;
Erfassen einer Vielzahl von Abtastungen des Eingangssignals in Antwort auf Übergänge der Vielzahl von Taktsignalen; und
Bestimmen der Phasenbeziehung zwischen dem Eingangssignal und dem ersten Taktsignal (214), wenigstens teilweise, durch Bestimmen basierend auf der Vielzahl von Abtastungen des Eingangssignals, ob ein Übergang

des Eingangssignals vor einem Übergang des ersten Taktsignals (214) auftritt und ob der Übergang des Eingangssignals nach dem Übergang des ersten Taktsignals (214) auftritt.

10. Verfahren nach Anspruch 9, wobei ein Generieren des ersten Steuersignals (514) ein Generieren eines digitalen Steuersignals aufweist, welches einen von wenigstens zwei möglichen Zuständen aufweist, basierend, wenigstens teilweise, darauf, ob der Übergang des Eingangssignals vor dem Übergang des ersten Taktsignals (214) auftritt und ob der Übergang des Eingangssignals nach dem Übergang des ersten Taktsignals (214) auftritt.

11. Verfahren nach Anspruch 8, wobei ein Generieren des ersten Steuersignals (514) ein Generieren eines digitalen Signals aufweist, welches erste und zweite Komponentensignale aufweist, wobei das erste Komponentensignal (UP) erklärt wird, wenn das erste Taktsignal (214) gegenüber dem Eingangssignal verzögert ist, und das zweite Komponentensignal (DN) erklärt wird, wenn das erste Taktsignal (214) dem Eingangssignal vorangeht.

12. Verfahren nach Anspruch 8, ferner mit einem Empfangen des Auswählsignals (212) von einer Vorrichtung, die extern zu dem integrierten Schaltkreis ist.

13. Verfahren nach Anspruch 8, ferner mit einem Speichern eines Moduswertes in einem programmierbaren Register (215) innerhalb des intergierten Schaltkreises, und wobei ein Generieren des ausgewählten Steuersignals (516) ein Generieren des Auswählsignals (212) gemäß dem Moduswert aufweist.

14. Verfahren nach Anspruch 8, ferner mit
Empfangen eines Befehls zum Speichern eines Moduswertes; und
Speichern des Moduswertes in einem Register (215) innerhalb des integrierten Schaltkreises; und
wobei ein Generieren des ausgewählten Steuersignals (516) ein Generieren des Auswählsignals (212) gemäß dem Moduswert aufweist.

15. Integrierte Schaltkreisvorrichtung mit einem integrierten Schaltkreis (205) wie in Anspruch 1 beansprucht, mit einer ersten CDR-Schaltung (205 (1)) zum Rückgewinnen von Takt- und Datensignalen von einer ersten Signalleitung (200 (1)), wobei die Steuerschaltung (209) eine erste Phasensteuerschaltung (209 (1)) zum Generieren des ersten Steuersignals aufweist,
wobei die integrierte Schaltkreisvorrichtung ferner aufweist:

eine zweite Taktdatenrückgewinnungs-(CDR)Schaltung (205 (0)) zum Rückgewinnen von Takt- und Datensignalen von einer zweiten Signalleitung (200 (0)), wobei die zweite CDR-Schaltung (205 (0)) aufweist:

eine zweite Phasensteuerschaltung (209 (0)) zum Generieren des zweiten Steuersignals, und
eine zweite Phasenanpassungsschaltung (213(0)) zum Anpassen der Phase eines zweiten rückgewonnenen Taktsignals (210 (0)) in Antwort auf das zweite Steuersignal (514).

16. Integrierte Schaltkreisvorrichtung nach Anspruch 15, wobei die Auswählschaltung (211 (1)) eine Multiplexerschaltung mit einem Steuereingang aufweist, der zum Empfangen des Auswählsignals (212 (1)) gekoppelt ist, und mit entsprechenden Eingangsanschlüssen, die zum Empfangen der ersten und zweiten Steuersignale von den ersten und zweiten Phasensteuerschaltung (209 (0)), (209 (1)) gekoppelt sind.

17. Integrierte Schaltkreisvorrichtung nach Anspruch 15, ferner mit zusätzlichen CDR-Schaltungen (205 (N-1)), wobei jede eine entsprechende Phasensteuerschaltung (209 (N-1)), eine Auswählschaltung und eine Phasenanpassungsschaltung (213 (N-1)) aufweist, wobei die Auswählschaltung (211 (N-1)) jeder der zusätzlichen CDR-Schaltungen (205 (N-1)) auf einen Steuereingang zum Ausgeben, als ein ausgewähltes Steuersignal, von einem des zweiten Phasensteuersignals und eines Phasensteuersignals antwortet, welches durch die Phasensteuerschaltung (209 (N-1)) der zusätzlichen CDR-Schaltung (205 (N-1)) ausgegeben ist, wobei die Phasenanpassungsschaltung (213 (N-1)) jeder der zusätzlichen CDR-Schaltungen (205 (N-1)) auf das ausgewählte Steuersignal, welches durch die Auswählschaltung (211 (N-1)) für die zusätzliche CDR-Schaltung (205 (N-1)) ausgegeben ist, zum Anpassen der Phase eines entsprechenden rückgewonnenen Taktsignals (210 (N-1)) antwortet.

18. Integrierte Schaltkreisvorrichtung nach Anspruch 15, wobei
die erste Empfangsschaltung (207 (1)) das Eingangssignal auf der ersten Signalleitung (201 (1)) abtastet, und
die zweite CDR-Schaltung (205 (0)) ferner eine zweite Empfangsschaltung (207 (0)) zum Abtasten eines Eingangssignals auf der zweiten Signalleitung (200 (0)) in Antwort auf das zweite rückgewonnene Taktsignal (210 (0)) aufweist.

19. Integrierte Schaltkreisvorrichtung nach Anspruch 1 oder 15, ferner mit einem Eingang zum Empfangen des Auswählsignals (212) von einer externen Vorrichtung.

20. Integrierte Schaltkreisvorrichtung nach Anspruch 1 oder 15, ferner mit einem programmierbaren Register zum Speichern eines Moduswertes, wobei das Auswählsignal (212) einen eines ersten Zustands oder zweiten Zustands gemäß dem Moduswert aufweist, und wobei die Auswählschaltung (211) eine Schaltung zum Auswählen des ersten Steuersignals, wenn das Auswählsignal (212) in dem ersten Zustand ist, und zum Auswählen des zweiten Steuersignals aufweist, wenn das Auswählsignal (212) in dem zweiten Zustand ist.

21. Integrierte Schaltkreisvorrichtung nach Anspruch 15, wobei die Auswählschaltung (211) auf das Auswählsignal (212) zum Abschalten einer Generation des zweiten Steuersignals antwortet, wenn das Auswählsignal (212) anzeigt, dass die Auswählschaltung (211) das erste Steuersignal ausgeben soll, welches als das ausgewählte Steuersignal auszugeben ist.

22. Ein Verfahren zum Steuern für den integrierten Schaltkreis nach Anspruch 1, wobei das Verfahren aufweist:

Ausgeben eines ersten Befehls an den integrierten Schaltkreis zum Einstellen einer ersten Taktdatenrückgewinnungs-(CDR)Schaltung (205 (1)) innerhalb des integrierten Schaltkreises auf einen ersten Modus, wobei die erste CDR-Schaltung (205 (1)) eine erste Auswählschaltung (211 (1)) zum Auswählen eines ersten Steuersignals zum Anpassen der Phase eines ersten Taktsignals (210 (1)) aufweist, wenn die erste CDR-Schaltung (205 (1)) in dem ersten Modus ist;
Verzögern um ein erstes Zeitintervall; und
Ausgeben, nach dem ersten Zeitintervall, eines zweiten Befehls an den integrierten Schaltkreis zum Einstellen der ersten CDR-Schaltung (205 (1)) auf einen zweiten Modus, wobei die Auswählschaltung der ersten CDR-Schaltung (205 (1)) ein zweites Steuersignal auswählt, wenn die erste CDR-Schaltung (205 (1)) in dem zweiten Modus ist,

gekennzeichnet durch
Generieren des zweiten Steuersignals in einer zweiten CDR-Schaltung (205 (0)).

23. Verfahren nach Anspruch 22, wobei ein Verzögern für das erste Zeitintervall ein Verzögern aufweist, bis eine bestimmte Anzahl von Zyklen eines Taktsignals vergangen ist.

24. Verfahren nach Anspruch 22, wobei ein Ausgeben des ersten Befehles an den integrierten Schaltkreis (205 (1)) zum Einstellen der ersten CDR-Schaltung auf den ersten Modus ein Ausgeben eines Befehls an den integrierten Schaltkreis zum Speichern eines Moduswertes in einem programmbierbaren Register (215) innerhalb des integrierten Schaltkreises aufweist, wobei der Moduswert den ersten Modus anzeigt.

25. Verfahren nach Anspruch 22, wobei ein Ausgeben des ersten Befehls an den integrierten Schaltkreis zum Einstellen der ersten CDR-Schaltung (205 (1)) auf den ersten Modus ein Ausgeben eines Modussignals an den integrierten Schaltkreis aufweist, wobei das Modussignal einem Auswähleingang der Auswählschaltung (211 (1)) zum Auswählen des ersten Steuersignals eingegeben wird.

26. Verfahren nach Anspruch 22, ferner mit einem periodischen Wiederholen des Ausgebens des ersten Befehls an den integrierten Schaltkreis, Verzögern für das erste Zeitintervall, und Ausgeben des zweiten Befehls an den integrierten Schaltkreis.

27. Verfahren nach Anspruch 22, ferner mit:

Erkennen eines vorbestimmten Zustandes; und
in Antwort auf das Bestimmen des vorbestimmten Zustandes, Wiederholen des Ausgebens des ersten Befehls an den integrierten Schaltkreis, Verzögern für das erste Zeitintervall, und Ausgeben des zweiten Befehls an den integrierten Schaltkreis.

28. Verfahren nach Anspruch 27, wobei das Erkennen des vorbestimmten Zustandes ein Erkennen einer Veränderung in einer Temperatur aufweist.

29. Verfahren nach Anspruch 27, wobei das Erkennen des vorbestimmten Zustandes ein Erkennen einer Veränderung

in einer Spannung aufweist.

30. Verfahren nach Anspruch 27, wobei das Erkennen des vorbestimmten Zustandes ein Erkennen eines Verlustes einer Synchronisation zwischen dem ersten Taktsignal (210 (1)) und einem Datensignal aufweist, welches in der ersten CDR-Schaltung (205 (1)) empfangen ist.

31. Ein System mit einem integrierten Schaltkreis (205), wie in Anspruch 1 beansprucht ist, wobei das System ferner aufweist:

eine erste Signalleitung (200 (1)), die das Eingangssignal bereitstellt;
eine Empfangsvorrichtung (203), die mit der ersten Signalleitung (200 (1)) gekoppelt ist, wobei die Empfangsvorrichtung (203) den integrierten Schaltkreis (205) als einen ersten Taktdatenrückgewinnungs-(CDR)Schaltkreis (205 (1)) zum Rückgewinnen von Takt- und Datensignalen von der ersten Signalleitung (200 (1)) aufweist, wobei die Auswählschaltung (211 (1)) auf einen ersten Moduswert als das Auswählsignal (212 (1)) antwortet; und
eine Steuervorrichtung (201), die mit der Empfangsvorrichtung (203) gekoppelt ist, zum Bereitstellen des ersten Moduswertes dazu.

32. System nach Anspruch 31, wobei die Steuervorrichtung (201) zum Bereitstellen des ersten Moduswertes an die Empfangsvorrichtung (203) über die erste Signalleitung (200 (1)) gekoppelt ist.

33. System nach Anspruch 31, ferner mit wenigstens einer zusätzlichen Signalleitung (200 (0)), wobei die wenigstens eine zusätzliche Signalleitung (200 (0)) mit der Empfangsvorrichtung (203) und der Steuervorrichtung (201) gekoppelt ist, wobei die Steuervorrichtung (201) einen ersten Moduswert an die Empfangsvorrichtung (203) über die wenigstens eine zusätzliche Signalleitung (200 (0)) bereitstellt.

34. System nach Anspruch 31, wobei die Steuervorrichtung (201) zum Ausgeben des ersten Moduswertes an die Empfangsvorrichtung (203) und dann, nach einem ersten Zeitintervall, zum Ausgeben eines zweiten Moduswertes als das Auswählsignal (212 (1)) zu der Empfangsvorrichtung (203) geeignet ist, wobei die Auswählschaltung (211 (1)) auf den ersten Moduswert zum Auswählen des ersten Steuersignals antwortet, das als das Auswählsteuersignal auszugeben ist, wobei die Auswählschaltung (211 (1)) auf den zweiten Moduswert zum Auswählen des zweiten Steuersignals antwortet, das als das Auswählsteuersignal auszugeben ist.

35. System nach Anspruch 34, ferner mit einer zweiten Signalleitung (200 (0)), die mit der Empfangsvorrichtung (203) gekoppelt ist, und wobei die Empfangsvorrichtung (203) eine zweite CDR-Schaltung (205 (0)) zum Rückgewinnen von Takt- und Datensignalen von der zweiten Signalleitung (200(0)) aufweist, wobei die zweite CDR-Schaltung (205 (0)) eine Steuerschaltung (209) zum Generieren des zweiten Steuersignals gemäß einer Phasenbeziehung zwischen einem Eingangssignal auf der zweiten Signalleitung (200 (0)) und einem zweiten Taktsignal (210 (0)) aufweist.

36. System nach Anspruch 31, wobei die Empfangsvorrichtung (203) in dem ersten integrierten Schaltkreis implementiert ist und die Steuervorrichtung (201) in einem zweiten integrierten Schaltkreis implementiert ist.

37. System nach Anspruch 36, wobei die ersten und zweiten integrierten Schaltkreise in separaten integrierten Schaltkreiseinheiten angeordnet sind.

38. System nach Anspruch 36, wobei die ersten und zweiten integrierten Schaltkreise in derselben integrierten Schaltkreiseinheit angeordnet sind.

39. System nach Anspruch 31, wobei die Empfangsvorrichtung (203) und die Steuervorrichtung (201) innerhalb eines einzigen integrierten Schaltkreises implementiert sind.

40. Verfahren eines Testens des integrierten Schaltkreises von Anspruch 1, der eine Taktdatenrückgewinnungs-(CDR) Schaltung (1005, 1205) und einen Phasensteueranschluss aufweist, wobei das Verfahren aufweist:

Ausgeben eines Befehls an den integrierten Schaltkreis zum Einstellen der CDR-Schaltung (1005, 1205) auf einen Modus eines Betriebs;
Anpassen der Phase eines Taktsignals (1010, 1210) gemäß eines Steuersignals (1014, 1214), welches durch eine Phasenanpassungsschaltung (1013, 1213) innerhalb der CDR-Schaltung (1005, 1205) verwendet wird; und
Ausgeben eines Phasensteuersignals an den Phasensteueranschluss des integrierten Schaltkreises zum An-

passen der Phase des Taktsignals (1010, 1210)

gekennzeichnet durch
Auswählen, in einer Auswählschaltung (1011,1211) der CDR-Schaltung (1005, 1205), des Phasensteueranschlusses zum Beziehen eines Steuersignals anstelle einer Phasensteuerschaltung (1009, 1209) innerhalb der CDR-Schaltung (1005, 1205) gemäß dem Modus eines Betriebs.

41. Verfahren nach Anspruch 40, wobei ein Ausgeben des Befehls an den integrierten Schaltkreis zum Einstellen der CDR-Schaltung (1205) auf den Modus eines Betriebs ein Ausgeben eines Befehls an den integrierten Schaltkreis zum Speichern eines Moduswertes in einem programmbierbaren Register (1215) innerhalb des integrierten Schaltkreises aufweist, wobei der Moduswert den Modus eines Betriebs anzeigt.

42. Verfahren nach Anspruch 40, wobei ein Ausgeben des Befehls an den integrierten Schaltkreis zum Einstellen der CDR-Schaltung (1005, 1205) auf einen Modus eines Betriebs ein Ausgeben eines Modussignals (1012, 1212) an den integrierten Schaltkreis aufweist, wobei das Modussignal einem Auswähleingang der Auswählschaltung (1011,1211) zum Auswählen des Phasensteueranschlusses zum Beziehen des Steuersignals (1014, 1214) eingegeben wird.

43. Verfahren zum Testen eines integrierten Schaltkreises nach Anspruch 40, wobei
ein Ausgeben des Phasensteuersignals an den Phasensteueranschluss des integrierten Schaltkreises zum Anpassen der Phase des Taktsignals (1010, 1210) ein Erklären des Phasensteuersignals an dem Phasensteueranschluss des integrierten Schaltkreises für ein erstes vorbestimmtes Zeitintervall aufweist, wobei die Phasenanpassungsschaltung (1013) innerhalb der CDR-Schaltung (1005) auf das Phasensteuersignal zum Anpassen der Phase des Taktsignals (1010) antwortet;
wobei das Verfahren ferner aufweist:

Nichterklären des Phasensteuersignals für ein zweites vorbestimmtes Zeitintervall; und
Messen des Taktsignals (1010) innerhalb einer Signalmessvorrichtung (1004) während eines Wiederholens eines Erklärens eines Phasensteuersignals und Nichterklärens des Phasensteuersignals wenigstens bis die Phase des Taktsignals (1010) um einen vorbestimmten Teil eines Zyklus des Taktsignals (1010) fortgeschritten ist.

44. Verfahren nach Anspruch 43, wobei der vorbestimmte Teil eines Zyklus des Taktsignals (1010) ein gesamter Zyklus des Taktsignals (1010) ist.

45. Verfahren nach Anspruch 43, wobei die Phasenanpassungsschaltung (1013) auf eine Erklärung des Steuersignals (1014) durch Fortschreiten der Phase des Taktsignals (1010) antwortet.

46. Verfahren nach Anspruch 43, wobei das erste vorbestimmte Zeitintervall zum Erlauben der Phasenanpassungsschaltung (1013) zum Fortschreiten der Phase des Taktsignals (1010) um einen vorbestimmten Phasenwinkel ausgewählt wird.

47. Verfahren nach Anspruch 43, wobei ein Messen des Taktsignals (1010) mit einer Signalmessvorrichtung (1004) ein Messen des Taktsignals (1010) mit einem Oszilloskop aufweist.

48. Integrierte Schaltkreisvorrichtung mit einem integrierten Schaltkreis, wie er in Anspruch 1 beansprucht ist, mit einer Taktdatenrückgewinnungs-(CDR)Schaltung (1205), wobei die integrierte Schaltkreisvorrichtung ferner aufweist:

einen ersten Signalgenerator (1223) zum Generieren des Eingangssignals als ein erstes Testsignal (1218); und
eine Vergleichschaltung (1231) zum Vergleichen von Abtastungen des ersten Testsignals (1218) mit einem Vergleichsignal (1224);

wobei die Empfangsschaltung (1207) einen Eingang aufweist, der schaltbar zum Empfangen des ersten Testsignals (1218) von dem ersten Signalgenerator (1223) gekoppelt ist.

49. Integrierte Schaltkreisvorrichtung nach Anspruch 48, wobei der erste Signalgenerator (1223) ein Linearrückkopplungsschieberegister ist und das erste Testsignal (1218) eine Pseudozufallsbitsequenz ist.

50. Integrierte Schaltkreisvorrichtung nach Anspruch 48, ferner mit einer Übertragungsschaltung (1227) mit einem Eingang und einem Ausgang, wobei der Eingang der Übertragungsschaltung schaltbar zum Empfangen des ersten Testsignals (1218) von dem ersten Signalgenerator (1223) gekoppelt ist, und der Ausgang der Übertragungsschaltung schaltbar mit dem Eingang der Empfangsschaltung (1207) gekoppelt ist.

51. Integrierte Schaltkreisvorrichtung nach Anspruch 48, ferner mit einer Modussteuerschaltung (209) zum Speichern eines Moduswertes, der einen Betriebsmodus der integrierten Schaltkreisvorrichtung anzeigt, wobei die Modussteuerschaltung (209) ein Testmodussignal (1217) ausgibt, wenn der Moduswert einen Testmodus eines Betriebs anzeigt, wobei das Testmodussignal den Eingang der Empfangsschaltung (1207) schaltet, die zum Empfangen des ersten Testsignals (1218) zu koppeln ist.

52. Integrierte Vorrichtung nach Anspruch 48, wobei die Vergleichschaltung (1231) einen zweiten Signalgenerator (1233) zum Generieren des Vergleichsignals (1224) aufweist.

53. Integrierte Schaltkreisvorrichtung nach Anspruch 48, wobei der erste Signalgenerator (1223) und der zweite Signalgenerator (1233) zum Generieren von identischen Signalen ausgestaltet sind.

54. Integrierte Schaltkreisvorrichtung nach Anspruch 48, wobei der erste Signalgenerator (1223) zum Bereitstellen des ersten Testsignals (1218) zu der Vergleichschaltung (1231) gekoppelt ist, wobei das Vergleichsignal (1224) das erste Testsignal (1218) ist.

55. Verfahren eines Testens eines integrierten Schaltkreises nach Anspruch 40, wobei das Verfahren ferner aufweist:

Eingeben eines Testsignals (1218) an einen Empfänger (1207) der CDR-Schaltung (1205);
Vergleichen des Testsignals (1218) gegen Abtastungen des Testsignals (1218), die durch die CDR-Schaltung (1205) generiert sind;
Erklären eines Fehlersignals (1216) wenn das Testsignal (1218) nicht mit den Abtastungen übereinstimmt; und
Wiederholen eines Vergleichens des Testsignals (1218), Erklären eines Fehlersignals (1216) und Erklären eines Phasensteuersignals zum Bestimmen einer Maximumphase und einer Minimumphase des Taktsignals für das das Fehlersignal (1216) nicht erklärt wird.

Revendications

1. Circuit intégré comprenant :

un premier circuit de réception (207) pour échantillonner un signal d'entrée en réponse à un premier signal d'horloge (214) générant ainsi des échantillons du signal d'entrée ;
un circuit de sélection (211) qui est sensible à un signal de sélection (212) pour sélectionner l'un d'un premier signal de commande (514) et d'un second signal de commande devant être délivré comme signal de commande sélectionné (516) ; et
un premier circuit de réglage de phase (213) couplé pour recevoir le signal de commande sélectionné (516) du circuit de sélection (211), le premier circuit de réglage de phase (213) étant sensible au signal de commande sélectionné (516) pour régler la phase du premier signal d'horloge (214) ;

caractérisé par
un circuit de commande (209) comparant les échantillons du signal d'entrée les uns avec les autres, générant ainsi le premier signal de commande (514) selon une relation de phase entre le signal d'entrée et le premier signal d'horloge (214) ; dans lequel le circuit de sélection (211) est couplé pour recevoir le premier signal de commande (514) du circuit de commande (209) et couplé pour recevoir le second signal de commande.

2. Circuit intégré selon la revendication 1, dans lequel
le premier circuit de réglage de phase (213) comprend un circuit pour délivrer une pluralité de signaux d'horloge comprenant le premier signal d'horloge (214) ;
le premier circuit de réception (207) capture une pluralité d'échantillons du signal d'entrée en réponse à des transitions de la pluralité de signaux d'horloge ;
le circuit de commande de phase (209) détermine, sur la base de la pluralité d'échantillons du signal d'entrée, si une transition du signal d'entrée a lieu avant une transition du premier signal d'horloge (214) et si la transition du

signal d'entrée a lieu après la transition du premier signal d'horloge (214) ; et
le premier circuit de réception (207) et le circuit de commande de phase (209) sont compris dans le circuit de commande (209).

3. Circuit intégré selon la revendication 2, dans lequel le premier signal de commande (514) est un signal numérique ayant l'un d'au moins deux états possibles, et dans lequel le circuit de commande de phase (209) comprend un circuit pour délivrer le premier signal de commande (514) dans un état sélectionné entre l'un d'un premier état et d'un second état des au moins deux états possibles sur la base, au moins en partie, du fait que la transition du signal d'entrée a lieu avant la transition du premier signal d'horloge (214) et que la transition du signal d'entrée a lieu après la transition du premier signal d'horloge (214).

4. Circuit intégré selon la revendication 1, dans lequel le premier signal de commande (514) comprend un premier signal de composant (UP) qui est rendu actif lorsque le premier signal d'horloge (214) est derrière le signal d'entrée et un second signal de composant (DN) qui est rendu actif lorsque le premier signal d'horloge (214) est devant le signal d'entrée.

5. Circuit intégré selon la revendication 1, dans lequel le premier signal de commande (514) est un signal analogique ayant un niveau de tension indicatif de la relation de phase entre le signal d'entrée et le premier signal d'horloge (214).

6. Circuit intégré selon la revendication 1, dans lequel le premier signal de commande (514) est un signal analogique ayant un niveau de courant indicatif de la relation de phase entre le signal d'entrée et le premier signal d'horloge (214)

7. Circuit intégré selon la revendication 1, dans lequel le circuit de sélection (211) comprend un circuit de multiplexage.

8. Procédé de fonctionnement d'un circuit intégré, le procédé comprenant :

l'échantillonnage d'un signal d'entrée en réponse à un premier signal d'horloge (214) générant ainsi des échantillons du signal d'entrée ;
la sélection entre un premier signal de commande (514) et un second signal de commande devant être délivré à circuit de réglage de phase (213) en tant que signal de commande sélectionné (516) ; et
le réglage, dans le circuit de réglage de phase (213), d'une phase d'un premier signal d'horloge (214) selon le signal de commande sélectionné (516)

caractérisé par
la comparaison des échantillons du signal d'entrée les uns avec les autres, déterminant ainsi une relation de phase entre le signal d'entrée et le premier signal d'horloge (214) ; et
la génération du premier signal de commande (514) selon la relation de phase entre le signal d'entrée et le premier signal d'horloge (214).

9. Procédé selon la revendication 8, comprenant en outre :

la fourniture d'une pluralité de signaux d'horloge, comprenant le premier signal d'horloge (214) ;
la capture d'une pluralité d'échantillons du signal d'entrée en réponse à des transitions de la pluralité de signaux d'horloge ; et
la détermination de la relation de phase entre le signal d'entrée et le premier signal d'horloge (214), au moins en partie, en déterminant, sur la base de la pluralité d'échantillons du signal d'entrée, si une transition du signal d'entrée a lieu avant une transition du premier signal d'horloge (214) et si la transition du signal d'entrée a lieu après la transition du premier signal d'horloge (214).

10. Procédé selon la revendication 9, dans lequel la génération du premier signal de commande (514) comprend la génération d'un signal de commande numérique ayant l'un de deux états possibles sur la base, au moins en partie, du fait que la transition du signal d'entrée a lieu avant la transition du premier signal d'horloge (214) et du fait que la transition du signal d'entrée a lieu après la transition du premier signal d'horloge (214).

11. Procédé selon la revendication 8, dans lequel la génération du premier signal de commande (514) comprend la génération d'un signal numérique ayant des premier et second signaux de composant, le premier signal de composant (UP) étant rendu actif lorsque le premier signal d'horloge (214) est derrière le signal d'entrée et le second signal de composant (DN) étant rendu actif lorsque le premier signal d'horloge (214) est devant le signal d'entrée.

12. Procédé selon la revendication 8, comprenant en outre la réception du signal de sélection (212) depuis un dispositif qui est extérieur au circuit intégré.

13. Procédé selon la revendication 8, comprenant en outre le stockage d'une valeur de mode dans un registre programmable (215) à l'intérieur du circuit intégré, et dans lequel la génération du signal de commande sélectionné (516) comprend la génération du signal de sélection (212) selon la valeur de mode.

14. Procédé selon la revendication 8, comprenant en outre
la réception d'une commande pour stocker une valeur de mode ; et
le stockage de la valeur de mode dans un registre (215) dans le circuit intégré ; et
dans lequel la génération du signal de commande sélectionné (516) comprend la génération du signal de sélection (212) selon la valeur de mode.

15. Dispositif de circuit intégré comprenant un circuit intégré (205) selon la revendication 1, comprenant un premier circuit CDR (205(1)) pour récupérer des signaux d'horloge et de données à partir d'une première ligne de signal (200(1)), dans lequel le circuit de commande (209) comprend un premier circuit de commande de phase (209(1)) pour générer le premier signal de commande,
le dispositif de circuit intégré comprenant en outre :

un second circuit de récupération de données d'horloge (CDR) (205(0)) pour récupérer des signaux d'horloge et de données à partir d'une seconde ligne de signal (200(0)), le second circuit CDR (205(0)) comprenant :

un second circuit de commande de phase (209(0)) pour générer le second signal de commande, et
un second circuit de réglage de phase (213(0)) pour régler la phase d'un second signal d'horloge récupéré (210(0)) en réponse au second signal de commande (514).

16. Dispositif de circuit intégré selon la revendication 15, dans lequel le circuit de sélection (211(1)) comprend un circuit de multiplexage ayant une entrée de commande couplée pour recevoir le signal de sélection (212(1)) et ayant des ports d'entrée respectifs couplés pour recevoir les premier et second signaux de commande depuis les premier et second circuits de commande (209(0), 209(1)).

17. Dispositif de circuit intégré selon la revendication 15, comprenant en outre des circuits CDR supplémentaires (205 (N-1)) ayant chacun un circuit de commande de phase (209(N-1)), un circuit de sélection et un circuit de réglage de phase (213(N-1)) respectifs, le circuit de sélection (211(N-1)) de chacun des circuits CDR supplémentaires (205 (N-1)) étant sensible à une entrée de commande pour délivrer, comme signal de commande sélectionné, l'un du second signal de commande de phase et d'un signal de commande de phase délivré par le circuit de commande de phase (209(N-1)) du circuit CDR supplémentaire (205(N-1)), le circuit de réglage de phase (213(N-1)) de chacun des circuits CDR supplémentaires (205-N-1)) étant sensible au signal de commande sélectionné délivré par le circuit de sélection (211 (N-1)) pour le circuit CDR supplémentaire (205 (N-1)) pour régler la phase d'un signal d'horloge récupéré respectif (210 (N-1)).

18. Dispositif de circuit intégré selon la revendication 15, dans lequel
le premier circuit de réception (207(1)) échantillonne le signal d'entrée sur la première ligne de signal (200(1)), et
le second circuit CDR (205(0)) comprend en outre un second circuit de réception (207 0)) pour échantillonner un signal d'entrée sur la seconde ligne de signal (200 (0)) en réponse au second signal d'horloge récupéré (210 (0)).

19. Dispositif de circuit intégré selon la revendication 1 ou 15, comprenant en outre une entrée pour recevoir le signal de sélection (212) d'un dispositif extérieur.

20. Dispositif de circuit intégré selon la revendication 1 ou 15, comprenant en outre un registre programmable pour stocker une valeur de mode, le signal de sélection (212) ayant l'un d'un premier état et d'un second état selon la valeur de mode, et le circuit de sélection (211) comprenant un circuit pour sélectionner le premier signal de commande lorsque le signal de sélection (212) est dans le premier état et pour sélectionner le second signal de commande lorsque le signal de sélection (212) est dans le second état.

21. Dispositif de circuit intégré selon la revendication 15, dans lequel le circuit de sélection (211) est sensible au signal de sélection (212) pour désactiver la génération du second signal de commande lorsque le signal de sélection (212) indique que le circuit de sélection (211) doit sélectionner le premier signal de commande devant être délivré comme

signal de commande sélectionné.

22. Procédé de commande pour le circuit intégré selon la revendication 1, le procédé comprenant :

la fourniture d'une première commande au circuit intégré pour placer un premier circuit de récupération de données d'horloge (CDR) (205 (1)) dans le circuit intégré sur un premier mode, le premier circuit CDR (205 (1)) comprenant un circuit de sélection (211 (1)) pour sélectionner un premier signal de commande pour régler la phase d'un premier signal d'horloge (210 (1)) lorsque le premier circuit CDR (205 (1)) est dans le premier mode ; une temporisation pendant un premier intervalle de temps ; et
la fourniture, après le premier intervalle de temps, d'une seconde commande au circuit intégré pour placer le premier circuit CDR (205 (1)) sur un second mode, le circuit de sélection du premier circuit CDR (205 (1)) pour sélectionner un second signal de commande lorsque le premier circuit CDR (205 (1)) est dans le second mode,

caractérisé par
la génération du second signal de commande dans un second circuit CDR (205 0)).

23. Procédé selon la revendication 22, dans lequel la temporisation pendant le premier intervalle de temps comprend une temporisation jusqu'à ce qu'un nombre prédéterminé de cycles d'un signal d'horloge aient eu lieu.

24. Procédé selon la revendication 22, dans lequel la fourniture de la première commande au circuit intégré (205 (1)) pour placer le premier circuit CDR sur le premier mode comprend la fourniture d'une commande au circuit intégré pour stocker une valeur de mode dans un registre programmable (215) dans le circuit intégré, la valeur de mode indiquant le premier mode.

25. Procédé selon la revendication 22, dans lequel la fourniture de la première commande au circuit intégré pour placer le premier circuit CDR (205 (1)) sur le premier mode comprend la fourniture d'un signal de mode au circuit intégré, le signal de mode étant entré sur une entrée de sélection du circuit de sélection (211 (1)) pour sélectionner le premier signal de commande.

26. Procédé selon la revendication 22, comprenant en outre la répétition de manière périodique de la fourniture de la première commande au circuit intégré, la temporisation pendant le premier intervalle de temps, et la fourniture de la seconde commande au circuit intégré.

27. Procédé selon la revendication 22, comprenant en outre :

la détection d'une condition prédéterminée ; et
en réponse à la détection de la condition prédéterminée, la répétition de la fourniture de la première commande au circuit intégré, la temporisation pendant le premier intervalle de temps et la fourniture de la seconde commande au circuit intégré.

28. Procédé selon la revendication 27, dans lequel la détection de la condition prédéterminée comprend la détection d'un changement de température.

29. Procédé selon la revendication 27, dans lequel la détection de la condition prédéterminée comprend la détection d'un changement de tension.

30. Procédé selon la revendication 27, dans lequel la détection de la condition prédéterminée comprend la détection d'une perte de synchronisation entre le premier signal d'horloge (210 (1)) et le signal de données reçu dans le premier circuit CDR (205 (1)).

31. Système comprenant un circuit intégré (205) selon la revendication 1, le système comprenant en outre :

une première ligne de signal (200 (1)) fournissant le signal d'entrée ;
un dispositif de réception (203) couplé à la première ligne de signal (200 (1)), le dispositif de réception (203) comprenant le circuit intégré (205) comme premier circuit de récupération de données d'horloge CDR (205 (1)) pour récupérer les signaux d'horloge et de données à partir de la première ligne de signal (200 (1)), dans lequel le circuit de sélection (211 (1)) est sensible à une première valeur de mode comme signal de sélection (212 (1)) ; et
un dispositif de commande (201) couplé au dispositif de réception (203) pour fournir la première valeur de mode

à celui.

32. Système selon la revendication 31, dans lequel le dispositif de commande (201) est couplé pour fournir la première valeur de mode au dispositif de réception (203) via la première ligne de signal (200 (1)).

33. Système selon la revendication 31, comprenant en outre au moins une ligne de signal supplémentaire (200 (0)), la au moins une ligne de signal supplémentaire (200 (0)) couplée au dispositif de réception (203) et au dispositif de commande (201), le dispositif de commande (201) pour fournir la première valeur de mode au dispositif de réception (203) via la au moins une ligne de signal supplémentaire (200 (0)).

34. Système selon la revendication 31, dans lequel le dispositif de commande (201) sert à délivrer la première valeur de mode au dispositif de réception (203) et ensuite, après un premier intervalle de temps, à délivrer une seconde valeur de mode comme signal de sélection (212 (1)) au dispositif de réception (203), le circuit de sélection (211 (1)) étant sensible à la première valeur de mode pour sélectionner le premier signal de commande devant être délivré comme signal de commande sélectionné, le circuit de sélection (211 (1) étant sensible à une seconde valeur de mode pour sélectionner le second signal de commande devant être délivré comme signal de commande sélectionné.

35. Système selon la revendication 34, comprenant en outre une seconde ligne de signal (200 (0)) couplée au dispositif de réception (203), et dans lequel le dispositif de réception (203) comprend un second circuit CDR (205 (0)) pour récupérer les signaux d'horloge et de données à partir de la seconde ligne de signal (200 (0)), le second circuit CDR (205 (0)) comprenant un circuit de commande (209) pour générer le second signal de commande selon une relation de phase entre un signal d'entrée sur la seconde ligne de signal (200 (0)) et un second signal d'horloge (210 (0)).

36. Système selon la revendication 31, dans lequel le dispositif de réception (203) est mis en oeuvre dans un premier circuit intégré et le dispositif de commande (201) est mis en oeuvre dans un second circuit intégré.

37. Système selon la revendication 36, dans lequel les premier et second circuits intégrés sont mis sous boîtier dans des boîtiers de circuit intégré séparés.

38. Système selon la revendication 36, dans lequel les premier et second circuits intégrés sont mis sous boîtier dans le même boîtier de circuit intégré.

39. Système selon la revendication 31, dans lequel le dispositif de réception (203) et le dispositif de commande (201) sont mis en oeuvre dans un circuit intégré unique.

40. Procédé de test du circuit intégré selon la revendication 1 qui comprend un circuit de récupération de données d'horloge (CDR) (1005, 1205) et un port de commande de phase, le procédé comprenant :

la fourniture d'une commande au circuit intégré pour placer le circuit CDR (1005, 1205) sur un mode de fonctionnement ;
le réglage de la phase d'un signal d'horloge (1010, 1210) selon un signal de commande (1014, 1214) qui est utilisé par un circuit de réglage de phase (1013, 1213) dans le circuit CDR (1005, 1205) ; et
la fourniture d'un signal de commande de phase au port de commande de phase du circuit intégré pour régler la phase du signal d'horloge (1010, 1210)

caractérisé par
la sélection, dans un circuit de sélection (1011, 1211) du circuit CDR (1005, 1205), du port de commande de phase servant à fournir un signal de commande au lieu d'un circuit de commande de phase (1009, 1209) dans le circuit CDR (1005, 1205) selon le mode de fonctionnement.

41. Procédé selon la revendication 40, dans lequel la fourniture de la commande au circuit intégré pour placer le circuit CDR (1205) sur le mode de fonctionnement comprend la fourniture d'une commande au circuit intégré pour stocker une valeur de mode dans un registre programmable (1215) dans le circuit intégré, la valeur de mode indiquant le mode de fonctionnement.

42. Procédé selon la revendication 40, dans lequel la fourniture de la commande au circuit intégré pour placer le circuit CDR (1005, 1205) sur un mode de fonctionnement comprend la fourniture d'un signal de mode (1012, 1212) au

circuit intégré, le signal de mode étant entré sur une entrée de sélection du circuit de sélection (1011, 1211) pour sélectionner le port de commande de phase pour fournir le signal de commande (1014, 1214).

43. Procédé de test d'un circuit intégré selon la revendication 40, dans lequel
la fourniture du signal de commande de phase au port de commande de phase du circuit intégré pour régler la phase du signal d'horloge (1010, 1210) comprend l'activation du signal de commande de phase au niveau du port de commande de phase du circuit intégré pendant un premier intervalle de temps prédéterminé, le circuit de réglage de phase (1013) dans le circuit CDR (1005) étant sensible au signal de commande de phase pour régler la phase du signal d'horloge (1010) ;
le procédé comprenant en outre :

la désactivation du signal de commande de phase pendant le second intervalle de temps prédéterminé ; et
la mesure du signal d'horloge (1010) avec un dispositif de mesure de signal (1004) tout en répétant l'activation d'un signal de commande de phase et la désactivation du signal de commande de phase au moins jusqu'à ce que la phase du signal d'horloge (1010) ait progressé jusqu'à une partie prédéterminée d'un cycle du signal d'horloge (1010).

44. Procédé selon la revendication 43, dans lequel la partie prédéterminée d'un cycle du signal d'horloge (1010) est un cycle entier du signal d'horloge (1010).

45. Procédé selon la revendication 43, dans lequel le circuit de réglage de phase (1013) répond à l'activation du signal de commande (1014) en avançant la phase du signal d'horloge (1010).

46. Procédé selon la revendication 43, dans lequel le premier intervalle de temps prédéterminé est sélectionné pour permettre au circuit de réglage de phase (1013) d'avancer la phase du signal d'horloge (1010) d'un angle de phase prédéterminé.

47. Procédé selon la revendication 43, dans lequel la mesure du signal d'horloge (1010) avec un dispositif de mesure de signal (1004) comprend la mesure du signal d'horloge (1010) avec un oscilloscope.

48. Dispositif de circuit intégré comprenant un circuit intégré selon la revendication 1, comprenant un circuit de récupération de données d'horloge (CDR) (1205), le dispositif de circuit intégré comprenant en outre :

un premier générateur de signal (1223) pour générer le signal d'entrée comme premier signal de test (1218) ; et
un circuit de comparaison (1231) pour comparer des échantillons du premier signal de test (1218) à un signal de comparaison (1224) ;

dans lequel le circuit de réception (1207) a une entrée couplée de manière commutable pour recevoir le premier signal de test (1218) du premier générateur de signal (1223).

49. Dispositif de circuit intégré selon la revendication 48, dans lequel le premier générateur de signal (1223) est un registre à décalage à boucle fermée linéaire et le premier signal de test (1218) est une séquence de bits pseudo-aléatoire.

50. Dispositif de circuit intégré selon la revendication 48, comprenant en outre un circuit de transmission (1227) ayant une entrée et une sortie, l'entrée du circuit de transmission couplée de manière commutable pour recevoir le premier signal de test (1218) du premier générateur de signal (1223), et la sortie du circuit de transmission couplée de manière commutable à l'entrée du circuit de réception (1207).

51. Dispositif de circuit intégré selon la revendication 48, comprenant en outre un circuit de commande de mode (209) pour stocker une valeur de mode indicative d'un mode de fonctionnement du dispositif de circuit intégré, le circuit de commande de mode (209) fournissant un signal de mode de test (1217) lorsque la valeur de mode est indicative d'un mode de fonctionnement de test, le signal de mode de test commutant l'entrée du circuit de réception (1207) pour être couplée pour recevoir le premier signal de test (1218).

52. Dispositif intégré selon la revendication 48, dans lequel le circuit de comparaison (1231) comprend un second générateur de signal (1233) pour générer le signal de comparaison (1224).

53. Dispositif de circuit intégré selon la revendication 48, dans lequel le premier générateur de signal (1223) et le second générateur de signal (1233) sont conçus pour générer des signaux identiques.

54. Dispositif intégré selon la revendication 48, dans lequel le premier générateur de signal (1223) est couplé pour fournir le premier signal de test (1218) au circuit de comparaison (1231), le signal de comparaison (1224) étant le premier signal de test (1218).

55. Procédé de test d'un circuit intégré selon la revendication 40, le procédé comprenant en outre :

l'entrée d'un signal de test (1218) dans un récepteur (1207) du circuit CDR (1205) ;
la comparaison du signal de test (1218) avec des échantillons du signal de test (1218) générés par le circuit CDR (1205) ;
l'activation d'un signal d'erreur (1216) lorsque le signal de test (1218) ne correspond pas aux échantillons ; et
la répétition de la comparaison du signal de test (1218), l'activation d'un signal d'erreur (1216) et l'activation d'un signal de commande de phase pour déterminer une phase maximale et une phase minimale du signal d'horloge pour laquelle le signal d'erreur (1216) n'est pas activé.

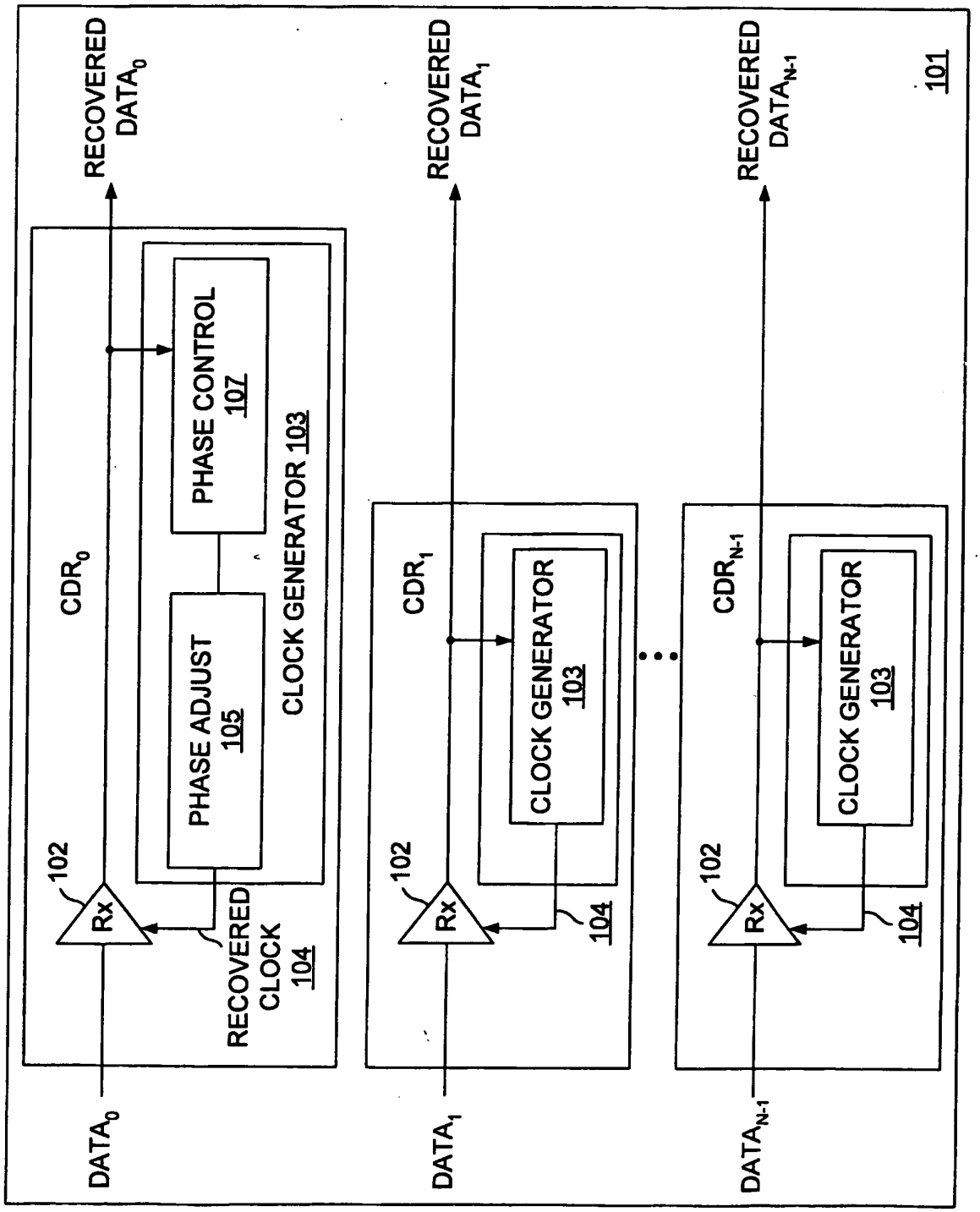


FIG. 1
(Prior Art)

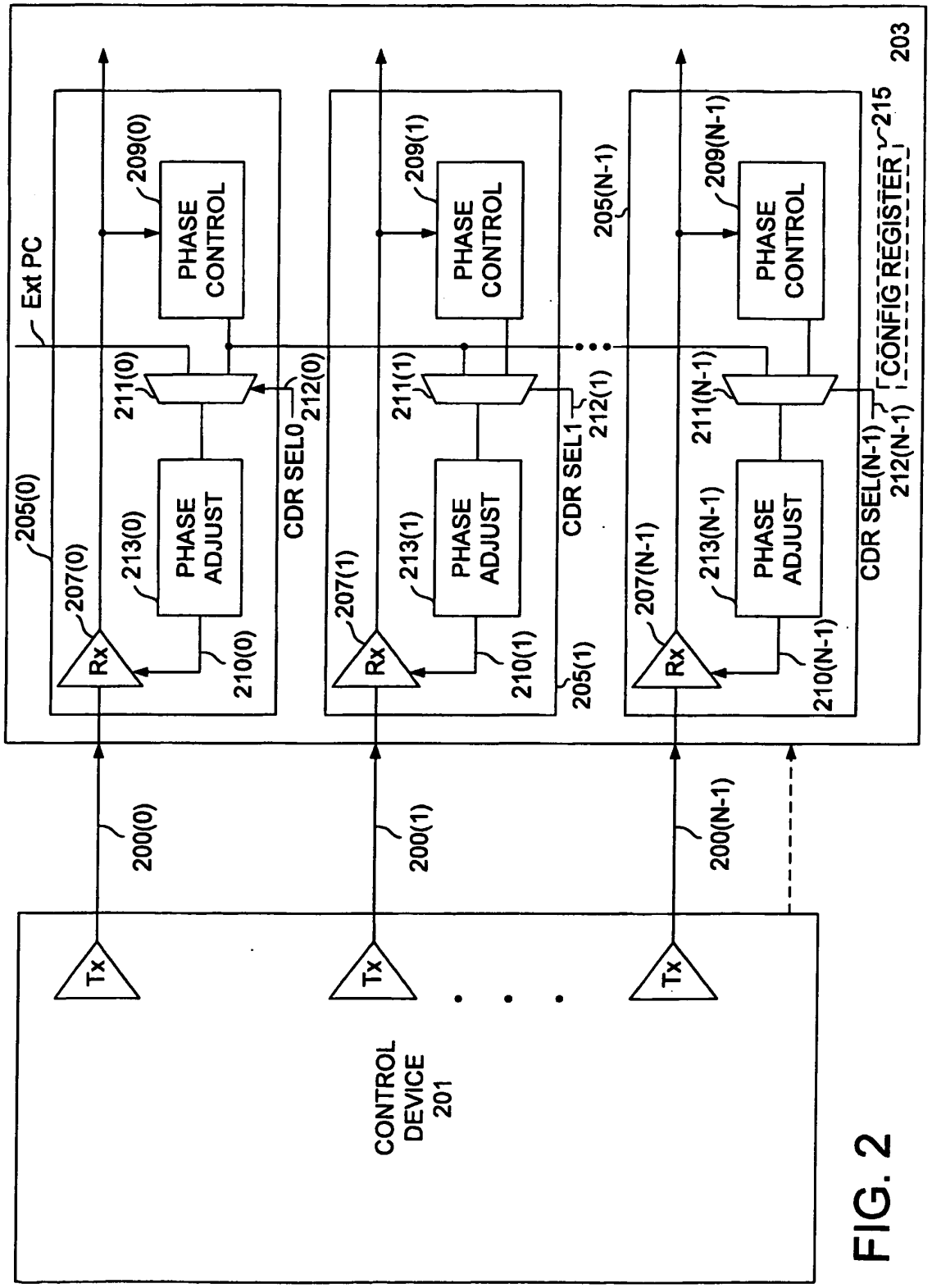

Ext PC
203
CONFIG REGISTER
215
PHASE CONTROL
PHASE ADJUST
Rx
Tx
CDR SEL0
CDR SEL1
CDR SEL(N-1)
205(0)
205(1)
205(N-1)
207(0)
207(1)
207(N-1)
209(0)
209(1)
209(N-1)
210(0)
210(1)
210(N-1)
211(0)
211(1)
211(N-1)
212(0)
212(1)
212(N-1)
213(0)
213(1)
213(N-1)
200(0)
200(1)
200(N-1)
CONTROL DEVICE 201

FIG. 2

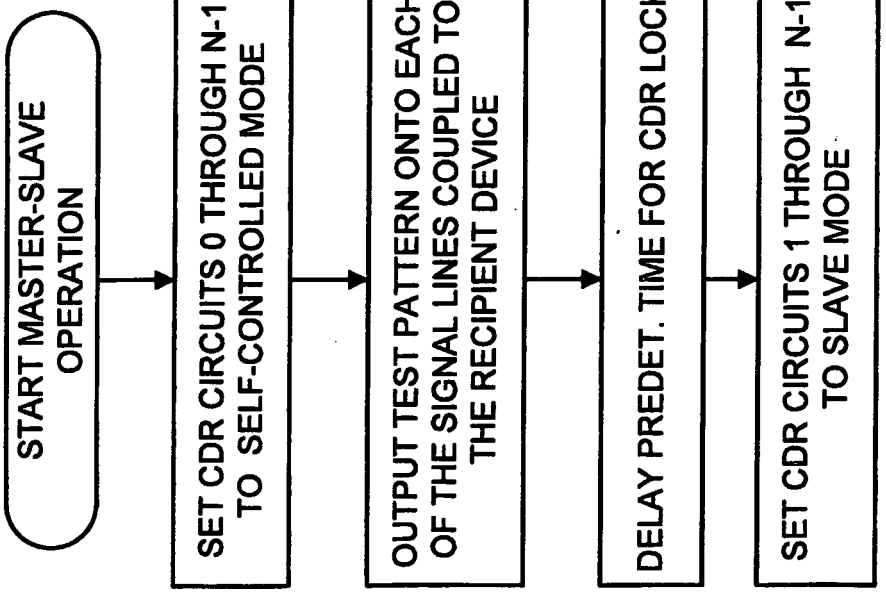

START MASTER-SLAVE OPERATION
301
SET CDR CIRCUITS 0 THROUGH N-1 TO SELF-CONTROLLED MODE
303
OUTPUT TEST PATTERN ONTO EACH OF THE SIGNAL LINES COUPLED TO THE RECIPIENT DEVICE
305
DELAY PREDET. TIME FOR CDR LOCK
307
SET CDR CIRCUITS 1 THROUGH N-1 TO SLAVE MODE

FIG. 3

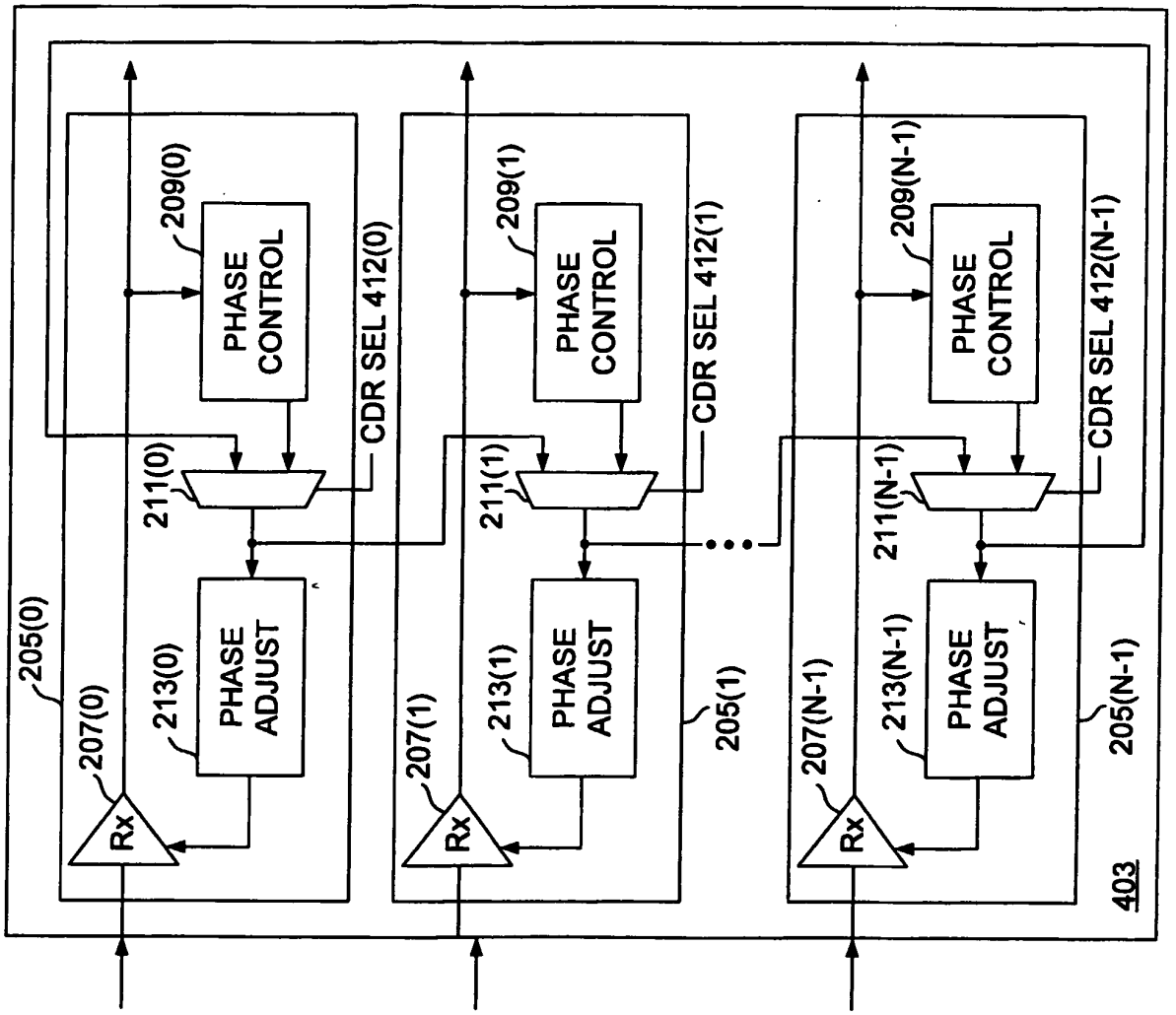

205(0)
207(0)
Rx
213(0)
PHASE ADJUST
211(0)
209(0)
PHASE CONTROL
CDR SEL 412(0)
207(1)
213(1)
205(1)
211(1)
209(1)
CDR SEL 412(1)
207(N-1)
213(N-1)
211(N-1)
209(N-1)
CDR SEL 412(N-1)
205(N-1)
403

FIG. 4

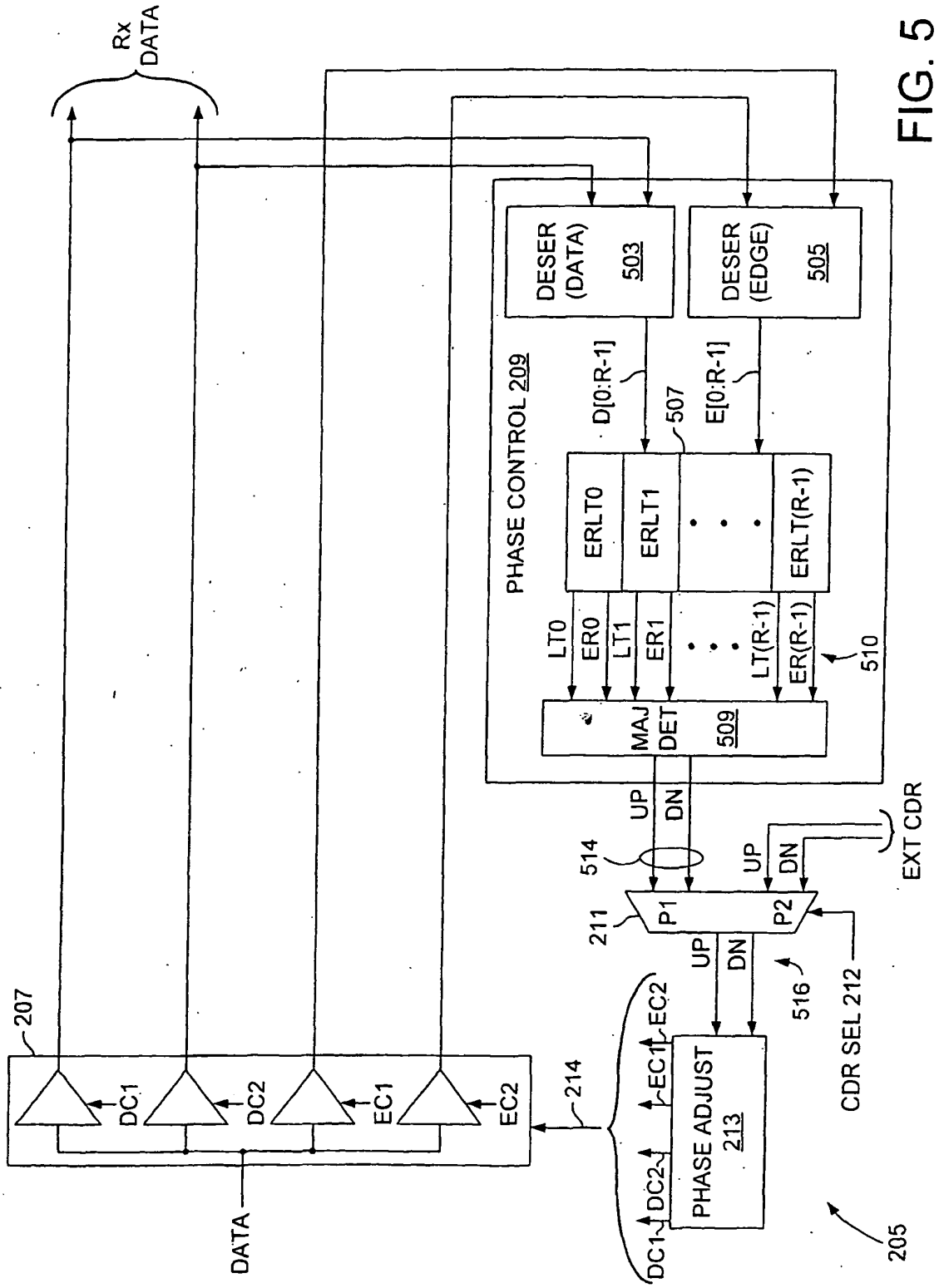

Rx DATA
DESER (DATA) 503
DESER (EDGE) 505
PHASE CONTROL 209
D[0:R-1]
E[0:R-1]
507
ERLT0
ERLT1
ERLT(R-1)
LT0
ER0
LT1
ER1
LT(R-1)
ER(R-1)
510
MAJ DET 509
UP
DN
514
EXT CDR
211
P1
P2
516
CDR SEL 212
207
DC1
DC2
EC1
EC2
214
PHASE ADJUST 213
DATA
205

FIG. 5

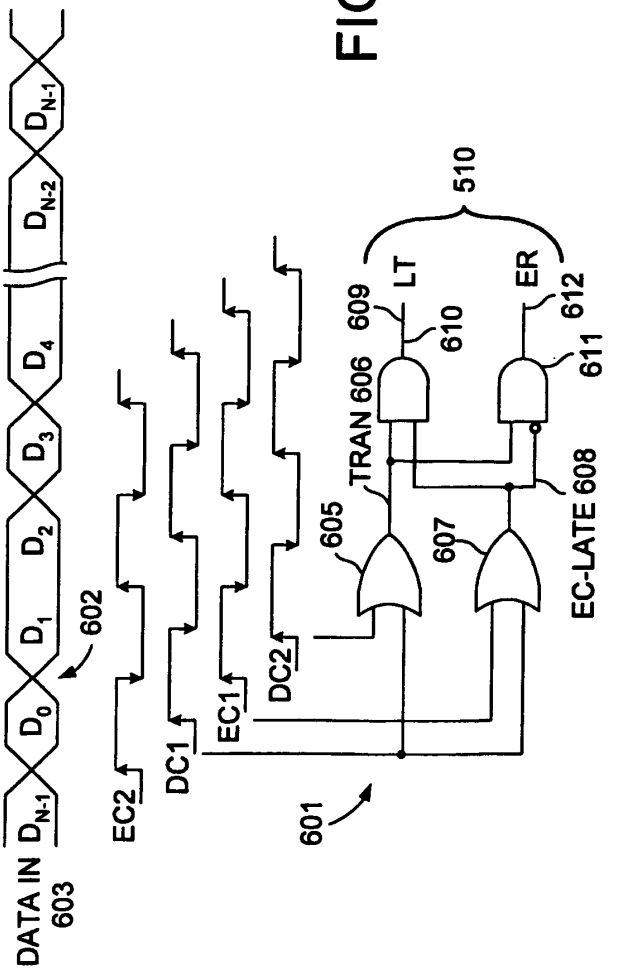


FIG. 6

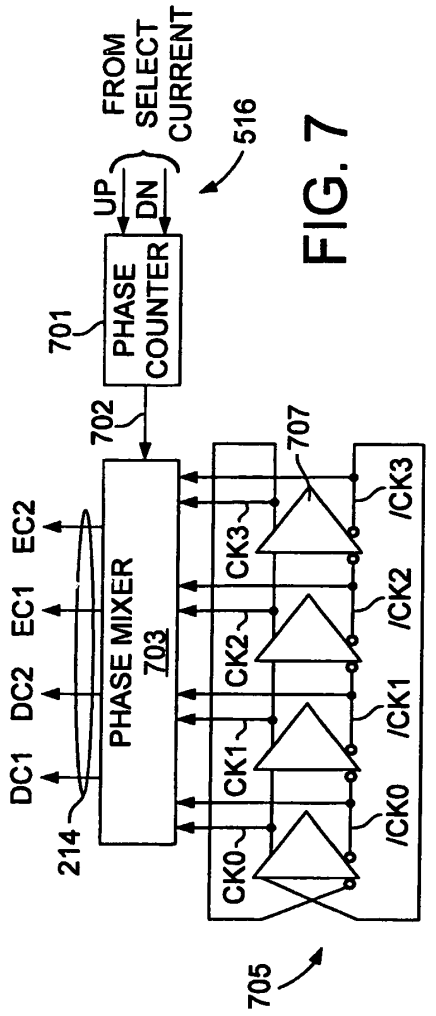


FIG. 7

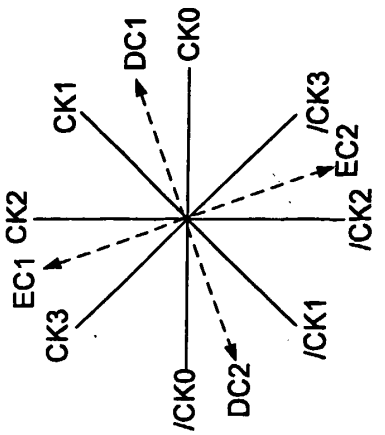


FIG. 8

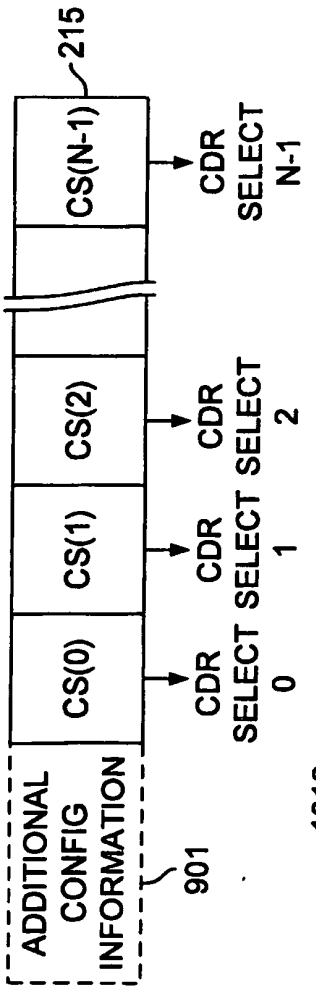

ADDITIONAL CONFIG INFORMATION
901
CS(0)
CS(1)
CS(2)
CS(N-1)
215
CDR SELECT 0
CDR SELECT 1
CDR SELECT 2
CDR SELECT N-1

FIG. 9

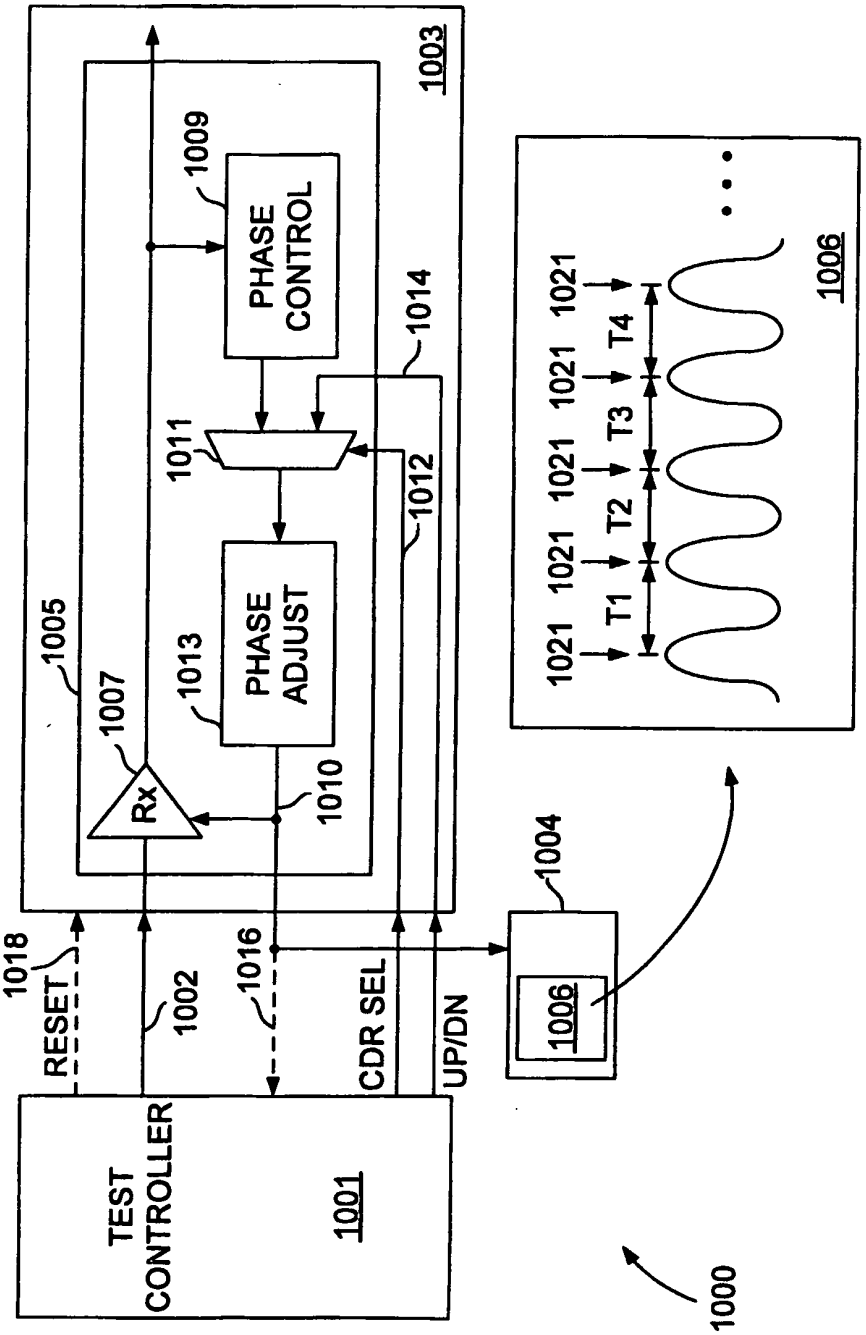
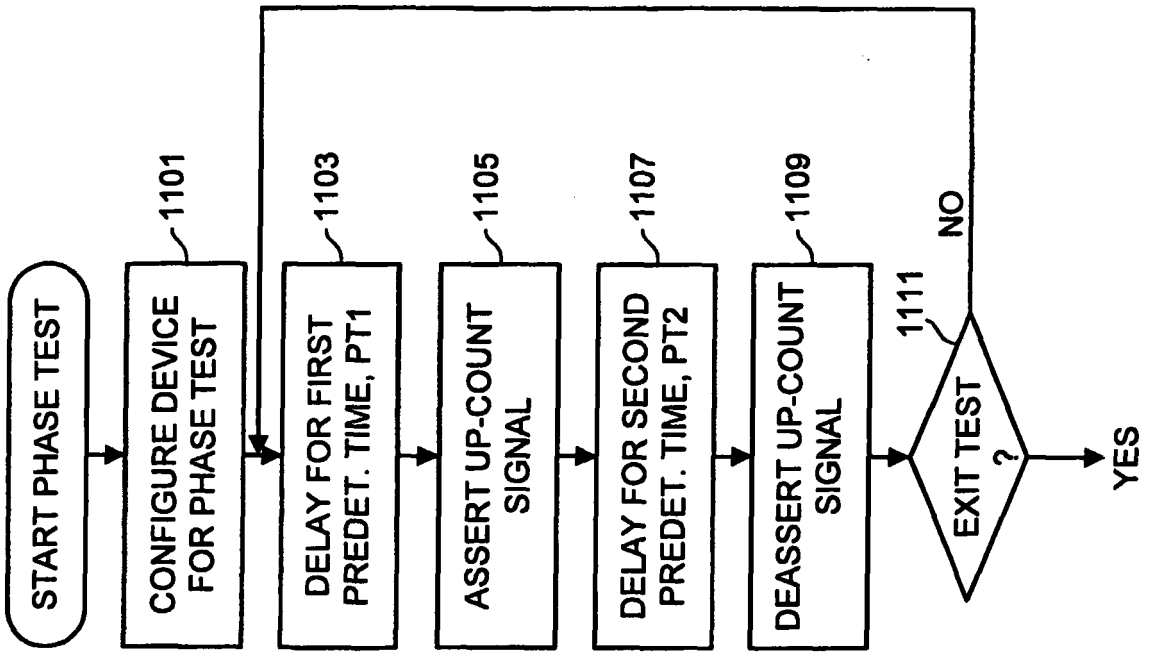

TEST CONTROLLER
1001
RESET
1018
1002
1016
CDR SEL
UP/DN
1003
1004
1005
1006
1007
Rx
1009
PHASE CONTROL
1010
1011
1012
1013
PHASE ADJUST
1014
1021
T1
T2
T3
T4
1000

FIG. 10

FIG. 11


START PHASE TEST
CONFIGURE DEVICE FOR PHASE TEST
1101
DELAY FOR FIRST PREDET. TIME, PT1
1103
ASSERT UP-COUNT SIGNAL
1105
DELAY FOR SECOND PREDET. TIME, PT2
1107
DEASSERT UP-COUNT SIGNAL
1109
EXIT TEST ?
1111
NO
YES

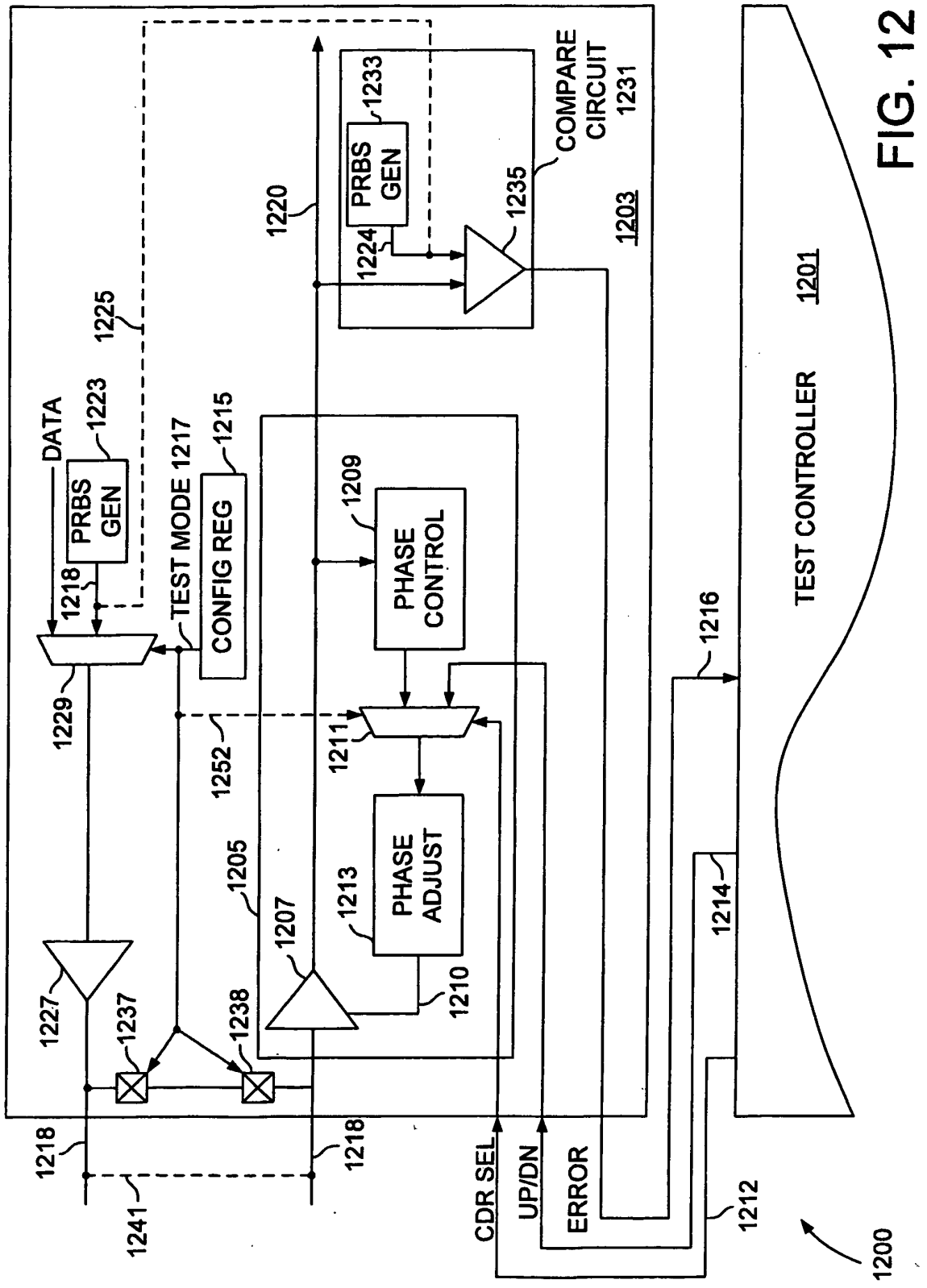

1200
1201
TEST CONTROLLER
1203
COMPARE CIRCUIT
1231
PRBS GEN
1233
1235
1224
1220
1225
DATA
1223
PRBS GEN
1218
TEST MODE 1217
CONFIG REG
1215
1209
PHASE CONTROL
1229
1211
1252
1205
1213
PHASE ADJUST
1207
1210
1227
1237
1238
1241
1218
1218
CDR SEL
UP/DN
ERROR
1216
1214
1212

FIG. 12

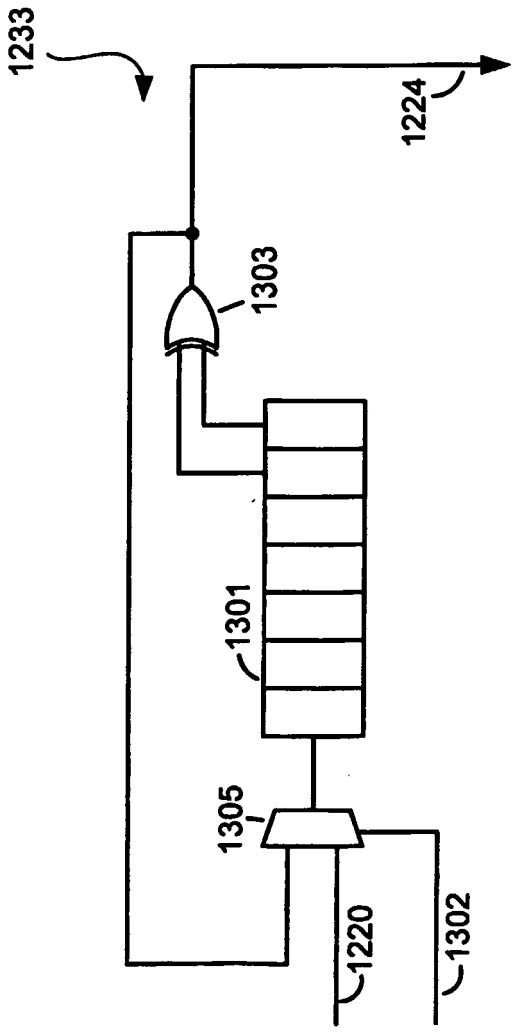
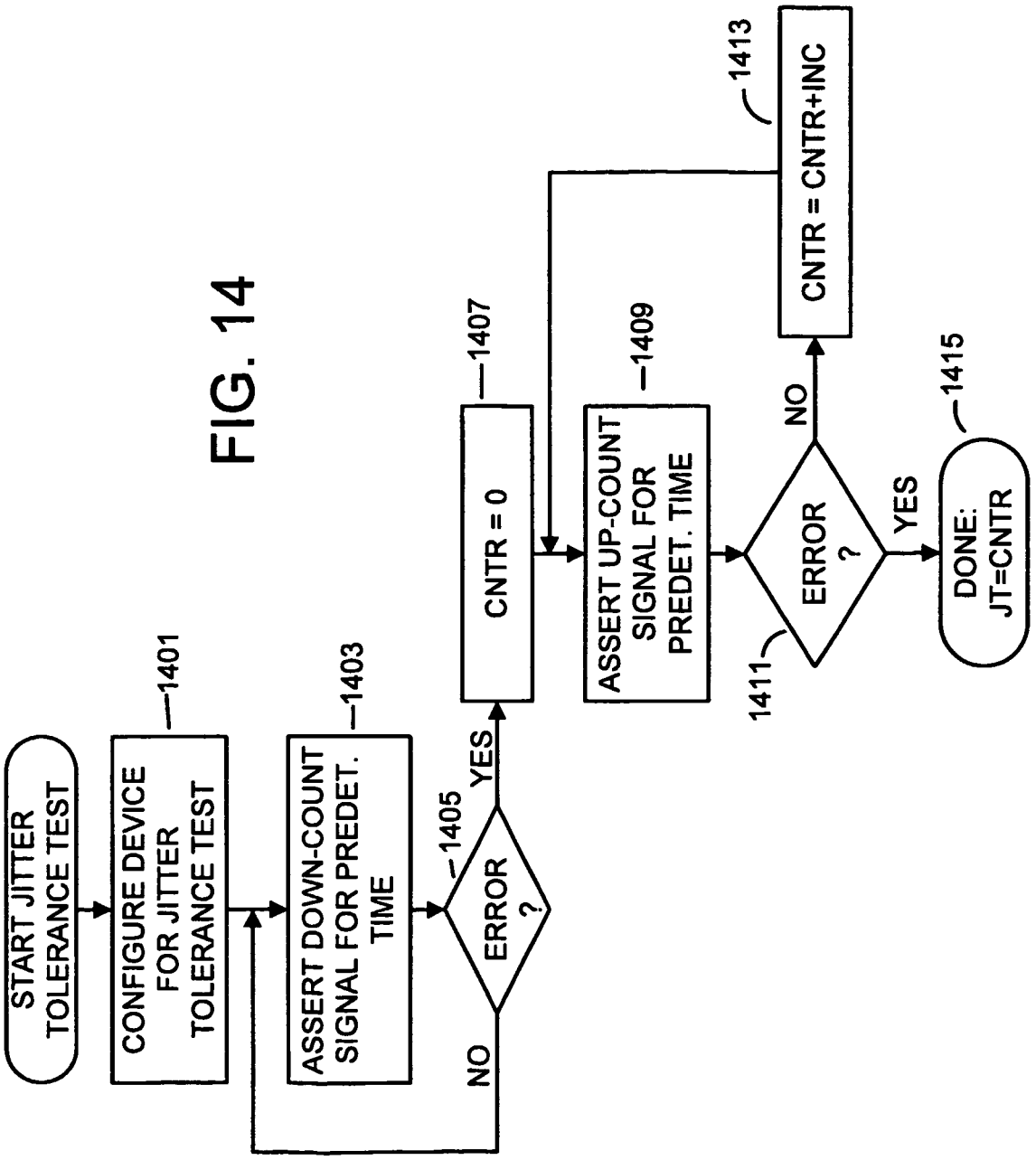


FIG. 13

FIG. 14


START JITTER TOLERANCE TEST
CONFIGURE DEVICE FOR JITTER TOLERANCE TEST
1401
ASSERT DOWN-COUNT SIGNAL FOR PREDET. TIME
1403
ERROR ?
1405
YES
NO
CNTR = 0
1407
ASSERT UP-COUNT SIGNAL FOR PREDET. TIME
1409
ERROR ?
1411
YES
NO
CNTR = CNTR+INC
1413
DONE: JT=CNTR
1415

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 5799048 A **[0009]**