

Jan. 27, 1970

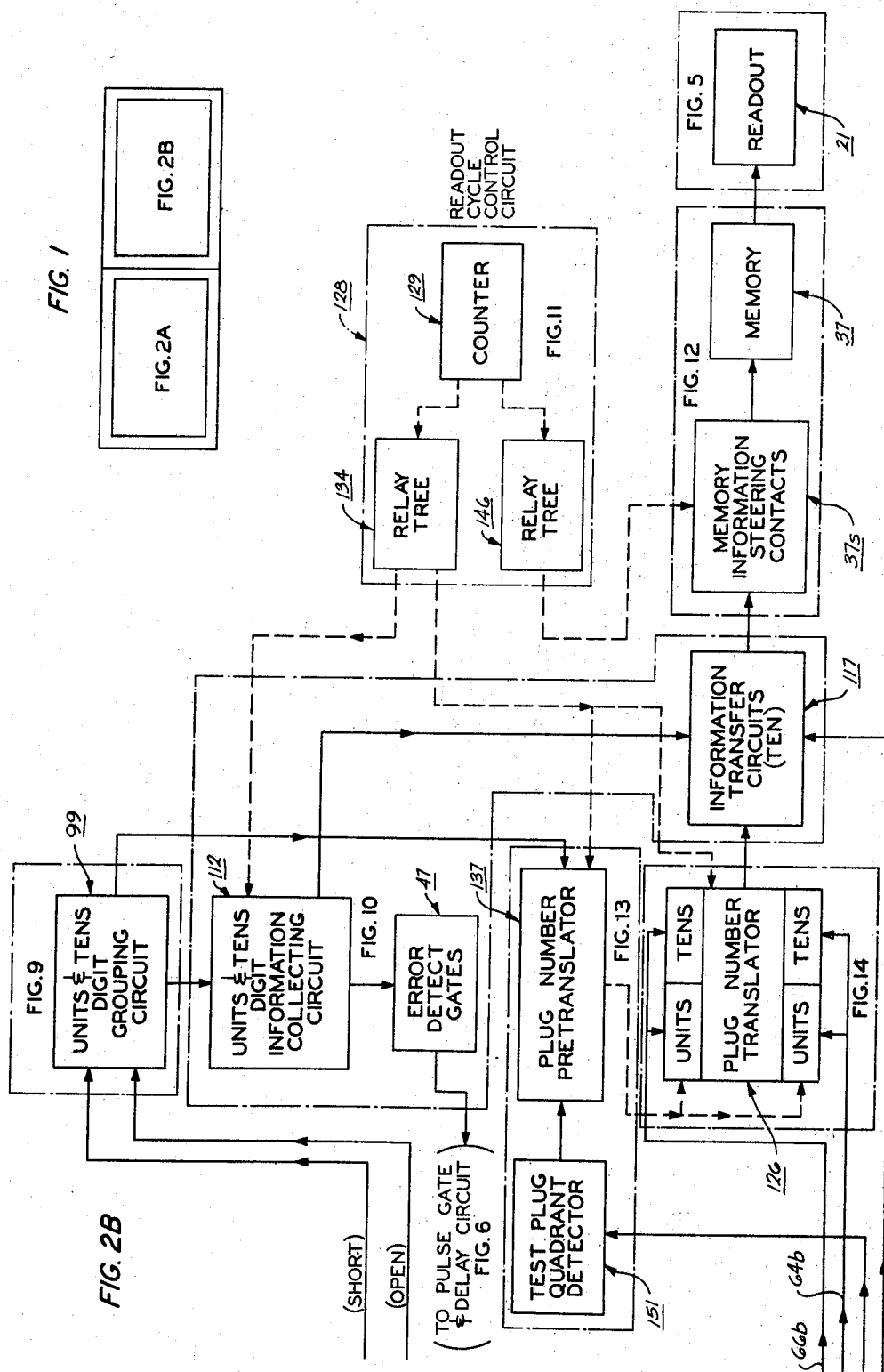
D. A. DESLER

3,492,571

APPARATUS FOR TESTING AN ELECTRICAL CIRCUIT FOR OPENS, SHORTS
AND CROSS CONNECTIONS WITH ITS TERMINAL
GROUPS BEING SEQUENTIALLY CONNECTED
TO THE APPARATUS

Filed Dec. 2, 1965

13 Sheets-Sheet 1



Jan. 27, 1970

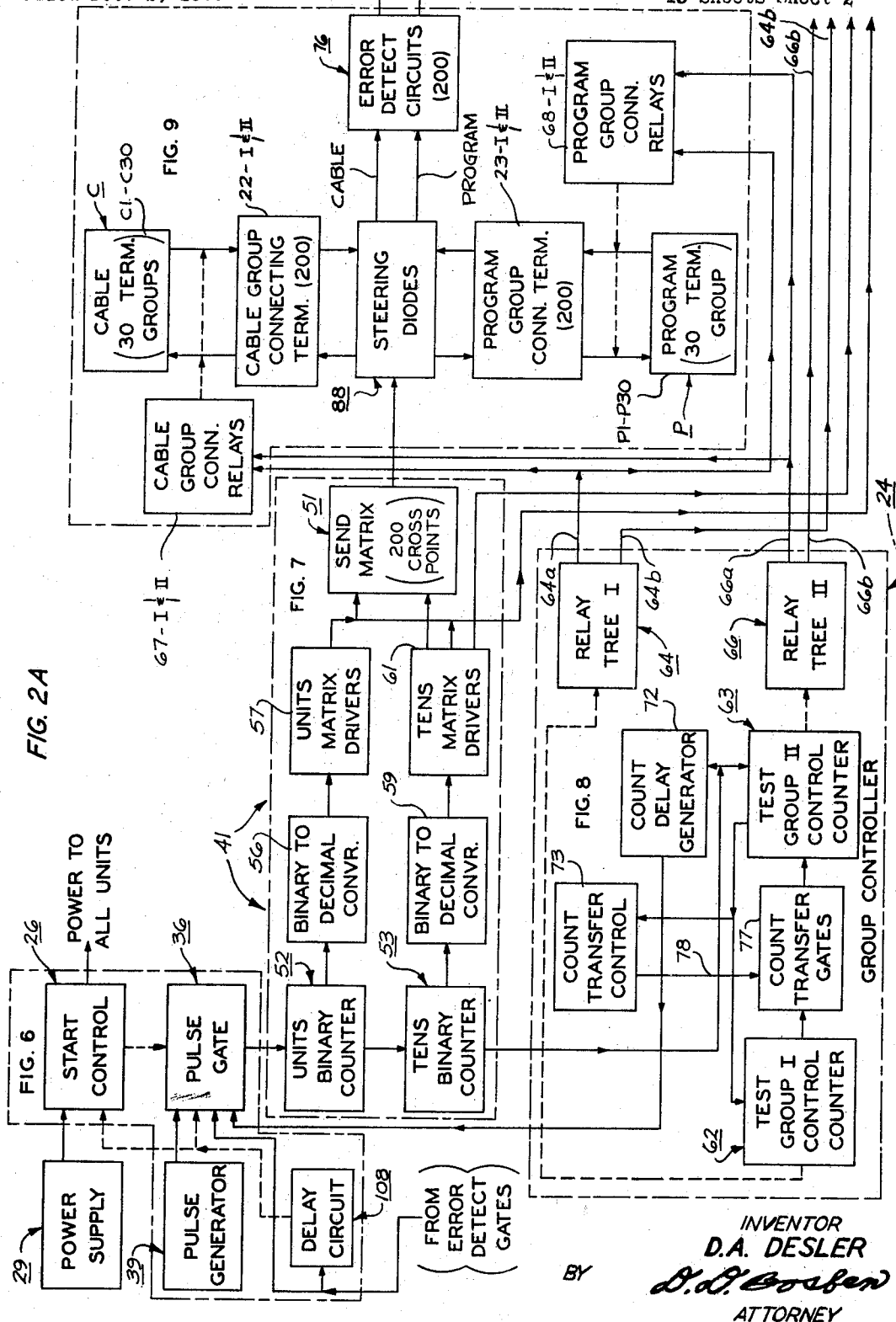
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13 Sheets-Sheet 2



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Filed Dec. 2, 1965

13 Sheets-Sheet 3

FIG. 3

P.00

C (C1-C30)

GROUP 1 PLUG 00 PLUG 01 (50 TERMS) (50 TERMS)	GROUP 7 PLUG 12 PLUG 13	GROUP 13 PLUG 24 PLUG 25	GROUP 19 PLUG 36 PLUG 37	GROUP 25 PLUG 48 PLUG 49
GROUP 2 PLUG 02 PLUG 03 (50 TERMS) (50 TERMS)	GROUP 8 PLUG 14 PLUG 15	GROUP 14 PLUG 26 PLUG 27	GROUP 20 PLUG 38 PLUG 39	GROUP 26 PLUG 50 PLUG 51
GROUP 3 PLUG 04 PLUG 05	GROUP 9 PLUG 16 PLUG 17	GROUP 15 PLUG 28 PLUG 29	GROUP 21 PLUG 40 PLUG 41	GROUP 27 PLUG 52 PLUG 53
GROUP 4 PLUG 06 PLUG 07	GROUP 10 PLUG 18 PLUG 19	GROUP 16 PLUG 30 PLUG 31	GROUP 22 PLUG 42 PLUG 43	GROUP 28 PLUG 54 PLUG 55
GROUP 5 PLUG 08 PLUG 09	GROUP 11 PLUG 20 PLUG 21	GROUP 17 PLUG 32 PLUG 33	GROUP 23 PLUG 44 PLUG 45	GROUP 29 PLUG 56 PLUG 57
GROUP 6 PLUG 10 PLUG 11	GROUP 12 PLUG 22 PLUG 23	GROUP 18 PLUG 34 PLUG 35	GROUP 24 PLUG 46 PLUG 47	GROUP 30 PLUG 58 PLUG 59 (50 TERMS) (50 TERMS)

T P.59 T

FIG. 4

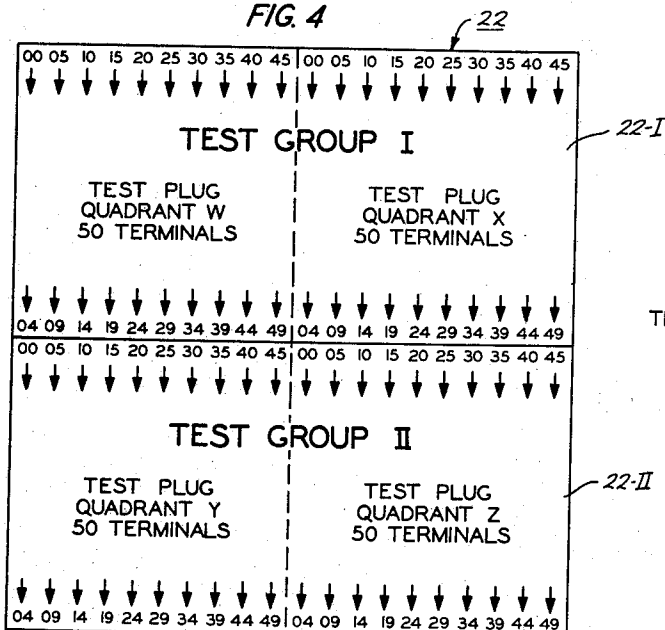
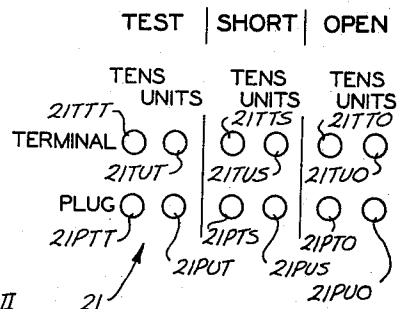


FIG. 5



Jan. 27, 1970

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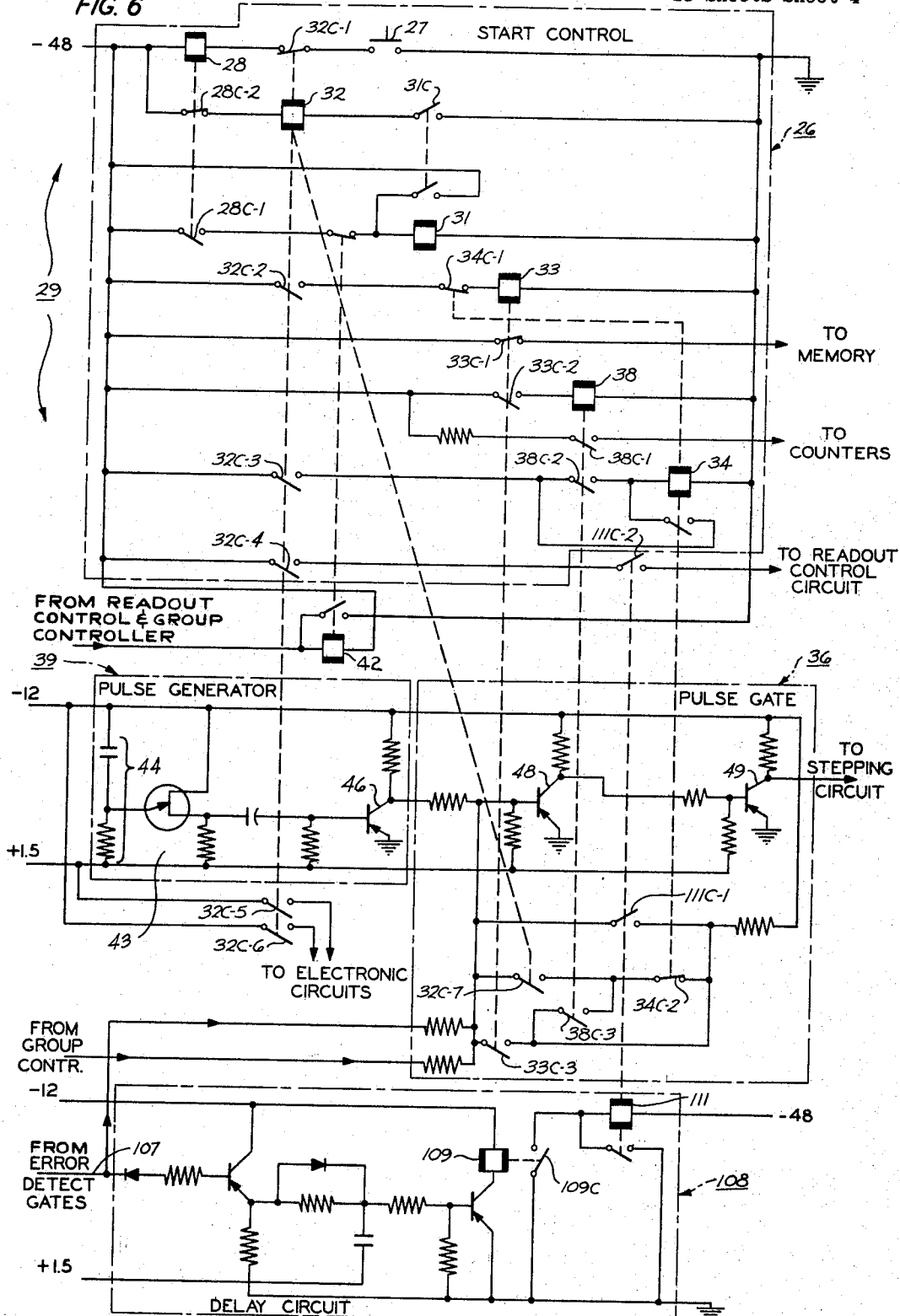
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Filed Dec. 2, 1965

13 Sheets-Sheet 4

FIG. 6



Jan. 27, 1970

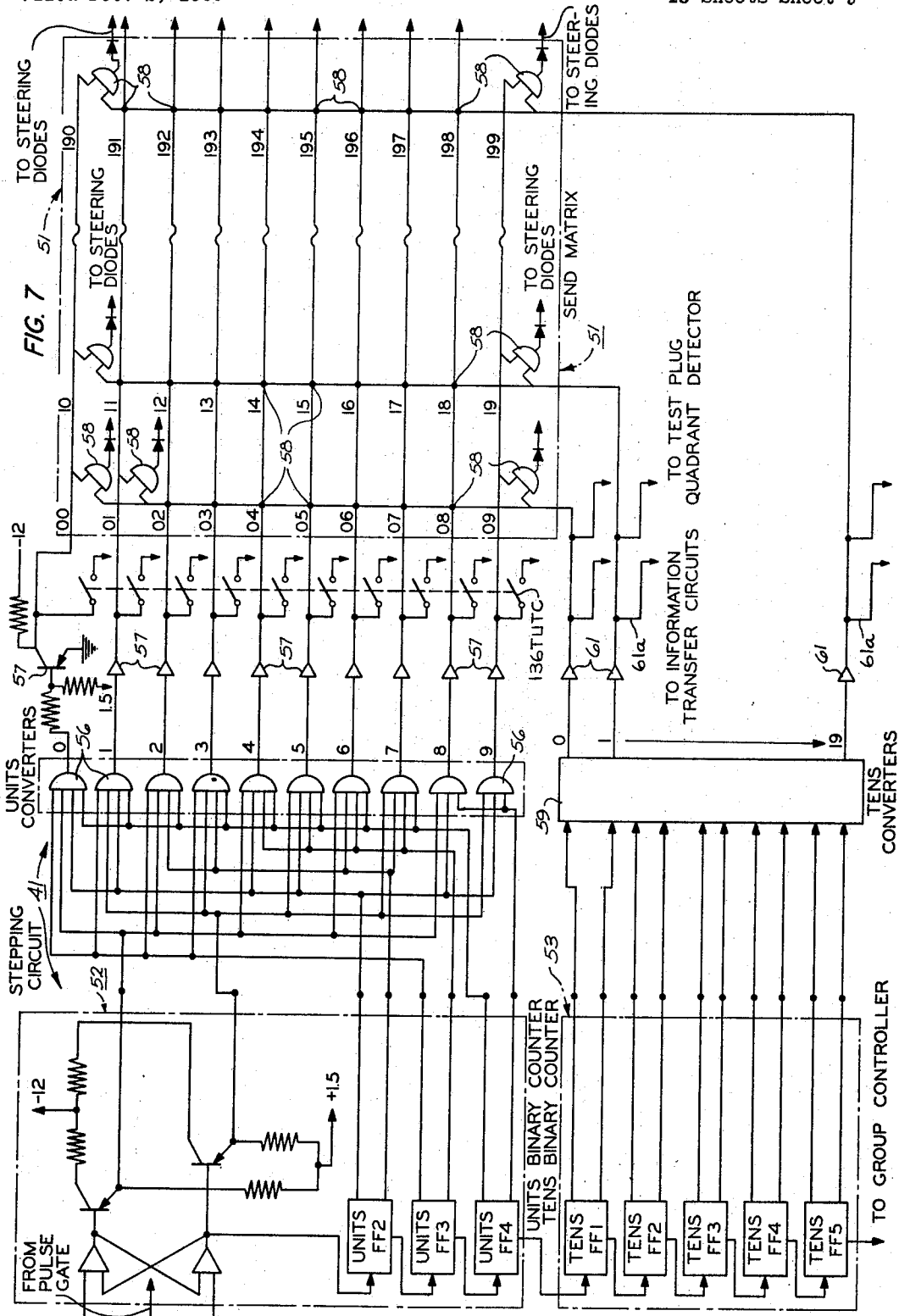
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Filed Dec. 2, 1965

13 Sheets-Sheet 5



Jan. 27, 1970

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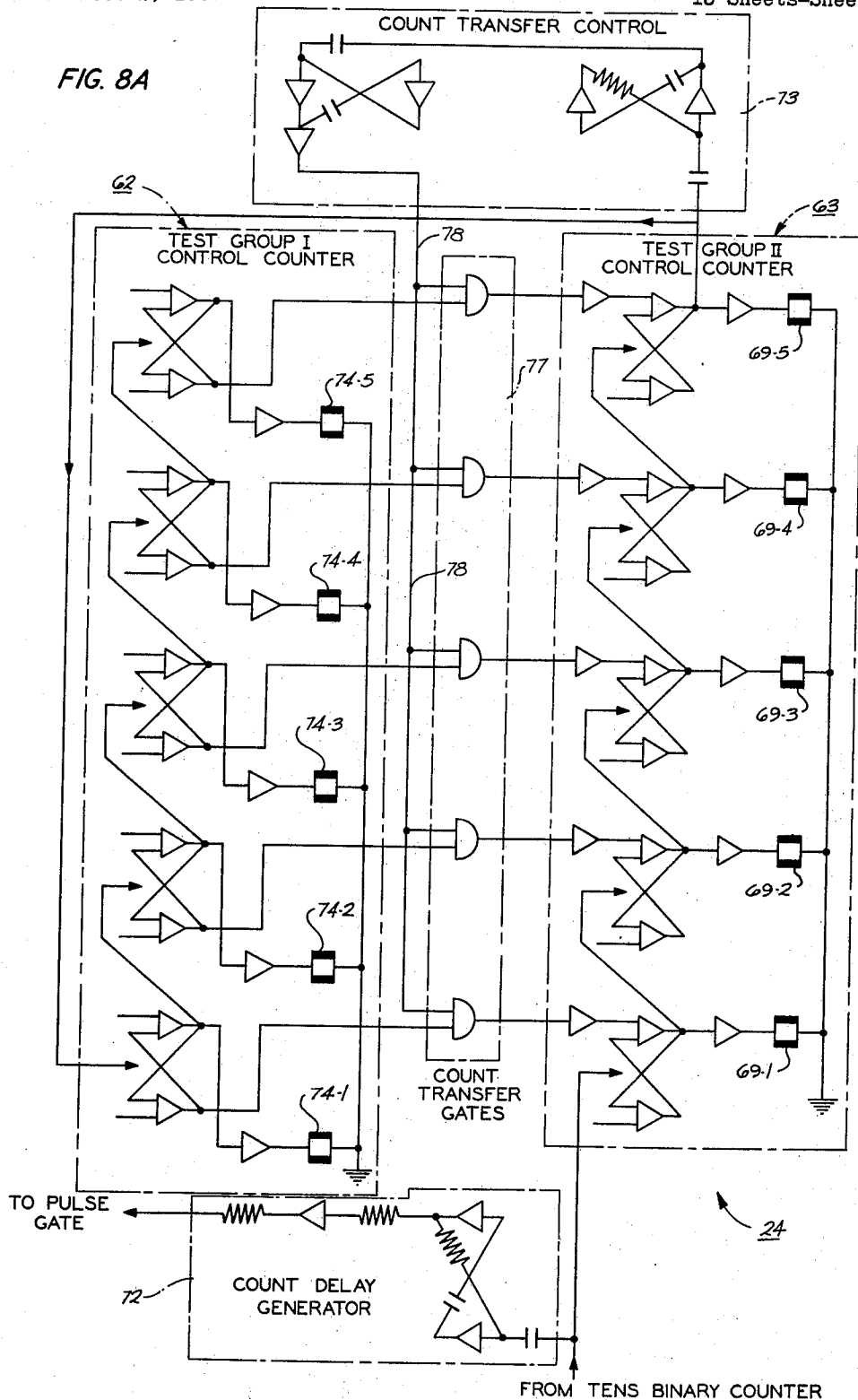
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Filed Dec. 2, 1965

13 Sheets-Sheet 6

FIG. 8A



Jan. 27, 1970

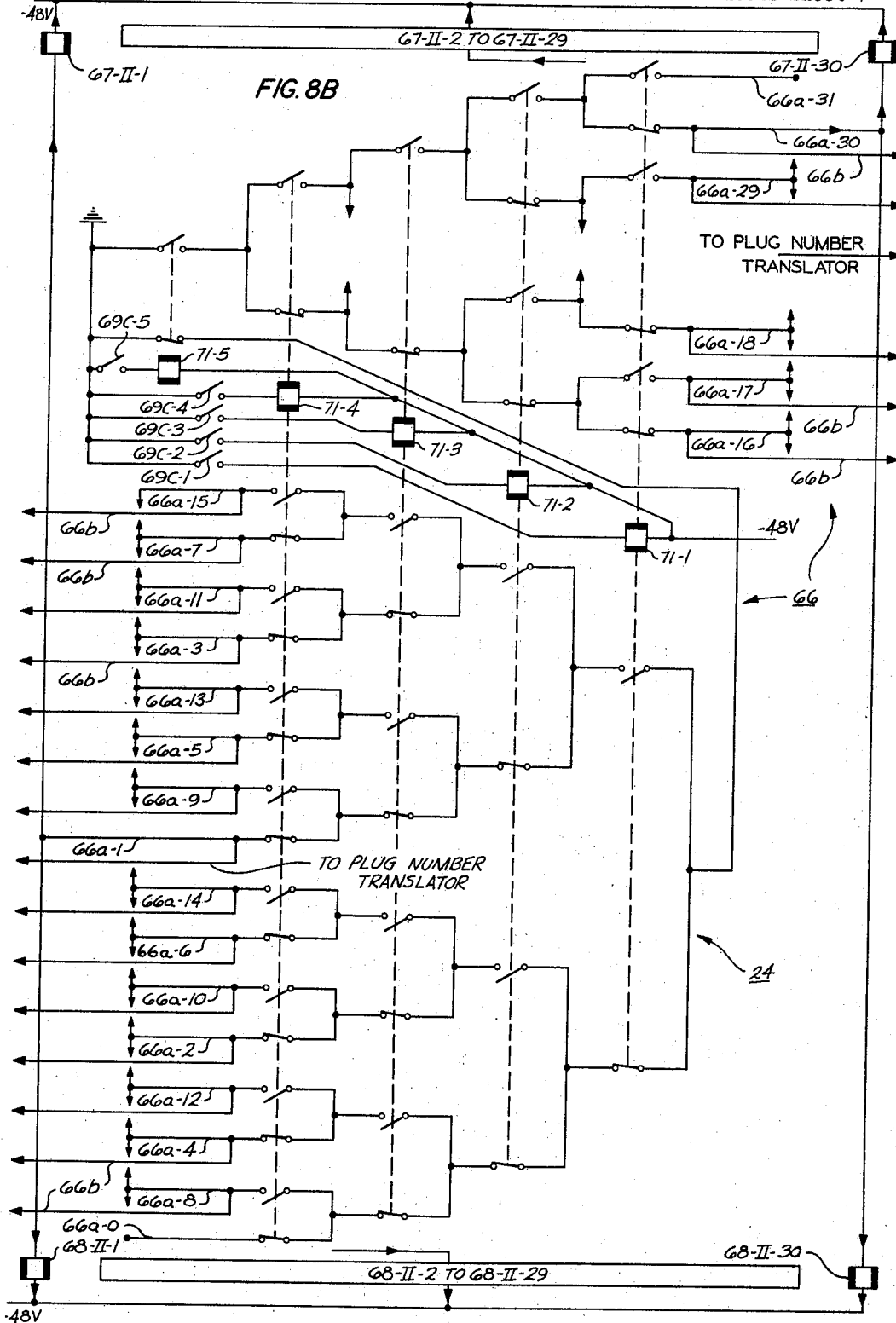
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Filed Dec. 2, 1965

13 Sheets-Sheet 7



Jan. 27, 1970

D. A. DESLER

3,492,571

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Filed Dec. 2, 1965

13 Sheets-Sheet 8

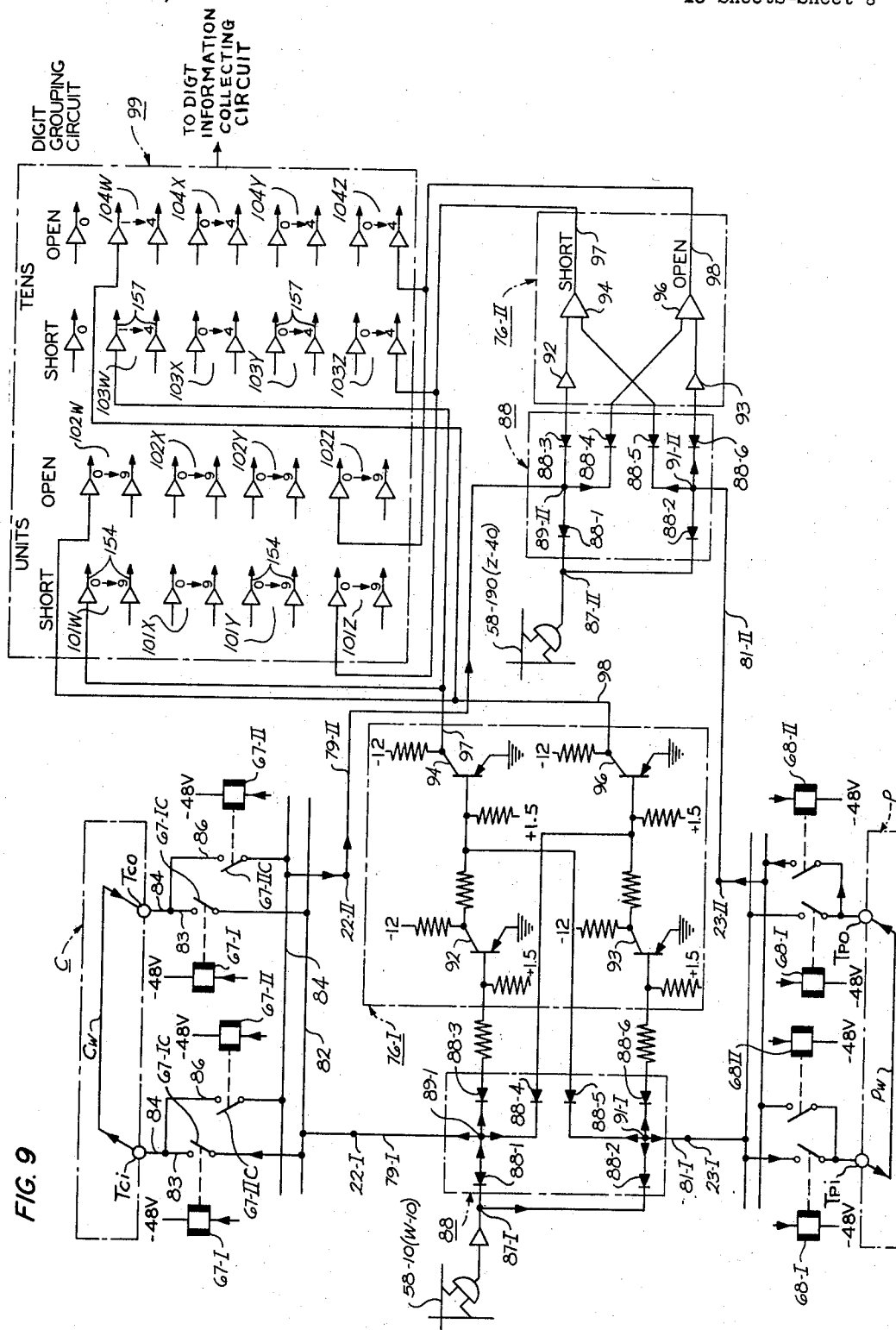


FIG. 9

Jan. 27, 1970

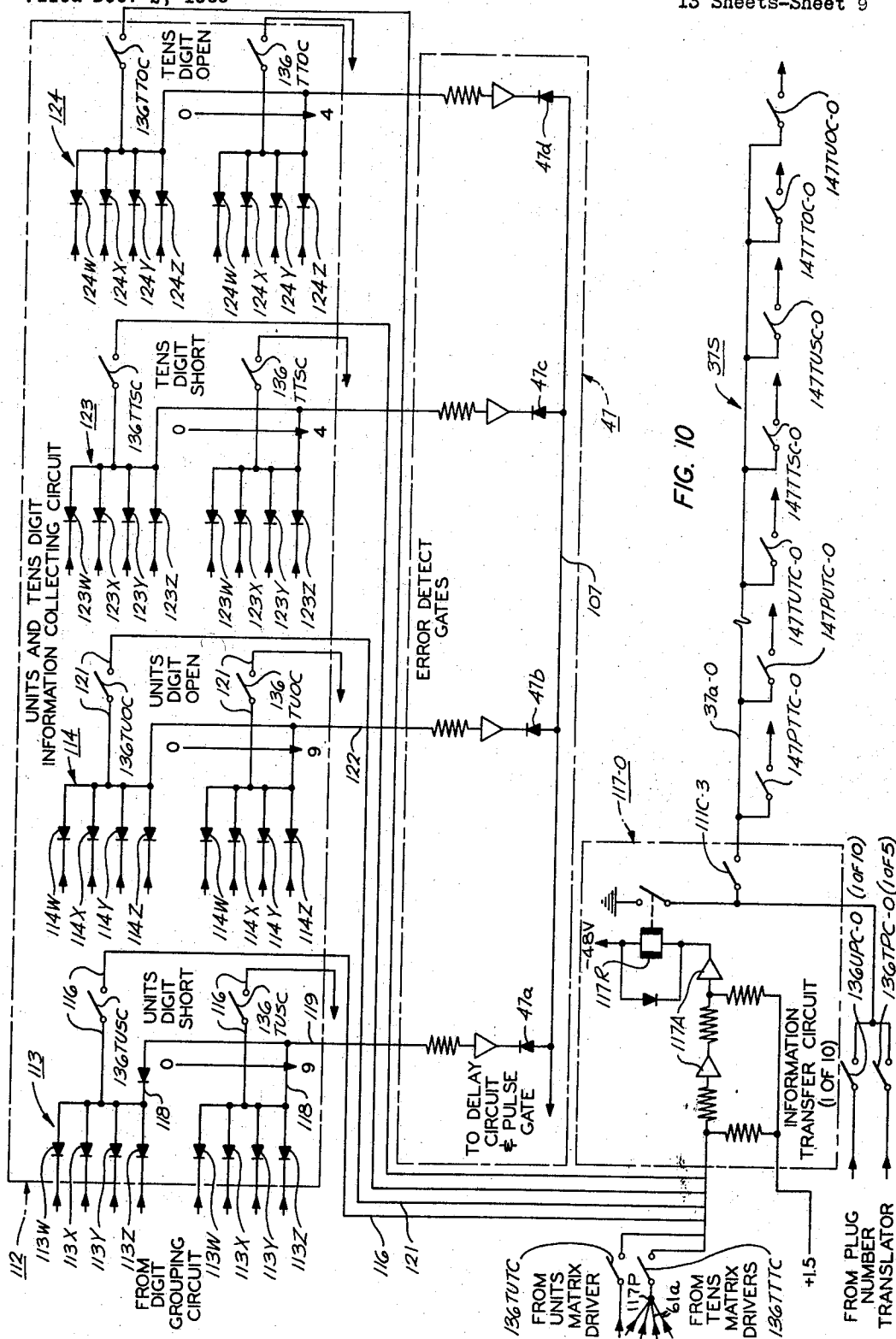
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Filed Dec. 2, 1965

13 Sheets-Sheet 9



Jan. 27, 1970

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Filed Dec. 2, 1965

13 Sheets-Sheet 10

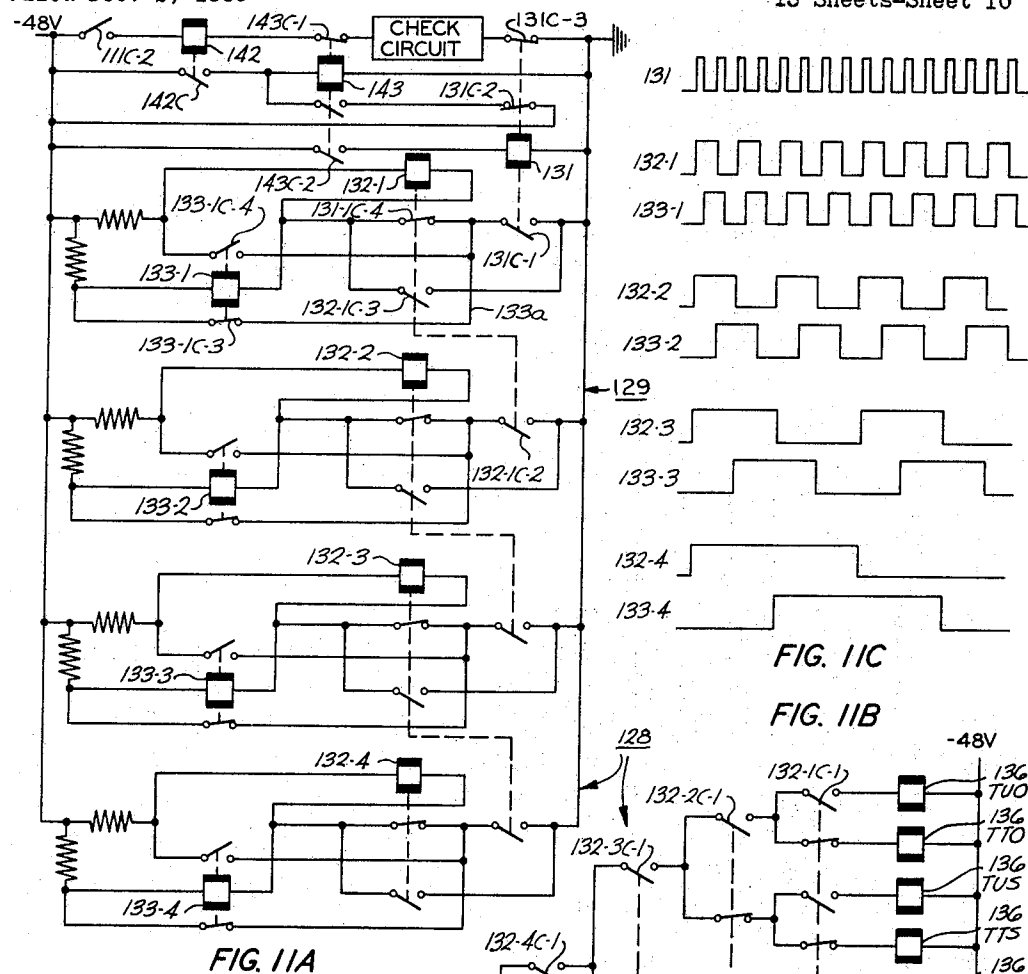


FIG. 11A

FIG. 11C

FIG. 11B

COUNT	RELAY 132-				
	1	2	3	4	
0	0	0	0	0	
1	1	1	1	1	TUO
2	0	1	1	1	TTO
3	1	0	1	1	TUS
4	0	0	1	1	TTS
5	1	1	0	1	TUT
6	0	1	0	1	TTT
7	1	0	0	1	PUO
8	0	0	0	1	PTO
9	1	1	1	0	PUS
10	0	1	1	0	PTS
11	1	0	1	0	PUT
12	0	0	1	0	PTT
13	1	1	0	0	RLS
14	0	1	0	0	IDLE
15	1	0	0	0	IDLE
16	0	0	0	0	

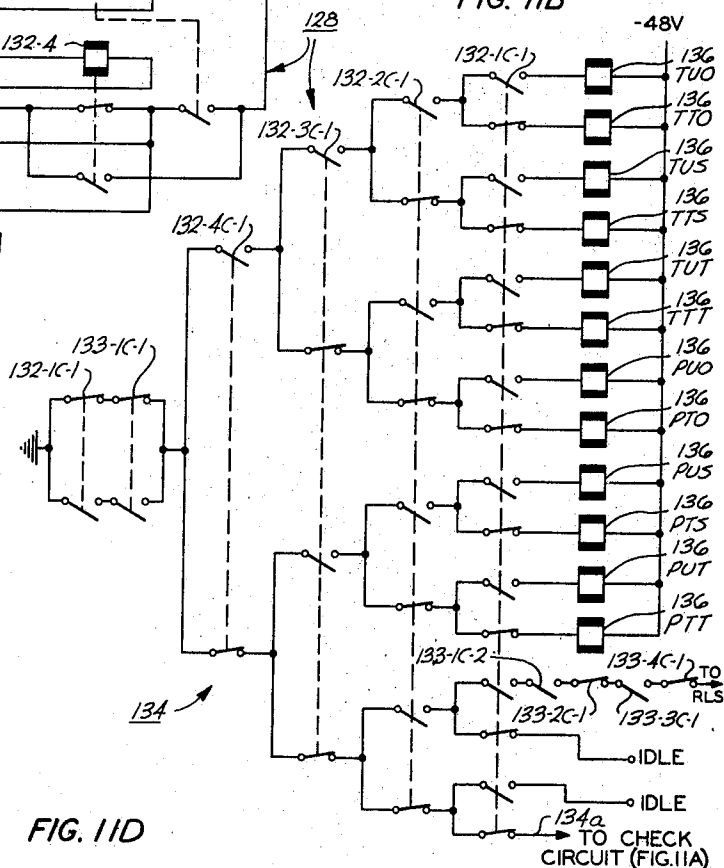


FIG. 11D

Jan. 27, 1970

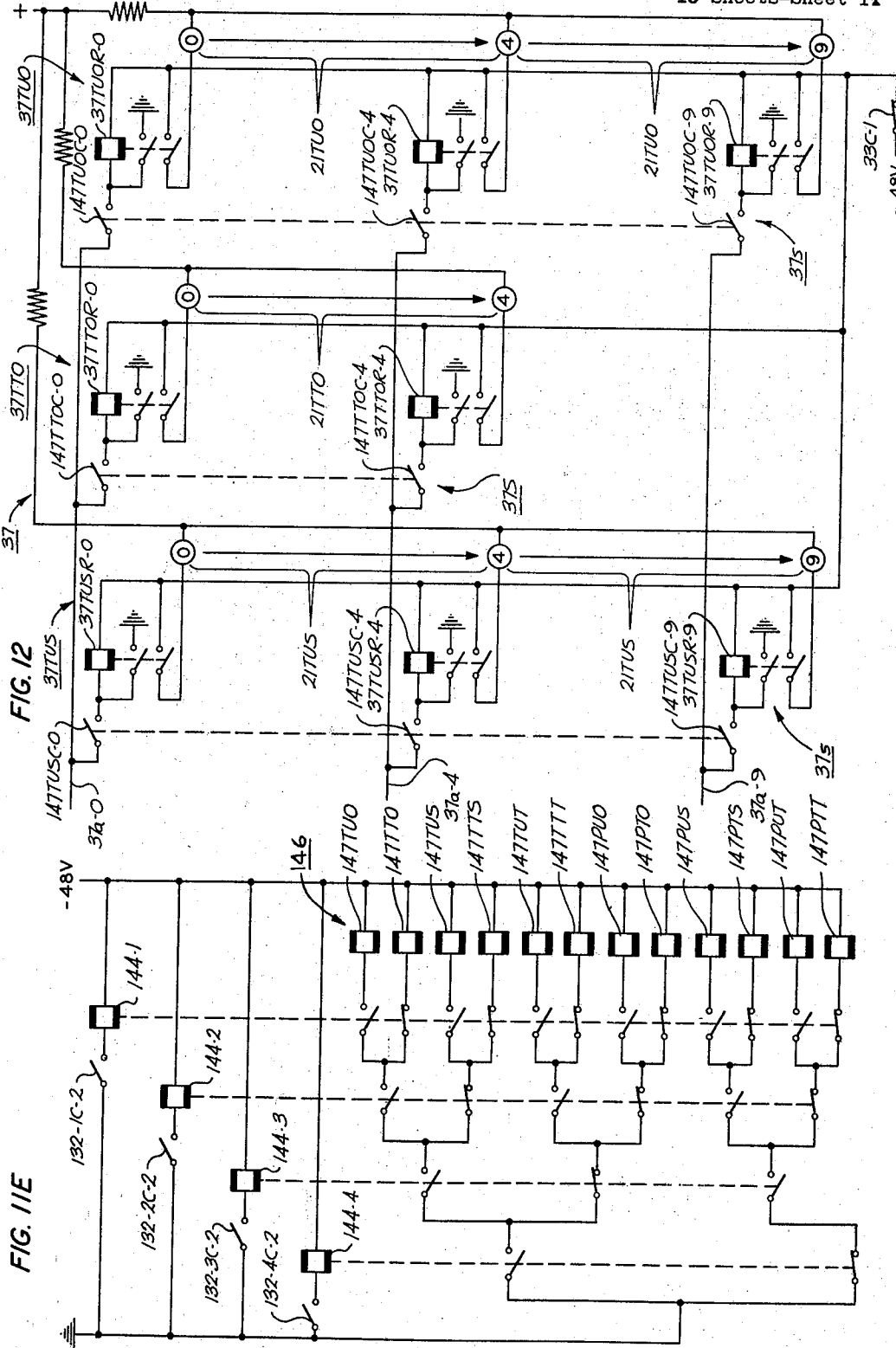
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Filed Dec. 2, 1965

13 Sheets-Sheet 11



Jan. 27, 1970

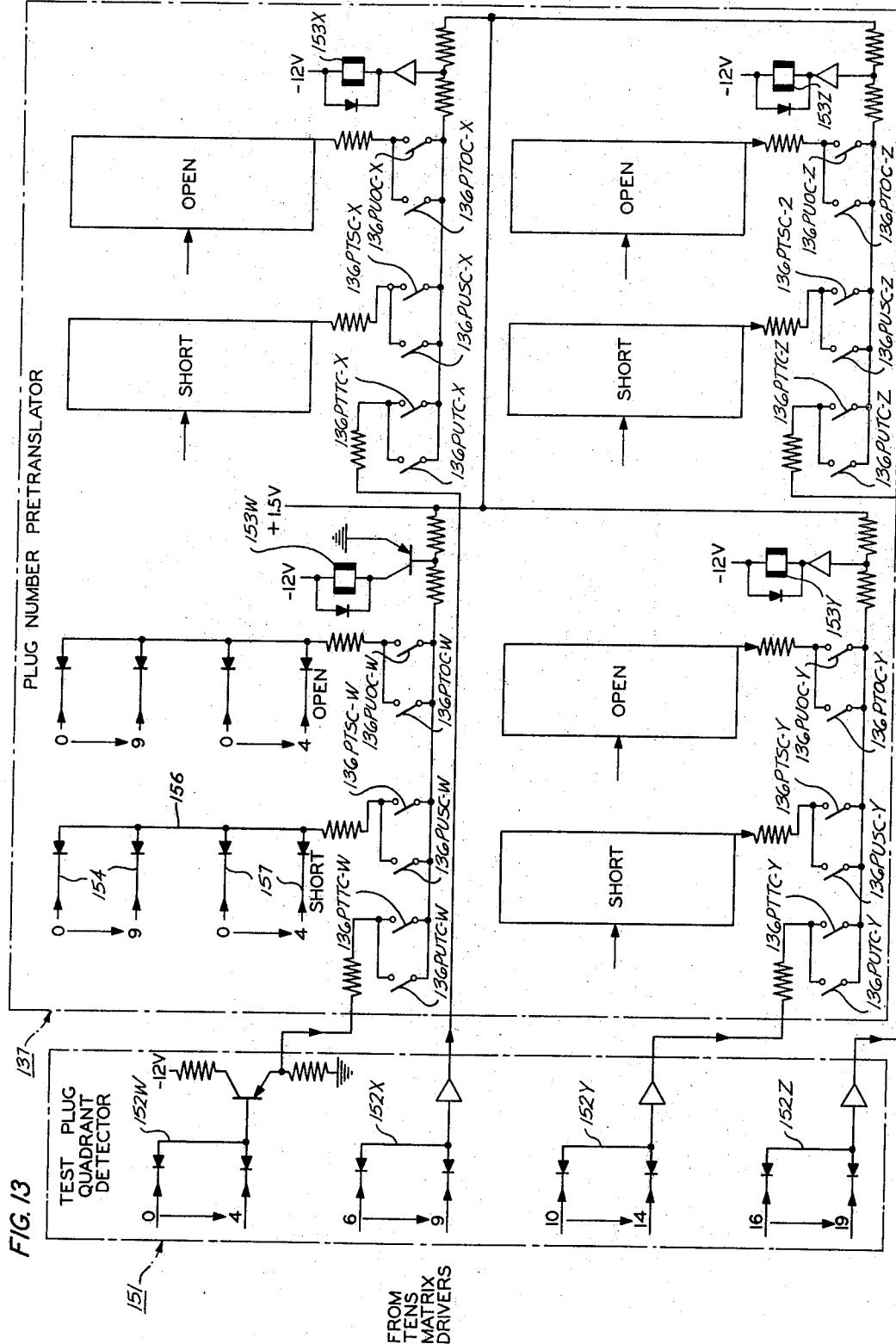
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TO THE APPARATUS

Filed Dec. 2, 1965

13 Sheets-Sheet 12



1

3,492,571

APPARATUS FOR TESTING AN ELECTRICAL CIRCUIT FOR OPENS, SHORTS AND CROSS CONNECTIONS WITH ITS TERMINAL GROUPS BEING SEQUENTIALLY CONNECTED TO THE APPARATUS

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13 Claims

ABSTRACT OF THE DISCLOSURE

In apparatus for testing an electrical circuit for continuity, shorts and cross connections, terminals of the circuit are tested in groups, with the terminal groups being sequentially connected to the apparatus in pairs. In testing a pair of the terminal groups, a separate signal is applied to each of the terminals thereof in succession and their other terminals are monitored to detect an error in the electrical circuit. Detection of an error interrupts the testing operation and energizes circuitry for indicating the terminals involved and the nature of the defect.

This invention relates to apparatus for testing electrical circuitry, and more particularly to apparatus for testing electrical circuitry which is relatively extensive and complex in nature. It is an object of this invention to provide new and improved apparatus of this character.

In the manufacture of electrical circuitry having a plurality of terminals which are interconnected by electrical conductors, such as a connector plug type cable used in a telephone PBX (private branch exchange), it is standard practice to test the cable for continuity, including shorted, open and cross-connected terminals. Any wiring errors are corrected as they are found, before incorporating the cable into the PBX.

Cable testing apparatus is known in which a signal is applied sequentially to each terminal of a cable and at the same time is applied to a corresponding terminal of a reference or control circuit, by means including electromechanical stepping switches. While the signals are being applied to each cable terminal and its corresponding reference circuit terminal, the signal outputs at the other cable terminals are compared with the signal outputs at their corresponding reference circuit terminals in sequence, by means of additional electromechanical stepping switches and associated circuitry, to detect any wiring errors in the cable.

The above described apparatus has various disadvantages and is not suited for testing the cables of more recently developed PBX devices, the wiring of which cables is relatively extensive and complex in nature. For example, as a result of the cable and reference terminals being compared in sequence, and the relatively slow operating times of the electromechanical switches, the apparatus has a relatively slow testing rate. By way of illustration, the minimum time which would be required to test a standard cable having three thousand interconnected terminals utilizing test apparatus of this type, assuming that no errors were found in the cable, would be on the order of several hours. In addition, the test apparatus would have to be of such size and complexity as to make its use impractical.

In another known cable testing apparatus, which is tape programmed, input signals are applied sequentially to terminals of a cable and the apparatus checks for an output signal only at those terminals at which an output signal should appear. While this apparatus provides a

2

reduction in cable test time as compared to the above-described type of apparatus, it is of limited capacity, and where the wiring of the cable being tested is relatively extensive in nature, considerable manual connecting and disconnecting of terminals to and from the apparatus is involved, such that the cable test time still is on the order of one hour or more. Further, if this apparatus were made of sufficient size so as to eliminate this manual connecting and disconnecting of the terminals, it would be of such size and complexity as to make its use impractical. This type of apparatus also is disadvantageous because it primarily tests the cable for continuity, and may not detect an error in which a terminal, while properly wired to one or more other terminals, also is shorted to another terminal.

Accordingly, an object of this invention is to provide new and improved apparatus which is particularly suited for the testing of electrical circuitry which is relatively extensive and complex in nature.

Another object of this invention is to provide new and improved apparatus for testing electrical circuitry which is relatively fast operating as compared to prior known apparatus.

A further object of this invention is to provide new and improved apparatus for testing electrical circuitry which is relatively small in size in comparison to prior known apparatus having a corresponding testing capacity.

A still further object of this invention is to provide new and improved apparatus for testing electrical circuitry in which manual connecting and disconnecting of terminals of the circuitry to and from the apparatus, other than at the beginning and end of a test operation, is eliminated.

A still further object of this invention is to provide new and improved apparatus for testing electrical circuitry having sets of terminals which are interconnected by electrical conductors, wherein the apparatus determines the terminals involved in an error in the electrical circuitry, including the set of terminals in which each of the involved terminals is located.

In accordance with the invention, in apparatus for testing an electrical circuit having a plurality of terminals which are interconnected by electrical conductors, a signal is applied sequentially to each of the terminals and at the same time a signal is applied to a corresponding terminal of a control circuit, so that the signals feed into the electrical and control circuits. An error in the electrical circuit then is detected by simultaneously comparing the signal outputs at the other terminals with the signal outputs at their corresponding reference terminals.

In a preferred embodiment of the invention, apparatus for testing an electrical circuit having sets of terminals which are interconnected by electrical conductors includes first control means for sequentially connecting groups of the terminals and corresponding groups of terminals of a reference circuit to the apparatus as first electrical circuit and reference circuit and reference circuit test groups, respectively. When each of the electrical circuit terminal groups and its corresponding reference circuit terminal group are connected to the apparatus as the first test groups, a second control means sequentially connects selected ones of the other electrical circuit and reference circuit terminal groups to the apparatus as second test groups, the second control means being connected to energize the first control means after the selected other terminal groups have been connected to the apparatus, so that the first control means connects the next succeeding pair of terminal groups to the apparatus as the first test groups. While each of the two pairs of electrical circuit and reference circuit terminal groups are connected to the apparatus, a signal is sequentially applied to each of the electrical circuit terminals, and at the same time a signal is applied to the corresponding

reference circuit terminal, so that the signals feed into the electrical circuit and the reference circuit, respectively. The electrical circuit then is checked by comparing the signal output at each of the other terminals of the two electrical circuit terminal groups, with the signal output at the corresponding reference circuit terminal, to detect any disparity in the signal outputs of the corresponding terminals as a result of an error. When an error is detected the apparatus determines whether the error is caused by shorted, open or cross-connected terminals, and also determines the terminals involved in the error, including the set of terminals in which each terminal is located.

This invention, together with further objects and advantages thereof, will best be understood by reference to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 illustrates the relative relationship of FIGS. 2A and 2B;

FIG. 2A is a block diagram of a portion of the apparatus;

FIG. 2B is a block diagram of the remainder of the apparatus;

FIG. 3 is a schematic representation of a PBX cable;

FIG. 4 is a schematic representation of cable connecting terminals of the apparatus as shown in FIG. 2A, which illustrates the manner in which terminals of the PBX cable represented in FIG. 3 are connected to the apparatus as test groups for test purposes;

FIG. 5 shows a read-out display of the apparatus;

FIG. 6 is a detailed circuit diagram of parts of the apparatus as shown in the block diagram of FIG. 2A, including a start control circuit, a pulse generator, a pulse gate and an associated delay circuit;

FIG. 7 is a detailed circuit diagram of a stepping circuit and a send matrix of the apparatus as shown in the block diagram of FIG. 2A;

FIG. 8A is a detailed circuit diagram of a part of a group controller circuit of the apparatus as shown in the block diagram of FIG. 2A;

FIG. 8B is a detailed circuit diagram of another part of the group controller circuit;

FIG. 9 is a detailed circuit diagram of error detect circuitry of the apparatus as shown in the block diagram of FIG. 2A, illustrating the manner in which a wiring error in the cable represented in FIG. 3 is detected, and also showing a digit grouping circuit of the apparatus as shown in the block diagram of FIG. 2B;

FIG. 10 is a detailed circuit diagram of a digit information collecting circuit and one of a plurality of information transfer circuits of the apparatus as shown in the block diagram of FIG. 2B;

FIGS. 11A, 11B and 11E are detailed circuit diagrams of parts of a read-out cycle control circuit of the apparatus as shown in the block diagram of FIG. 2B;

FIGS. 11C and 11D show a diagram and a chart, respectively, illustrating an operating cycle for the part of the read-out cycle control circuit shown in FIG. 11A;

FIG. 12 is a detailed circuit diagram of a memory circuit and associated information steering contacts of the apparatus as shown in the block diagram of FIG. 2B;

FIG. 12 is a detailed circuit diagram of a cable test plug quadrant detector and a cable plug number pre-translator of the apparatus as shown in the block diagram of FIG. 2B, and

FIGS. 14A, B and C are detailed circuit diagrams illustrating a cable plug translator of the apparatus as shown in the block diagram of FIG. 2B.

The illustrated embodiment of the invention is designed to test a PBX cable for continuity, including shorted, open and cross-connected terminals. More specifically, the apparatus is designed to test a PBX cable C, as illustrated in FIG. 3, which includes sixty terminal plugs P-00 through P-59, each having fifty terminals T for a total of three thousand terminals. Each of the terminals

T, which in the illustrated embodiment of the invention are assigned the numbers 00 through 49, as shown in FIG. 4, is wired to one or more selected other terminals by suitable conductor wires. The cable C is connected into a PBX apparatus by plugging the cable plugs P-00 through P-59 to respective fixed plugs of the apparatus, and the cable is connected to the subject test apparatus by inserting the plugs into suitable receptacles (not shown) having terminals which are connectible to the test apparatus in a manner to be described.

In the event of an error in the cable C, the apparatus indicates the number of the plug P-00 through P-59 and the number of the terminal T-00 through T-49 under test, that is, the input terminal, when the error is found and whether the error is a short, an open wire or a cross connection. If the error is a short, the apparatus also indicates the number of the plug P-00 through P-59 and the number of the terminal T-00 through T-49 to which the test terminal is shorted, or if the fault is an open wire, the number of the plug and the number of the terminal to which the test terminal should be connected. For this purpose, the apparatus includes a read out 21 in the form of a nixie lamp display, as illustrated in FIG. 5, which indicates the tens digit and the units digit for the test plug number P-00 through P-59, the tens and the units digits for the test terminal T-00 through T-49, etc., for a total of twelve digits or pieces of information which are provided by the apparatus. A reading on the read-out display 21 of both a shorted terminal T-00 through T-49 and an open terminal, is an indication that a cross connection exists in the cable C.

With respect to the cable terminals T-00 through T-49 and the cable plugs P-00 through P-59, various abbreviations used on the drawings, as for example in FIG. 5 for read-out lamps 21TUT, 21TUS, etc., of the read-out 21, and in the following description are defined as follows: TUT designates "Terminal Units Test," that is, the units digit of the terminal under test (input terminal) when an error is found; TUS designates "Terminal Units Short," the units digit of a terminal to which the test terminal is shorted; TUO designates "Terminal Units Open," the units digit of a terminal to which the test terminal should be connected but is not, and with respect to which the test terminal thus is "open"; PUT designates "Plug Units Test," the units digit of the plug in which the input terminal is located; PUS designates "Plug Units Short," the units digit of a plug having a shorted terminal; and PUO designates "Plug Units Open," the units digit of a plug having an open terminal. Similarly, TTT designates "Terminal Tens (digit) Test"; TTS designates "Terminal Tens Short"; TTO designates "Terminal Tens Open"; PTT designates "Plug Tens Test"; PTS designates "Plug Tens Short," and PTO designates "Plug Tens Open."

The illustrated embodiment of the invention operates upon the principle of comparing the cable C under test with a control reference circuit, hereinafter referred to as the program P (FIG. 2A), which is wired in the manner that the cable should be wired. Preferably, the program P is made up of removable circuit boards in a manner well known to those skilled in the art, to facilitate changing of the program for the testing of other cables or electrical wiring.

The three thousand terminals T of the cable C are connected to the apparatus for test purposes in groups, rather than simultaneously, so as to reduce the size of the apparatus required. Accordingly, in the illustrated embodiment of the invention, as is shown in FIG. 3, the cable C is divided into thirty terminal groups C1-C30 with each group including two of the plugs P-00 through P-59, or one hundred of the terminals T.

Two of the terminal groups C1-C30 (four plugs or two hundred terminals) are connected to the apparatus at any one time through two hundred cable connecting terminals 22 (FIGS. 2A, 4 and 9). More specifically, referring to FIG. 4, it is seen that the two hundred cable

connecting terminals 22 are divided into two groups of one hundred terminals each, one of the groups being designated as "test group I" or 22-I and the other group of terminals being designated as "test group II" or 22-II. Each of the test groups 22-I and 22-II further is divided into two sets of fifty terminals, with the resulting sets being designated as test plug quadrants W, X, Y and Z, and with the terminals of each quadrant having assigned numbers 00 through 49.

Each of the cable terminal groups C1-C30 is connectible to the one hundred cable connecting terminals 22-I and to the one hundred cable connecting terminals 22-II. When one of the cable terminal groups C1-C30 is connected to the cable connecting terminals 22-I, the terminals T of one cable plug of the group are connected to respective ones of the cable connecting terminals in test plug quadrant W, and the terminals of the other plug of the group are connected to respective ones of the cable connecting terminals in test plug quadrant X. Similarly, when the same cable terminal group is connected to the cable connecting terminals 22-II, the terminals T of the group's plugs are connected to respective ones of the cable connecting terminals of test plug quadrants Y and Z, respectively. Thus, the test plug quadrants W, X, Y and Z of the cable connecting terminals 22 are representative of respective ones of the four of the cable plugs P-00 through P-59 which are connected to the testing portion of the apparatus at any one time.

The program P also is divided into thirty plug terminal groups P1-P30, as indicated in FIG. 2A, which are identical to the cable terminal groups C1-C30 shown in FIG. 3. When two of the cable terminal groups C1-C30 are connected to the apparatus for test purposes, the two corresponding ones of the program terminal groups P1-P30 also are connected to the apparatus as described in the preceding paragraph, through two hundred program connecting terminals 23, which are divided into test groups I and II in the same manner as the connecting terminals 22 shown in FIG. 4. The connection of the cable terminal groups C1-C30 and their corresponding program terminal groups P1-P30 to the apparatus in pairs is accomplished sequentially by a terminal group controller 24 (FIGS. 2A and 8), which subsequently is described in greater detail.

START CONTROL CIRCUIT (FIGS. 2A and 6)

Referring to FIGS. 2A and 6, it is seen that a start control circuit 26 is provided for initiating operation of the apparatus. After the cable plugs P-00 through P-59 of the cable C have been inserted into the above-mentioned receptacles, a start button 27 is depressed to energize a start relay 28 from a suitable voltage source of a power supply 29, the voltage source in the illustrated embodiment of the invention being shown in FIG. 6 as having a magnitude of -48 v. The start relay 28 closes a contact 28C-1 to energize a hold relay 31 which locks operated and closes a contact 31C to condition a lock-out relay 32 for operation.

When the start button 27 is released, the start relay 28 is deenergized to release a contact 28C-2 to its normally closed position to cause energization of the conditioned lock-out relay 32. The lock-out relay 32 then opens a contact 32C-1 in the energizing circuit of the start relay 28 to prevent energization of the start relay during the test operation as a result of inadvertent pressing of the start button 27. The lock-out relay 32 also closes a contact 32C-2 to energize a delay relay 33; a contact 32C-3 to condition a test relay 34 for operation; a contact 32C-4 to condition read-out control circuitry (subsequently to be described) for operation; contacts 32C-5 and 32C-6 to apply battery to electronic circuits (subsequently to be described) from suitable voltage sources of the power supply 29, the voltage sources in the illustrated embodiment of the invention being shown in FIG. 6 as having magnitudes of -12 v. and +1.5 v., respectively; and a gate closing contact 32C-7 in a pulse gate 36.

The delay relay 33 opens a contact 33C-1 to remove battery from a memory 37 (FIG. 2B), to restore the memory to a neutral condition and to cause it to "forget" any previously stored information. The delay relay 33 also closes a contact 33C-2 to energize a counter zero set relay 38, and closes a gate closing contact 33C-3 in the pulse gate 36.

The counter zero set relay 38 closes a contact 38C-1 to cause a voltage pulse to be fed from the -48 v. voltage source of the power supply 29 to reset inputs of all electronic counters of the apparatus, to reset their outputs to a zero state. The zero set relay 38 also closes a contact 38C-2 to cause energization of the conditioned test relay 34, which locks operated. In addition the zero set relay 38 closes a gate closing contact 38C-3 in the pulse gate 36.

The energized test relay 34 opens a contact 34C-1 to deenergize the delay relay 33, and also opens a gate closing contact 34C-2 in the pulse gate 36. The deenergized delay relay 33 then releases the contact 33C-1 to its normally closed position to restore power to the memory 37, releases the contact 33C-2 to its normally open position to deenergize the counter zero set relay 38, and releases the gate closing contact 33C-3 in the pulse gate 36. When the counter zero set relay 38 is deenergized it releases the normally open counter reset contact 38C-1 and the normally open test relay energizing contact 38C-2. The relay 38 also releases the normally open contact 38C-3 in the pulse gate 36, thereby opening the gate and permitting pulses to flow from a pulse generator 39 through the gate to a stepping circuit 41 (FIG. 2A).

Upon completion of the testing of the cable C or the completion of the read out of an error, a release relay 42 (FIG. 6) is energized to open a contact in the energizing circuit of the hold relay 31, thereby dropping out the hold relay, and thus the lock-out relay 32 and the test relay 34, to deenergize the apparatus.

PULSE GENERATOR

The pulse generator 39 may be of any suitable type, and in the illustrated embodiment of the invention is shown in FIG. 6 as including a unijunction transistor relaxation oscillator 43, which produces a negative going output voltage pulse. The output pulse frequency of the oscillator 43, and thus the testing rate if the apparatus, is determined by a series RC circuit 44 in a well-known manner. The negative going pulses from the oscillator 43 are coupled by a suitable coupling capacitor to a NOR amplifier 46, which causes a 180° phase reversal of the pulses to make them positive going, and these positive going pulses then feed to the input of the pulse gate 36.

PULSE GATE (FIGS. 2A and 6)

The pulse gate 36, which is normally open to permit the flow of pulses from the pulse generator 39 to the stepping circuit 41 (FIGS. 2A and 7), is closed to preclude passage of pulses therethrough by the start control circuit 26, as described hereinabove, and also by a signal from an error detect gate circuit 47 (FIG. 2B), or a signal from the group controller 24 (FIG. 2A), as will subsequently be described in greater detail. The pulse gate 36 includes a pair of series connected NOR amplifiers 48 and 49, with the output of the amplifier 49 being connected to the input of the stepping circuit 41.

STEPPING CIRCUIT (FIGS. 2A and 7)

As the stepping circuit 41 is energized in response to the pulses from the pulse gate 36, it cooperates with an associated two hundred cross point send matrix 51 to cause signals to be applied sequentially to the two hundred cable connecting terminals 22, and thus sequentially to the terminals T of the two of the cable terminal groups C1-C30 which are connected thereto at any one time. As a signal is applied to each cable connecting terminal 22, it also is applied to the corresponding program connect-

ing terminal 23, and thus to the program terminal which is connected to the program connecting terminal at that time.

The stepping circuit 41 includes a units digit binary counter 52 and a tens digit binary counter 53. As is shown in detail in FIG. 7, the counters 52 and 53 are in the form of nine saturated flip-flop circuits arranged in a simple series string. The units counter 52 includes four of the flip-flops (UNITS FF1-FF4) and has a basic count of sixteen, only ten of which (one for each units digit) are required for testing the cable C, while the tens counter 53 includes five of the flip-flop (tens FF1-FF5) and has a basic count of thirty-two, only twenty of which (one for every ten terminals) are required for testing the cable as shown in the illustrated embodiment of the invention.

Accordingly, to reduce the test set cycle time, the count of each of the counters 52 and 53 may be reduced by feeding back a signal from one flip-flop of the counter to a preceding flip-flop, in a well-known manner, if desired. For example, the basic count of the tens counter 53 may be converted from thirty-two to a basic count of twenty-four, twenty of the digits being used for the actual testing of the cable C and the remaining extra four digits being used for self-testing if the apparatus, or being available for other purposes, such as the testing of selected terminals of an electrical circuit, as set forth at the end of this description. The basic count of the units counter 52 may be reduced in a similar manner.

The outputs of the flip-flops of the units counter 52 are connected to binary to decimal converters 56-0 through 56-9 in the form of positive AND gates so as to energize the gates sequentially in a manner well known to those skilled in the art. The positive output pulse or signal from each of the energized AND gates 56-0 through 56-9 is amplified and inverted by a units digit send matrix driver 57 in the form of a NOR amplifier, and then is applied to respective ones of two hundred cross points 58-00 through 58-199 of the send matrix 51. Similarly, the output signals of the flip-flops of the tens counter 53 energize binary to decimal converters 59-0 through 59-19 sequentially, and the output signal of each of these converters is amplified by a send matrix driver 61 and then is applied to respective ones of the cross points 58-00 through 58-199 of the send matrix 51. Where digit counts of the counters 52 and 53 are used for self-testing of the apparatus, or for other purposes, additional ones of the binary to decimal converters 56 and 59 may be provided, as necessary. The last flip-flop (TENS FF5) of the tens counter 53 also is connected to feed a pulse to the group controller 24 as the tens counter completes each counting cycle, that is, as the stepping circuit 41 completes each sweep through the send matrix 51.

SEND MATRIX (FIGS. 2A AND 7)

Each of the two hundred cross points 58-00 through 58-199 of the send matrix 51 is a negative AND gate, at both inputs of which a negative potential must be present before a negative potential is produced at its output, and each AND gate is wired to apply signal, when energized, to an associated pair of the cable and program connecting terminals 22 and 23. As is illustrated in FIG. 7, the units and tens send matrix drivers 57 and 61 are wired to the AND gates 58-00 through 58-199 such that only one of the AND gates will receive a negative potential from both a units driver and a tens driver at any one time, and thus a signal is produced at the output of only one of the AND gates at any one time.

GROUP CONTROLLER (FIGS. 2A, 8A AND 8B)

Referring to FIG. 2A, it is seen that the group controller 24 for sequentially connecting the cable terminal groups C1-C30 to the apparatus in pairs, and for simultaneously connecting the corresponding ones of the program terminal groups P1-P30 to the apparatus, includes

a first binary counter 62 for connecting each cable terminal group and the corresponding program terminal group to the apparatus as test group I terminals. A second binary counter 63 is provided for connecting the cable and program terminal groups C1-C30 and P1-P30 to the apparatus as test group II terminals. In this regard, the group control counters 62 and 63 control relay trees 64 and 66, respectively, and each of the relay trees have output leads 64a and 66a wired to cable group connecting relays 67-I and 67-II, respectively, for connecting the cable terminal groups C1-C30 to the cable connecting terminals 22-I and 22-II, and also wired to program group connecting relays 68-I and 68-II, respectively, for connecting the program terminal groups P1-P30 to the program connecting terminals 23-I and 23-II.

More specifically, referring to FIG. 8A, it is seen that the counters 62 and 63 are in the form of flip-flop circuits in a simple series array, with the first flip-flop of the test group I control counter 62 receiving input pulses from the last flip-flop of the test group II control counter 63. As noted hereinabove, the counter 63 receives input pulses from the output of the tens binary counter 53 of the send matrix stepping circuit 41, and thus, for each sweep of the stepping circuit through the cross points 58-00 through 58-199 of the send matrix 51, an input pulse is received by the counter 63.

As the counter 63 receives input pulses from the send matrix stepping circuit 41, the flip-flops of the counter are energized to energize respective control relays 69-1 through 69-5. Referring to FIG. 8B, it is seen that as the relays 69-1 through 69-5 are energized they close respective contacts 69C-1 through 69C-5 to energize respective relays 71-1 through 71-5 of the relay tree 66. The relays 71-1 through 71-5 control contacts in the relay tree Z6 in a well-known manner, to complete electrical paths through the relay tree to its output leads 66a-0 through 66a-31 in sequence, thereby sequentially actuating the cable group connecting relays 67-II-1 through 67-II-30 and their corresponding program group connecting relays 68-II-1 through 68-II-30, and thus connecting the cable and program terminal groups C1-C30 and P1-P30 to the apparatus as test group II terminals for test purposes.

A portion of each input pulse to the counter 63 energizes a count delay generator 72 (FIGS. 2A and 8A) of the group controller 24, in the form of a monostable multivibrator. The generator 72 feeds a pulse back to the pulse gate 36 (FIGS. 2A and 6) to close the gate temporarily, so as to permit time for the above-described relays 67, 68, 69 and 71, as well as relays (subsequently to be described) of the counter 62 and the relay tree 64, to open and close their respective contacts, and for transient conditions as a result of this relay action to die out, before the next counting cycle of the stepping circuit begins.

As the counter 63 completes each of its counting cycles, one portion of the output pulse from its last flip-flop is applied to a count transfer control 73 in the form of two series connected one-shot multivibrators, for a purpose subsequently to be described, and the other portion of the pulse is applied to the first flip-flop of the counter 62, as noted above. Thus, for each complete counting cycle of the counter 63, the counter 62 is advanced one count.

As the counter 62 proceeds through its counting cycles in response to input pulses from the counter 63, it causes each of the cable terminal groups C1-C30 and its corresponding one of the program terminal groups P1-P30 to be connected to the apparatus as test groups I terminals (FIG. 4), by means of group control relays 74-1 through 74-5 and the relay tree 64 (FIG. 2A), in the same manner as described above with respect to the counter 63 for the test group II terminals. In this regard, the relay tree 64, which is not shown in detail in the drawing since it is substantially identical in construction and operation to the relay tree 66 (FIG. 8B), includes contacts which correspond to the contacts 69C-1 through 69C-5 and

which are closed by the relays 74-1 through 74-5, to energize relays which correspond to the relays 71-1 through 71-5 and which control respective contacts in the relay tree 64 to energize sequentially the cable and program group connecting relays 67-I and 68-I (FIG. 2A).

From the foregoing description, it is seen that when the stepping circuit 41 makes its initial sweep through the send matrix 51, none of the cable and program terminal groups C1-C30 and P1-P30 have yet been connected to the apparatus by the group controller 24. Instead, the apparatus tests itself to insure that signals are being fed from the send matrix 51, this being accomplished by error detect series 76 (FIGS. 2A and 9) subsequently to be described.

After the stepping circuit 41 completes its initial sweep through the send matrix 51, the output pulse from the tens binary counter 53 is applied to the counter 63 to raise it one count. The stepping circuit 41 then sweeps through the send matrix 51 again, whereupon the counter 63 is raised to its next count to energize the relays 67-II-1 and 68-II-1, thereby causing the first of the cable terminal groups C1 and its corresponding program terminal group P1 to be connected to the apparatus as test group II terminals. This sequence of operation is continued until all thirty cable terminal groups C1-C30 and their corresponding program terminal groups P1-P30 have been connected to the apparatus. During this initial counting cycle, the counter 62 has not yet been actuated to connect any of the terminal groups C1-C30 and P1-P30 to the apparatus as test group I terminals.

After the counter 63 completes its first counting cycle the output pulse from its last flip-flop is applied to the counter 62 to raise it one count, whereupon the apparatus proceeds through another counting cycle of the counter 63. When the next output pulse from the last stage of the counter 63 is applied to the counter 62, the counter 62 causes cable and program terminal groups C1 and P1 to be connected to the apparatus as test group I terminals. Up to this time the apparatus has been testing itself, and for shorts within the individual plugs P-00 through P-59.

When the counter 63 receives its next input pulse from the send matrix stepping circuit 41, the counter causes cable and program terminal groups C2 and P2 to be connected to the apparatus as test group II terminals. Now, as the stepping circuit 41 sweeps through the send matrix 51, the cable wiring between the cable terminal groups C1 and C2 is checked by the error detect circuits 76. When the stepping circuit 41 completes this sweep cycle the output pulse from the tens binary counter 53 to the counter 63 causes cable and program terminal groups C3 and P3 to be connected to the apparatus as test group II terminals, and the cable wiring between the cable terminal groups C1 and C3 is checked by the error detect circuits 76. This procedure continues until all subsequent cable terminal groups C4-C30 have been connected to the apparatus and checked with respect to cable terminal group C1, whereupon the counter 62 again is actuated from the counter 63 to connect cable and terminal groups C2 and P2 to the apparatus as test group I terminals. Cable terminal group C2 then is checked with respect to subsequent cable terminal groups C3-C30, with the cable and program terminal groups C2 and P2 as the test group I terminals. This testing procedure continues until all of the cable terminal groups C1-C30 have been connected to the apparatus by the operation of the counter 62 and tested as test group I terminals.

Referring to FIG. 8B, it is seen that the leads 66a-0 and 66a-31 are open and not connected to any other circuitry of the apparatus. Similarly, the lead of the relay tree 64 (not shown in detail) corresponding to the lead 66a-0 is open; however, the lead of the relay tree 64 corresponding to the lead 66a-31 is connected to the release relay 42 (FIG. 6), for energizing the relay and shutting off the apparatus, as above described, upon the completion of the test operation.

As noted hereinabove, each of the cable terminal groups C1-C30 is tested as test group I terminals against only the cable terminal groups subsequent thereto. In this regard, if the test group II control counter 63 began each counting cycle at its lowest count, all of the groups C1-C30 would be tested twice, thereby doubling the test time. To obviate this, the group controller 24 is arranged so that the counter 63 begins each counting cycle at a count which is one unit above the starting count of its preceding cycle.

For this purpose, the output of each flip-flop stage of the test group I control counter 62 is connected to a first leg of an associated count transfer gate in the form of an AND gate 77, and the output of each AND gate is connected to the corresponding flip-flop stage in the counter 63. Further, the output of the count transfer control 73 is connected to second legs of the AND gates 77 by a lead 78.

In the illustrated embodiment of the invention, the counter 63 begins its first counting cycle with a first count which is arbitrarily designated zero, and the final output pulse from the counter splits to energize the counter 62, to advance it to a first count of zero, and to energize the count transfer control 73. The count transfer control 73 then feeds a delayed pulse to each of the AND gates 77, and this pulse combines with a pulse from the energized first flip-flop stage of the counter 62 to energize the AND gate to which this stage is connected. The energized AND gate 77, which can energize any or all of the flip-flop stages in the counter 63, then energizes the first stage, thereby setting this counter at the same binary count as the counter 62, that is, a count of zero. In the transfer of the count of the counter 62 to the counter 63 upon the completion of the subsequent counting cycles of the counter 63, the delayed pulse from the count transfer control 73 combines with one or more pulses from the flip-flop stages of the counter 62, depending upon which stages are energized. Thus, as the counter 63 receives its first input pulse from the stepping circuit tens binary counter 53, at the beginning of its second counting cycle, the counter is stepped immediately to its second count of one, at the start of its third counting cycle it will be stepped immediately to a count of two, etc.

ERROR DETECT CIRCUITS (FIGS. 2A and 9)

Associated with each of the one hundred pairs of cable and program connecting terminals 22-I and 23-I, and the cross point 58 of the send matrix 51 from which the terminals of the pair receive their input signals, is one of the above-mentioned error detect or compare circuits 76, one of which, for the cross point 58-10, is shown in detail in FIG. 9 and designated 76-I. Similarly, associated with each of the one hundred pairs of cable and program connecting terminals 22-II and 23-II and its respective cross point 58 is another one of the compare circuits 76, one of which, for the cross point 58-190, also is shown in detail in FIG. 9 and designated 76-II. Inasmuch as all of the compare circuits 76-I are identical, and all of the compare circuits 76-II are identical, only the two circuits shown in FIG. 9 will be described.

The compare circuits 76-I and 76-II in FIG. 9 are connected to their respective cable connecting terminals 22-I and 22-II by leads 79-I and 79-II, and to their respective program connecting terminals 23-I and 23-II by leads 81-I and 81-II. The cable connecting terminal 22-I is connected to a respective one of one hundred leads 82 (only one shown), and each of the thirty cable terminals T (one from each of the cable terminal groups C1-C30, with two being shown in FIG. 9 and designated a cable input terminal T_{ci} and a cable output terminal T_{co}) which receives signals from and passes signals to the connecting terminal, is connectible to the lead 82 through a normally open contact 67-IC located in a lead 83 and closed by a respective one of the thirty cable connecting

relays 67-I as described hereinabove. Similarly, the cable connecting terminal 22-II is connected to a lead 84 and each of the thirty cable terminals T which receives signals from and passes signals to this connecting terminal is connectible to the lead 84 by a normally open contact 67-II located in a lead 86 and closed by a respective one of the thirty cable connecting relays 67-II. The corresponding terminals of the program terminal groups P1-P30 are connectible to the program connecting terminals 23-I and 23-II in the same manner by circuitry including contacts controlled by respective ones of the program connecting relays 68-I and 68-II.

As shown in FIG. 9, the compare circuit 76-I illustrates the function of one of the compare circuits when associated with the cable input terminal T_{ci} , while the compare circuit 76-II illustrates the function of one of the compare circuits when associated with the cable output terminal T_{co} , with the terminals T_{ci} and T_{co} properly connected by a cable wire C_w .

As each of the AN gates 58 of the send matrix 51, such as the gate 50-10 shown in FIG. 9, is energized, its output signal feeds to a point 87-I where the signal splits, with a portion of the signal feeding through a steering diode 88-1 to a point 89-I where it again splits with a portion then feeding to the cable connecting terminal 22-I by means of the lead 79-I. The other portion of the output signal feeds through a second steering diode 88-2 to a point 91-I where it again splits, with a portion then feeding to the program connecting terminal 23-I by means of the lead 81-I. At the points 89-I and 91-I, the other signal portions feed into the compare circuit 76-I and the compare circuit verifies that the send matrix output signal was received at both points.

From the program connecting terminal 23-I the signal portion feeds to a program input terminal T_{pi} , through a program wire P_w to a program output terminal T_{po} , to the program connecting terminal 23-II, and then to the compare circuit 76-II along the lead 81-II to a point 91-II. Similarly, the signal portion at the cable input connecting terminal 22-I feeds to the cable input terminal T_{ci} , through the cable wire C_w to the cable output terminal T_{co} , to the cable connecting terminal 22-II, and then to the compare circuit 76-II along the lead 79-II to a point 89-II.

Each compare circuit 76(-I or II) includes four NOR amplifiers 92, 93, 94 and 96, the amplifiers 94 and 96 being output amplifiers and having output leads 97 and 98, respectively. The amplifiers 92, 93, 94 and 96 are wired, as illustrated in FIG. 9, such that if the compare circuit 76 (-I or II) receives a signal at both of its associated points 89 (-I or II) and 91 (-I or II), or receives no signal at either point, neither of the output amplifiers 94 and 96 is energized and no signal appears on either of their output leads 97 and 98.

Thus, in the operation of the compare circuit 76-I in FIG. 9, if signals are received at both of the points 89-I and 91-I, signal portions feed from the point 89-I through steering diodes 88-3 and 88-4 into the compare circuit, and from the point 91-I through steering diodes 88-5 and 88-6 into the compare circuit, whereby neither of the output amplifiers 94 and 96 is energized and no signal appears on either of their output leads 97 and 98. However, if one of the points 89-I or 91-I receives no signal, one or the other of the output amplifiers 94 and 96 will be energized to initiate a sequence of operations culminating in shut down of the apparatus, as will subsequently become apparent.

Similarly, in the operation of the compare circuit 76-II in FIG. 9, the signals fed to the points 89-II and 91-II pass through diodes 88-3, 88-4, 88-5, and 88-6 into the compare circuit 76-II, whereby neither of its output amplifiers 94 and 96 is energized. At the same time, if the cable input terminal T_{ci} is not shorted to, or open with respect to another terminal T of the cable C, none of the other compare circuits 76-I and 76-II of the

apparatus will be energized and the stepping circuit 41 (FIG. 7) steps to the next send matrix cross point 58-11.

If the cable input terminal T_{ci} is improperly connected to the cable output terminal T_{co} by the wire C_w , or is shorted to the cable output terminal rather than properly wired thereto, the program wire P_w , instead of being connected to the cable output terminal T_{po} as shown in FIG. 9, would be connected to a different program terminal. An output signal then is received from the cable output terminal T_{co} at the point 89-II when it should not be receiving a signal, but no signal is received at the program point 91-II, and thus the output amplifier 94 of the compare circuit 76-II is energized to indicate a short.

Similarly, if the wire C_w is broken, or instead of being properly connected to the cable output terminal T_{co} as shown in FIG. 9 is improperly connected to a different terminal T of the cable C, an output signal from the program output terminal T_{po} is received at the program point 91-II, but no signal is received at the cable point 89-II, and the output amplifier 96 of the compare circuit 76-II is energized to indicate an open.

From FIG. 9, it is seen that as the stepping circuit 41 (FIG. 7) proceeds through the send matrix 51 beyond the cross point 58-10 and subsequently applies a signal to the cross point 58-190, the signal will feed to a point 87-II which corresponds to the point 87-I. It is apparent that portions of the signal then will flow into the compare circuit 76-II, and in reverse directions through the cable and program wires C_w and P_w to the compare circuit 76-I, whereby the functions of the two compare circuits are reversed from that as above described. Thus, each wire C_w of the cable C is tested twice by the apparatus as it proceeds through its normal cycle of operation.

UNITS AND TENS DIGIT GROUPING CIRCUIT (FIGS. 2B and 9)

In connection with a units and tens digit grouping circuit 99 of the apparatus, reference is first made to FIGS. 4 and 7 for the purpose of further illustrating the relationship between the two hundred cross points 58-00 through 58-199 of the send matrix 51, the compare circuits 76-I and 76-II, and the two hundred terminals T of four of the test plugs P-00 through P-59 which are connected to the apparatus at any one time. In this regard, cross points 58-00 through 49 apply signals sequentially to the cable connecting terminals 22-I-00 through 49 of the test plug quadrant W; cross points 58-50 through 99 apply signals sequentially to the terminals 22-I-00 through 49 of the test plug quadrant X; cross points 58-100 through 149 apply signals sequentially to the terminals 22-II-0 through 49 of the test plug quadrant Y; and cross points 58-150 through 199 apply signals sequentially to the terminals 22-II-00 through 49 of the test plug quadrant Z. Thus, by way of illustration, the cross point 58-10 in FIG. 9 feeds input signals to the cable connecting terminal 22-I-10 in test plug quadrant W (W-10), and thus to the terminal 10 of the plugs P-00 through P-59 which are connected to the apparatus in test plug quadrant W, and this cross points compare circuit 76-I receives output signals from these terminals. Similarly, the cross points 58-190 in FIG. 9 feeds input signals to the cable connecting terminal 22-II-40 in quadrant Z (Z-40), and thus to the terminal 40 of the plugs P-00 through P-59 which are connected to the apparatus in test plug quadrant Z, and this cross points compare circuit 76-II receives output signals from these terminals.

Referring to FIG. 9, it is seen that the purpose of the units and tens digit grouping circuit 99 is to collect short and open digit information from the output amplifiers 94 and 96 of the compare circuits 76-I and 76-II. With respect to the test plug quadrant W, all compare circuit output amplifiers 94 (shorted terminal) for the cable connecting terminals 22-I having the same units digit feed to a respective one of a plurality of ten (one

for each of the units digits 0 through 9) gating circuits 101W; all output amplifiers 96 (open terminal) for the cable connecting terminals having the same units digit feed to a respective one of a plurality of ten gating circuits 102W; the amplifiers 94 for the cable connecting terminals having the same tens digit feed to a respective one of a plurality of five gating circuits 103W; and the amplifiers 96 for the cable connecting terminals having the same tens digit feed to a respective one of a plurality of five gating circuits 104W. For example, the output amplifiers 94 for the terminals W-10 through W-19, having the common tens digit 1, are all connected to the gating circuit 103W-1, and the output amplifiers 96 for these terminals all are connected to the gating circuit 104W-1, as is illustrated in FIG. 9 by the output amplifiers 94 and 96 for the terminal W-10 (cross points 58-10). The output amplifiers 94 and 96 of the compare circuits 76-I and 76-II for the cable connecting terminals 22-I and 22-II in the test plug quadrants X, Y and Z are connected in the same manner to gating circuits 101X, Y and Z, 102X, Y and Z, 103X, Y and Z and 104X, Y and Z.

When a malfunction in the apparatus or a fault in the cable C is found by the compare circuits 76-I and 76-II such that one of the grouping gates 101W, X, Y and Z through 104W, X, Y and Z receives an input pulse from one of its associated compare circuits, the output pulse of the grouping gate energizes the error detect gate circuit 47 (FIG. 2B). The output pulse of the error detect gate circuit 47 causes closing of the pulse gate 36, as noted hereinabove, causing the apparatus to lock on the error.

More specifically, when any one of the units digit short grouping gates 101W, X, Y and Z has a pulse applied thereto from one of its associated compare circuits 76, the output pulse of the grouping gate is applied to a gate 47a (FIG. 10) of the circuit 47. Similarly, the output pulse of any one of the units digit open grouping gates 102W, X, Y and Z is applied to a gate 47b, the output pulse of any one of the tens digit short grouping gates 103W, X, Y and Z is applied to a gate 47c, and the output pulse of any one of the tens digit open grouping gates 104W, X, Y and Z is applied to a gate 47d. The gates 47a, b, c and d have their outputs connected to a common lead 107 which is connected to feed an output pulse from one of these gates to the pulse gate 36 (FIG. 6) to close the gate by temporarily inhibiting the flow of pulses from the pulse generator 39 to the pulse gate. This output pulse also feeds by way of the lead 107 to energize a delay circuit 108 (FIG. 6).

After a predetermined time delay, a relay 109 of the delay circuit 108 is energized and closes a contact 109C to energize a relay 111. The energized relay 111 closes a first contact 111C-1 in the pulse gate 36 to lock the gate closed and also closes a contact 111C-2 to initiate a read-out cycle, as will subsequently be described. In this regard, however, the time delay of the delay circuit 108 is such as to permit transient conditions in the apparatus to die out, whereby the compare circuits 76-I and 76-II can verify that an error in the cable or a malfunction in the apparatus is actually present, and that the initial inhibiting of the flow of pulses from the pulse generator 39 to the pulse gate 36 was not due to transient conditions. If the initial pulse inhibiting was due to transient conditions, the relay 109 of the delay circuit 108 does not become energized, and when the transient conditions have dissipated, the pulses again will begin to flow from the pulse generator 39 through the pulse gate 36, whereas if the inhibiting was due to an actual error, the relay 109 is energized to energize the relay 111, which then locks the pulse gate closed and initiates the read-out cycle.

DIGIT INFORMATION COLLECTING CIRCUITS (FIGS. 2B AND 10)

The grouping gates 101W, X, Y and Z through 104W, X, Y and Z of the digit grouping circuit 99 are wired to the error detect gates 47a, b, c and d through a digit

information collecting circuit 112, which also is designed to combine units and tens digit information for the four test plug quadrants W, X, Y and Z. In this regard, as is shown in detail in FIG. 10, the circuit 112 includes ten sets (one for each of the units digits 0 through 9) of four gates 113W, X, Y and Z for collecting units digit short information, and ten sets of four gates 114W, X, Y and Z for collecting units digit open information. Thus, the four grouping gates 101W, X, Y and Z (units digit short information) for each units digit are wired to respective ones of the collecting gates 113W, X, Y and Z for that digits, and the four grouping gates 102W, X, Y and Z (units digit open information) for each units digit are wired to respective ones of the collecting gates 114W, X, Y and Z for that digit. For example, the four grouping gates 101W-0, 101X-0, 101Y-0 and 101Z-0 are wired to the collecting gates 113W, X, Y and Z, respectively, for the units digit zero.

Each set of the units digit short information collecting gates 113W, X, Y and Z has a first normally open output lead 116 for connecting the gates to a first input of a respective one of ten information transfer circuits 117-0 through 117-9 (only circuit 117-0 being shown), and a second output lead 118 connected by a lead 119 to the input of the error detect gate 47a. The sets of units digit open information collecting gates 114W, X, Y and Z are connectible to the information transfer circuits 117 by normally open output leads 121, and are connected by a lead 122 to the error detect gate 47b in the same manner.

Similarly, the grouping gates 103W, X, Y and Z for tens digit short information are wired to five sets of tens digit short information collecting gates 123W, X, Y and Z, the grouping gates 104W, X, Y and Z for tens digit open information are wired to five sets of tens digit open information collecting gates 124W, X, Y and Z, these collecting gates also being connectible to the information transfer circuits 117, and being connected to the error detect gates 47c and 47d, respectively.

INFORMATION TRANSFER CIRCUITS (FIGS. 2B AND 10)

As noted hereinabove, the apparatus is designed to provide twelve digits or pieces of information (FIG. 5), each of which could be any one of a plurality of digits, and which in the case of a units digit could be any one of ten digits 0-9. Accordingly, to reduce the amount of wiring required and the size of the apparatus, the apparatus is designed to transfer test information from the send matrix drivers 57 and 61 (FIGS. 2A and 7), the digit information collecting circuit 112 (FIGS. 2B and 10), and from a plug number translator 126 (FIGS. 2B and 14), to the memory 37 (FIGS. 2B and 12) and ultimately to the read out 21 (FIGS. 2B, 5 and 12), one item or digit at a time rather than simultaneously, by means of the information transfer circuits 117.

As is shown in FIG. 10 by the information transfer circuit 117-0, each of the ten information transfer circuits 117-0 through 117-9 includes suitable signal amplifiers 117A, and a relay 117R which controls an associated contact for the purpose of transferring cable terminal digit information from the send matrix drivers 57 and 61 and the information collecting circuit 112 to the memory 37, in a manner to be described. Each of the information transfer circuits 117 also includes a normally open contact 111C-3, which is closed by the relay 111 of the delay circuit 108 upon the apparatus detecting an error, as above described, to connect the information transfer circuit to a respective one of a plurality of input leads 37a-0 through 37a-9 (FIGS. 10 and 12) of the memory 37.

Associated with each of the information transfer circuits 117-0 through 117-4 is a terminal tens test information collecting point 117P (left-hand side of FIG. 10) to which the tens matrix drivers 61 are wired by leads 61a through suitable diodes, which are not shown. More

specifically, the tens matrix drivers 61 which cause the send matrix 51 to apply signals to the cable plug terminals T which have the same tens digit, are all wired to the collecting point 117P for that digit. For example, wired to the collecting point 117P of the information transfer circuit 117-0 which is shown in FIG. 10, are the tens matrix drivers 61-0, 61-5, 61-10 and 61-15, which cause signals to be applied to the cable plug terminals T having the tens digit zero (see FIGS. 4 and 7).

MEMORY (FIGS. 2B AND 12)

The memory circuit 37 includes twelve circuit branches, one for each type of digit information to be determined, and three of these branches, 37TUO for terminal units open information, 37TTO for terminal tens open information and 37TUS for terminal units short information, are shown in FIG. 12. In addition, the memory circuit 37 includes nine other branches, which are not shown, and which, in accordance with the previously described abbreviations, are designated as branches 37TTS, TUT, TTT, PUO, PTO, PUS, PTS, PUT and PTT.

Inasmuch as the various units digit information branches 37TUO, TUS, PUO, etc., of the memory circuit 37 are identical, only one of the branches will be described. Referring to FIG. 12, it is seen that the branch 37TUO includes ten relays 37TUOR, one for each of the digits 0-9. Each of the relays 37TUOR is connectible to the input lead 37a which represents the same digit as the relay, and as noted hereinabove, the input lead 37a is connectible to the information transfer circuit 117 for the digit through the transfer circuit's contact 111C-3 (FIG. 10). As is shown in FIG. 12, each of the relays 37TUOR, when energized, locks operated, and closes a contact to light a respective digit indicating filament of the read-out lamp 21TUO.

The terminal tens digit information branches 37TTO, etc. of the memory circuit 37, are arranged and operate in the same manner as the units digit information branches 37TUO, etc., except that, as is illustrated by the branch 37TTO in FIG. 12, only five relays 37TTOR are required, one for each of the digits 0-4. Similarly, the plug tens digit information branches 37PTO, etc. (not shown), require only six relays, one for each of the digits 0-5.

READ-OUT CYCLE CONTROL CIRCUIT (FIGS. 2B AND 11)

The apparatus determines the digits involved in an error and transfers them into the read out 21 sequentially under the control of a read-out cycle control circuit 128. Referring to FIG. 11A, it is seen that the read-out cycle control circuit 128 includes a relay type binary counter 129 which is responsive to pulses produced by a pulsing relay 131, the pulsing relay alternately closing and opening a contact 131C-1 in the operating path of the first stage of the counter. The counter 129 includes four relay stages having respective relays 132-1 through 132-4 and 133-1 through 133-4. The relays 132-1 through 132-4 control respective contacts 132-1C-1 through 132-4C-1 in a relay tree 134 (FIG. 11B) to energize sequentially relay tree relays 136TUO, TTO, TUS, etc. Further, the relays 132-1 through 132-4, by the control of certain of these contacts (lower portion of FIG. 11B), cooperate with the relays 133-1 through 133-4, which control contacts 133-1C-1 and 2, and 133-2C-1 through 133-4C-1 in the relay tree 134, to complete an operating path to the release relay 42 (FIG. 6) when the read-out cycle is completed, as will be apparent to those skilled in the art, to shut off the apparatus.

To illustrate the operation of the relay tree 134 in the information determining and transferring operation, the relay 136TUS of the relay tree, when energized, closes ten contacts 136TUSC (FIG. 10) in the leads 116 to connect the ten sets of units digit short collecting gates 113W, X, Y and Z to the first inputs of respective ones of the ten information transfer circuits 117. Similarly, the relays 136

TUO, TTS and TTO close contacts 136 TUOC, TTSC and TOC (respectively, to connect the sets of gates 114W, X, Y and Z, 123W, X, Y and Z and 124W, X, Y and Z, to the first inputs of respective ones of the information transfer circuits 117.

The relay 136TUT, upon being energized, closes ten contacts 136TUTC (FIG. 7 and left-hand side of FIG. 10) to connect the units matrix drivers 57 to the first inputs of respective ones of the information transfer circuits 117. Similarly, the relay 136TTT closes five contacts 136TTTC (one shown in FIG. 10) to connect the terminal tens test information collecting points 117P, and thus the tens matrix drivers 61, to the first inputs of the information transfer circuits 117-0 through 117-4.

Referring to FIG. 13, it is seen that the relays 136 PUO, PTO, PUS, PTS, PUT and PTT each close four contacts 136 PUOC-W, X, Y and Z, 136 PTOC-W, X, Y and Z, etc., in a plug number pretranslator 137 for determining plug number information in a manner to be described. Referring to the lower portion of FIG. 14B, it is seen that the relays 136 PUO, PUS and PUT also close respective contacts 136PUOC', PUSC', and PUTC' to energize a relay 136UP which closes ten contacts 136UPC-0 through 9 (one also shown in FIG. 10) in the plug number translator 126 to connect the translator to second inputs of the information transfer circuits 117 during the information determining and transferring operation. Similarly, as is shown in the lower portion of FIG. 14C, the relays 136 PTO, PTS and PTT close respective contacts 136PTOC', PTSC' and PTTC' to energize a relay 136TP which closes five contacts 136TPC-0 through 5 (one also shown in FIG. 10) to connect the translator 126 to the second inputs of respective ones of the information transfer circuits 117. The contact 111C-2 (FIGS. 6 and 11A), which is closed by the relay 111 upon the detection of an error, is included in the operate path of a delay relay 142. The operate path of the delay relay 142 preferably also includes a suitable relay check circuit (top of FIG. 11A) which includes contacts (not shown) controlled by selected relays of the read-out control circuit 128. As desired, and having certain of the contacts 132-1C through 132-4C of the relay tree 134 connected thereto by a lead 134a, as illustrated at the bottom of FIG. 11B, whereby the operate path for the delay relay 142 is completed by the closing of the contact 111C-2 only if all of the relays involved are in a deenergized state at the beginning of the information determining and transferring operation.

Upon being energized the delay relay 142 closes a contact 142C to energize a relay 143 which locks operated, which opens a contact 143C-1 to drop out the relay 142, and which closes a contact 143C-2 to energize the pulsing relay 131. The energized relay 131 then opens a contact 131C-2 in the lock path of the relay 143 to drop out this relay, and opens a contact 131C-3 in the operate path of the relay 142 to maintain this relay temporarily inoperative. The relay 143, upon being deenergized, releases its contact 143C-2 to deenergize the relay 131, whereupon this relay releases its contact 131C-3 to reenergize the relay 142, and the cycle repeats.

Referring to FIG. 11E, it is seen that as the relays 132-1 through 132-4 of the counter 129 are energized in response to the pulsing relay 131, they also close respective contacts 132-1C-2 through 132-4C-2, to energize relays 144-1 through 144-4. The relays 144-1 through 144-4 control respective contacts in a relay tree 146 so as to energize sequentially relays 147 TUO, TTO, TUS, etc., which correspond to the relays 136 TUO, TTO, TUS, etc. of the relay tree 134 (FIG. 11B) and which sequentially close respective contacts 147 TUOC, TTOC, TUSC, etc. (FIG. 12) forming a memory information steering 37S, to connect outputs of the information transfer circuits 117 sequentially to the memory branches 37TUO, 37TTO, 37TUS, etc., during the information determining and transferring operation.

17

The first stage of the counter 129 is energized by the closing of the contact 131C-1 by the pulsing relay 131, and subsequent stages are energized by the closing of a contact by the relay 132 of the preceding stage. To illustrate the manner in which each stage operates, upon closing of the contact 131C-1 by the relay 131, the relay 132-1 is energized and closes a contact 132-1C-3 to lock operated, and also opens a contact 132-1C-4 in the operating path of the relay 133-1 so that its battery side is at ground potential through the contact 131C-1 and a lead 133a, and thus the relay cannot operate. Upon release of the contact 131C-1, however, the relay 133-1 becomes energized through the lock path of the relay 132-1, to open a first contact 133-1C-3 and to close a second contact 133-1C-4. Upon the next closing of the contact 131C-1 the battery side of the relay 132-1 is connected to ground through this contact and the contact 133-1C-4. This deenergizes the relay 132-1 and it releases its associated contacts 132-1C-3 and 4 so that upon release of the contact 131C-1 the relay 133-1 is deenergized. Upon the next closing of the contact 131C-1, the cycle then repeats. From this description, and from FIGS. 11C and 11D, which illustrate the operate times of the relays 132 and 133, and a truth table for the relays 132, respectively, the manner in which the counter 129 operates to control the relay trees 134 and 146, as above described, will be apparent to those skilled in the art.

Assuming that the apparatus has found an error in the cable C and that the error detect gate circuit 47 has caused the apparatus to lock upon the error as above-described, the apparatus proceeds to determine the nature of the error, and the terminal numbers and plug numbers involved. For example, in determining whether the error is an open wire, and if so, the units digit of the terminal T which is open, the relay 136TUO of the relay tree 134 (FIG. 11B) in the read-out cycle control circuit 128 is energized and closes the ten contacts 136TUOC (FIG. 10) in the output leads 121 of the digit information collecting circuit 112 to connect the ten sets of gates 114W, X, Y and Z to the first inputs of respective ones of the ten information transfer circuits 117. At the same time the relay 147TUO in the relay tree 146 (FIG. 11E) of the read-out cycle control circuit 128 closes its ten contacts 147TUOC (FIGS. 10 and 12) of the memory information steering 37S to connect the information transfer circuits 117 to respective ones of the ten relays 37TUOR in the memory 37. Thus an input pulse to one of the ten sets of gates 114W, X, Y and Z of the digit information collecting circuit 112, from the digit grouping circuit 99, energizes the relay 117R (FIG. 10) of the information transfer circuit 117 for the digit involved to connect the respective one of the ten relays 37TUOR to ground, whereby the relay operates to energize the read-out lamp 21TUO to indicate the digit.

The determination and transfer of the tens digit of an open terminal T, and of the units and tens digits of a shorted terminal, is similar to the operation set forth above with regard to the determination and transfer of the units digit for an open terminal, utilizing the relays 136TTO, TUS and TTS, the relays 147TTO, TUS and TTS, the memory branches 37TTO, TUS and TTS, and the read-out lamps 21TTO, TUS and TTS.

In determining the units digit of the terminal T under test when an apparatus malfunction or a cable error is found, the relay 136TUT of the relay tree 134 closes its ten contacts 136TUTC (FIGS. 7 and 10) to connect the send matrix units digit drivers 57 to respective ones of the information transfer circuits 117. At the same time the relay 147TUT in the relay tree 146 closes its ten contacts 147TUTC (one shown in FIG. 10) of the memory information steering 37S to connect the information transfer circuits 117 to their respective memory relays 37TUTR (not shown). Thus, when the apparatus finds and locks upon an error, the units driver 57 which is then energized applies a pulse to its information transfer cir-

18

cuit 117 to energize the relay 117R of the circuit, thereby causing the memory relay 37TUTR for the digit involved to operate the read-out lamp 21TUT.

In determining the tens digit of the terminal T under test when an error is found, the apparatus operates in a manner similar to that described above for determining the units digit. Thus, the relay 136TTT operates its five contacts 136TTTC (one shown in FIG. 10) so that the information collecting points 117P (and thus the send matrix tens drivers 61 in FIG. 7) are connected to the information transfer circuits 117-0 through 4. Further, the relay 147TTT closes its five contacts 147TTTC (not shown) in the memory steering 37S, and the memory branch relay 37TTTR (not shown) for the digit involved energizes the read-out lamp 21TTT.

TEST PLUG QUADRANT DETECTOR (FIGS. 2B AND 13)

In determining the number of the plug P-00 through P-59 which is under test when an error is found, the apparatus first ascertains the quadrant W, X, Y or Z (FIG. 4) in which the plug is located, by circuitry including a test plug quadrant detector 151 (FIGS. 2B and 13). In this regard, the send matrix tens digit drivers 61-0 through 4 (FIGS. 2A and 7), for causing signals to be applied to the terminals T of the cable plugs P-00 through P-59 which are connectible to the apparatus in quadrant W, also apply input signals to a first gating circuit 152W, as shown in FIG. 13; the tens digit drivers 61-5 through 9, for causing signals to be applied to the terminals of the plugs of quadrant X also apply input signals to a gating circuit 152X; the tens digit drivers 61-10 through 61-14, for causing signals to be applied to the terminals of the plugs of quadrant Y also apply input signals to a gating circuit 152Y; and the tens digit drivers 61-15 through 19, for causing signals to be applied to the terminals of the plugs of quadrant Z also apply input signals to a gating circuit 152Z.

PLUG NUMBER PRETRANSLATOR (FIGS. 2B AND 13)

The circuitry for determining the quadrant of the test plug P-00 through P-59 also includes the plug number pretranslator 137 (FIGS. 2B and 13). In this regard, the gating circuits 152W, X, Y and Z of the test plug quadrant detector 151 are connectible to relays 153W, X, Y and Z (FIG. 13) of the pretranslator 137 by the contacts 136PUTC-W, X, Y and Z, or the contacts 136TTTC-W, X, Y and Z, of the relays 136PUT and 136PTT of the cycle control circuit 128, for energizing one of the relays and thus determining the quadrant W, X, Y or Z in which the test plug is located.

To enable the plug number pretranslator 137 to determine the quadrant W, X, Y or Z in which a shorted one of the plugs P-00 through P-59 is located, the ten grouping gates 101W (FIG. 9) of the grouping circuit 99 are connected to the pretranslator by respective leads 154 and through suitable diodes to a common lead 156. Similarly, the five grouping gates 103W for the tens digits also are connected by respective leads 157 through diodes to the lead 156. The lead 156 is connectible to the relay 153W through either the contact 136PUSC-W or 136PTSC-W of the read-out cycle control circuit relays 136PUS and 136PTS. The terminal units and tens digits grouping gates 101X, Y and Z and 103X, Y and Z for the plug quadrants X, Y and Z, are wired in the same manner to respective ones of the plug pretranslator relays 153X, Y and Z, as illustrated in FIG. 13.

Accordingly, assuming that the units digit for a shorted one of the plugs P-00 through P-59 is being determined, the relay 136PUS in the cycle control circuit 128 closes the contacts 136PUSC-W, X, Y and Z in the four branches of the plug pretranslator 137 so that an input pulse to the pretranslator from an energized one of the grouping gates 101W, X, Y and Z actuates one of the

relays 153W, X, Y and Z, depending upon the quadrant in which the shorted plug is located. Similarly, when the tens digit for the shorted plug is being determined, the relay 136PTS in the cycle control circuit 128 closes the four contacts 136PTSC-W, X, Y and Z, whereby one of the relays 153W, X, Y and Z is actuated from the energized one of the tens digit grouping gates 103W, X, Y and Z.

The grouping gates 102W, X, Y and Z and 104W, X, Y and Z for collecting terminal open information, are wired to the plug number pretranslator 137 in the same manner as the grouping gates 101W, X, Y and Z and 103W, X, Y and Z for collecting terminal short information. Further, operation of the pretranslator 137 when the apparatus is determining open plug information is similar to its operation for the determination of shorted plug information, as above described, with the contacts 136PUOC-W, X, Y and Z and then contacts 136PTOC-W, X, Y and Z, being sequentially closed by the relays 136PUO and 136PTO of the read-out cycle control circuit 128.

PLUG NUMBER TRANSLATOR (FIGS. 2B AND 14)

The units digit and the tens digit of one of the plugs P-00 through P-59 which is under test, shorted and/or open, is finely determined by the plug number translator 126, shown in detail in FIG. 14. The translator 126 includes a first relay circuit 126-I (FIG. 14A), which is associated with the test group I cable connecting terminals 22-I illustrated in FIG. 4, and a second relay circuit 126-II, which is associated with the test group II cable connecting terminals 22-II. Since the relay circuits 126-I and 126-II are identical in construction, only the relay circuit 126-II is shown in detail, with the relay circuit 126-I being illustrated schematically.

The output leads 66a of the group controller relay tree 66 (FIGS. 2A and 8B) which controls the connection of the cable and program terminal groups C1-C30 and P1-P30 to the apparatus as test group II terminals, are connected to respective points 158-II-1 through 158-II-30 of the relay circuit 126-II by leads 66b, and the output leads 64a of the relay tree 64 (FIG. 2A), which controls the connection of the cable and program terminal groups to the apparatus as test group I terminals, similarly are connected to respective points 158-I-1 through 158-I-30 of the relay circuit 126-I in the same manner by leads 64b.

The circuitry of the plug number translator 126 on the left-hand side of FIG. 14A, together with the circuitry in FIG. 14B, determines the units digits of the plugs P-00 through P-59 which are involved when an error is found. In this regard, it is seen that the relay circuit 126-II includes ten relays 159-II, one for each of the units digits 0-9, and that the relay circuit 126-I similarly includes ten relays 159-I. Each of the thirty points 158-II of the relay circuit 126-II is wired to two of the relays 159-II which are representative of the units digits of the two plugs in the cable terminal group C1-C30 which is connected to that point. For example, referring to FIG. 3, it is seen that the cable plugs P-00 and P-01 are in cable terminal group C-1, and therefore relay circuit point 158-II-1 is wired to the relays 159-II-0 and 159-II-1. Similarly, cable plugs P-02 and P-03 are in cable terminal group C-2, and therefore, the relay circuit point 158-II-2 is wired to the relays 159-II-2 and 159-II-3, the cable plugs P-24 and P-25 are in cable terminal group C-13, and therefore relay circuit point 158-II-13 is wired to relays 159-II-4 and 159-II-5, etc.

From FIGS. 3 and 4, it is seen that when one of the cable terminal groups C1-C30 is connected to the apparatus as test group II terminals, the even numbered ones of the plugs P-00 through P-59 always are located in test plug quadrant Y and the odd numbered cable plugs always are located in test plug quadrant Z. There-

fore, the even numbered ones of the relays 159-II are wired to a common lead 162 which includes a contact 153YC controlled by the relay 153Y in the plug number pretranslator 137 (FIG. 13), and the odd numbered ones of the relays 159-II are wired to a common lead 163 which includes a contact 153ZC controlled by the relay 153Z in the plug number pretranslator.

The relay circuit 126-I is wired in the same manner as the relay circuit 126-II, and thus the even numbered ones of the relays 159-I are wired to a common lead 164 which includes a contact 153WC controlled by the relay 153W in the plug number pretranslator 137, and the odd numbered ones of these relays are connected to a common lead 166 including a contact 153XC controlled by the pretranslator relay 153X.

The relays 159-I-0 and 159-II-0, when energized, close respective contacts 159-IC-0 and 159-IIC-0 (FIG. 14B) connected in common to the contact 136UPC-0 for connecting the plug number translator 126 to the second input of the information transfer circuit 117-0 (FIG. 10). Similarly, other relay contacts 159-IC-1 through 159-IC-9 and 159-IIC-1 through 159-IIC-9 are wired in pairs to the contacts 136UPC-1 through 136UPC-9 for connecting the plug number translator 126 to the second inputs of the other nine information transfer circuits 117-1 through 117-9.

With the apparatus locked upon an error which has been found by the error detect circuits 76-I and 76-II, one of the points 158-II-1 through 158-II-30 of the relay circuit 126-II is connected to ground through the set of operative output leads 66a and 66b of the relay tree 66 (FIG. 8B) in the group controller 24. Similarly, one of the points 158-I-1 through 158-I-30 of the relay circuit 126-I is connected to ground through the operative set of output leads 64a and 64b of the group controller relay tree 64.

Assuming that the apparatus is determining the units digit of the one of the plugs P-00 through P-59 which is under test, the relay 136UP (lower portion of FIG. 14B), which is energized upon the closing of the contact 136PUTC' by the relay 136PUT (FIG. 11B) of the relay tree 134 in the cycle control circuit 128, closes its ten contacts 136UPC-0 through 9 to connect the plug number translator 126 to the second inputs of the information transfer circuits 117 (FIG. 10); the relay 147PUT (FIG. 11E) of the relay tree 146 in the read-out cycle control circuit 128 closes its ten contacts 147PUTC (one shown in FIG. 10) in the memory steering 37S to connect the information transfer circuits 117 to the relays 37PUTR (not shown) in the memory 37; the relay 136PUT also closes its four contacts 136PUTC-W, X, Y and Z in the plug number pretranslator 137 (FIG. 13) to connect the sets of gates 152W, X, Y and Z of the test plug quadrant detector 151 to the relays 153W, X, Y and Z, respectively, whereby one of these relays is energized by a pulse from the operative tens matrix driver 61 (FIGS. 2A and 7); the relay 136UP also closes contacts 136UPC' (left-hand side of FIG. 14A) in the leads 162, 163, 164 and 166, whereby one of the contacts 153WC, XC, YC or ZC is closed by the energized relay 153W, X, Y or Z to energize either one of the two relays 159-I which is connected to the grounded point 158-I, or one of the two relays 159-II which is connected to the grounded point 158-II. The energized relay 159-I or 159-II, as the case may be, then closes its associated one of the contacts 159-IC-0 through 9 or 159-IIC-0 through 9 (FIG. 14B), thereby connecting the respective information transfer circuit 117 to ground to cause operation of its associated memory relay 37PUTR (not shown) and energization of the read-out lamp 21PUT (FIG. 5) to indicate the digit involved.

For example, if plug P-24 of cable terminal group C-13 is connected to the apparatus in test group II, and is the plug under test, the relay 153Y (FIG. 13) closes the contact 153YC (FIG. 14A) to energize the relay

159-II-4, which then closes its contact 159-IIC-4 to connect the information transfer circuit 117-4 to ground. If the plug P-24 were connected to the apparatus as test group I, contact 153WC would be closed by the relay 153W to energize the relay 159-I-4 (not shown), which would then close its contact 159-IC-4 to connect the information transfer circuit 117-4 to ground.

The operation of the plug number translator 126 in determining the units digit for one of the plugs P-00 through P-59 which is shorted or open, is the same as described above for the determination of the units digit of a plug under test, utilizing the relays 136PUS, 136PUO, 147PUS and 147PUO of the read-out cycle control circuit 128 and the circuitry associated with these relays.

The circuitry of the plug member translator 126 shown on the right-hand side of FIG. 14A and in FIG. 14C is used in the determining of the tens digit information of the cable plugs P-00 through P-59 which are involved when an error is found, and the operation thereof is quite similar to the operation of the circuitry for determining plug units digit information. Thus, each of the thirty points 158-II of the relay circuit 126-II is wired to one of five relays 167-II representative of the tens digit of the plugs in the cable terminal group C1-C30 for that point. For example, as is shown in FIG. 3, cable terminal groups C1-C5 include plugs P-00 through P-09 and thus the points 158-II-1 through 158-II-5 are wired to relay 167-II-0, the cable terminal groups C6-C10 include plugs P-12 through P-19, and thus points 158-II-6 through 158-II-10 are wired to relay 167-II-1, etc. The points 158-I in the relay circuit 126-I are wired in the same way to relays 167-I-0 through 167-I-5.

The relays 167-I-0 and 167-II-0, when energized, close respective contacts 167-IC-0 and 167-IIC-0 (FIG. 14C) connected in common to the contact 136TPC-0 for connecting the plug number translator 126 to the second input of the information transfer circuit 117-0 (FIG. 10). Similarly, the relays 167-I-1 through 167-I-5 and 167-II-1 through 167-II-5 control contacts wired in pairs to the contacts 136TPC-1 through 136TPC-5 for connecting the plug number translator 126 to the second inputs of the information transfer circuits for the digits 1 through 5.

In the operation of the plug number translator 126 to determine the tens digit of one of the plugs P-00 through P-59, such as the plug under test, the relay 136TP (lower portion of FIG. 14C) is energized by the relay 136PTT (FIG. 11B) to close the six contacts 136TPC, and the relay 147PTT (FIG. 11E) closes its six contacts 147PTTC (one shown in FIG. 10) in the memory steering 37S. The relay 136TP also closes four contacts 136TPC' (left-hand side of FIG. 14A), and one of the contacts 153WC, XC, YC or ZC is closed by its associated relay 153W, X, Y or Z (FIG. 13) to energize either one of the relays 167-I which is connected to the grounded point 158-I, or one of the relays 167-II which is connected to the grounded point 158-II. The energized relay 167-I or 167-II, as the case may be, then closes its associated one of the contacts 167-IC-0 through 5 or 167-IIC-0 through 5, thereby connecting the respective information transfer circuit 117 to ground to cause operation of its associated memory relay 37PTTR (not shown), and of the read-out lamp 21PTT to indicate the digit involved.

In determining the tens digit information for one of the plugs P-00 through P-59 which is shorted or open, the translator 126 operates in the same manner as above described for determining the tens digit of the plug under test, utilizing the relays 136PTS, 136PTO, 147PTS and 147PTO of the cycle control circuit 128 and the circuitry associated with these relays.

OPERATION

In operation, after the cable plugs P-00 through P-59 of the cable C have been plugged into the apparatus by insertion into the above-mentioned receptacles, the start

button 27 (FIG. 6) of the start control circuit 26 (FIGS. 2A and 6) is depressed to energize the start relay 28 from the power supply 29. The start relay 28 closes the contact 28C-1 to energize the hold relay 31 which locks operated and closes the contact 31C to condition the lock out relay 32 for operation.

When the start button 27 is released, the start relay 28 is deenergized to release the contact 28C-2 to its normally closed position to cause energization of the conditioned lock out relay 32. The lock out relay 32 then opens the contact 32C-1 to prevent energization of the start relay 28 during the test operation as a result of inadvertent pressing of the start button 27. The lock out relay 32 also closes the contact 32C-2 to energize the delay relay 33; the contact 32C-3 to condition the test relay 34 for operation; the contact 32C-4 to condition the read-out cycle control circuit 128 (FIGS. 2B and 11) for operation; the contacts 32C-5 and 32C-6 to apply battery to the various electronic circuits from the power supply 29; and the gate closing contact 32C-7 in the pulse gate 36.

The delay relay 33 opens the contact 33C-1 to remove battery from the memory 37 (FIGS. 2B and 12), to restore the memory to a neutral condition and to cause it to "forget" any previously stored information. The delay relay 33 also closes the contact 33C-2 to energize the counter zero set relay 38, and closes the gate closing contact 33C-3 in the pulse gate 36.

The counter zero set relay 38 closes the contact 38C-1 to cause a voltage pulse to be fed from the power supply 29 to the reset inputs of the counters 52 and 53 (FIGS. 2A and 7) of the stepping circuit 41, and of the counters 62 and 63 (FIGS. 2A and 8A) of the group controller 24, to reset their outputs to a zero state. The zero set relay 38 also closes the contact 38C-2 to cause energization of the conditioned test relay 34, which locks operated. In addition the zero set relay 38 closes the gate closing contact 38C-3 in the pulse gate 36.

The energized test relay 34 opens the contact 34C-1 to deenergize the delay relay 33, and also opens the gate closing contact 34C-2 in the pulse gate 36. The deenergized delay relay 33 then releases the contact 33C-1 to its normally closed position to restore power to the memory 37, releases the contact 33C-2 to deenergize the zero set relay 38, and releases the normally open gate closing contact 33C-3 in the pulse gate 36. When the zero set relay 38 is deenergized it releases the counter reset contact 38C-1 and the test relay energizing contact 38C-2 to their normally open positions. The relay 38 also releases the normally open contact 38C-3 in the pulse gate 36 to open the gate, thereby permitting pulses to flow from the pulse generator 39 through the gate to the stepping circuit 41 (FIGS. 2A and 7).

As the stepping circuit 41 is energized in response to the pulses from the pulse gate 36, it cooperates with the two hundred cross point send matrix 51 to cause signals to be applied sequentially to the two hundred cable connecting terminals 22-I and 22-II (FIGS. 2A and 9), and thus sequentially to the terminals T of the two of the cable terminal groups C1-C30 which are connected to the connecting terminals at any one time. As a signal is applied to each of the cable connecting terminals 22-I and 22-II, it also is applied to the corresponding program connecting terminal 23-I or II, and thus to the program terminal which is connected to the program connecting terminal at that time.

More specifically, as the pulses from the pulse gate 36 feed into the units binary counter 52 of the stepping circuit 41, the counter causes sequential energization of the binary to decimal converters 56-0 through 56-9. The output signal from each of the energized converters 56 is amplified and inverted by its respective send matrix driver 57 and then is applied to respective ones of the cross points 58-00 through 58-199 of the send matrix 51. Similarly, the tens binary counter 53, as it receives pulses from the units binary counter 52, causes sequen-

tial energization of the binary to decimal tens converters 59-0 through 59-19, and the output signal of each of these converters is amplified by its send matrix driver 61 and then applied to respective ones of the cross points 58-00 through 58-199. As the cross points 58-00 through 58-199 receive signals from the drivers 57 and 61, the cross points are energized in sequence so as to apply signals to their respective cable and program connecting terminals 22-I and 22-II, and 23-I and 23-II.

As the tens binary counter 53 completes each counting cycle, that is, as the stepping circuit 41 completes each sweep through the send matrix 51, the counter feeds a pulse to the test group II control counter 63 (FIGS. 2A and 8A) of the group controller 24. These input pulses energize the flip-flops of the control counter 63 to energize their respective group control relays 69-1 through 69-5, whereby these relays close their respective contacts 69C-1 through 69C-5 (FIG. 8B) to energize the relays 71-1 through 71-5 of the relay tree 66 in sequence. As the relays 71-1 through 71-5 are energized they control their associated contacts in the relay tree 66 to complete electrical paths through its output leads 66a-0 through 66a-31 in sequence, thereby sequentially actuating the cable group connecting relays 67-II-1 through 67-II-30 (FIGS. 2A and 8B) and their corresponding program group connecting relays 68-II-1 through 68-II-30, to connect the cable and program terminal groups C1-C30 and P1-P30 to the apparatus as test group II terminals for test purposes.

A portion of each input pulse to the test group II control counter 63 also energizes the count delay generator 72 (FIGS. 2A and 8B) so that the generator feeds a pulse back to the pulse gate 36 (FIGS. 2A and 6) to close it temporarily and thereby permit time for the necessary relay action in the group controller 24 to take place, and for transient conditions as a result of this relay action to die out before the next counting cycle of the stepping circuit 41 begins.

As the test group II control counter 63 completes its counting cycles, portions of its output pulse are applied to the first flip-flop of the test group I control counter 62 to cause sequential energization of the relays 74-1 through 74-5. As the relays 74-1 through 74-5 are energized they control the relay tree 64 (FIG. 2A) to cause the cable and program group connecting relays 67-I and 68-I (FIG. 2A) to be energized to connect the cable terminal groups C1-C30 and their corresponding program terminal groups P1-P30 to the apparatus sequentially as test group I terminals, in the same manner as described above with respect to the test group II control counter 63 for the test group II terminals.

During the initial sweep of the stepping circuit 41 through the send matrix 51, since none of the cable and program terminal groups C1-C30 and P1-P30 have yet been connected to the apparatus by the group controller 24, the error detect circuits 76-I and 76-II (FIGS. 2A and 9) merely test to insure that signals are being fed from the send matrix 51.

After the stepping circuit 41 completes its initial sweep through the send matrix 51, the output pulse from the tens binary counter 53 raises the test group II control counter 63 one count. The stepping circuit 41 then sweeps through the send matrix 51 again, whereupon the counter 63 is raised to its next count to energize the relays 67-II-1 and 68-II-1, thereby causing the cable terminal group C-1 and the program terminal group P-1 to be connected to the apparatus as test group II terminals. This sequence of operation continues until all thirty cable and program terminal groups C1-C30 and P1-P30 have been connected to the apparatus.

After the test group II control counter 63 completes its first counting cycle its output pulse raises the test group I control counter 62 one count, and also feeds to energize the count transfer control circuit 73, which then feeds a

delay pulse down the lead 78 to each of the count transfer gates 77. This delay pulse combines with the output pulse from the energized first flip-flop stage of the test group I control counter 62 to energize the transfer gate 77 to which this stage is connected. The energized gate 77, which can energize any or all of the flip-flop stages in the test group II control counter 63, then energizes this counter's first stage to set the counter at the same binary count as the test group I control counter 62, that is, a count of zero.

Upon again being energized from the send matrix stepping circuit 41, the test group II control counter 63 is stepped immediately to a count of one and the apparatus proceeds through another counting cycle of the counter. Now the output pulse from the counter 63 energizes the test group I control counter 62 so that it causes the cable and program terminal groups C1 and P1 to be connected to the apparatus as test group I terminals, and again energizes the count transfer control circuit 73 so that it cooperates with the count transfer gates 77 to transfer the new count of the counter 62 to the counter 63. Up to this time the apparatus has been testing itself and for shorts within the individual plugs P-00 through P-59.

When the test group II control counter 63 receives its next input pulse from the send matrix stepping circuit 41, the counter is immediately stepped to its count of two to cause the cable program terminal groups C2 and P2 to be connected to the apparatus as test group II terminals. Now, as the stepping circuit 41 sweeps through the send matrix 51, the cable wiring between the cable terminal groups C1 and C2 is checked by the error detect circuits 76-I and 76-II. When the stepping circuit 41 completes this sweep cycle the output pulse from its tens binary counter 53 to the counter 63 causes cable and program terminal groups C3 and P3 to be connected to the apparatus as test group II terminals, and the cable wiring between the cable terminal groups C1 and C3 is checked by the error detect circuits 76-I and 76-II. This procedure continues until all subsequent cable terminal groups C4-C30 have been connected to the apparatus and checked with respect to cable terminal group C1.

The test group I control counter 62 then is energized from the test group II control counter 63 to connect the cable and program terminal groups C2 and P2 to the apparatus as test group I terminals. Cable terminal group C2 then is checked with respect to subsequent cable terminal groups C3-C30, with the cable and program terminal groups C2 and P2 as the test group I terminals. This testing procedure continues until all of the cable terminal groups C1-C30 have been connected to the apparatus by the operation of the test group I control counter 62 and tested as test group I terminals. When the test group I control counter 62 is stepped to its last count of 31, its relays 74-1 through 74-5 energize the relay tree 64 (FIG. 2A), which is not shown in detail in the drawings, to close the operating path of the release relay 42 (FIG. 6) through the lead of the relay tree which corresponds to the lead 66a-31 (FIG. 8B) of the relay tree 66, to energize the relay 42. The energized relay 42 then drops out the hold relay 31, and thus the lock out relay 32 and the test relay 34, to deenergize the apparatus.

Reference now is made to FIG. 9, in which the compare circuit 76-I illustrates the function of one of the compare circuits 76-I and 76-II when associated with cable and program input terminals T_{ci} and T_{pi} , and in which the compare circuit 76-II illustrates the function of one of the compare circuits when associated with cable and program output terminals T_{co} and T_{po} .

The output signal of one of the AND gates 58 of the send matrix 51, such as the gate 58-10, as shown in FIG. 9, feeds to the point 87-I where the signal splits, with a portion of the signal feeding through the steering diode 88-1 to the point 89-I where it again splits, with a portion then feeding to the cross point's associated cable connecting terminal 22-I by means of the lead 79-I. The

other portion of the output signal feeds through the second steering diode 88-2 to the point 91-I where it again splits, with a portion then feeding to the program connecting terminal 23-I by means of the lead 81-I.

From the program connecting terminal 23-I, the signal portion feeds to the program input terminal T_{pi} through the program wire P_w to the program output terminal T_{po} , to the program connecting terminal 23-II, and then to the compare circuit 76-II along the lead 81-II to the point 91-II. Similarly, the signal portion at the cable input connecting terminal 22-I feeds to the cable input terminal T_{ci} through the cable wire C_w to the cable output terminal T_{co} , to the cable connecting terminal 22-II and then to the compare circuit 76-II along the lead 79-II to the point 89-II.

In the operation of the compare circuit 76-I to verify that signals were received from the send matrix 51 at the points 89-I and 91-I, portions of the signals feed into the compare circuit from the point 89-I through the steering diodes 88-3 and 88-4, and from the point 91-I through the steering diodes 88-5 and 88-6. If the compare circuit 76-I receives a signal from both of the points 89-I and 91-I, neither of the output amplifiers 94 or 96 of the compare circuit is energized and no signal appears on either of their output leads 97 and 98. However, if the compare circuit 76-I receives a signal from only one of the points 89-I and 91-I, a signal will appear on either the output lead 97 or 98.

Similarly, in the operation of the compare circuit 76-II in FIG. 9, the signals fed to the points 89-II and 91-II pass through the diodes 88-3, 88-4, 88-5 and 88-6 into the compare circuit 76-II, whereby neither of its output amplifiers 94 or 96 is energized. At the same time, if the cable input terminal T_{ci} is not shorted to, or open with respect to another terminal T of the cable C, none of the other compare circuits 76-I and 76-II of the apparatus will be energized and the stepping circuit 41 (FIG. 7) steps to the next send matrix cross point 58-11.

If the cable input terminal T_{ci} is improperly connected to the cable output terminal T_{co} by the wire C_w , or is shorted to the cable output terminal rather than properly wired thereto, the program wire P_w , instead of being connected to the cable output terminal T_{po} as shown in FIG. 9, would be connected to a different program terminal. An output signal from the cable output terminal T_{co} then is received at the point 89-II when it should not be receiving a signal, but no signal is received at the program point 91-II, and thus the output amplifier 94 of the compare circuit 76-II is energized to indicate a short.

Similarly, if the cable wire C_w is broken, or instead of being properly connected to the cable output terminal T_{co} as shown in FIG. 9, is improperly connected to a different terminal T of the cable C, an output signal from the program output terminal T_{po} is received at the program point 91-II, but no signal is received at the cable point 89-II, and the output amplifier 96 of the compare circuit 76-II is energized to indicate an open.

From FIG. 9, it is seen that as the stepping circuit 41 (FIG. 7) proceeds through the send matrix 51 beyond the cross point 58-10 and subsequently applies a signal to the cross point 58-190, the signal will feed to the point 87-II and portions of the signal then will flow into the compare circuit 76-II, and in reverse directions through the cable and program wires C_w and P_w to the compare circuit 76-I, whereby the functions of the two compare circuits are reversed from that as above described. Thus, each wire C_w of the cable C is tested twice by the apparatus as it proceeds through its normal cycle of operation.

Referring to FIGS. 2A and 2B, it is seen that when one of the compare circuits 76-I or 76-II detects a malfunction in the apparatus or a fault (short or open) in the cable C, the compare circuit feeds a pulse to the units and tens digit grouping circuit 99 (FIG. 2B), which pulse then passes through the units and tens digit information collecting circuit 112 to energize the error detect gate cir-

cuit 47. The output of the error detect gate circuit 47 then feeds to the pulse gate 36 (FIG. 2A) and the delay circuit 108.

More specifically, referring to FIG. 9, it is seen that the output pulse of the energized one of the compare circuit amplifiers 94 or 96 feeds to the respective one of the grouping gates 101W, X, Y and Z through 104W, X, Y and Z of the digit grouping circuit 99, then to the set of the collecting gates 113, 114, 123 or 124 (FIG. 10) to which the grouping gate is connected, and then by one of the leads such as the lead 119 to one of the error detect gates 47a, b, c or d. The output of the energized error detect gate 47a, b, c or d then feeds by means of the lead 107 to close the pulse gate 36 (FIGS. 2A and 6) by temporarily inhibiting the flow of pulses from the pulse generator 39 through the pulse gate, and to energize the delay circuit 108.

After a predetermined time delay, which permits transient conditions to die out, whereby the compare circuits 76-I and 76-II can verify that an error in the cable C or a malfunction in the apparatus is actually present, the relay 109 of the delay circuit 108 becomes energized and closes its contact 109C to energize the relay 111. The energized relay 111 closes its contact 111C-1 in the pulse gate 36 to lock the gate closed, its contact 111C-2 (FIGS. 6 and 11A) to energize the read-out cycle control circuit 128 (FIGS. 2B and 11), and the contacts 111C-3 (FIG. 10) to connect the information transfer circuits 117 (FIGS. 2B and 10) to the memory information steering contacts 37S (FIGS. 2B, 10 and 12). In this regard however, if the initial pulse inhibiting was due to transient conditions, rather than an actual error, the relay 109 does not become energized and when the transient conditions have dissipated the pulses will again begin to flow from the pulse generator 39 through the pulse gate 36 to the stepping circuit 41.

Referring to FIG. 11A, the closing of the contact 111C-2, providing the relay check circuit shown adjacent the top of this figure is satisfied, energizes the relay 142. The relay 142 then closes its contact 142C to energize the relay 143, which locks operated, opens the contact 143C-1 to drop out the relay 142, and closes the contact 143C-2 to energize the pulsing relay 131 for the binary counter 129 of the read-out control circuit 128. The energized relay 131 closes its contact 131C-1 to energize the counter 129, opens its contact 131C-2 to drop out the relay 143, and opens its contact 131C-3 to maintain the relay 142 temporarily inoperative. The deenergized relay 143 then releases its contact 143C-2 to deenergize the relay 131, which then releases its contact 131C-3 to re-energize the relay 142, whereupon the cycle repeats.

The pulsing of the relay 131 and the resultant opening and closing of its contact 131C-1 in the first stage of the counter 129 causes energization of the relays 132-1 through 132-4 and the relays 133-1 through 133-4 of the counter, as indicated by the operating time chart in FIG. 11C. As the relays 132-1 through 132-4 are energized they control their respective contacts 132-1C-1 through 132-4C-1 in the relay tree 134 (FIG. 11B), and in cooperation with the relay 133-1 (which controls the contacts 133-1C-1 in the relay tree) cause sequential energization of the relay tree relays 136TUO through 136PTT. Referring to FIG. 11E, the relays 132-1 through 132-4 also close their respective contacts 132-1C-2 through 132-4C-2 to cause energization of the relays 144-1 through 144-4. As the relays 144-1 through 144-4 are energized they control their respective contacts in the relay tree 146 to cause sequential energization of the relay tree relays 147TUO through 147PTT, whereby error information is transferred into the memory 37 (FIGS. 2B and 12), and the read out 21 (FIGS. 2B, 5 and 12) is energized to indicate the digits of the terminals T and of the plugs P-00 through P-59 which are involved in the error.

In determining whether the error is an open wire, and

if so, the units digit of the terminal T which is open, the relay 136TUO (FIG. 11B) is energized and closes the ten contacts 136TUOC (FIG. 10) in the output leads 121 of the digit information collecting circuit 112 to connect the ten sets of gates 114W, X, Y and Z to the first inputs of respective ones of the ten information transfer circuits 117. At the same time the relay 147TUO (FIG. 11E) closes its ten contacts 147TUOC (FIGS. 10 and 12) of the memory information steering 37S to connect the information transfer circuits 117 to respective ones of the ten relays 37TUOR in the memory 37. Thus an input pulse to one of the ten sets of gates 114W, X, Y and Z from the digit grouping circuit 99 energizes the relay 117R (FIG. 10) of the information transfer circuit 117 for the digit involved to connect the respective one of the ten relays 37TUOR to ground, whereby the relay operates to energize the read-out lamp 21TUO to indicate the digit.

The determination and transfer of the tens digit of an open terminal T, and of the units and tens digits of a shorted terminal, is similar to the operation set forth above with regard to the determination and transfer of the units digit for an open terminal, utilizing the relays 136TTO, TUS and TTS, the relays 147TTO, TUS and TTS, the memory branches 37TTO, TUS and TTS, and the read-out lamps 21TTO, TUS and TTS.

In determining the units digit of the terminal T under test when an apparatus malfunction or a cable error is found, the relay 136TUT closes its ten contacts 136TUTC (FIGS. 7 and 10) to connect the send matrix units digit drivers 57 to the second inputs of respective ones of the information transfer circuits 117. At the same time the relay 147TUT closes its ten contacts 147TUTC (one shown in FIG. 10) of the memory information steering 37S to connect the information transfer circuits 117 to their respective memory relays 37TUTR (not shown). Thus, with the apparatus locked upon the error, the units driver 57 which is then energized feeds a signal through its information transfer circuit 117 to energize the relay 117R of the circuit, thereby causing the memory relay 37TUTR for the digit involved to operate the read-out lamp 21TUT.

In determining the tens digit of the terminal T under test when an error is found, the apparatus operates in a manner similar to that described above for determining the units digit. Thus, the relay 136TTT operates its five contacts 136TTTC (one shown in FIG. 10) so that the terminal tens test information collecting points 117P (and thus the send matrix tens drivers 61 in FIG. 7) are connected to the information transfer circuits 117-0 through 117-4. Further, the relay 147TTT closes its five contacts 147TTTC (not shown) in the memory steering 37S, to cause the memory branch relay 37TTTR (not shown) for the digit involved to energize the read-out lamp 21TTT.

With respect to the determining of plug number information, referring to FIGS. 8B and 14A, it is seen that with the apparatus locked upon the error which has been found by the error detect circuits 76-I and 76-II, one of the points 158-II-1 through 158-II-30 (FIG. 14A) of the relay circuit 126-II is connected to ground through the set of operative output leads 66a and 66b of the relay tree 66 (FIG. 8B) in the group controller 24. Similarly, one of the points 158-I-1 through 158-I-30 of the relay circuit 126-I is connected to ground through the operative set of output leads 64a and 64b of the group controller relay tree 64 (FIG. 2A).

In determining the units digit of the one of the plugs P-00 through P-59 which is under test, the relay 136UP (lower portion of FIG. 14B), which is energized upon the closing of the contact 136PUTC' by the relay 136PUT (FIG. 11B), closes its ten contacts 136UPC-0 through 9 to connect the plug number translator 126 to the second inputs of the information transfer circuits 117 (FIGS. 2B and 10); the relay 147PUT (FIG. 11E) closes its ten contacts 147PUTC (one shown in FIG. 10) in the mem-

ory steering 37S to connect the information transfer circuits 117 to the relays 37PUTR (not shown) in the memory 37; the relay 136PUT also closes its four contacts 136PUTC-W, X, Y and Z in the plug number pretranslator 137 (FIG. 13) to connect the sets of gates 152W, X, Y and Z of the test plug quadrant detector 151 to the relays 153W, X, Y and Z, respectively, whereby one of these relays is energized by a pulse from the operative tens matrix driver 61 (FIGS. 2A and 7); and the relay 136UP also closes the four contacts 136UPC' (left-hand side of FIG. 14A) in the leads 162, 163, 164 and 166, whereby one of the contacts 153WC, XC, YC or ZC is closed by the energized relay 153W, X, Y or Z to energize either one of the two relays 159-I which is connected to the grounded point 158-I, or one of the two relays 159-II which is connected to the grounded point 158-II. The energized relay 159-I or 159-II, as the case may be, then closes its associated one of the contacts 159-IC-0 through 9 or 159-IIC-0 through 9, thereby connecting the respective information transfer circuit 117 to ground to cause operation of its associated memory relay 37PUTR (not shown) and energization of the read-out lamp 21PUT (FIG. 5) to indicate the digit involved.

For example, if plug P-24 of cable terminal group C-13 is connected to the apparatus in test group II, and in the plug under test, the relay 153Y (FIG. 13) closes the contact 153YC (FIG. 14A) to energize the relay 159-II-4, which then closes its contact 159-IIC-4 to connect the information transfer circuit 117-4 to ground. If the plug P-24 were connected to the apparatus as test group I, contact 153WC would be closed by the relay 153W to energize the relay 159-I-4 (not shown), which would then close its contact 159-IC-4 to connect the information transfer circuit 117-4 to ground.

The operation of the plug number translator 126 in determining the units digit for one of the plugs P-00 through P-59 which is shorted or open, is substantially the same as described above for the determination of the units digit of a plug under test, utilizing the relays 136PUS (FIG. 11B), 136PUO, 147PUS (FIG. 11E) and 147PUO and the circuitry associated with these relays.

In the operation of the plug number translator 126 to determine the tens digit of one of the plugs P-00 through P-59, such as the plug under test, the relay 146TP (lower portion of FIG. 14C), is energized by the relay 136PTT (FIG. 11B) to close the six contacts 136TPC; the relay 147PTT (FIG. 11E) closes its six contacts 147PTTC (one shown in FIG. 10) in the memory steering 37S; the relay 136PTT also closes its contacts 136PTTC-W, X, Y and Z in the plug number pretranslator 137 (FIG. 13); and the relay 136TP also closes the four contacts 136TPC' (left-hand side of FIG. 14A), whereby one of the contacts 153WC, XC, YC or ZC is closed by its associated relay 153W, X, Y or Z of the pretranslator to energize either one of the relays 167-I which is connected to the grounded point 158-I, or one of the relays 167-II which is connected to the grounded point 158-II. The energized relay 167-I or 167-II, as the case may be, then closes its associated one of the contacts 167-IC-0 through 5 or 167-IIC-0 through 5, thereby connecting the respective information transfer circuit 117 to ground to cause operation of its associated memory relay 37PTTR (not shown) and of the read-out lamp 21PTT to indicate the digit involved.

In determining the tens digit information for one of the plugs P-00 through P-59 which is shorted or open, the translator 126 operates in substantially the same manner as above described for determining the tens digit of the plug under test, utilizing the relays 136TS (FIG. 11B), 136PTO, 147PTS (FIG. 11E) and 147PTO and the circuitry associated with these relays.

Referring to the lower portion of FIG. 11B and to FIGS. 11C and 11D, it is seen that when the counter 129 reaches its thirteenth count the energized states of the relays 132-I through 132-4 (FIG. 11A) and of the re-

lays 133-1 through 133-4 are such that the release relay 42 (FIG. 6) is connected to ground through certain of the contacts of the relay tree 134. This energizes the release relay 42 to drop out the hold relay 31 in the start control circuit 26, and thus the lock out relay 32 and the test relay 34, to deenergize the apparatus.

The detected error in the cable C, or malfunction in the apparatus, as indicated by the read out 21, then is corrected, whereupon the cable C is tested again by closing and releasing of the start button 27 in the start control circuit 26.

The operating time for the apparatus, whether no error is detected in the cable C, or an error is detected and then indicated by the read-out lamps 21, is less than one minute, as compared to prior known apparatus in which the testing of a cable of the size and complexity of the cable C would require several hours.

It is apparent that for the testing of circuits or cables having terminals which are numbered in a manner other than 00 through 49, as are the terminals T in the illustrated embodiment of the invention, the numbers of the terminals involved in an error readily can be determined by referring to a suitable conversion table which lists the numbers as they will appear in the read out 21 and the corresponding numbers of the terminals being tested.

In the alternative, certain wiring changes can be made in the apparatus as necessary so that the terminal numbers involved in an error are indicated in the read out 21 directly. For example, in certain PBX cables the terminals of the plugs are numbered 01 through 50, instead of 00 through 49. In this instance the above-mentioned extra digit counts of the tens binary counter 53 (FIG. 7) can be utilized for testing of the terminals which are numbered 50. Thus, since there is no terminal numbered 00, a send matrix driver 61 for one of the extra digit counts may be provided and wired to the AND gate at the cross points 58-00 of the send matrix 51. The cross point 58-00 then is arbitrarily assigned the number 50 and is wired to feed signals to the terminals numbered 50 of the cable plugs which are connected to the apparatus in test plug quadrant W. Then, by suitably wiring this cross point's compare circuit 76-I to the digit grouping circuit 99 (FIGS. 2B and 9), wiring the send matrix driver 61 to the test plug quadrant detector 131 (FIGS. 2B and 13), and the information transfer circuitry 117 (FIGS. 2B and 10), and providing additional components and wiring of the apparatus as necessary, as will be apparent to those skilled in the art, when the terminal 50 of the quadrant W is involved in an error, the apparatus will indicate this fact directly in the read out 21. Similarly, three additional send matrix drivers 61 may be provided and wired to the AND gates of the send matrix cross points 58-50, 58-100 and 58-150 for testing the terminals numbered 50 of the cable plugs which are connected to the apparatus in the test plug quadrants X, Y and Z, respectively.

While in the illustrated embodiment of the invention the contacts 111C-3 (FIG. 10) for connecting the information transfer circuit 117 to the memory steering 37S are shown as remaining closed during the read-out cycle, the contacts may be controlled so as to be opened and closed between each step in the read-out cycle, if so desired, to help preclude transient conditions in the apparatus, as the result of relay action during the read-out cycle, from causing an extraneous pulse to be fed into the memory 37, thereby causing a false indication of an error in the read-out 21. For example, the contacts 111C-3 may be closed by a relay which is energized by the delay relay 142 (FIG. 11A) of the read-out cycle control circuit 128, with the added relay energizing the relay 143 and then subsequently being deenergized by operation of the relay 143, during each step of the read-out cycle.

What is claimed is:

1. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, which comprises:

first control means for sequentially connecting each of the groups of terminals to the apparatus as a first test group;

second control means which is operative when each of the groups of terminals is connected to the apparatus as the first test group, for sequentially connecting at least the groups of terminals having subsequent designations in the series to the apparatus as a second test group, to test each of the groups of terminals with respect to each of the other groups of terminals, each of said first and second control means also being operative to disconnect its respective group of terminals which is connected to the apparatus at any one time, from the apparatus, upon its being operative to connect a next succeeding group of terminals to the apparatus;

means for sequentially applying a separate signal to each of the terminals in the groups of terminals which are connected to the apparatus as the first and second test groups at any one time, so that the signal feeds into the electrical circuit; and

error detecting means for monitoring each of the other terminals of the groups of terminals which are connected to the apparatus as the first and second test groups at any one time, to detect an error in the electrical circuit.

2. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 1, wherein the terminals are numbered and which further comprises:

means responsive to said error detecting means for determining the nature of the error and digit information for each terminal involved in the error; a read-out display for indicating the nature of the error and the number of each terminal involved in the error;

ten digit information transfer circuits, one for each of the digits 0 through 9, by which digit information relative to the terminals involved in an error is transferred from said terminal digit information determining means into said read-out display; and

cycle control means for causing the digits of the digit information to be transferred sequentially from said terminal digit information determining means over said transfer circuits into said read-out display one digit at a time.

3. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 1, which further comprises:

means responsive to said error detecting means for determining the input terminal involved in the error; means responsive to said error detecting means for determining whether the error is caused by the input terminal being shorted to another terminal, and for determining the terminal to which the input terminal is shorted; and

means responsive to said error detecting means for determining whether the error is caused by the input terminal being open with respect to another terminal, and for determining the terminal with respect to which the input terminal is open.

4. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have

been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 1, in which:

each of said first and second control means includes a counter which controls the sequential connection of the groups of terminals to the apparatus, said counter of said second control means being connected to energize said counter of said first control means as said second counter completes each counting cycle, so that said first counter is advanced one count for each counting cycle of said second counter.

5. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 4, which further comprises:

circuit means for setting said second counter at the same count as said first counter after said first counter has been advanced each count, so that said second counter begins each counting cycle subsequent to its initial counting cycle at a count one unit above its starting count on its preceding cycle.

6. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 5, in which said circuit means includes:

a plurality of AND gates each having a first input connected to receive a signal from an output of a respective stage of said first counter and having an output connected to feed a signal into a corresponding stage of said second counter; and

a delay circuit energized by said second counter as said second counter completes each counting cycle, said delay circuit being connected to feed a delayed signal to second inputs of said AND gates so that the delayed signal and the signals from the outputs of the stages of said first counter cooperate with said AND gates to set said second counter at the same count as said first counter after said first counter has been advanced each count.

7. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 4, which further comprises:

first relays and second relays connected to be energized by respective stages of said first and second counters; separate relay means for connecting the groups of electrical terminals to the electrical circuit as first and second test groups;

a first relay tree controlled by said first relays as said first relays are energized by their respective stages of said first counter, said first relay tree energizing respective ones of said connecting relay means in sequence to connect the groups of electrical terminals to the electrical circuit in sequence as first test groups, and each of said energized connecting relay means being released by said first relay tree upon the energization of a next succeeding connecting relay means by said first relay tree; and

a second relay tree controlled by said second relays as said second relays are energized by their respective stages of said second counter, said second relay tree also energizing respective ones of said connecting relay means in sequence to connect groups of electrical terminals to the electrical circuit in sequence as second test groups, and each of said energized connecting relay means also being released by said second relay tree upon the energization of a next succeeding connecting relay means by said second relay tree, whereby a maximum of two groups of electrical

terminals are connected to the electrical circuit at a time.

8. Apparatus for testing an electrical circuit having groups of terminals wherein the groups of terminals have been assigned successive designations to form a series and the terminals of the groups are interconnected by electrical conductors, as recited in claim 1, wherein the terminals are numbered and are mounted on numbered connector plugs, and which further comprises:

means responsive to said error detecting means for determining the nature of the error and digit information for each terminal involved in the error;

means responsive to said error detecting means for determining digit information for each connector plug involved in the error;

a read-out display for indicating the nature of the error, the number of each terminal involved in the error, and the number of each connector plug involved in the error; and

means for transferring the terminal and connector plug digit information from said terminal and connector plug digit information determining means to said read-out display.

9. Apparatus for testing an electrical circuit having a plurality of terminals which are interconnected by electrical conductors, which comprises:

first control means for sequentially connecting groups of the terminals and corresponding groups of terminals of a reference circuit to the apparatus as first electrical circuit and reference circuit test groups, respectively;

second control means which is operative when each of the electrical circuit terminal groups and the corresponding reference circuit terminal group are connected to the apparatus as the first test groups, for sequentially connecting selected ones of the other electrical circuit and reference circuit terminal groups to the apparatus as second electrical circuit and reference circuit test groups, respectively, each of said first and second control means also being operative to disconnect its respective electrical and reference circuit terminal groups which are connected to the apparatus at any one time, from the apparatus, upon its being operative to connect a next succeeding electrical circuit terminal group and the corresponding reference circuit terminal group to the apparatus;

means for sequentially applying a signal to each of the terminals in the electrical circuit terminal groups which are connected to the apparatus as the first and second electrical circuit test groups at any one time, and at the same time applying a signal to the corresponding reference circuit terminal, so that the signals feed into the electrical circuit and the reference circuit, respectively; and

means for detecting an error in the electrical circuit by comparing the signal output at each of the other terminals of the electrical circuit terminal groups which are connected to the apparatus as the first and second electrical circuit test groups at any one time, with the signal output at the corresponding reference circuit terminal, said error detecting means being responsive to a disparity in the signal outputs at one of the electrical circuit terminals and its corresponding reference circuit terminal as a result of the error.

10. Apparatus for testing an electrical circuit having sets of terminals which are interconnected by electrical conductors, which comprises:

first control means for sequentially connecting groups of the terminals and corresponding groups of terminals of a reference circuit to the apparatus as first electrical circuit and reference circuit test groups, respectively;

second control means which is operative when each of the electrical circuit terminal groups and the corresponding reference circuit terminal group are con-

connected to the apparatus as the first test groups, for sequentially connecting selected ones of the other electrical circuit and reference circuit terminal groups to the apparatus as second electrical circuit and reference circuit test groups, respectively, each of said first and second control means also being operative to disconnect its respective electrical and reference circuit terminal groups which are connected to the apparatus at any one time, from the apparatus, upon its being operative to connect a next succeeding electrical circuit terminal group and the corresponding reference circuit terminal group to the apparatus, and said second control means being connected to energize said first control means after the selected other electrical circuit and reference circuit terminal groups have been connected to the apparatus as the second test groups, so that said first control means connects the next succeeding electrical circuit and reference circuit terminal groups to the apparatus as the first test groups;

means for sequentially applying a signal to each of the terminals in the electrical circuit terminal groups which are connected to the apparatus as the first and second electrical circuit test groups at any one time, and at the same time applying a signal to the corresponding reference circuit terminal, so that the signals feed into the electrical circuit and the reference circuit, respectively;

means for detecting an error in the electrical circuit by comparing the signal output at each of the other terminals of the electrical circuit terminal groups which are connected to the apparatus as the electrical circuit test groups at any one time, with the signal output at the corresponding reference circuit terminal, said error detecting means being energized in response to a disparity in the signal outputs at one of the electrical circuit terminals and its corresponding reference circuit terminal as a result of the error, to produce an output signal;

means responsive to the output signal of said error detecting means for rendering said signal applying means inoperative;

means responsive to the output signal of said error detecting means for determining the electrical circuit input terminal involved in the error, including the set of terminals in which the input terminal is located;

means responsive to the output signal of said error detecting means for determining whether the error is caused by the input terminal being shorted to another electrical circuit terminal, and for determining the terminal to which the input terminal is shorted, including the set of terminals in which the terminal is located; and

means responsive to the output signal of said error detecting means for determining whether the error is caused by the input terminal being open with respect to another electrical circuit terminal, and for determining the terminal to which the input should be connected, including the set of terminals in which the terminal is located, the energization of both said shorted terminal determining means and said open terminal determining means being an indication of a cross connection in the electrical circuit.

11. Apparatus for testing an electrical circuit having numbered sets of terminals wherein each set of terminals includes a plurality of numbered terminals and the terminals are interconnected by electrical conductors, which comprises:

control means for sequentially connecting the sets of terminals to the apparatus such that at least two sets of terminals are connected to the apparatus at a time for testing and such that each set of terminals is connected to the apparatus with each of the other sets

of terminals for testing, said control means also being operative to disconnect a set of terminals which is connected to the apparatus at any one time, from the apparatus, upon its being operative to connect another set of terminals, to the apparatus;

means for sequentially applying a separate signal to each of the terminals of the electrical circuit which are connected to the apparatus at any one time, so that the signal feeds into the electrical circuit;

error detecting means for monitoring the other terminals of the electrical circuit which are connected to the electrical circuit at any one time, to detect an error in the electrical circuit;

means responsive to said error detecting means when an error is detected, for interrupting the test operation and rendering said signal applying means inoperative;

means responsive to said error detecting means for determining the nature of an error and digit information for each terminal involved in the error;

means responsive to said error detecting means for determining, from among the sets of terminals then connected to the apparatus, digit information for each set of terminals involved in the error;

a read-out display for indicating the nature of the error, the number of each terminal involved in the error and the number of each set of terminals involved in the error; and

means for transferring the terminal and terminal set digit information from said terminal and terminal set digit information determining means to said read-out display.

12. Apparatus for testing an electrical circuit having numbered sets of terminals wherein each set of terminals includes a plurality of numbered terminals and the terminals are interconnected by electrical conductors, as recited in claim 11, in which said digit information transferring means includes:

ten digit information transfer circuits, one for each of the digits 0 through 9, by which digit information relative to the terminals and the sets of terminals involved in an error is transferred from said digit information determining means into said read-out display; and

cycle control means for causing the digits of the digit information to be transferred sequentially from said digit information determining means over said transfer circuits into said read-out display one digit at a time.

13. Apparatus for testing an electrical circuit having numbered sets of terminals wherein each set of terminals includes a plurality of numbered terminals and the terminals are interconnected by electrical conductors, as recited in claim 11, which further comprises:

means responsive to said error detecting means for determining digit information relative to the input terminal involved in the error and relative to the set of terminals in which the input terminal is located;

means responsive to said error detecting means for determining whether an error is caused by the input terminal being shorted to another terminal, and for determining digit information relative to the terminal to which the input terminal is shorted and relative to the set of terminals in which the shorted terminal is located; and

means responsive to said error detecting means for determining whether an error is caused by the input terminal being open with respect to another terminal, and for determining digit information relative to the terminal with respect to which the input terminal is open and relative to the set of terminals in which the open terminal is located.

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U.S. Cl. X.R.

UNITED STATES PATENT OFFICE CERTIFICATE OF CORRECTION

Patent No. 3,492,571

Dated January 27, 1970

Inventor(s) D. A. DESLER

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 62, "12" should read --13--. Column 4, line 30, "indicated" should read --indication--. Column 6, line 49, "amplifiier" should read --amplifier--. Column 7, line 12, "flop" should read --flops--; line 25, "if" should read --of--; line 30 "fiip" should read --flip--. Column 8, line 35, "Z6" should read --66--. Column 9, line 13, "series" should read --circuits--. Column 11, line 20, "AN" should read --AND--; line 21, "50-10" should read --58-10--. Column 14, line 23, "1179-9" should read --117-9--. Column 15, line 54, "hte" (second occurrence) should read --the--. Column 16, line 2, "TOC" should read --TTOC--. Column 18, line 48, "136TTC-W" should read --136PTTC-W--. Column 28, line 26, "in" should read --is--; line 44, "146TP" should read --136TP--; line 69, "136TS" should read --136PTS--. Column 29, line 25, "coresponding" should read --corresponding--. Claim 10, column 33, line 59, after "input" insert --terminal--.

SIGNED AND
SEALED
OCT 6 - 1970

(SEAL)

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