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(54) TELEPHONE EXCHANGE APPARATUS

(71) We, FUJITSU LIMITED, a Japanese Corporation, of No. 1015, Kamikodanaka, Nakahara-ku, Kawasaki, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to telephone exchange apparatus, for use in a telephone exchange connected to a plurality of telephone lines.

Information relating to the operative state of a telephone exchange is transferred to an attendant, or operator, console which provides indication of that information, and hence of the operative state of the exchange, for example by means of lamps, and when a key operation is effected in the attendant, or operator, console, key information is transferred to the telephone exchange to cause appropriate operations to be carried out in the exchange. It is desirable to strictly limit such information to that which is necessary and sufficient, in order to obtain an economical construction for the exchange. With improvements in performance of exchange control equipment services offered by exchanges are becoming more diversified. Further, since exchange services are not fixed but differ in dependence upon user's requirements, it is desirable from the operator's point of view that the attendant, or operator, console be easy to operate. With the diversification of the exchange services, the amount of information to be transferred to the console increases and the content of transferred information will differ in accordance with particular user requirements. It has been found that previously proposed systems are generally limited in flexibility, economic viability, operation and maintenance.

Figure 1 of the accompanying drawings is a block diagram explanatory of a previously proposed attendant console control system, in which subscribers' telephones 1*a* to 1*n* are connected to a network 3 through line circuits 2*a* to 2*n*, and connected to a distant office through a trunk 4. Attendant consoles 5*a* and 5*b* have connected to display portions thereof C-lines of the line circuits 2*a* to 2*n*. Key information generated by key operation of the attendant consoles 5*a* and 5*b* is transferred to common control equipment 8 through position controllers 7*a* and 7*b*, respectively, and signals giving information relating to the operative state of the exchange (lamp/display signals) are transferred from the common control equipment 8 to the attendant consoles 5*a* and 5*b* through the position controllers 7*a* and 7*b*, respectively. The attendant consoles 5*a* and 5*b* are connected to the network 3 by respective position trunks 6*a* and 6*b* (operator speech circuits) as shown.

Signals giving information relating to the status of subscriber lines (line status signals) are sent to the attendant consoles and the information is displayed in the attendant consoles 5*a* and 5*b*, in dependence upon whether the C-lines of the line circuits 2*a* to 2*n* are grounded or not. With an increase in the number of C-lines connected to the display portion of an attendant console wiring can become complicated and the construction of the system can become very uneconomical. Further, in a case where it is necessary to change a subscriber's telephone number, wiring modification, for example, is required, so that the previously proposed system can be lacking in flexibility.

The position controllers 7*a* and 7*b* control and monitor the operations of the attendant consoles and act as interfaces between those consoles and the common control equipment.

According to the present invention there is provided telephone exchange apparatus, for use in a telephone exchange connected to a plurality of telephone lines, the apparatus comprising an attendant console, having a plurality of signalling keys, for use by an

attendant at the console to provide control and data signals, line status display means for indicating to the attendant the operational statuses of a predetermined number of such telephone lines, and exchange status display means for indicating to the attendant the operational status of the telephone exchange, a position controller, for controlling and monitoring operations of the attendant console, a busy lamp field controller, for providing line status signals indicative of the operational statuses of such telephone lines, and exchange control circuitry in dependence upon which the busy lamp field controller is operable to provide such line status signals and to pass such line status signals to the attendant console to provide such an indication in the line status display means, and which is operable to provide exchange status signals and to pass on such exchange status signals to the attendant console to provide an indication in the exchange status display means, and which is further operable, in response to such control and data signals passed from the attendant console to the position controller, to control operations in the exchange, wherein the said control and data signals are passed from the attendant console to the position controller in a bit serial manner, and wherein such line status signals from the busy lamp field controller and such exchange status signals from the position controller are passed to the attendant console in a bit serial and time sharing manner along a common signal path.

In an embodiment of the present invention line status information transferred from a telephone exchange to the operator attendant console in time-sharing manner is used to provide indications of statuses of individual lines.

Further, an embodiment of the present invention can be constructed in which key information from the attendant console is transferred to an exchange in time-sharing manner.

Further in an attendant console embodying the present invention testing of the display of the console can be provided for in a simple manner.

Briefly stated, an embodiment of the present invention can be constructed in which key information generated by a key operation of the attendant console can be transferred to common control equipment of the exchange (c.f. the above description of the previously-proposed console control system) in a bit serial manner (i.e. as a sequence of bits), and there being provided a memory holding subscribers' telephone numbers and the line status information corresponding to each of the telephone numbers. When the key information is line status display requesting information, information contained in the key information indicating a line of interest, corresponding to the telephone number in respect of which line status display is requested, is employed to cause read out of line status information relating to a plurality of telephone lines, including the line of interest, and the read out line status information is arranged in the numerical order of lower order digits of the telephone numbers corresponding to the plurality of lines and the information thus arranged is transferred to the attendant console in bit serial manner.

For a better understanding of the present invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which:-

Figure 1 as mentioned above, is a block diagram explanatory of a previously-proposed attendant console control system;

Figure 2 is a block diagram explanatory of an embodiment of the present invention;

Figure 3 is a block diagram showing in more detail the arrangement of parts of the embodiment of Figure 2;

Figure 4 is a block diagram illustrating in more detail another part of the embodiment of Figure 2;

Figure 5 is a time chart;

Figure 6 is a block diagram showing in still more detail parts of an item illustrated in Figure 3;

Figure 7 is a block diagram illustrating in more detail parts of another item illustrated in Figure 3;

Figures 8A and *8B* are time charts;

Figure 9 is a block diagram showing in more detail parts of an item illustrated in Figure 3;

Figure 10 is a block diagram explanatory of operational procedures available in an embodiment of the present invention; and

Figure 11 is a block diagram explanatory of further operational procedures available in an embodiment of this invention.

Figure 2 shows in block form exchange equipment employing apparatus embodying the present invention. In Figure 2 subscriber telephones 11*a* to 11*n* are connected to a network 13 through respective line circuits 12*a* to 12*n*, and are connected to distant offices through a trunk 14. Attendant, or operator, consoles 15*a* and 15*b* are connected to the network 13 through position trunks (operator speech circuits) 16*a* and 16*b* respectively, and, further, the attendant consoles 15*a* and 15*b* are each connected to a position controller 17 through a

status display signal line 20*a*, a clock signal line 20*b* and key signal line 20*c*. The status display signal lines carries line status signals and lamp/display signals (collectively called "status display" signals). The position controller 17 is connected to common control equipment 18 and a busy lamp field controller 19. The position controller controls and monitors operations at the different operator positions, that is operator, or attendant, consoles, and acts as an interface between the consoles and the common control equipment 18 and the busy lamp field controller 19. No C-line is connected to the attendant consoles 15*a* and 15*b* from the line circuits 12*a* to 12*n*, and key information and line status information are transferred in a bit serial manner, so that the attendant consoles 15*a* and 15*b* and the position controller 17 are interconnected simply through the status display signal lines 20*a*, the clock signal lines 20*b* and the key signal lines 20*c*. This can markedly simplify the wiring in the apparatus as compared with that present in previously proposed attendant console control systems. The present embodiment is illustrated in connection with a case in which four attendant consoles are provided for (only two being shown in the Figures).

Figure 3 is a block diagram showing the arrangement and connection of an attendant console and the position controller (17 of Figure 2) which controls the console (the operator position provided by that console). An attendant console 100 comprises a direct station selection key signal transmit portion 101, a general-purpose key signal transmit portion 102, a busy lamp field portion 103, a lamp/display signal receiver and indicative portion 104, an OR gate 105, a line driver 106 and line receivers 107 and 108. The position controller 200 comprises a key signal receiver portion 201, a clock distribute portion 202, a lamp/display signal transmit portion 203, line receivers 204, line drivers 205 and 206 and OR gates 207.

Clock signals from the clock distribute portion 202 are supplied to each attendant, or operator, console and key signals indicative of key information, from the direct station selection key signal transmit portion 101 or the general-purpose key signal transmit portion 102 of a console are provided with a heading bit and an ending bit, and transferred to the key signal receiver portion 201 of the position controller 200 in a bit serial manner, and thence the key information is transferred to the common control equipment.

Line status display information (line status signals) from the busy lamp field controller (19 in Figure 2) is transferred through the OR gates 207 (and line drivers 206 and line receiver 108) to the lamp/display signal receiver and indicative portion 104 of the attendant console 100 in a bit serial manner for passage to the busy lamp field portion 103. In this case, line status display information (line status signals) is transferred in a time-sharing manner with lamp/display signals sent from the lamp/display signal transmit portion 203 along a common signal path, and the former signals are provided with heading bits whilst the latter signals are provided with heading bits and ending bits.

Figure 4 shows in block form the busy lamp field controller (19 in Figure 2), which comprises a register 301, a control circuit 302, random access memories 303 and 304, selectors 305 to 307, a two-digit decade counter 308, a matcher 309, a timing signal generator 310, data buses 311, address buses 312, AND gates A1 to A6, OR gates G1 to G4 and flip-flops FF1 to FF4, and in which display information (line status signals S1 to S4) is derived from the OR gates G1 to G4.

An initial setting is achieved by registering all subscribers' telephone numbers in the memory 303. For example, a 4-digit telephone number is transferred, in the form of a BCD code, from a map or the like of the common control equipment of an exchange in which the attendant console control apparatus is employed, to the register 301 through the data buses 311, and the control circuit 302 applies a write pulse WP-1 to the memory 303 to write therein the content of the register 301. The memory 303 has a 16-bit wide area (a) for writing therein the aforesaid 4-digit BCD coded telephone numbers and, for example, a 1-bit wide line status bit area (b) corresponding to the telephone numbers. The telephone numbers can be written into the memory at locations the addresses of which are independent of the telephone numbers themselves.

If potential awkwardness in relation to the modification of telephone numbers can be disregarded to an extent, a read-only memory (ROM) or a programmable read-only memory (P-ROM) can be used to provide the area (a) of the memory 303. This can provide a merit of further simplification of apparatus construction.

After initial setting, upon detection of a status transition in relation to a particular line, by means of an on-hook or off-hook operation in relation to a particular telephone number, the common control equipment of the exchange sets a status indicating signal and the telephone number in the register 301. This telephone number is retrieved by the matcher 309 from the telephone numbers registered in the memory 303, under the control of the control circuit 302, and the area (b) corresponding to the retrieved telephone number is updated in accordance with the status indicating signal set in register 301. Accordingly, the content of the memory 303 is always indicative of the latest line status.

An embodiment of the present invention could be constructed in which all the line statuses can be displayed at one time in accordance with the content of the memory 303, but it is sufficient, in general, to provide only a display of line statuses relating to about one hundred lines at any one time, so that, in the present example, use is made of the two lower-order digits of the relevant telephone numbers to arrange those numbers in numerical order to provide a display of the line statuses relating to one hundred lines.

For instance, when the console attendant dials the two higher-order numerals of the telephone number of a subscriber upon reception of a request for a call to that subscriber, the two higher-order digits of the telephone number are set by the common control equipment of the exchange in the register 301 (which has areas for setting the two higher-order digits, each area corresponding to one attendant console, through these are not shown). The selector 305 is controlled by the control circuit 302 and the timing signals generator 310 so that it applies the two higher-order digits set in the register 301 to the matcher 309 so that they may be matched with the two higher-order digits of telephone numbers registered in the memory 303. For example, when a call is to be made to a line having a telephone number "1215", matching of the two higher-order digits "12" is achieved and the line statuses in the area (b) relating to the telephone numbers "1200" to "1299" are read out from memory 303 and, at the same time as the line statuses are read out the selector 306 accesses the memory 304 in dependence upon the two lower-order digits "00" to "99" of the telephone numbers to which the line statuses relate. At this time, the control circuit 302 produces a write pulse WP-2 to write the line statuses read out from the area (b) of 303 into memory 304. That is, when the output signals from the control circuit 302 and the matcher 309 are both "1", a line status bit from the area (b) is written in the memory 304 through the AND gate A1, which memory is accessed using the two lower-order digits of the telephone number to which the bit relates as address information. Accordingly, the memory 304 stores line status relating to telephone lines in the numerical order of the two lower-order digits of telephone numbers corresponding to those lines. Since it is considered that there may be requests for display of the line statuses of a number of different levels (e.g. the twelve hundreds, the thirteen hundreds, etc) of telephone numbers from a plurality of console attendants at one time, such re-arrangement of the telephone numbers as described above is carried out in a time-sharing manner, with the registers respectively corresponding to the attendant consoles selected by the selector 307.

On the other hand, the memory 304 is read out in the following manner:- The clock signals from the timing signal generator 310 are counted by the two-digit decade counter 308, the output from which is applied as address information through the selector 306 to the memory 304 to periodically access the memory 304 in the intervals between the aforesaid write times. Accordingly, the line status information is read out from the memory 304 in accordance with the numerical order of the telephone numbers of the lines to which the information relates. Switching of the operation of selector 306 is performed in response to the output from the AND gate A2.

From the memory 304, the line status information relating to a plurality of lines (one hundred, for example), is read out and applied to the AND gates A3 to A6, respectively, and in accordance with signals from the timing signal generator 310, the line status information from the memory 304 is applied to any one of the flip-flops FF1 to FF4. For instance, if a request for display of line status information comes from the operator of the indicative portion of a first attendant console and concerns a telephone having a number in the 1500s, read-out information corresponding to the hundred lines having telephone numbers from 1500 to 1599 is applied to the flip-flop FF1 in the bit serial manner. If a request for display of line status information comes from the operator of the indicative portion of a second console and concerns a telephone having a number in the 2200s, read-out information relating to the hundred lines having telephone numbers from 2200 to 2299 is similarly applied to the flip-flop FF2. In a similar manner, read-out information relating to one hundred lines complying with display requests from the operators of the other consoles is also applied to each of the flip-flops FF3 and FF4.

The flip-flops FF1 to FF4 are D-type flip-flops, reference character C indicating clock signal input terminals and D data input terminals. Their Q-terminal outputs are respectively applied to the OR gates G1 to G4, to which are applied heading bits from the timing signal generator 310.

Accordingly, display information (line status signals) S1 to S4 (each signal relating to one hundred telephone lines) is headed by a heading bit and composed of the line status information arranged in the order of the two lower-order digits 00 to 99 of the telephone numbers, as shown in the time chart of Figure 5, and each line status signal is sent out to the indicative portion of an attendant console in the time-sharing manner.

Figure 6 illustrates in block form the principal parts of the busy lamp field portion (line status indicative portion) 103 of Figure 3. Line status information Si (i = 1, 2, 3, 4) is

sequentially set in a main-shift register 401 (the bits of a line status signal are serially fed into the register 401). Heading bit ST (see Figure 5) is detected by a control circuit 402 and the appearance of this heading bit ST at a tap at the output end of the main-shift register 401 is detected by the control circuit 402. Taps are led out from the main-shift register 401 every 16 bits, and connected to sub-shift registers 403 to 409, respectively.

When the control circuit 402 detects the appearance of the heading bit ST at the output end tap connected to the shift register 403, 16 shift clock pulses are applied from the control circuit 402 to each of the shift registers 403 to 409, causing them to perform 16-bit shifts from the main-shift register 401. Thus, the outputs from the shift registers 403 to 409 (one output provided for each register stage, i.e. each bit held in a register) provide the line status information, each output providing the value of the line status bit corresponding to a telephone number the two lower-order digits of which are the same as the number of the input as illustrated in Figure 6.

When providing a BLF (busy lamp field) display relating to, for example, the aforesaid telephone number "1215", the line status of each of the lines from "1200" to "1299" is indicated as by luminescent diodes 410. In this case, if the line "15" is indicated to be busy and if the line "16" is indicated to be idle, it is decided that the line "1215" is busy and that the line "1216" is idle.

In this display process, during the shifting operations of the shift registers 403 to 409, indicator elements such as the luminescent diodes 410 go on and off in response to the values of the line status bits as they are shifted through the registers. By having a sufficiently high shift speed, such flashing of the indicator elements can be limited to occur over a very short shifting period, and a predetermined fixed indication of line statuses can then be provided. Accordingly, the flashing will neither give the operator an unpleasant feeling nor lead him to misinterpretation of the line status indications. In this manner, line status information serially transmitted (a line status signal comprising a series of line status bits) is converted by the shift registers 403 to 409 into a parallel form, so that there is no need to repeatedly apply the same line status information to the same indicative portion. Even where a plurality of indicative portions are provided (for example in respective attendant consoles), since the busy lamp field controller as shown in Figure 4, which is the line status information sending portion, is shared by the consoles the construction can be made economical.

The above example has been described in connection with the case where the line status information provides indications as to whether telephone lines are busy or idle. However, if information such as class of subscriber, their presence or absence, etc. is stored in the memory 303 in correspondence with the respective telephone numbers of telephone lines, such status information can be displayed by operations as described above. Further, the numbers of higher- and lower-order digits which are employed in the busy lamp field controller, for matching in memory 303 and for addressing memory 304, can be selected in accordance with the numbers of digits of the telephone numbers and the number of indicator elements provided in the indicative portions used to display line statuses, so that the telephone numbers may be "split" into higher- and lower-order digits in ways different from the "split" into two higher-order digits and two lower-order digits used in the above example.

In the indicative portion, indicator elements such as luminescent diodes 410, for example, can be driven directly by the parallel outputs provided by the shift register 403 to 409, but it is also possible to control the indicator elements by relays or drivers, for example, for flashing. Moreover, the number of indicative portions can be increased, of course, and this need not introduce undue complexity in the construction.

As described above, merely by providing a construction as described with reference to Figure 4 in a telephone exchange and providing a construction as shown in Figure 6 in an attendant console used with the exchange, line status information can be indicated in a form to be easily recognised. For example, where the indicative portion of Figure 6 is formed with C-MOS and TTL circuit elements, it can be realised using 21 integrated circuits and can be loaded on one or on a number of printed circuit boards, so that a required space therefor can be very small. Further, the busy lamp field controller of Figure 4 can, in essence, be shared by a plurality of indicative portions, and hence is of economical construction.

Figure 7 illustrates in block form the direct station selection key signal transmit portion 101 and the general-purpose key signal transmit portion 102 of Figure 3. The direct station selection key signal transmit portion comprises a direct station selection key matrix 501, a decoder 502, a multiplexer 503, a row counter 504, a column counter 505, a scanning control circuit 506, a column register 507, a row register 508, a sending control circuit 509 and an OR gate 510. The general-purpose key signal transmit portion 102 comprises a key matrix 601, a row encoder 602, a column encoder 603, a control circuit 604, a shift register

605, a rising edge detector circuit 606, a trailing edge detector circuit 607, OR gates 608, 609 and 612 and AND gates 610 and 611.

The key matrix 601 is, for instance, an 8 × 8 key matrix, and when a key P is turned on, its position is converted (encoded) by the row and column encoders 602 and 603 into a binary number which is indicative of the position of the key point P in terms of the X- and Y-coordinates of the matrix. At the same time, by means of outputs from the row and column encoders 602 and 603, an output "1" is derived from the AND gate 611 and a signal detecting the moment of rising of the output of AND gate 611 from "0" to "1" is obtained by the rising edge detector circuit 606 and then applied to the control circuit 604.

Upon application thereto of the rising edge detection signal, the control circuit 604 applies a set instruction signal to the shift register 605 to set therein the encoded outputs from the row and column encoders 602 and 603 and, at the same time, in response to a transfer instruction signal issued from the control circuit 604, the content of the shift register 605 is transferred in a bit serial manner to the position controller (17 in Figure 2) through the OR gates 612 and 105 and the line driver 106. In this case, a heading bit and an ending bit are respectively added by the control circuit 604 to the head and tail of the key information and the output contents of the row and column encoders 602 and 603 are fed back to the shift register 605 and held therein.

When the key P is turned off, the output from the AND gate 610, shown to correspond to the key P, is altered from "1" to "0" and its trailing edge is detected by the trailing edge detector circuit 607. The circuit 607 then generates a trailing edge detecting signal in response to which the control circuit 604 sends a transfer instruction signal to the shift register 605 to transfer its content in a bit serial manner. Also in this case, heading and ending bits are added by the control circuit to the key information.

For indicating whether the key P is in the on or off state, a special bit may be added to the key information, or the ending bit may be used; for instance, its on and off state being indicated by "1" and "0", respectively.

Figure 8A is a time chart explanatory of the operation of the abovesaid general-purpose key signal transmit portion 102, *a* showing the on and off states of the key and *b* the rising edge detecting signal. Upon obtaining this detecting signal, the key information is transferred in a bit serial manner, as indicated by *c*. When the trailing edge detecting signal is obtained as indicated by *d*, the key information is transferred again in the bit serial manner, as indicated by *c*. Exactly the same operation can also be provided in connection with the other keys of the key matrix 601. In Figure 8A, *e* indicates that there may be provided in the key matrix keys for which key information is sent only upon rising edge detection when the key is turned "on".

The key matrix 501 of the direct station selection key signal transmit portion 101 is, for example a 10 × 10 key matrix. Each cross point of the key matrix is scanned to determine whether or not the key at the crosspoint is depressed. All the crosspoints are scanned in turn with a scanning cycle time of, for instance, 1 ms. Clock pulses from the scanning control circuit 506 are applied to the row and column counters 504 and 505. A count output signal from the row counter 504 is applied to decoder 502, which decodes that output signal and applies row selection pulses to the rows of the key matrix 501 in turn, in a cyclically repeating manner, in dependence upon the counts represented by the count output signal. When a row selection pulse is applied to a row of the key matrix along which a key is depressed that pulse is applied to the multiplexer 503 *via* the depressed key. All the columns of the matrix are scanned in turn, in dependence upon the counts represented by a count output signal from the column counter 505, each time a new row is selected. Upon scanning of that column in which a depressed key is located, when the row in which that key lies is selected, the row selection pulse applied to that row is returned as a column information pulse (return pulse) to the scanning control circuit 506 from the multiplexer 503.

The scanning control circuit 506 monitors whether or not a row selection pulse is returned as a column information pulse. When the column information pulse is received as a return pulse, the scanning control circuit 506 applies a set instruction signal to each of the row and column registers 507 and 508 to set therein the count values of the column and row counters 505 and 504, respectively, and starts the sending control circuit 509.

The sending control circuit 509 firstly causes the content of the column register 507 to be sent in a bit serial manner, and after a predetermined period of time, for example, 20 ms, causes the content of the row register 508 to be sent in bit serial manner. During such sending operations, a busy signal is applied from the sending control circuit 509 to the scanning control circut 506 to inhibit the sending of a further set instruction signal to the column and row registers 507 and 508.

By causing the contents of the column and row registers 507 and 508 to correspond to the tens and the units digits of the telephone numbers of subscribers, the key information from

the key matrix 501 is equivalent to two digits of a dialled telephone number.

Figure 8B is a time chart explanatory of the above operations of the direct station selection key signal transmit portion, *a* indicating the on and off states of a key in matrix 501, *b* indicating column information pulses, and t1 the scanning cycle time (one key of the matrix is depressed, and as that key is scanned in each successive scanning cycle column information pulses as shown at *b* are provided). When the column information pulse indicated by *b* is obtained (the first such pulse), the set instruction signal indicated by *c* is provided and the busy signal indicated by *d* is applied from the sending control circuit 509 to the scanning control circuit 506. The column information is sent in the bit serial manner, as indicated by *e* and after a predetermined period t2, row information is obtained as indicated by *f*.

Figure 9 shows in block form the principal parts of the lamp/display signal transmit portion 203 of the position controller 200 and the lamp/display signal receiver and indicative portion 104 of the attendant console 100 of Figure 3. The lamp/display signal transmit portion 203 comprises a random access memory 701, for holding information relating to the operative state of the exchange, a write register 702, a read register 703, an address counter 704 and a signal distributor circuit 705. A lamp/display signal (i.e. a signal containing information relating to the operative state of the exchange) can be read out from the random access memory 701 in accordance with the content of the address counter 704, and applied by the distributor circuit 705 in a bit serial manner to a predetermined one of the attendant consoles through the OR gate 207 and the line driver 206 (see also Figure 3) so that a display may be provided at the console indicative of the operative state (or some aspect of that state) of the exchange. In this case, heading and ending bits are added to the lamp/display signal.

The lamp/display signal receiver and indicative portion 104 comprises a main-shift register 801, a control circuit 802, AND gates 803 and 804, a plurality of sub-shift registers 805, a lamp/display portion 806, a power switch circuit 807, a gated latch circuit 808, a lamp check circuit 809, an OR gate 810 and a key 811.

Lamp/display signals and line status signals received by the line receiver 108 (see also Figure 3) are applied to the lamp/display signal receiver and indicative portion 104. Clock signals are applied through line receiver 107 (see Figure 3).

Lamp/display signals from the lamp/display signal transmit portion 203 are applied to the main-shift register 801, and converted by the sub-shift register 805 into a parallel signal in a manner similar to the way in which line status signals are processed in the busy lamp field portion of Figure 6. It will be understood that although both line status signals and lamp/display signals, relating respectively to the operative conditions of subscriber lines and to the operative condition of the exchange are both applied to the lamp signal receiver and indicative portion 104, the line status signals are passed onto the busy lamp field portion whilst lamp/display signals are passed to shift register 801.

The power switch circuit 807 is to turn off the power supply of the lamp/display portion 806 to prevent display lamps therein from repeatedly turning on and off while the tap outputs from the main-shift register 801 are shifted in series and set in the lamp/display portion.

When a lamp/display signal is set in the main-shift register 801, the output from the AND gate 803 is made "1" by the heading and ending bits of the signal whereby the control circuit 802 is started to supply shift clock pulses to the sub-shift registers 805. At the same time, the power switch circuit 807 is controlled to be turned off and the gated latch circuit 808 is also controlled to be turned off.

Lamp/display signals and line status signals are transferred in a time-sharing manner, so that at the moment of completion of setting of a lamp/display signal in the sub-shift registers 805, after setting in the main-shift register 801, the AND gate 804 is opened so that a line status signal can be relayed through that gate and transferred to the busy lamp field portion 103 (see Figure 6).

When a lamp/display signal is set in the sub-shift registers 805, the power switch circuit 807 is turned on to light the indicative lamps of the lamp/display portion 806, thereby indicating the operative state of the exchange. As long as the state of the exchange remains unchanged, the same content is repeatedly read out from the memory 701 by the address counter 704, so that the indicated content of the lamp/display portion 806 remains unchanged. Even if a temporary transfer error occurs, the correct lamp/display signal is received in the next read out period, substantially ensuring the provision of a correct lamp indication at all times.

The gated latch circuit 808 is provided for return testing. Test mode information is applied to the gated latch circut 808 at a predetermined bit position, and when the test mode bit is, for example, "1", a predetermined number of bits, for instance sixteen bits, are set in the gated latch circuit 808 from a predetermined one of the sub-shift registers 805.

The content of the gated latch circuit 808 is applied to the row and column encoders 602 and 603 of the key matrix 601 of the general-purpose key signal transmit portion 102 (refer to Figure 7) and a signal similar to a signal obtainable by actuation of a key in the key matrix 601 is transferred to the position controller 200.

Such return testing can be achieved by utilizing an NT (Night Mode) key which is provided, for example, in the attendant console, that is, a key which is actuated by the console operator when that operator leaves the console. For instance, as shown in Figure 10 which is explanatory of return testing, a mode decision circuit 20 and an operation mode switchover circuit 21 are provided for the attendant console 15, the position controller 17 and the busy lamp field controller 19, and switching between a call processing portion 22 and a maintenance and administration processing portion 23 of the exchange is effected in dependence upon a decision signal provided by the mode decision circuit 20.

When the aforesaid NT key is turn on, the position controller 17 transfers an NT lamp ON signal to the attendant console 15 and the mode decision circuit 20 decides that a test mode is to be adopted in response to the NT lamp ON signal, and by means of the operation mode switchover circuit 21, switching is effected from the call processing portion 22 to the maintenance and administration processing portion 23. Thus, normal processing is suspended and a test mode is adopted. The maintenance and administration processing portion 23 controls sending of a test pattern from the position controller 17. The test pattern is distinguished from information sent in the course of normal operations by the setting of the test mode bit to "1" as described above with reference to Figure 9. In the lamp/display signal receiver and indicative portion 104 (see Figure 9), the test mode bit is transferred to the gated latch circut 808 from whence signals are sent to the general-purpose key signal transmit portion 102 (see Figure 3 also), and then signals sent from portion 102 to the position controller 17 as a signal corresponding to the key operation of the key matrix 601.

Accordingly, by checking the received "key" signal for the expected test pattern in the position controller, signal receiving functions and the key information transfer functions of the attendant console and normality of the transmission line are automaticaly tested.

For such return testing, the NT key can be utilised, so that there is no need of providing a special key. Further, where switching between the call processing portion 22 and the maintenance and administration processing portion 23 is effected, tests other than return tests can be achieved. Accordingly, tests can be carried out by means of key operation of an attendant console without providing an input/output device such as a typewriter or the like solely for maintenance and administration purposes. This provides an economical construction.

Figure 11 is a block diagram explanatory of display lamp checking operations, illustrating in detail principal parts of the lamp/display signal receiver and indicative portion 104. The control circuit 802 of Figure 9 comprises a J-K flip-flop 821, AND gate 822 and counter 823. The indicative lamp portion 806 comprises lamps or light emission diodes 831 supplied with the parallel output from the sub-shift registers 805, and protective resistors 832. The power switch circuit 807 is formed with transistors 841.

When the heading and ending bits set in the main-shift register 801 are detected by the AND gate 803, the flip-flop 821 of the control circuit 802 is set at the timing of clock pulses applied to the CL-terminal thereof, and the Q-terminal output from the flip-flop 821 becomes "1" and clock pulses are supplied to the counter 823 and the sub-shift registers 805 through the AND gate 822. Having counted a required number of clock pulses which are shifted in series from the main-shift register 801 to the sub-shift registers 805 and set therein, the counter 823 overflows and applies an overflow signal to a K-terminal of the flip-flop 821 to reset it.

Since the Q-terminal output from the flip-flop 821 is applied to the bases of the pnp transistors 841 of the power switch circuit 807, the power switch circuit 807 is held in the off state while the flip-flop 821 is set, that is, while the clock pulses are shifted in series to the sub-shift registers 805.

The operations such as described above are repeated and the light emission diodes 831 of the lamp/display portion 806 are lit in accordance with the contents of the sub-shift registers.

During lamp checking, a signal "1" is continuously applied to the main-shift register 801 by turning on a key 811 of a lamp check circit 809. Consequently, the flip-flop 821 is reset only when the counter 823 produces the overflow signal, and is immediately set by the next clock pulse. That is, the flip-flop 821 is reset only for the period of one clock pulse and the resetting period is the counting period of the counter 823.

For example, if the counter 823 is a 4-bit counter, the light emission diodes 831 are lit dimly, that is to say they are lit with a duty cycle of 1/16. When all of the light emission diodes 831 are dimly lit this indicates that operation is normal, but if one or more of the light emission diodes are not dimly lit, it is thereby indicated that a malfunction exists

somewhere in the system. A decision as to where the malfunction exists is made in accordance with the following table in which the light emission diodes 831, the control circuit 802, the sub-shift register 805 and the power switch circuit 807 are identified as LED, CTL, SSR and PSW, respectively, and in which "O" indicates normal function and "X" indicates a malfunction.

	LED	CTL	SSP	PSW
All LEDs dimly lit	O	O	O	O
No LEDs lit, or all LEDs brightly lit	O	X	O	O
One or more LEDs not lit	X	O	O	O
Tow or more LEDs not dimly lit	O	O	X	O
Two or more LEDs, driven in common from PSW, not dimly lit, or brightly lit	O	O	O	X

The lamp check takes place independently of a lamp drive control circuit in previously proposed console control apparatus. In the present embodiment of this invention, however, as is seen from the above, the lamp check covers the circuits neighbouring the lamp. Further, even during normal call processing, the lamp check can be effected in the attendant console without exerting any influence on the position controller. Moreover, the structure employed for effecting lamp check may be a simple structure to which a signal indicating lamp lighting can be continuously applied, and which is not related to the number of display lamps. In addition, the point at which a malfunction occurs can be deduced from the lighting status, as shown in the above table, and since the dim lighting of the lamps (lighting with a duty cycle of 1/16th) is taken as the normal status, the power supply is not overloaded even though all the display lamps are lit in the normal state.

In Figure 6, the light emission diodes 410 are driven directly by the parallel outputs from the sub-shift registers 403 to 409. Thus, in the arrangement of Figure 6, bright lighting of the diodes is used as the normal status, but the parts of the arrangement of Figure 6 can be checked in accordance with a system similar to that outlined above with reference to the above table. In Figure 6, the power switch circuit can be added, as shown in Figures 9 and 11.

As described above, in an embodiment of the present invention, key information is transferred in a bit serial manner and line status information is transferred in a bit serial manner and in a time-sharing manner with lamp/display signals along a common signal path, so that it is sufficient to provide only three pairs of signal lines, including the clock signal line, between each attendant console and the position controller. Accordingly, the construction of an embodiment of this invention can be made very simple. Further, when a line accommodated in the exchange is called the line status information of the called line is obtained before the attendant's operation for calling the line. Accordingly, service for the reception of a call can be improved.

In the line status information display, line status information corresponding to respective telephone numbers is stored in a memory and, at a line status display request, the line status information designated by the higher-order digits of the respective telephone numbers is read out from the memory and arranged and transferred in the numerical order of the lower-order digits. There is no need for coordinating the order of the telephone numbers to that of the memory addresses. Accordingly, changing of the number of subscribers or modification of the telephone numbers can also readily be achieved simply by modifying the corresponding part of the memory (by effecting the initial setting again).

Moreover, since it is not necessary to provide indicator elements corresponding to all subscribers, the line status display portion is small and simple, and can be attached to an existing attendant console also.

Further, line status information is periodically transferred from the position controller to the attendant console in a bit serial manner, in a time-sharing manner, so that even if a temporary bit error occurs, it can be corrected by the information transferred in the next period, and return testing and lamp checking can be easily achieved.

Since key information from the direct station selection key signal transmit portion can be sent in the same form as a pattern of a dial number, the key information can be processed regardless of whether the key information is of a dial operation or a key operation.

Thus, an embodiment of the present invention can be provided in which key information from the attendant console can be transferred to a telephone exchange in a bit serial manner, and line status information from the telephone exchange is transferred periodically to the console in a bit serial manner to indicate line status in the console. The line status information can be transferred in time-sharing manner. At a request from the attendant console, line status information can be transferred from the telephone exchange to the attendant console in the bit serial manner, and subjected to serial-parallel conversion to obtain parallel signals for driving lamp indicator portions to provide an indication of the line status information. The number of signal lines connected to the attendant console can thus be markedly reduced as compared with previous proposals and, in the case of telephone number modification, for example, proper steps can be taken immediately and can be relatively simple.

WHAT WE CLAIM IS:-

1. Telephone exchange apparatus, for use in a telephone exchange connected to a plurality of telephone lines, the apparatus comprising an attendant console, having a plurality of signalling keys, for use by an attendant at the console to provide control and data signals, line status display means for indicating to the attendant the operational statuses of a predetermined number of such telephone lines, and exchange status display means for indicating to the attendant the operational status of the telephone exchange, a position controller, for controlling and monitoring operations of the attendant console, a busy lamp field controller, for providing line status signals indicative of the operational statuses of such telephone lines, and exchange control circuitry in dependence upon which the busy lamp field controller is operable to provide such line status signals and to pass such line status signals to the attendant console to provide such an indication in the line status display means, and which is operable to provide exchange status signals and to pass on such exchange status signals to the attendant console to provide an indication in the exchange status display means, and which is further operable, in response to such control and data signals passed from the attendant console to the position controller, to control operations in the exchange, wherein the said control and data signals are passed from the attendant console to the position controller in a bit serial manner, and wherein such line status signals from the busy lamp field controller and such exchange status signals from the position controller are passed to the attendant console in a bit serial and time sharing manner along a common signal path.

2. Apparatus as claimed in claim 1, wherein the said busy lamp field controller comprises memory means operable to hold in respect of each of the said plurality of telephone lines, in association with a number indicative of the line, line status data indicative of the operational statuses of the lines, and the busy lamp field controller being operable in response to receipt thereat of a request signal, from the attendant console, for supply of such a line status signal to the said line status display means, to read out from the memory means such line status data relating to each of such a predetermined number of lines, for delivery to the attendant console, and to the line status display means, in a line status signal.

3. Apparatus as claimed in claim 2, wherein, in response to such a request signal, line status data relating to each of lines of the said plurality whose numbers have one or more higher-order digits in common are read out, when the apparatus is in use, such line status data being delivered to the said line status display means in an order determined by the numerical values of the lower-order digits of the numbers of the telephone lines concerned.

4. Apparatus as claimed in claim 3, wherein the said memory means comprise first and second memory devices and a decimal counter, the first memory device being operable to hold the said line status data indicative of the operational statuses of each line of the said plurality in association with the numbers indicative of those lines, and wherein when the apparatus is in use, in response to receipt at the memory means of such a request signal, the line status data relating to each of the said lines whose numbers have the said one or more higher-order digits in common are read out from the first memory device and written into the second memory device, the numerical values of the said lower-order digits of the numbers indicative of the lines being employed to designate respective storage addresses in the second memory device for the line status data relating to those lines, the said line status data being read out from the second memory device in sequence in response to the supply of successive counting signals from the decimal counter to the second memory device, whereby the line status data is delivered in the said order.

5. Apparatus as claimed in any one of claims 1 to 4, wherein the said line status display means include a serial-parallel converter whereby the line status data in a line status signal

supplied to the display means is supplied in parallel, contemporaneously, to respective display elements of the display means, when the apparatus is in use.

6. Apparatus as claimed in claim 5, wherein the said serial-parallel converter comprises a main shift register and a plurality of secondary shift registers, the said main shift register being connected to receive and store such line status data, inputs of the respective secondary shift registers being connected to respective stages of the main shift register that are regularly spaced apart from one another (by other stages of the main shift register), and the stages of each secondary shift register having respective outputs connected to respective such display elements, whereby the contents of respective stages of the main shift register are transferred to respective stages of a secondary shift register, the outputs of which stages are connected to supply respective display elements, all of the display elements being so supplied contemporaneously, when the apparatus is in use.

7. Apparatus as claimed in claim 6, further comprising display element checking means whereby checking data, of predetermined value, is supplied to the said main shift register in place of such line status data.

8. Apparatus as claimed in claim 6 or 7, wherein the said line status display means comprises power supply control means operable to cut off power supply to the display elements whilst data is being transferred through the stages of the shift registers.

9. Apparatus as claimed in any preceding claim, wherein the attendant console includes a general-purpose key signal transmit portion and a direct station selection key signal transmit portion, wherein the general-purpose key signal transmit portion sends out key information in a bit serial manner when a signalling key thereof is turned on and off, and wherein the direct station selection key signal transmit portion scans the signalling keys thereof, and when a key is turned on sends out information designating the position of the turned on key in a bit serial manner.

10. Apparatus as claimed in claim 9, wherein the general-purpose key signal transmit portion and the direct station selection key signal transmit portion comprise respective key matrixes.

11. Apparatus as claimed in claim 9 or 10, wherein key information is sent out from the general-purpose key signal transmit portion and the direct station selection key signal transmit portion in a time-sharing manner.

12. Apparatus as claimed in claim 9, 10 or 11, wherein the general-purpose key signal transmit portion includes means for adding a key on-off information bit to the key information sent out therefrom when a key is turned on and off, adding means being employed to cause the content of at least one bit of the key information sent in the bit serial manner to correspond to the on and off states of the key.

13. Apparatus as claimed in claim 10 or either of claims 11 and 12 when they are appended to claim 10, wherein the direct station selection key signal transmit portion includes means for scanning the key matrix to read out information designating the position of a turned on key in the matrix, and wherein the row and column positions of a key in the matrix correspond to the tens and the units digit of a telephone number, respectively, and wherein row position information and column position information relating to a turned-on key of the key matrix are sent out in a time-sharing manner.

14. Apparatus as claimed in claim 1, substantially as hereinbefore described with reference to Figure 2, Figures 2 and 3 or Figures 2 to 11 of the accompanying drawings.

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1577461 COMPLETE SPECIFICATION

10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

FIG. 1

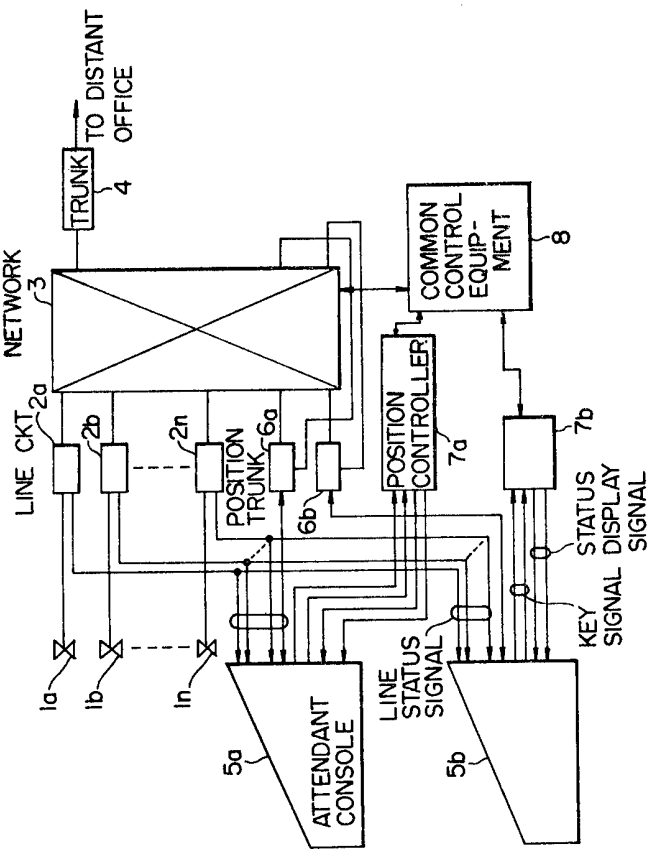
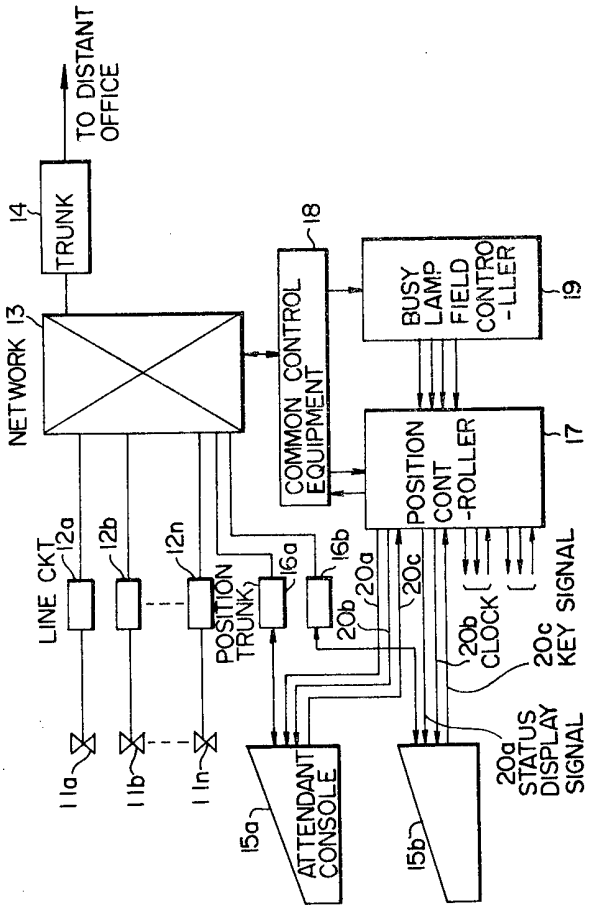


FIG. 2


TO DISTANT OFFICE
14
TRUNK
13
NETWORK
18
COMMON CONTROL EQUIPMENT
BUSY LAMP FIELD CONTRO -LLER
19
POSITION CONT -ROLLER
17
LINE CKT
12a
12b
12n
POSITION TRUNK
16a
16b
20a
20b
20c
20b CLOCK
20c KEY SIGNAL
20a STATUS DISPLAY SIGNAL
11a
11b
11n
15a
ATTENDANT CONSOLE
15b

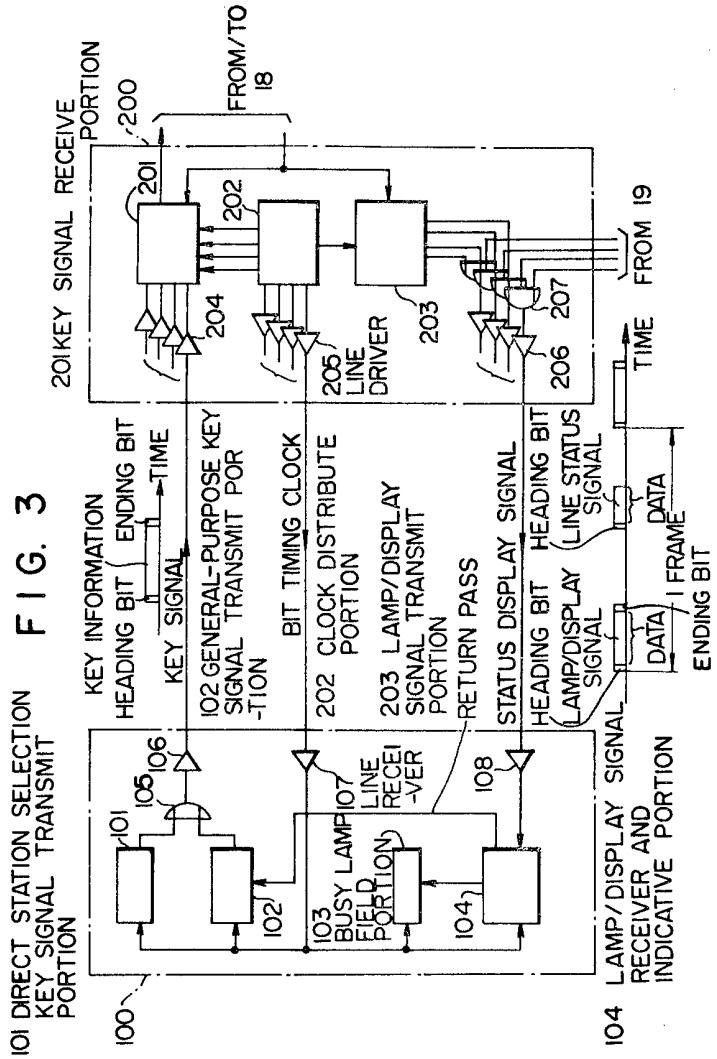

101 DIRECT STATION SELECTION KEY SIGNAL TRANSMIT PORTION
100
KEY INFORMATION
HEADING BIT
ENDING BIT
TIME
KEY SIGNAL
102 GENERAL-PURPOSE KEY SIGNAL TRANSMIT POR -TION
BIT TIMING CLOCK
202 CLOCK DISTRIBUTE PORTION
203 LAMP/DISPLAY SIGNAL TRANSMIT PORTION
RETURN PASS
STATUS DISPLAY SIGNAL
HEADING BIT
LAMP/DISPLAY SIGNAL
101
105
106
102
103 BUSY LAMP FIELD PORTION
107 LINE RECEI -VER
108
104
201 KEY SIGNAL RECEIVE PORTION
200
FROM/TO 18
201
202
204
205 LINE DRIVER
203
206
207
FROM 19
TIME
LINE STATUS SIGNAL
DATA
DATA
1 FRAME
ENDING BIT
104 LAMP/DISPLAY SIGNAL RECEIVER AND INDICATIVE PORTION

FIG. 3

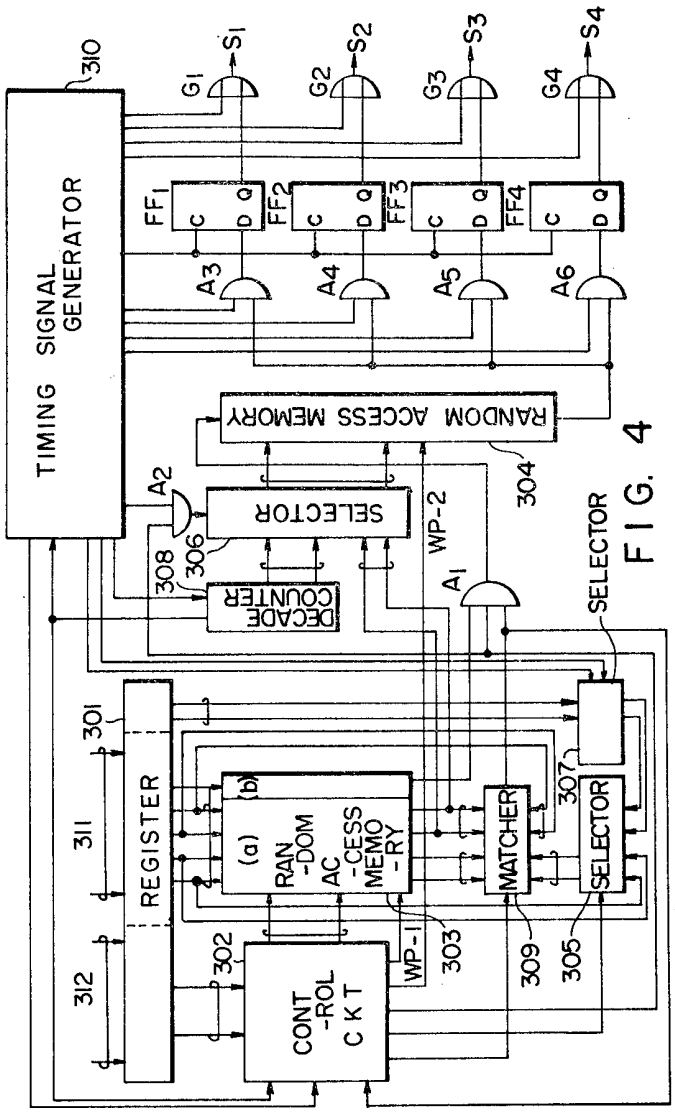
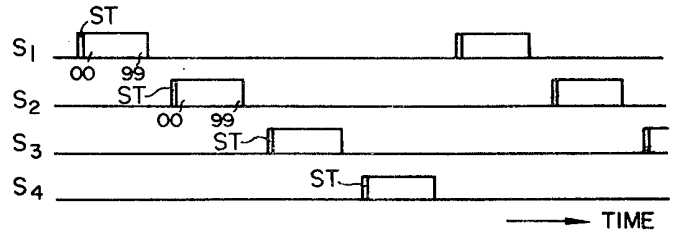

TIMING SIGNAL GENERATOR
310
G1
G2
G3
G4
S1
S2
S3
S4
FF1
FF2
FF3
FF4
C
D
Q
A3
A4
A5
A6
RANDOM ACCESS MEMORY
304
A2
SELECTOR
306
308
DECADE COUNTER
WP-2
A1
SELECTOR
301
311
312
REGISTER
(b)
(a)
RAN-DOM AC-CESS MEMO-RY
MATCHER
307
SELECTOR
302
CONT-ROL C K T
WP-1
303
309
305

FIG. 4

FIG. 5


ST
S1
00
99
S2
ST
00
99
S3
ST
S4
ST
TIME

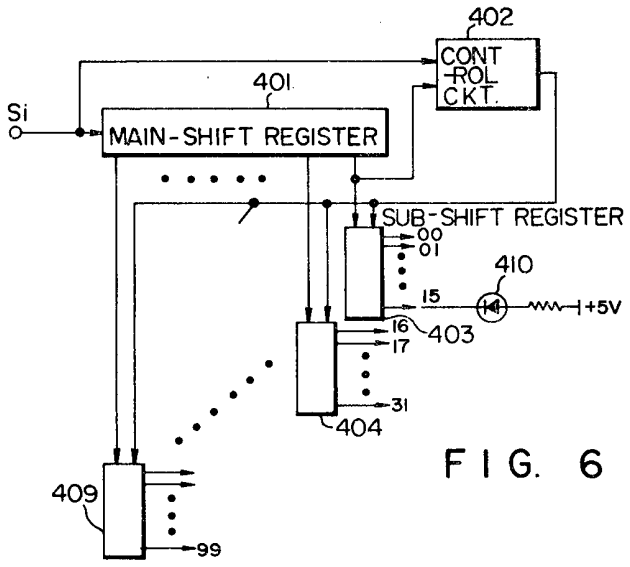

402
CONT
-ROL
CKT.
401
Si
MAIN-SHIFT REGISTER
SUB-SHIFT REGISTER
00
01
410
15
+5V
16
17
403
31
404
409
99

FIG. 6

FIG. 7

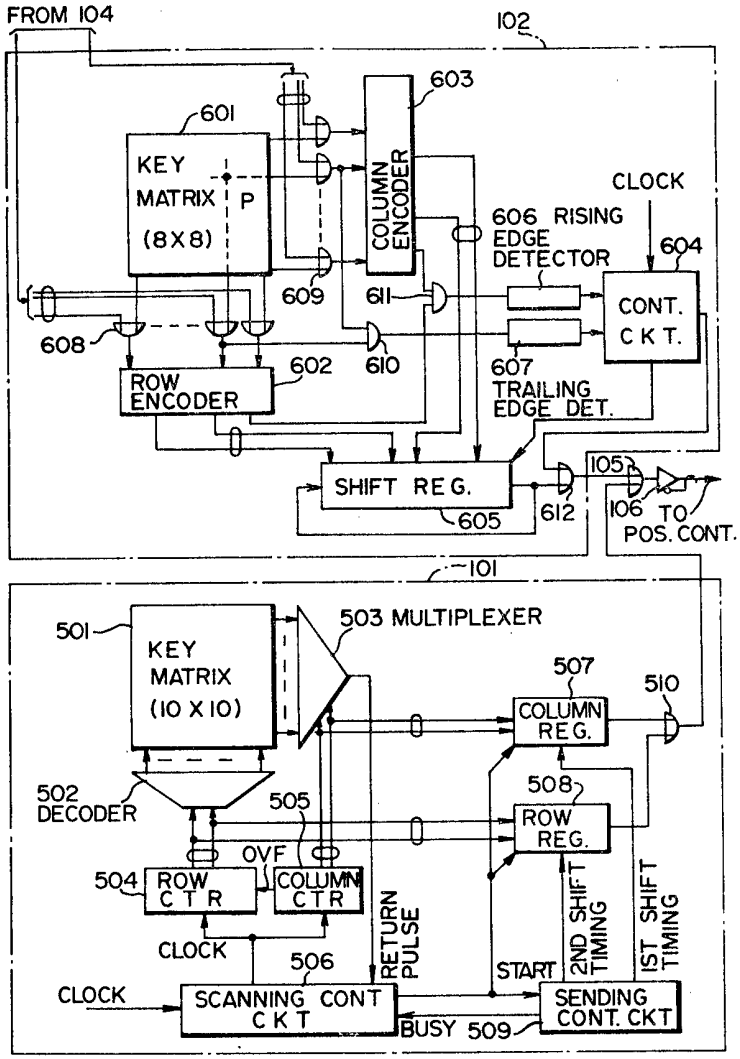

FROM 104
102
603
601
KEY MATRIX (8X8)
P
COLUMN ENCODER
CLOCK
606 RISING EDGE DETECTOR
604
609
611
CONT. C K T.
608
602
610
607 TRAILING EDGE DET.
ROW ENCODER
105
SHIFT REG.
612
106 TO POS. CONT.
605
101
501
KEY MATRIX (10 X 10)
503 MULTIPLEXER
507
510
COLUMN REG.
502 DECODER
505
508
ROW REG.
OVF
504
ROW C T R
COLUMN C T R
RETURN PULSE
2ND SHIFT TIMING
1ST SHIFT TIMING
CLOCK
506
START
CLOCK
SCANNING CONT C K T
SENDING CONT. CKT
BUSY 509

FIG. 8A

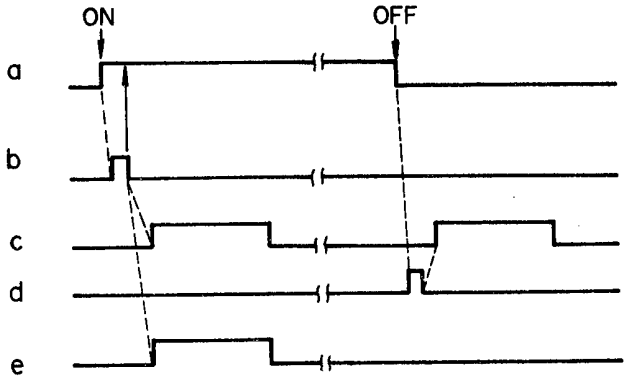
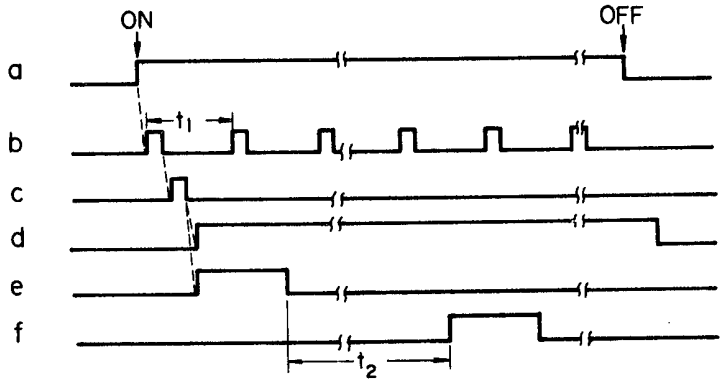


FIG. 8B



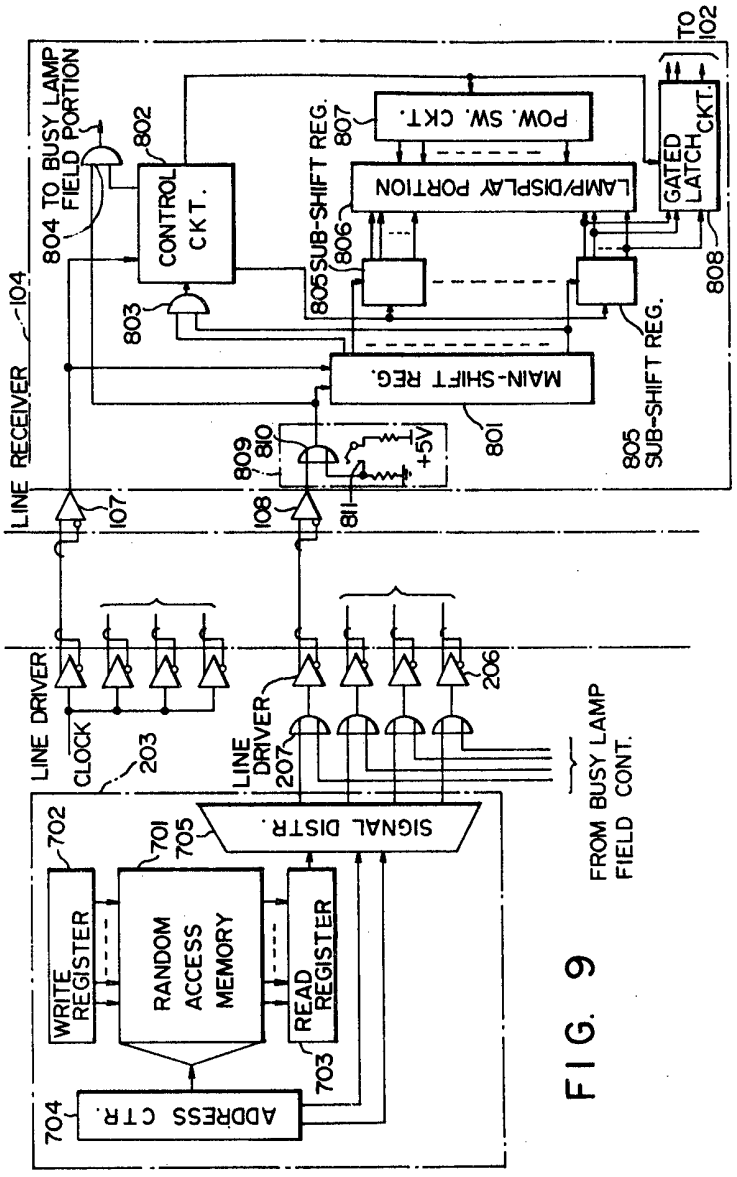
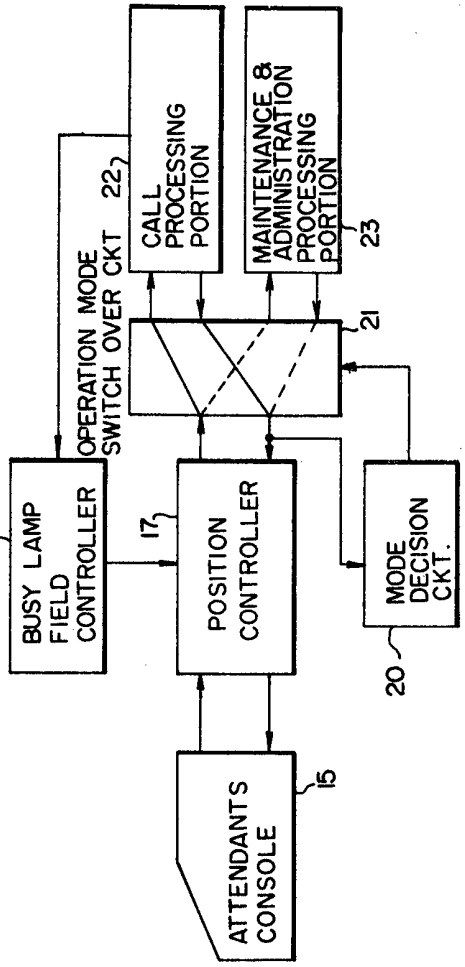

TO 102
804 TO BUSY LAMP FIELD PORTION
802
CONTROL CKT.
803
104
LINE RECEIVER
SUB-SHIFT REG. 807
POW. SW. CKT.
LAMP/DISPLAY PORTION
GATED LATCH CKT.
805 SUB-SHIFT REG. 806
808
MAIN-SHIFT REG.
801
809
810
+5V
805 SUB-SHIFT REG.
107
108
811
LINE DRIVER
206
CLOCK
203
LINE DRIVER 207
FROM BUSY LAMP FIELD CONT.
SIGNAL DISTR.
702
701
705
WRITE REGISTER
RANDOM ACCESS MEMORY
READ REGISTER
703
704
ADDRESS CTR.

FIG. 9

FIG. 10


CALL PROCESSING PORTION
MAINTENANCE & ADMINISTRATION PROCESSING PORTION
23
OPERATION MODE SWITCH OVER CKT
22
21
BUSY LAMP FIELD CONTROLLER
19
POSITION CONTROLLER
17
MODE DECISION CKT.
20
ATTENDANTS CONSOLE
15

1577461 COMPLETE SPECIFICATION
10 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 10

FIG. 11