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(54) **Title**: POLYSILICON FILMS BY HDP-CVD

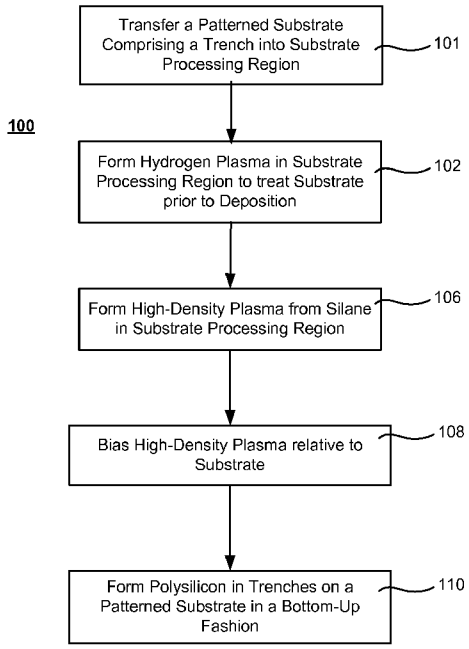

FIG. 1

(57) **Abstract**: Methods of forming polysilicon layers are described. The methods include forming a high-density plasma from a silicon precursor in a substrate processing region containing the deposition substrate. The described methods produce polycrystalline films at reduced substrate temperature (e.g. < 500°C) relative to prior art techniques. The availability of a bias plasma power adjustment further enables adjustment of conformality of the formed polysilicon layer. When dopants are included in the high density plasma, they may be incorporated into the polysilicon layer in such a way that they do not require a separate activation step.

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POLYSILICON FILMS BY HDP-CVD

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a PCT application of U.S. Patent Application No. 13/089,966, entitled "POLYSILICON FILMS BY HDP-CVD," filed April 19, 2011, and is related to and claims the benefit of U.S. Provisional Patent Application No. 61/435,487, entitled "DEPOSITION OF POLYSILICON FILM BY HDP-CVD," filed January 24, 2011, both of which are incorporated herein by reference in their entirety for all purposes.

BACKGROUND OF THE INVENTION

Semiconductor device geometries have dramatically decreased in size since their introduction several decades ago. Modern semiconductor fabrication equipment routinely produces devices with 45 nm, 32 nm, and 28 nm feature sizes, and new equipment is being developed and implemented to make devices with even smaller geometries. The decreasing feature sizes result in structural features on the device having decreased spatial dimensions. The widths of gaps and trenches on the device narrow to a point where the aspect ratio of gap depth to its width becomes high enough to make it challenging to fill the gap with material.

Polycrystalline silicon (often shortened to polysilicon) is a material which has multiple uses in the production of microcircuitry and solar cells. Polysilicon is deposited most commonly by thermal chemical vapor deposition (e.g. LP-CVD). It has also been deposited using plasma-enhanced CVD (i.e. PE-CVD) as well as formed through recrystallization of amorphous silicon. In many applications, polysilicon is doped and used as a gate or electrode. In other applications, polysilicon is used for portion(s) of transistors themselves, in which case they may be doped or intrinsic. The diversity of applications requires flexible methods for depositing polysilicon conformally as well as non-conformally.

New deposition methods are required which offer the flexibility to vary the conformality of the deposition of a polysilicon layer. These new methods should also enable deposition at reduced substrate temperatures in order to stay within increasingly stringent thermal budgets.

BRIEF SUMMARY OF THE INVENTION

Methods of forming polysilicon layers are described. The methods include forming a high-density plasma from a silicon precursor in a substrate processing region containing the deposition substrate. The described methods produce polycrystalline films at reduced substrate temperature (e.g. < 500°C) relative to prior art techniques. The availability of a bias plasma power adjustment further enables adjustment of conformality of the formed polysilicon layer. When dopants are included in the high density plasma, they may be incorporated into the polysilicon layer in such a way that they do not require a separate activation step.

Embodiments of the invention include methods of depositing a polysilicon layer in a trench of a patterned substrate in a substrate processing region of a substrate processing chamber. The methods include transferring the patterned substrate into the substrate processing region. The methods further include growing the polysilicon layer on the patterned substrate by forming a high density plasma in the substrate processing region from a deposition process gas comprising a silicon source while maintaining a mean pressure within the substrate processing region of about 20 mTorr or less and maintaining a mean patterned substrate temperature of 500°C or less. The methods further include removing the patterned substrate from the substrate processing region.

Additional embodiments and features are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the invention. The features and advantages of the invention may be realized and attained by means of the instrumentalities, combinations, and methods described in the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flow chart indicating selected steps in growing a gapfill polysilicon film according to embodiments of the invention.

FIG. 2 is a flow chart indicating selected steps in growing a conformal polysilicon film according to embodiments of the invention.

FIG. 3A is a simplified diagram of one embodiment of a high-density-plasma chemical-vapor-deposition system according to embodiments of the invention.

FIG. 3B is a simplified cross section of a gas ring that may be used in conjunction with the exemplary processing system of FIG. 3A.

DETAILED DESCRIPTION OF THE INVENTION

Methods of forming polysilicon layers are described. The methods include forming a high-density plasma from a silicon precursor in a substrate processing region containing the deposition substrate. The described methods produce polycrystalline films at reduced substrate temperature (e.g. < 500°C) relative to prior art techniques. The availability of a bias plasma power adjustment further enables adjustment of conformality of the formed polysilicon layer. When dopants are included in the high density plasma, they may be incorporated into the polysilicon layer in such a way that they do not require a separate activation step.

Depositing polysilicon on patterned substrate has been determined to be possible using high-density plasma techniques, with or without applied bias power. Stress typically associated with high-density plasma films has been found to be accommodated especially in systems with exposed silicon oxide on the patterned substrate. Conformal and bottom-up gapfill deposition regimes have both been determined and depend predominantly on the presence of a bias power and the polysilicon film growth rate. In both the conformal and bottom-up gapfill regimes, a hydrogen plasma treatment of the patterned substrate, prior to depositing the polysilicon, has been found to promote the growth of the polysilicon layer. The high density plasma chemical vapor deposition (HDP-CVD) technique may be used to enhance gap-fill as well as allowing deposition at the reduced substrate temperatures.

Conformal deposition of polysilicon has been found to occur at lower temperatures (e.g., <350° C) using HDP CVD. Low deposition rates (e.g., <500Å/min) and/or a high pressure (e.g., 10-30 mTorr) have also been found to produce conformal polysilicon films having side-wall (horizontal) and top (vertical) growth rates within about 50% of one another, in embodiments of the invention. HDP-CVD can also enable bottom up polysilicon deposition useful for filling gaps and trenches on a patterned substrate. The hydrogen pre-treatment of the exposed patterned substrate has been found to help produce dense polysilicon films with both column and/or grain-like structure. This may result from cleaning the exposed substrate and/or chemically terminating the exposed surfaces with hydrogen.

As used herein, a high-density-plasma process is a plasma CVD process that employs a plasma having an ion density on the order of 10^{11} ions/cm^3 or greater. A high-density plasma

may also have an ionization fraction (ion/neutral ratio) on the order of 10^{-4} or greater. Typically HDP-CVD processes include simultaneous deposition and sputtering components. Some HDP-CVD processes embodied in the present invention are different from traditional HDP-CVD processes which are typically optimized for gap-fill. In some steps and embodiments, conformal polycrystalline silicon films are achieved with substantially reduced (<10% of total plasma power) substrate bias power and thus create less sputtering than HDP-CVD processes that employ significant bias power. Despite this departure from traditional HDP process parameters, a scalar characterization involving sputtering and deposition rates will be useful and is defined below.

The relative levels of the combined deposition and sputtering characteristics of a high-density plasma may depend on such factors as the gas flow rates used to provide the gaseous mixture, the source power levels applied to maintain the plasma, the bias power applied to the substrate, and the like. A combination of these factors may be conveniently characterized by a "deposition-to-sputter ratio" defined as

$$\frac{(net\ deposition\ rate) + (blanket\ sputtering\ rate)}{(blanket\ sputtering\ rate)}$$

The deposition-to-sputter ratio increases with increased deposition and decreases with increased sputtering. As used in the definition of the deposition-to-sputter ratio, the "net deposition rate" refers to the deposition rate that is measured when deposition and sputtering are occurring simultaneously. The "blanket sputter rate" is the sputter rate measured when the process recipe is run without deposition gases (leaving nitrogen and a fluent for example). The flow rates of the remaining gases are increased, maintaining fixed ratios among them, to attain the pressure present in the process chamber during normal processing.

Other functionally equivalent measures may be used to quantify the relative deposition and sputtering contributions of the HDP process, as is known to those of skill in the art. A common alternative ratio is the "etching-to-deposition ratio"

$$\frac{(source-only\ deposition\ rate) + (net\ deposition\ rate)}{(source-only\ deposition\ rate)}$$

which increases with increased sputtering and decreases with increased deposition. As used in the definition of the etching-to-deposition ratio, the "net deposition rate" again refers to the deposition rate measured when deposition and sputtering are occurring simultaneously. The

"source-only deposition rate," however, refers to the deposition rate that is measured when the process recipe is run with no sputtering. Embodiments of the invention are described herein in terms of deposition-to-sputter ratios. While deposition-to-sputter and etching-to-deposition ratios are not precise reciprocals, they are inversely related and conversion between them will be understood to those of skill in the art.

Typical HDP-CVD processes are geared towards the gap-fill of trench geometries. In gapfill processes, a substrate bias RF power is used to accelerate ions toward the substrate which produces a narrow range of approach trajectories. This narrowing combined with sputtering activity allows gaps to be filled before the top corners of a growing via come together to form and maintain a void. Deposition-to-sputter ratios (D:S) in such gap fill applications may range from about 3:1 to about 10:1, for example, , with some exotic applications having deposition-to-sputter ratios to about 25:1, for example. Silicon oxide films grown according to embodiments of the present invention may be produced with an HDP-CVD process using little or no substrate bias power. The blanket sputtering rate under these conditions may be low and the deposition-to-sputter ratio can generally be expected to be above about 50:1 to about 100:1 in different embodiments.

In order to better understand and appreciate the invention, reference is now made to FIG. 1 which is a flow chart indicating selected steps in growing a gapfill polysilicon film according to embodiments of the invention. The gapfill polysilicon formation process begins when a patterned substrate having a trench is transferred into a substrate processing region (operation 101). Hydrogen (H_2) is introduced into the substrate processing region and a high density plasma is formed (operation 102) to pretreat the surface of the patterned substrate before polysilicon is deposited. Next, silane is flowed to the substrate processing region and a high density plasma is formed (operation 106) to deposit polysilicon on the patterned substrate.

A plasma bias is applied between the high-density plasma and the substrate to accelerate ions toward the substrate in operation 108. As a result, gapfill polysilicon is formed in the trench in a bottom-up fashion. The substrate bias power may be adjusted to control the deposition-to-sputter ratio during the growth of the polysilicon gapfill layer. Exemplary deposition-to-sputter ratios may range from about 2:1 to about 6:1 during deposition. Allowing significant sputtering to occur during deposition reduces the chances for significant void formation in the deposited bulk-gap fill layer.

FIG. 2 is a flow chart indicating selected steps in growing a conformal polysilicon film according to embodiments of the invention. The conformal polysilicon formation process begins when a substrate (patterned or unpatterned) is transferred into a substrate processing region (operation 202). Hydrogen (H_2) is introduced into the substrate processing region and a high density plasma is formed (operation 204) to pretreat the surface of the patterned substrate before polysilicon is deposited. Next, silane is flowed to the substrate processing region and an unbiased (or lightly-biased) high density plasma is formed (operation 206) to deposit polysilicon on the patterned substrate. Little or no plasma bias is applied between the high-density plasma and the substrate to accelerate ions toward the substrate. As a result, conformal polysilicon is formed on the substrate.

Forming either gapfill or conformal polysilicon according to the methods herein enables the process to be conducted at relatively low substrate temperatures. Whereas typical thermal polysilicon deposition processes may be carried out at substrate temperatures of 650°C or more, the substrate temperatures used during formation of HDP polysilicon may be below or about 500°C, below or about 450°C or below or about 400°C in embodiments of the invention. The temperature of the substrate may be controlled in a variety of ways. In FIGS. 1-2 the substrate may be heated to the deposition temperature using the hydrogen plasma. In situations where the plasmas would raise the substrate temperature above these ranges, the back of the substrate may be cooled by a backside flow of helium. Growing polysilicon below about 300°C has been found to grow a mixture of polysilicon and amorphous silicon.

Polysilicon layers formed using high density plasmas may possess compressive stress. Underlying silicon dioxide material (which is present on portions of the underlying substrate, in embodiments) may absorb some of the stress associated with the gapfill polysilicon layer.

Silane is not the only silicon source useful for forming polysilicon. Disilane and higher order silanes would also be able to form these films, as would silanes having one or more double bond between adjacent silicon atoms. Silanes used to form polysilicon are devoid of halogens, in embodiments of the invention, to avoid the incorporation of halogens in the forming film. In general, these silicon sources may be used alone or combined in any combination with one another and referred to collectively as the deposition process gas. Substitutes for some or all hydrogen (H_2) are also available. It has been found that ammonia (NH_3) is a useful source of hydrogen (H) for the pre-deposition treatment operation. Hydrazine (N_2H_4) and other nitrogen-and-hydrogen-containing compounds are also expected to work as inputs to the pre-treatment plasma. In general, these hydrogen sources may be

used alone or combined in any combination with one another and referred to collectively as the pretreatment process gas.

Any of the process gases referred to herein may be combined with inert gases which may assist in stabilizing the high-density plasma or improving the uniformity of the polisyilicon deposition across a substrate. Argon, neon and/or helium are added to these process gases in embodiments of the invention and will be referred to as fluent gases. Fluent gases may be introduced during one or more of the steps to alter (e.g., increase) the plasma density. Increasing the plasma density may help to increase the ionization and dissociation probabilities within the plasma.

A source of dopants may also be included in the deposition process gas in order to incorporate dopants in some polysilicon films, in embodiments of the invention. The nature of the high-density plasma allows the dopants to bond more tightly within the polysilicon films which obviates the requirement for a separate thermal dopant activation step, in embodiments. A boron-containing precursor may be added to the deposition process gas (e.g. TEB, TMB, BH_3, B_2H_6, higher order boranes, ...) in order to put activated boron (B) doping centers in the forming polysilicon layer. Alternatively, activated phosphorus (P) doping centers may be included in the polysilicon layer, in embodiments, by adding a phosphorus-containing precursor (e.g. PH_3 ...) to the deposition process gas.

The source of dopants may also introduce dopants, such as carbon, which are valence isoelectronic with the primary atomic constituent (silicon), in embodiments of the invention. Carbon may be introduced by including a hydrocarbon in the source of dopants. Suitable hydrocarbons include CH_4, C_2H_6, C_2H_4, C_2H_2, C_3H_8, C_3H_6 and so on. The concentration of carbon in carbon-doped polysilicon films may be high, in excess of 10% or 20% in embodiments of the invention.

Exemplary Substrate Processing System

The inventors have implemented embodiments of the invention with the ULTIMA™ system manufactured by APPLIED MATERIALS, INC., of Santa Clara, Calif., a general description of which is provided in commonly assigned U.S. Pat. No. 6,170,428, "SYMMETRIC TUNABLE INDUCTIVELY COUPLED HDP-CVD REACTOR," filed July 15, 1996 by Fred C. Redeker, Farhad Moghadam, Hirogi Hanawa, Tetsuya Ishikawa, Dan Maydan, Shijian Li, Brian Lue, Robert Steger, Yaxin Wang, Manus Wong and Ashok Sinha, the entire disclosure of which is incorporated herein by reference. An overview of the system is

provided in connection with FIGS. 3A and 3B below. FIG. 3A schematically illustrates the structure of such an HDP-CVD system 310 in an embodiment. The system 310 includes a chamber 313, a vacuum system 370, a source plasma system 380A, a substrate bias plasma system 380B, a gas delivery system 333, and a remote plasma cleaning system 350.

The upper portion of chamber 313 includes a dome 314, which is made of a ceramic dielectric material, such as aluminum oxide or aluminum nitride. Dome 314 defines an upper boundary of a plasma processing region 316. Plasma processing region 316 is bounded on the bottom by the upper surface of a substrate 317 and a substrate support member 318.

A heater plate 323 and a cold plate 324 surmount, and are thermally coupled to, dome 314. Heater plate 323 and cold plate 324 allow control of the dome temperature to within about +10° C. over a range of about 100° C. to 200° C. This allows optimizing the dome temperature for the various processes. For example, it may be desirable to maintain the dome at a higher temperature for cleaning or etching processes than for deposition processes. Accurate control of the dome temperature also reduces the flake or particle counts in the chamber and improves adhesion between the deposited layer and the substrate.

The lower portion of chamber 313 includes a body member 322, which joins the chamber to the vacuum system. A base portion 321 of substrate support member 318 is mounted on, and forms a continuous inner surface with, body member 322. Substrates are transferred into and out of chamber 313 by a robot blade (not shown) through an insertion/removal opening (not shown) in the side of chamber 313. Lift pins (not shown) are raised and then lowered under the control of a motor (also not shown) to move the substrate from the robot blade at an upper loading position 357 to a lower processing position 356 in which the substrate is placed on a substrate receiving portion 319 of substrate support member 318. Substrate receiving portion 319 includes an electrostatic chuck 320 that secures the substrate to substrate support member 318 during substrate processing. In a preferred embodiment, substrate support member 318 is made from an aluminum oxide or aluminum ceramic material.

Vacuum system 370 includes throttle body 325, which houses twin-blade throttle valve 326 and is attached to gate valve 327 and turbo-molecular pump 328. It should be noted that throttle body 325 offers minimum obstruction to gas flow, and allows symmetric pumping. Gate valve 327 can isolate pump 328 from throttle body 325, and can also control chamber pressure by restricting the exhaust flow capacity when throttle valve 326 is fully open. The

arrangement of the throttle valve, gate valve, and turbo-molecular pump allow accurate and stable control of chamber pressures up to about 1 mTorr to about 2 Torr.

The source plasma system 380A includes a top coil 329 and side coil 330, mounted on dome 314. A symmetrical ground shield (not shown) reduces electrical coupling between the coils. Top coil 329 is powered by top source RF (SRF) generator 331A, whereas side coil 330 is powered by side SRF generator 331B, allowing independent power levels and frequencies of operation for each coil. This dual coil system allows control of the radial ion density in chamber 313, thereby improving plasma uniformity. Side coil 330 and top coil 329 are typically inductively driven, which does not require a complimentary electrode. In a specific embodiment, the top source RF generator 331A provides up to 5,000 watts of RF power at nominally 2 MHz and the side source RF generator 331B provides up to 7,500 watts of RF power at nominally 2 MHz. The operating frequencies of the top and side RF generators may be offset from the nominal operating frequency (e.g. to 1.7-1.9 MHz and 1.9-2.1 MHz, respectively) to improve plasma-generation efficiency.

A substrate bias plasma system 380B includes a bias RF ("BRF") generator 331C and a bias matching network 332C. The bias plasma system 380B capacitively couples substrate portion 317 to body member 322, which act as complimentary electrodes. The bias plasma system 380B serves to enhance the transport of plasma species (e.g., ions) created by the source plasma system 380A to the surface of the substrate. In a specific embodiment, the substrate bias RF generator provides up to 10,000 watts of RF power at a frequency of about 13.56 MHz.

RF generators 331A and 331B include digitally controlled synthesizers. Each generator includes an RF control circuit (not shown) that measures reflected power from the chamber and coil back to the generator and adjusts the frequency of operation to obtain the lowest reflected power, as understood by a person of ordinary skill in the art. RF generators are typically designed to operate into a load with a characteristic impedance of 50 ohms. RF power may be reflected from loads that have a different characteristic impedance than the generator. This can reduce power transferred to the load. Additionally, power reflected from the load back to the generator may overload and damage the generator. Because the impedance of a plasma may range from less than 5 ohms to over 900 ohms, depending on the plasma ion density, among other factors, and because reflected power may be a function of frequency, adjusting the generator frequency according to the reflected power increases the

power transferred from the RF generator to the plasma and protects the generator. Another way to reduce reflected power and improve efficiency is with a matching network.

Matching networks 332A and 332B match the output impedance of generators 331A and 331B with their respective coils 329 and 330. The RF control circuit may tune both matching networks by changing the value of capacitors within the matching networks to match the generator to the load as the load changes. The RF control circuit may tune a matching network when the power reflected from the load back to the generator exceeds a certain limit. One way to provide a constant match, and effectively disable the RF control circuit from tuning the matching network, is to set the reflected power limit above any expected value of reflected power. This may help stabilize a plasma under some conditions by holding the matching network constant at its most recent condition.

Other measures may also help stabilize a plasma. For example, the RF control circuit can be used to determine the power delivered to the load (plasma) and may increase or decrease the generator output power to keep the delivered power substantially constant during deposition of a layer.

A gas delivery system 333 provides gases from several sources, 334A-334E to a chamber for processing the substrate by way of gas delivery lines 338 (only some of which are shown). As would be understood by a person of skill in the art, the actual sources used for sources 334A-334E and the actual connection of delivery lines 338 to chamber 313 varies depending on the deposition and cleaning processes executed within chamber 313. Gases are introduced into chamber 313 through a gas ring 337 and/or a top nozzle 345. FIG. 3B is a simplified, partial cross-sectional view of chamber 313 showing additional details of gas ring 337.

In one embodiment, first and second gas sources, 334A and 334B, and first and second gas flow controllers, 335A' and 335B', provide gas to ring plenum 336 in gas ring 337 by way of gas delivery lines 338 (only some of which are shown). Gas ring 337 has a plurality of source gas nozzles 339 (only one of which is shown for purposes of illustration) that provide a uniform flow of gas over the substrate. Nozzle length and nozzle angle may be changed to allow tailoring of the uniformity profile and gas utilization efficiency for a particular process within an individual chamber. In a preferred embodiment, gas ring 337 has 12 source gas nozzles made from an aluminum oxide ceramic.

Gas ring 337 also has a plurality of oxidizer gas nozzles 340 (only one of which is shown), which in one embodiment are co-planar with and shorter than source gas nozzles 339, and in

one embodiment receive gas from body plenum 341. In some embodiments it is desirable not to mix source gases and oxidizer gases before injecting the gases into chamber 313. In other embodiments, oxidizer gas and source gas may be mixed prior to injecting the gases into chamber 313 by providing apertures (not shown) between body plenum 341 and gas ring plenum 336. In one embodiment, third, fourth, and fifth gas sources, 334C, 334D, and 334D', and third and fourth gas flow controllers, 335C and 335D', provide gas to body plenum by way of gas delivery lines 338. Additional valves, such as 343B (other valves not shown), may shut off gas from the flow controllers to the chamber. In implementing certain embodiments of the invention, source 334A comprises a silane SiH_4 source, source 334B comprises a molecular nitrogen N_2 source, source 334C comprises a TSA source, source 334D comprises an argon Ar source, and source 334D' comprises a disilane Si_2H_6 source.

In embodiments where flammable, toxic, or corrosive gases are used, it may be desirable to eliminate gas remaining in the gas delivery lines after a deposition. This may be accomplished using a 3-way valve, such as valve 343B, to isolate chamber 313 from delivery line 338A and to vent delivery line 338A to vacuum foreline 344, for example. As shown in FIG. 3A, other similar valves, such as 343A and 343C, may be incorporated on other gas delivery lines. Such three-way valves may be placed as close to chamber 313 as practical, to minimize the volume of the unvented gas delivery line (between the three-way valve and the chamber). Additionally, two-way (on-off) valves (not shown) may be placed between a mass flow controller ("MFC") and the chamber or between a gas source and an MFC.

Referring again to FIG. 3A, chamber 313 also has top nozzle 345 and top vent 346. Top nozzle 345 and top vent 346 allow independent control of top and side flows of the gases, which improves film uniformity and allows fine adjustment of the film's deposition and doping parameters. Top vent 346 is an annular opening around top nozzle 345. In one embodiment, first gas source 334A supplies source gas nozzles 339 and top nozzle 345. Source nozzle MFC 335A' controls the amount of gas delivered to source gas nozzles 339 and top nozzle MFC 335A controls the amount of gas delivered to top gas nozzle 345. Similarly, two MFCs 335B and 335B' may be used to control the flow of oxygen to both top vent 346 and oxidizer gas nozzles 340 from a single source of oxygen, such as source 334B. In some embodiments, oxygen is not supplied to the chamber from any side nozzles. The gases supplied to top nozzle 345 and top vent 346 may be kept separate prior to flowing the gases into chamber 313, or the gases may be mixed in top plenum 348 before they flow into chamber 313. Separate sources of the same gas may be used to supply various portions of the chamber.

A remote microwave-generated plasma cleaning system 350 is provided to periodically clean deposition residues from chamber components. The cleaning system includes a remote microwave generator 351 that creates a plasma from a cleaning gas source 334E (e.g., molecular fluorine, nitrogen trifluoride, other fluorocarbons or equivalents) in reactor cavity 353. The reactive species resulting from this plasma are conveyed to chamber 313 through cleaning gas feed port 354 by way of applicator tube 355. The materials used to contain the cleaning plasma (e.g., cavity 353 and applicator tube 355) must be resistant to attack by the plasma. The distance between reactor cavity 353 and feed port 354 should be kept as short as practical, since the concentration of desirable plasma species may decline with distance from reactor cavity 353. Generating the cleaning plasma in a remote cavity allows the use of an efficient microwave generator and does not subject chamber components to the temperature, radiation, or bombardment of the glow discharge that may be present in a plasma formed in situ. Consequently, relatively sensitive components, such as electrostatic chuck 320, do not need to be covered with a dummy wafer or otherwise protected, as may be required with an in situ plasma cleaning process. In FIG. 3A, the plasma-cleaning system 350 is shown disposed above the chamber 313, although other positions may alternatively be used.

A baffle 361 may be provided proximate the top nozzle to direct flows of source gases supplied through the top nozzle into the chamber and to direct flows of remotely generated plasma. Source gases provided through top nozzle 345 are directed through a central passage 362 into the chamber, while remotely generated plasma species provided through the cleaning gas feed port 354 are directed to the sides of the chamber by the baffle 361.

Seasoning the interior of the substrate processing region has been found to improve many high-density plasma deposition processes. The formation of polysilicon is no exception. Seasoning involves the deposition of silicon oxide on the chamber interior before a deposition substrate is introduced into the substrate processing region. In embodiments, seasoning the interior of the substrate processing region comprises forming a high density plasma in the substrate processing region from a seasoning process gas comprising an oxygen source and a silicon source. The oxygen source may be diatomic oxygen (O_2) and the silicon source may be silane (SiH_4), though other precursors may also suffice.

Comparative tests are run to measure the amount of stress in polycrystalline silicon films deposited in gaps with and without a silicon dioxide liner layer. The bulk gap-fill polysilicon layers are deposited in gaps formed on 300 mm diameter substrate wafers placed in an Ultima HDP processing chamber made by Applied Materials, Inc. of Santa Clara, CA. The substrate

was maintained at 350° C during HDP-CVD deposition and the total source plasma RF power applied can be 10.6 Watts/cm^2 (7500 Watts) excluding bias power. The lining layer is grown with a substrate bias power of about 5.0 Watts/cm^2 (3500 Watts). Bias power in the range 3.5-10.0 Watts/cm^2 (2500-7000 Watts over a 300 mm diameter wafer) was applied to the substrate during growth of the polycrystalline silicon of the bulk gap-fill layer. The thickness of the lining layer can be about 200 Å and 500 Å, respectively. The thickness of the bulk gap-fill layer can be about 2.0 μm.

Those of ordinary skill in the art will realize that processing parameters can vary for different processing chambers and different processing conditions, and that different precursors can be used without departing from the spirit of the invention. Appropriate silicon containing precursors may include trisilylamine (TSA, $(SiH_3)_3N$) and disilane (Si_2H_6) in addition to silane. Other variations will also be apparent to persons of skill in the art. These equivalents and alternatives are intended to be included within the scope of the present invention. Therefore, the scope of this invention should not be limited to the embodiments described, but should instead be defined by the following claims.

The term "trench" is used throughout with no implication that the etched geometry has a large horizontal aspect ratio. Viewed from above the surface, trenches may appear circular, oval, polygonal, rectangular, or a variety of other shapes. The term “via” is used to refer to a low aspect ratio trench which may or may not be filled with metal to form a vertical electrical connection. As used herein, a conformal layer refers to a generally uniform layer of material on a surface in the same shape as the surface, i.e., the surface of the layer and the surface being covered are generally parallel. A person having ordinary skill in the art will recognize that the deposited material likely cannot be 100% conformal and thus the term "generally" allows for acceptable tolerances.

Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of the invention.

Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Each smaller range between any

stated value or intervening value in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of these smaller ranges may independently be included or excluded in the range, and each range where either, neither or both limits are included in the smaller ranges is also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

As used herein and in the appended claims, the singular forms "a", "an", and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a process" includes a plurality of such processes and reference to "the precursor" includes reference to one or more precursor and equivalents thereof known to those skilled in the art, and so forth.

Also, the words "comprise," "comprising," "include," "including," and "includes" when used in this specification and in the following claims are intended to specify the presence of stated features, integers, components, or steps, but they do not preclude the presence or addition of one or more other features, integers, components, steps, acts, or groups.

WHAT IS CLAIMED IS:

1. A method of depositing a polysilicon layer in a trench of a patterned substrate in a substrate processing region of a substrate processing chamber, the method comprising:

transferring the patterned substrate into the substrate processing region;

growing the polysilicon layer on the patterned substrate by forming a high density plasma in the substrate processing region from a deposition process gas comprising a silicon source while maintaining a mean pressure within the substrate processing region of about 20 mTorr or less and maintaining a mean patterned substrate temperature of 500°C or less;

removing the patterned substrate from the substrate processing region.

2. The method of claim 1, further comprising pretreating the patterned substrate in a high density plasma in the substrate processing region from a pretreatment process gas comprising a hydrogen source before growing the polysilicon layer on the patterned substrate.

3. The method of claim 1, wherein essentially no bias is applied between the patterned substrate and the high density plasma while growing the polysilicon layer such that the polysilicon layer is essentially conformal.

4. The method of claim 3, wherein a growth rate of the polysilicon layer is below about 500 Å/minute.

5. The method of claim 3, wherein a horizontal growth rate of the polysilicon layer as measured on a wall of the trench is between about 50% and 100% of a vertical growth rate on a surface around the opening of the trench.

6. The method of claim 1, wherein a plasma bias power is applied between the patterned substrate and the high density plasma while growing the polysilicon layer such that the trench fills with polysilicon.

7. The method of claim 1, wherein the silicon source is silane.

8. The method of claim 1, wherein the process gas further comprises a fluent gas selected from argon, neon, and helium flowed with a fourth flow rate during the growth of at least one of the two layers.

9. The method of claim 1, wherein the mean patterned substrate temperature is less than or about 400° C.

10. The method of claim 1, wherein the process gas further comprises a doping source which provides a dopant to the polysilicon layer during growth, wherein the dopant is already activated following formation of the polysilicon layer and no separate dopant activation operation is necessary.

11. The method of claim 1, wherein the process gas further comprises a source of phosphorous or boron.

12. The method of claim 1, wherein the process gas comprises PH_3 flowed at a fourth gas flow rate.

13. The method of claim 1, wherein a deposition-to-sputter ratio during growth of the polysilicon layer is between about 2:1 and 6:1.

14. The method of claim 1, wherein the interior of the substrate processing region is seasoned with silicon oxide prior to the operation of transferring the patterned substrate into the substrate processing region.

15. The method of claim 14, wherein seasoning the interior of the substrate processing region comprises forming a high density plasma in the substrate processing region from a seasoning process gas comprising an oxygen source and a silicon source.

16. The method of claim 15, wherein the oxygen source is diatomic oxygen (O_2) and the silicon source is silane (SiH_4).

17. The method of claim 1, wherein the process gas further comprises a source of carbon and the polysilicon layer is a carbon-doped polysilicon layer.

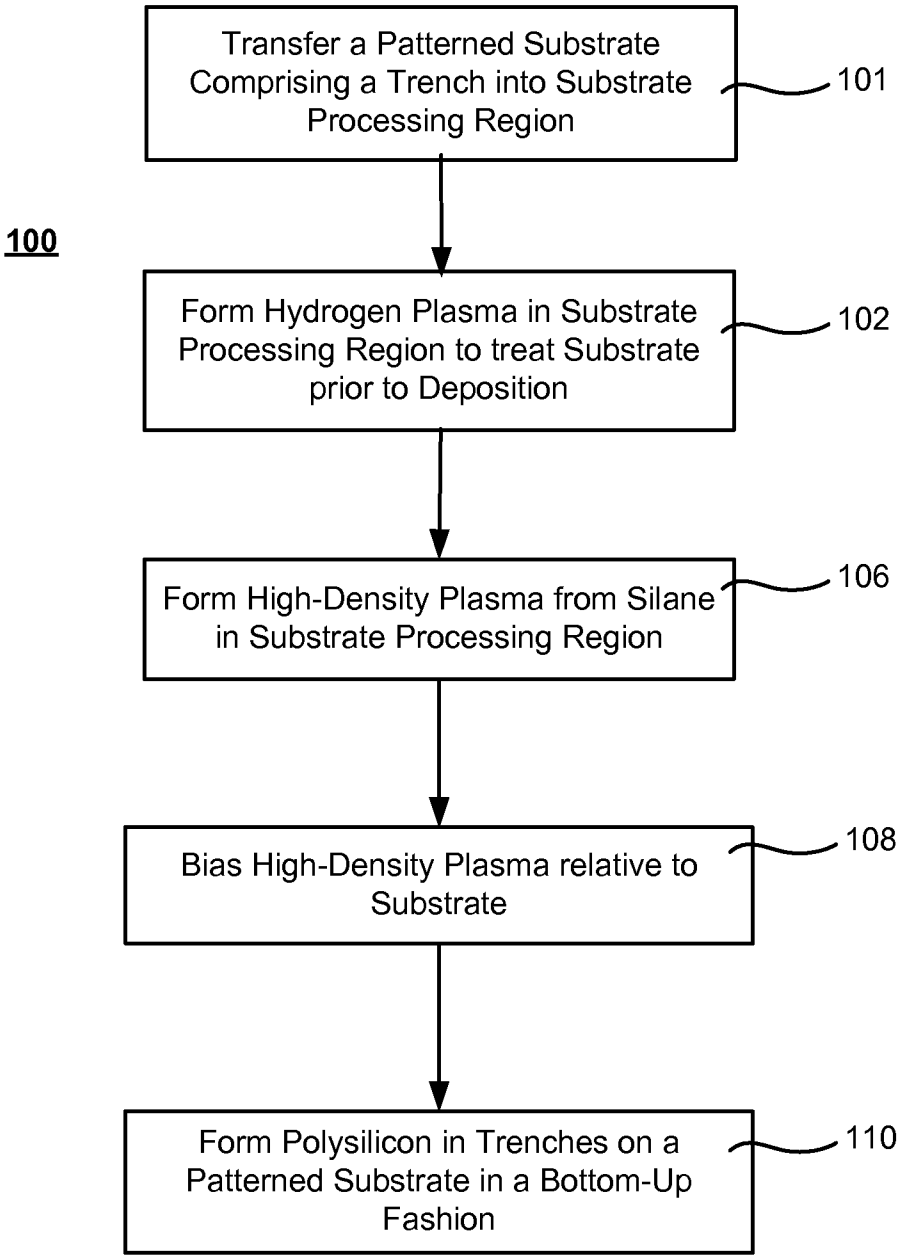

100
Transfer a Patterned Substrate Comprising a Trench into Substrate Processing Region
101
Form Hydrogen Plasma in Substrate Processing Region to treat Substrate prior to Deposition
102
Form High-Density Plasma from Silane in Substrate Processing Region
106
Bias High-Density Plasma relative to Substrate
108
Form Polysilicon in Trenches on a Patterned Substrate in a Bottom-Up Fashion
110

FIG. 1

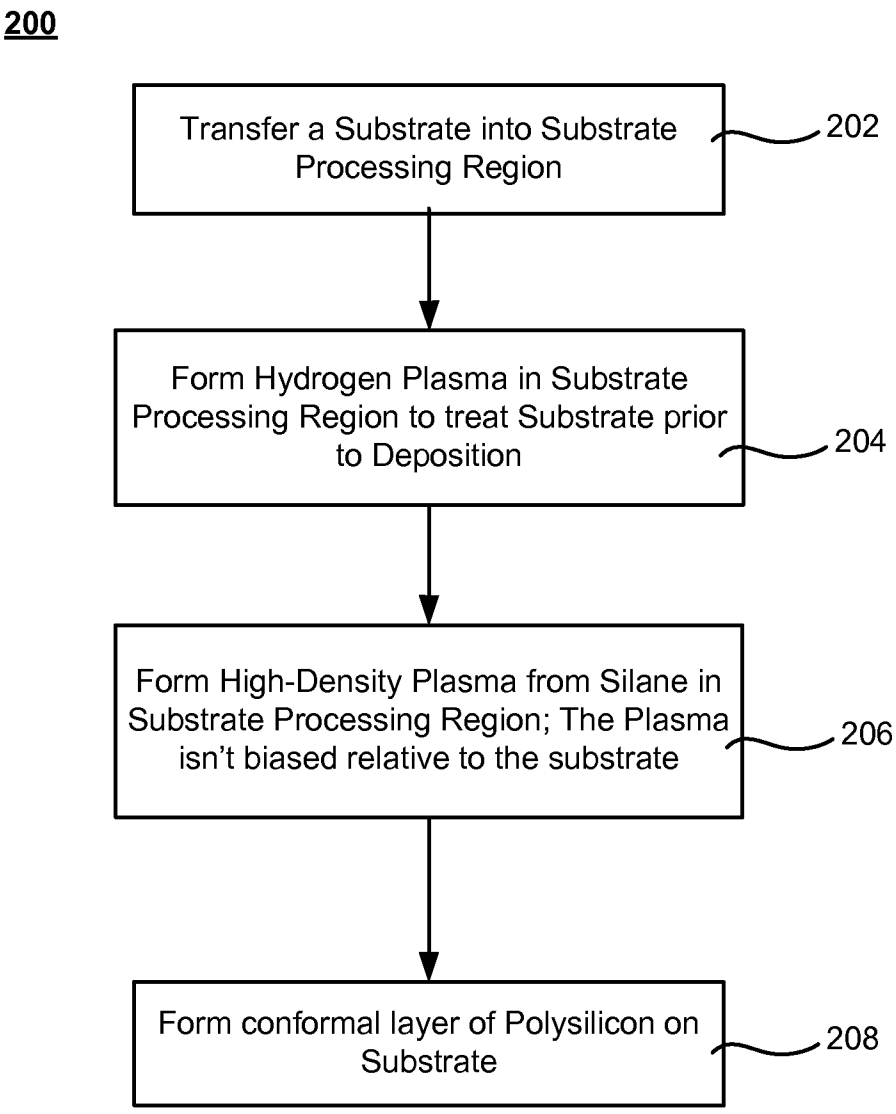
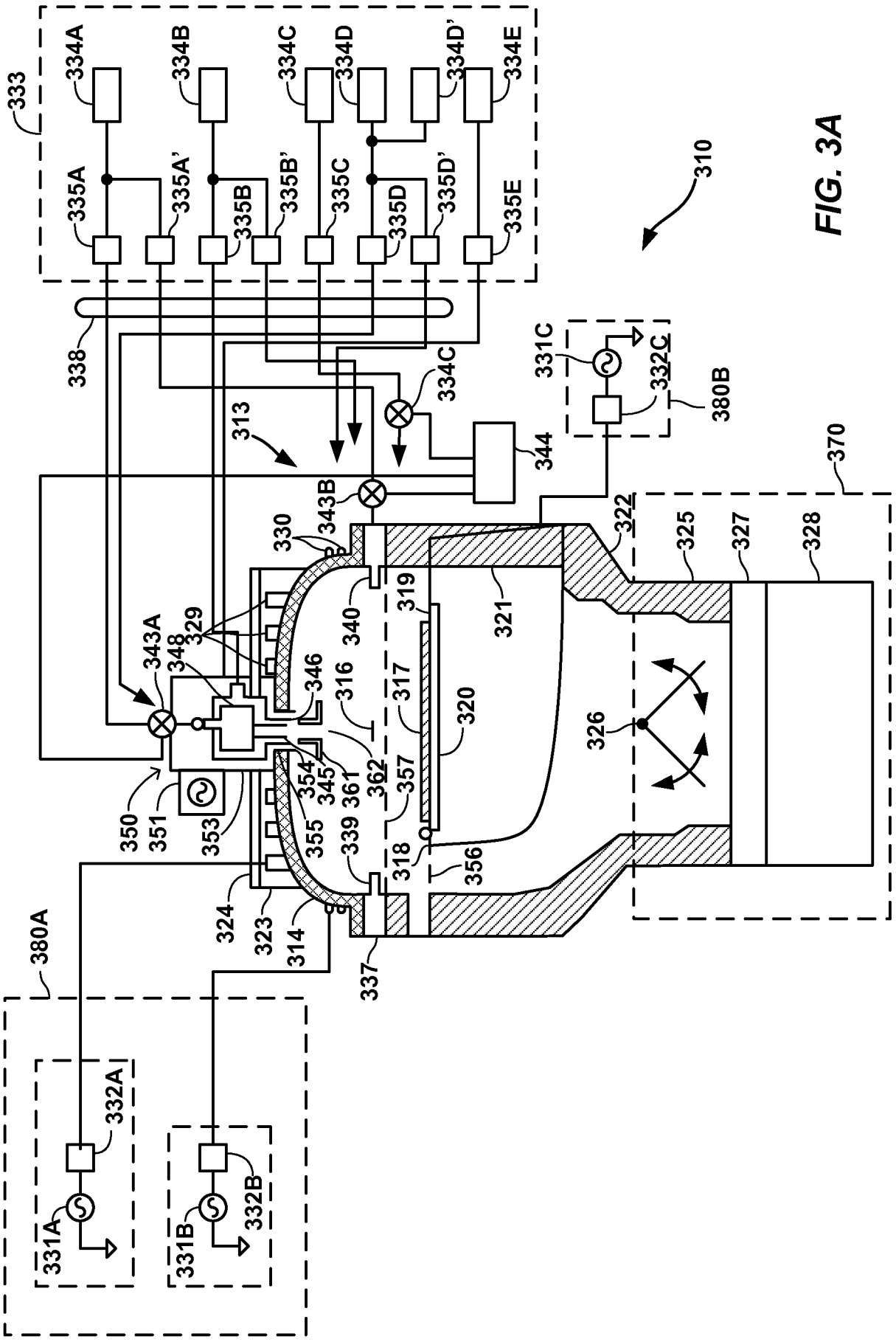

200
Transfer a Substrate into Substrate Processing Region
202
Form Hydrogen Plasma in Substrate Processing Region to treat Substrate prior to Deposition
204
Form High-Density Plasma from Silane in Substrate Processing Region; The Plasma isn't biased relative to the substrate
206
Form conformal layer of Polysilicon on Substrate
208

FIG. 2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334A
334B
334C
334D
334D'
334E
335A
335A'
335B
335B'
335C
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335D'
335E
338
313
310
331C
332C
380B
334C
344
370
343B
330
322
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343A
348
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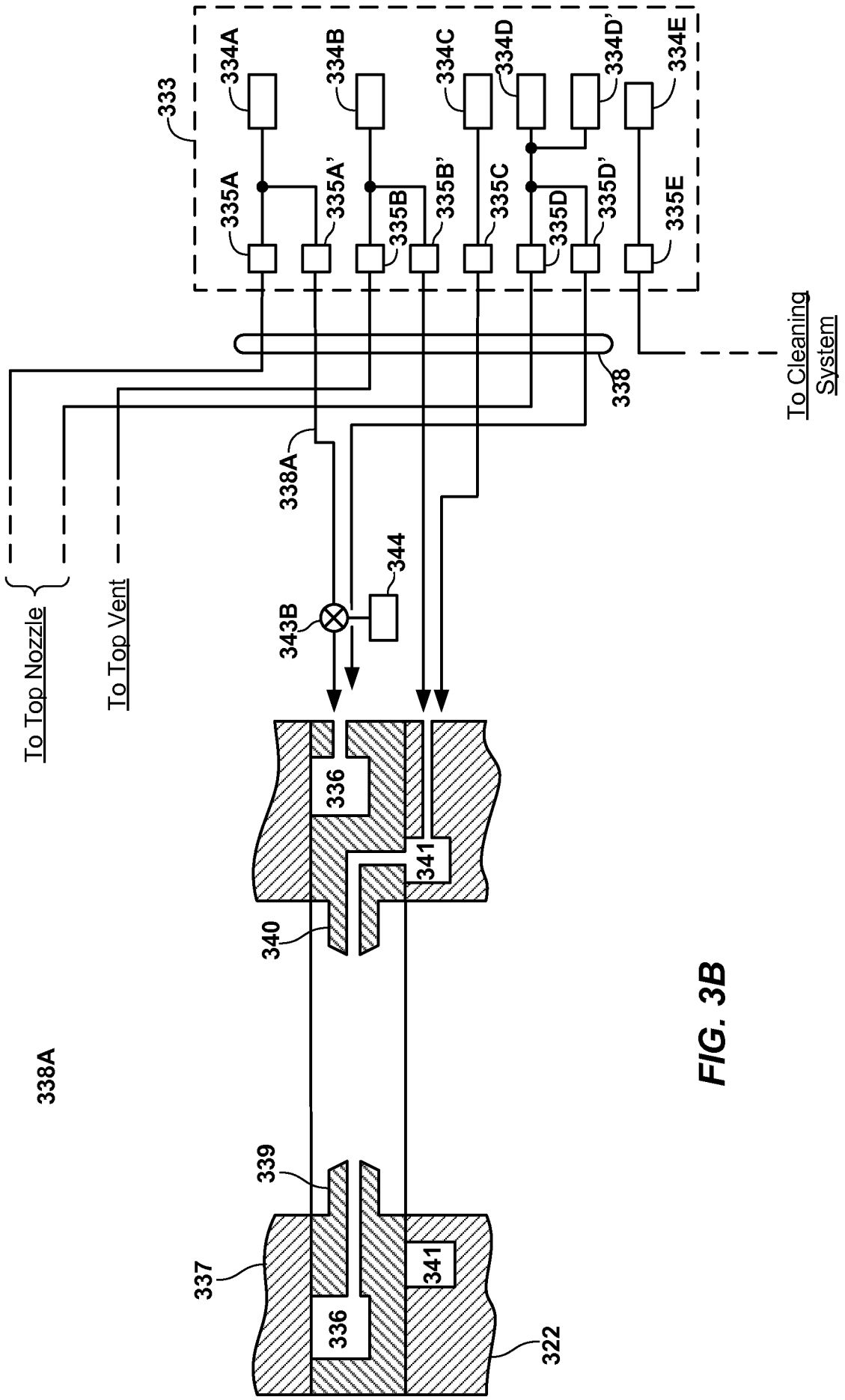
337
380A
331A
332A
331B
332B

FIG. 3A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334A
334B
334C
334D
334D'
334E
335A
335A'
335B
335B'
335C
335D
335D'
335E
338
To Cleaning System
338A
To Top Nozzle
To Top Vent
343B
344
336
341
340
339
337
322

FIG. 3B