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(71) Applicant *(for all designated States except US)*: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **HESTER, Richard, K.** [US/US]; 5811 Woodcreek Circle, Mckinney, TX 75071 (US).

(74) Agents: **FRANZ, Warren, L.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

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(54) **Title**: REDUCING RIPPLE CURRENT IN A SWITCHED-MODE POWER CONVERTER EMPLOYING A BRIDGE TOPOLOGY

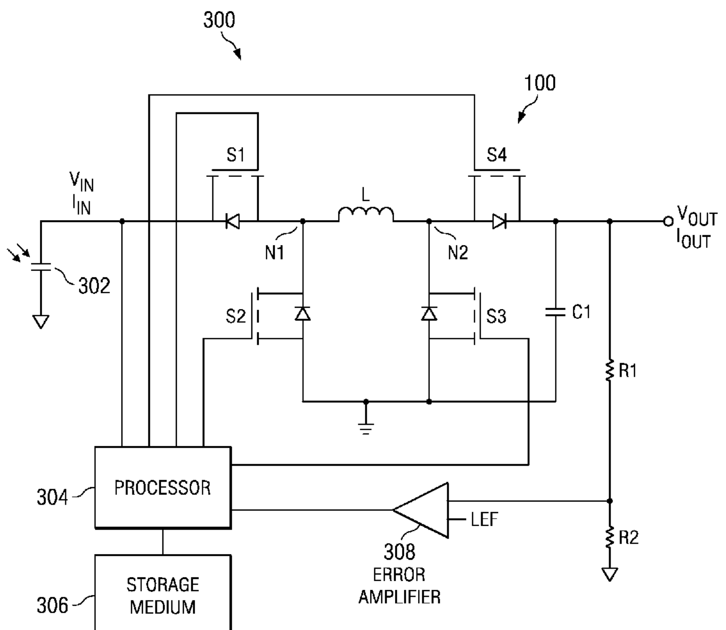

FIG. 3

(57) **Abstract**: A buck-boost switching regulator (bridge 100, including switches S1-S4, and capacitor C1) is adapted to operate in a buck mode, boost mode, and bridge mode. Control circuitry (voltage divider R1, R2, error amplifier 308, processor 304, and storage medium 306) is coupled to input/output terminals of the switching regulator. The control circuitry measures input/output voltages or currents and generates pulse width modulation (PWM) or control signals for switches S1 - S4 to adjust phase relationships between corresponding boost switches and buck switching in bridge mode to reduce ripple current in the buck-boost switching regulator.

WO 2012/030952 A2

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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REDUCING RIPPLE CURRENT IN A SWITCHED-MODE POWER CONVERTER EMPLOYING A BRIDGE TOPOLOGY

[0001] The invention relates generally to power converters and, more particularly, to power converters using a bridge topology.

BACKGROUND

[0002] There are a number of applications that may need a switching regulator or switched mode power supply to operate in non-inverting buck or boost modes, transitioning relatively seamlessly between the two. Turning to FIG. 1, an example of a bridge 100, which can operate in boost and buck modes can be seen. This bridge 100 is generally an H-bridge, using switches S1 to S4, and an inductor L, which is coupled between the switching nodes of the H-bridge. In buck mode, switches S4 and S3 are closed and open, respectively, while pulse width modulation (PWM) signals are provided to switches S1 and S2. Alternatively, in boost mode, switches S1 and S2 are closed and open, respectively, while PWM signals are provided to switches S3 and S4.

[0003] The most inefficient mode of operation, however, is a bridge mode or buck-boost mode, where two of the switches S1 to S4 are closed to generate an inductor voltage V_L. Some reasons for the inefficiency are that switching losses are incurred in all four of switches S1 to S4 and that this mode results in a high average inductor current I_L. Also contributing to the inefficiency is the rippled current (or variations in the inductor current I_L). As can be seen in FIG. 2, switches S1 and S3 are, for example, closed at the same time, and the inductor current I_L varies between the periods in which both switches S1 and S3 are close or open, namely between times t1 to t2 and times t3 to t4.

[0004] Some other conventional circuits are described in U.S. Patent Nos. 6,166,527 and 6,037,755 and in U.S. Patent Publ. No. 2009/0039852.

SUMMARY

[0005] An example embodiment of the invention, accordingly, provides an apparatus. The apparatus comprises a buck-boost switching regulator having buck switches, boost switches, an input terminal, and an output terminal, wherein the buck-boost switching regulator is adapted to operate in a buck mode, boost mode, and bridge mode; and control circuitry that is coupled to at least one of the output terminal and the input terminal and that controls the buck-boost switching regulator with control signals, and wherein the control circuitry adjusts phase relationships between corresponding boost switches and buck switching in bridge mode to reduce ripple current in the buck-boost switching regulator.

[0006] In accordance with an example embodiment of the invention, the buck-boost switching regulator further comprises: a first switch that is coupled between the input terminal and a first switching node; a second switching that is coupled between the first switching node and ground; an inductor that is coupled between the first switching node and a second switching node; a third switch that is coupled between the second switching node and ground; and a fourth switching that is coupled between the second switching node and the output terminal.

[0007] In accordance with an example embodiment of the invention, the control circuitry provides a first, second, third, and fourth control signals for the first, second, third, and fourth switches, respectively.

[0008] In accordance with an example embodiment of the invention, the control circuitry adjusts the third control signal to have an on-time for the third switch that is centered to an off-time for the first switch.

[0009] In accordance with an example embodiment of the invention, the control circuitry adjusts the second control signal to have an on-time for the second switch that is centered to an off-time for the fourth switch.

[0010] In accordance with an example embodiment of the invention, the control circuitry further comprises: a voltage divider that is coupled to the output terminal; and an error amplifier that receives a reference voltage and that is coupled to the voltage divider and the processor.

[0011] In accordance with an example embodiment of the invention, the processor is a digital signal processor (DSP).

[0012] In accordance with an example embodiment of the invention, a method is provided. The method comprises detecting at least one of an input voltage, an output voltage, an input current, and an output current of a buck-boost switching regulator having buck switches, boost switches, an input terminal, and an output terminal, wherein the buck-boost switching regulator is adapted to operate in a buck mode, boost mode, and bridge mode; and operating the buck-boost switching regulator in a bridge mode, wherein phase relationships between corresponding boost switches and buck switching are adjusted to reduce ripple current in the buck-boost switching regulator.

[0013] In accordance with an example embodiment of the invention, the buck-boost switching regulator further comprises: a first switch that is coupled between the input terminal and a first switching node, wherein the first switch receives a first control signal; a second switching that is coupled between the first switching node and ground, wherein the second switch receives a second control signal; an inductor that is coupled between the first switching node and a second switching node; a third switch that is coupled between the second switching node and ground, wherein the third switch receives a third control signal; and a fourth switching that is coupled between the second switching node and the output terminal, wherein the fourth switch receives a fourth control signal.

[0014] In accordance with an example embodiment of the invention, the step of operating further comprises adjusting the third control signal to have an on-time for the third switch that is centered to an off-time for the first switch.

[0015] In accordance with an example embodiment of the invention, the step of operating further comprises adjusting the second control signal to have an on-time for the second switch that is centered to an off-time for the fourth switch.

[0016] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a solar cell; a buck-boost switching regulator having buck switches, boost switches, an input terminal, and an output terminal, wherein the buck-boost switching regulator is adapted to operate in a buck mode, boost mode, and bridge mode, wherein the input terminal is coupled to the solar cell; and control circuitry that is coupled to at least one of the output terminal and the input terminal and that controls the buck-boost switching regulator with control signals, and wherein the control circuitry adjusts phase relationships between corresponding boost switches and buck switching in bridge mode to reduce ripple current in the buck-boost switching regulator.

[0017] In accordance with an example embodiment of the invention, the solar cell further comprises a plurality of solar cells.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Example embodiments are described with reference to accompanying drawings, wherein:

FIG. 1 is a circuit diagram of a conventional bridge;

FIG. 2 is a timing diagram illustrating the relationship between bridge control signals and inductor ripple current for FIG. 1; and

FIG. 3 is an example of a system in accordance with an example embodiment of the invention; and

FIG. 4 is a timing diagram illustrating the relationship between bridge control signals and inductor ripple current for FIG. 3.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0019] FIG. 3 illustrates a system 300 in accordance with an example embodiment of the invention can be seen. System 100 generally comprises a bridge 100, solar cell 302, capacitor C1, voltage divider (resistors R1 and R2), error amplifier 308, processor 304, and storage medium 306. Collectively, the voltage divider, error amplifier 308, processor 304, and storage medium 306 generally operate as a control circuitry, while bridge 100 and capacitor C1 generally operate as a buck-boost switching regulator. In operation, an input voltage V_{IN} and input current I_{IN} are provide to the input terminal of the switching regulator from, for example, a solar cell 302 (which may include multiple solar cells coupled in series or parallel to the input terminal) so as to generate an output voltage V_{OUT} and an output current I_{OUT} at the output terminal. The control circuitry measures the output voltage V_{OUT} and the input voltage V_{IN} and generates the appropriate pulse width modulation (PWM) or control signals for switches S1 through S4. The error amplifier 308 compares an output from the voltage divider to a reference voltage REF so that the processor 304 can perform correction of the PWM signals. In an alternative arrangement, the error amplifier 308 and voltage divider can be removed, with the functionality being provided by the processor 304. In other alternative arrangements, input current I_{IN}, output current I_{OUT}, or input voltage V_{IN} may be used instead of the output voltage V_{OUT} for correction of the PWM signals. Additionally, the processor 304 may be a digital signal processor or DSP.

[0020] For conventional bridge switching or buck-boost operation modes, pairs of switches S1/S3 or S2/S4 are switched on and off at about the same time. As can be seen in FIG. 4, adjustment of the phase relationship between correspond buck switches (S1 or S2) and boost switches (S3 or S4) can result in a substantially reduced ripple in the inductor current I_L. Specifically, FIG. 4 shows that the on-time for switch S3 is centered at the off-time for switch S1, regardless of the on-time pulse width for switch S3. This same adjustment can also be made for the phase relationship between switches S2 and S4. As a result, with this phase relationship adjustment by processor 304, the inductor current I_L is relatively constant, reducing losses during a bridge or buck-boost mode.

[0021] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments and that other embodiments may be implemented within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a buck-boost switching regulator having buck switches, boost switches, an input terminal, and an output terminal, wherein the buck-boost switching regulator is adapted to operate in a buck mode, boost mode, and bridge mode; and

control circuitry that is coupled to at least one of the output terminal and the input terminal and that controls the buck-boost switching regulator with control signals;

wherein the control circuitry adjusts phase relationships between corresponding boost switches and buck switching in bridge mode to reduce ripple current in the buck-boost switching regulator.

2. The apparatus of claim 1, wherein the buck-boost switching regulator further comprises:

a first switch that is coupled between the input terminal and a first switching node;

a second switch that is coupled between the first switching node and ground;

an inductor that is coupled between the first switching node and a second switching node;

a third switch that is coupled between the second switching node and ground; and

a fourth switch that is coupled between the second switching node and the output terminal.

3. The apparatus of claim 2, wherein the control circuitry provides first, second, third, and fourth control signals for the first, second, third, and fourth switches, respectively.

4. The apparatus of claim 3, wherein the control circuitry adjusts the third control signal to have an on-time for the third switch that is centered to an off-time for the first switch.

5. The apparatus of claim 3, wherein the control circuitry adjusts the second control signal to have an on-time for the second switch that is centered to an off-time for the fourth switch.

6. The apparatus of claim 3, wherein the control circuitry further comprises:

a voltage divider that is coupled to the output terminal; and

an error amplifier that receives a reference voltage and that is coupled to the voltage divider and the processor.

7. The apparatus of claim 1, further comprising a solar cell coupled to the input terminal of the buck-boost switching regulator.

8. A method comprising:

detecting at least one of an input voltage, an output voltage, an input current, and an output current of a buck-boost switching regulator having buck switches, boost switches, an input terminal, and an output terminal, wherein the buck-boost switching regulator is adapted to operate in a buck mode, boost mode, and bridge mode; and

operating the buck-boost switching regulator in a bridge mode, wherein phase relationships between corresponding boost switches and buck switching are adjusted to reduce ripple current in the buck-boost switching regulator.

9. The method of Claim 8, wherein the buck-boost switching regulator further comprises:

a first switch that is coupled between the input terminal and a first switching node, wherein the first switch receives a first control signal;

a second switch that is coupled between the first switching node and ground, wherein the second switch receives a second control signal;

an inductor that is coupled between the first switching node and a second switching node;

a third switch that is coupled between the second switching node and ground, wherein the third switch receives a third control signal; and

a fourth switch that is coupled between the second switching node and the output terminal, wherein the fourth switch receives a fourth control signal.

10. The method of Claim 9, wherein the step of operating further comprises adjusting the third control signal to have an on-time for the third switch that is centered to an off-time for the first switch.

11. The method of Claim 9, wherein the step of operating further comprises adjusting the second control signal to have an on-time for the second switch that is centered to an off-time for the fourth switch.

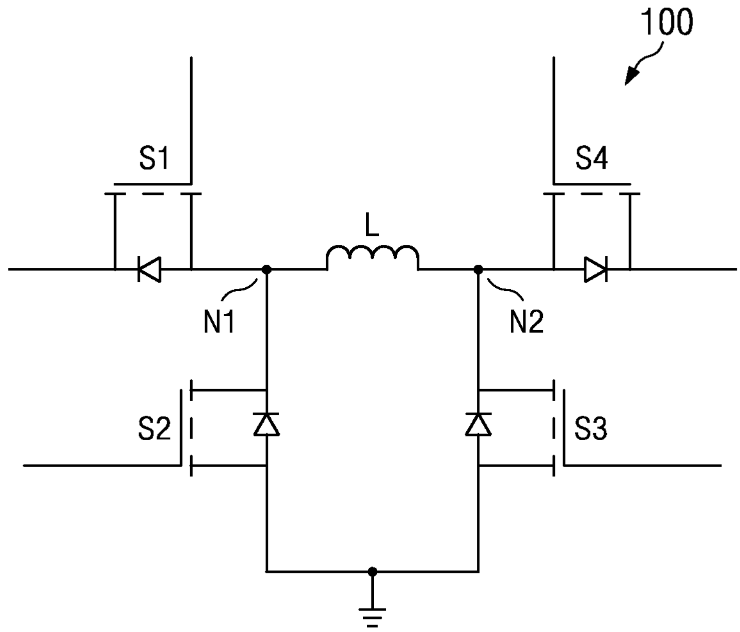

FIG. 1
(PRIOR ART)

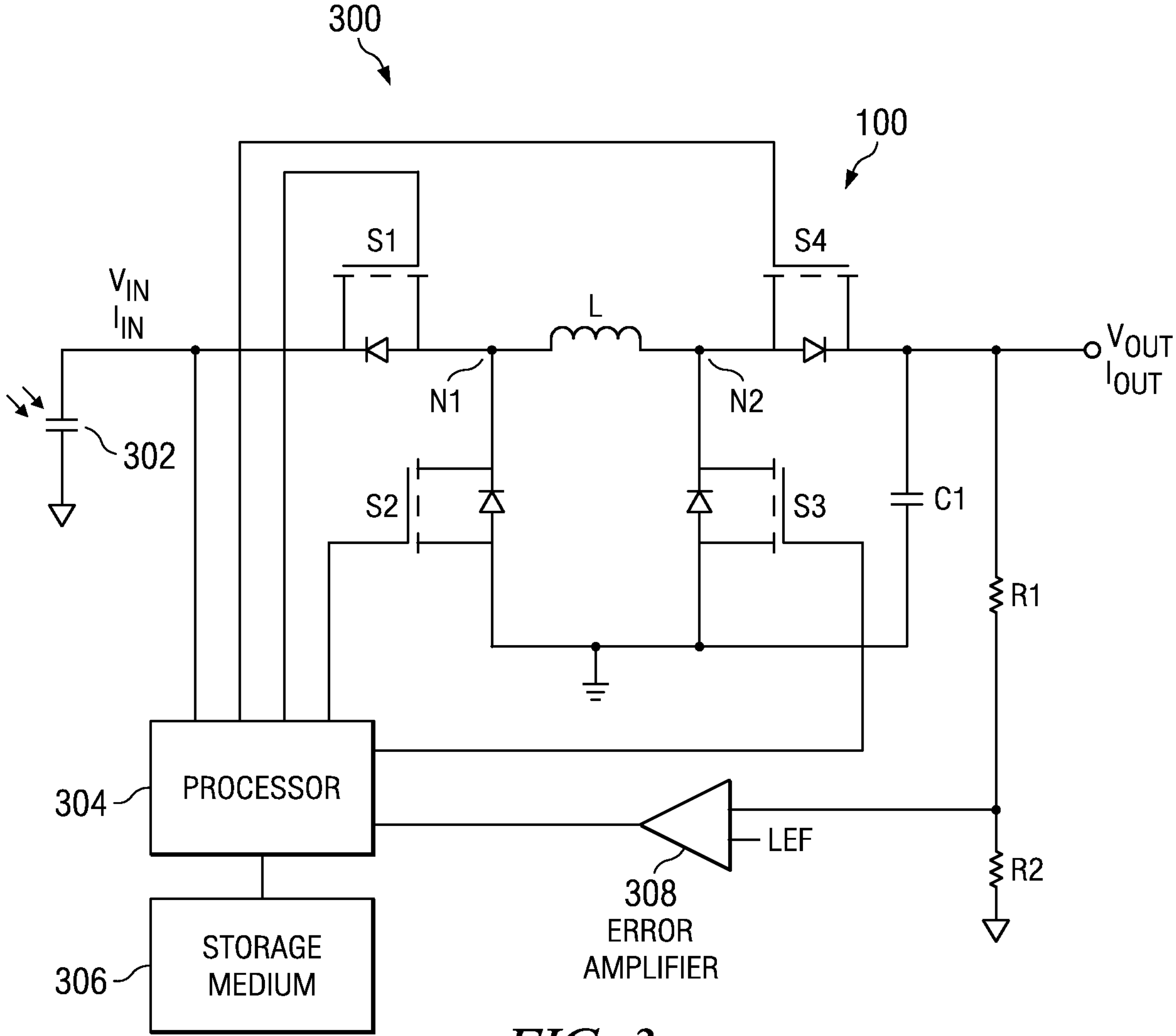

FIG. 3

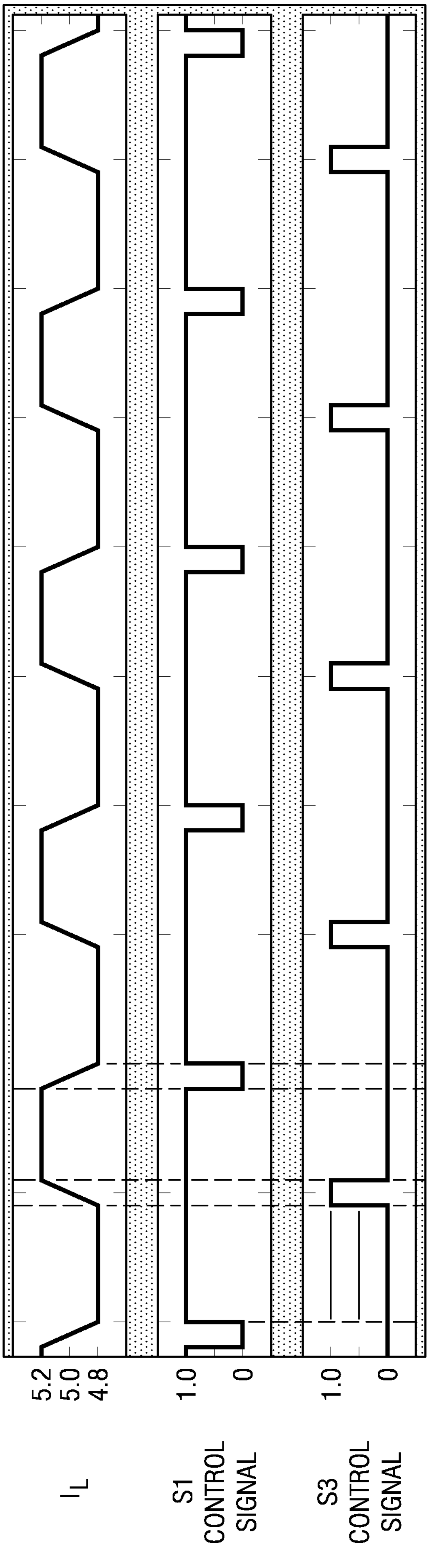

FIG. 2
(PRIOR ART)

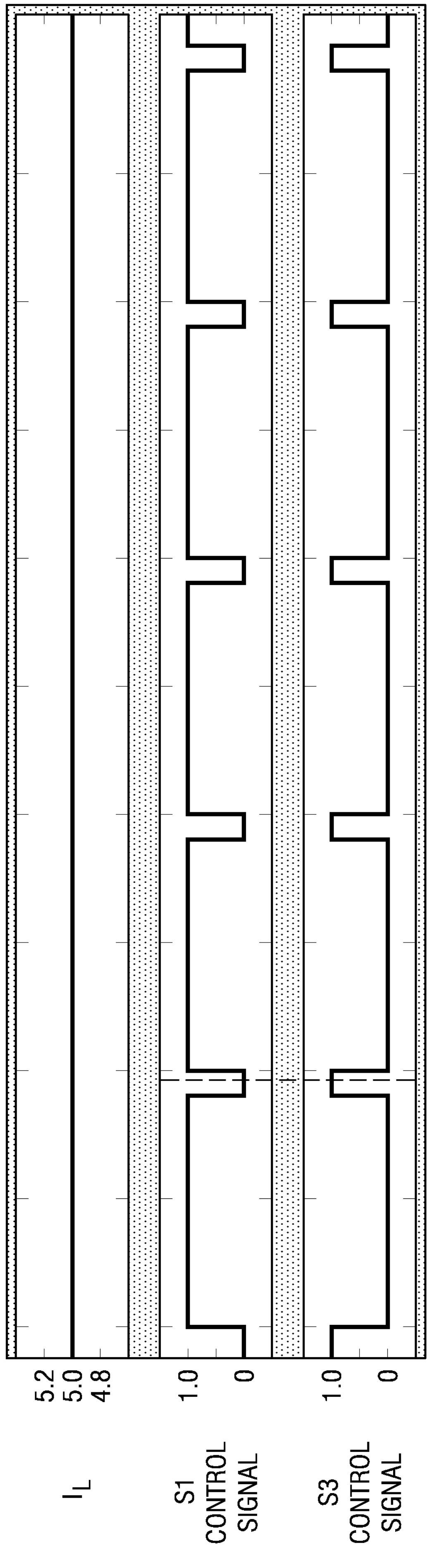

FIG. 4