United States Patent [19]

Odom

[11] **3,806,872**

[45] **Apr. 23, 1974**

[54] **ADDRESS INTERRUPT AND CURRENT STATUS DISPLAY**

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[73] Assignee: **Avco Corporation,** Huntsville, Ala.

[22] Filed: **May 10, 1973**

[21] Appl. No.: **358,862**

[52] **U.S. Cl.**..... **340/147 R,** 340/409, 340/167 A
[51] **Int. Cl.**..... **H04q 9/00,** G08b 29/00
[58] **Field of Search**..... 340/152 T, 147 R, 163, 340/167 A, 167 R, 409

[56] **References Cited**

UNITED STATES PATENTS

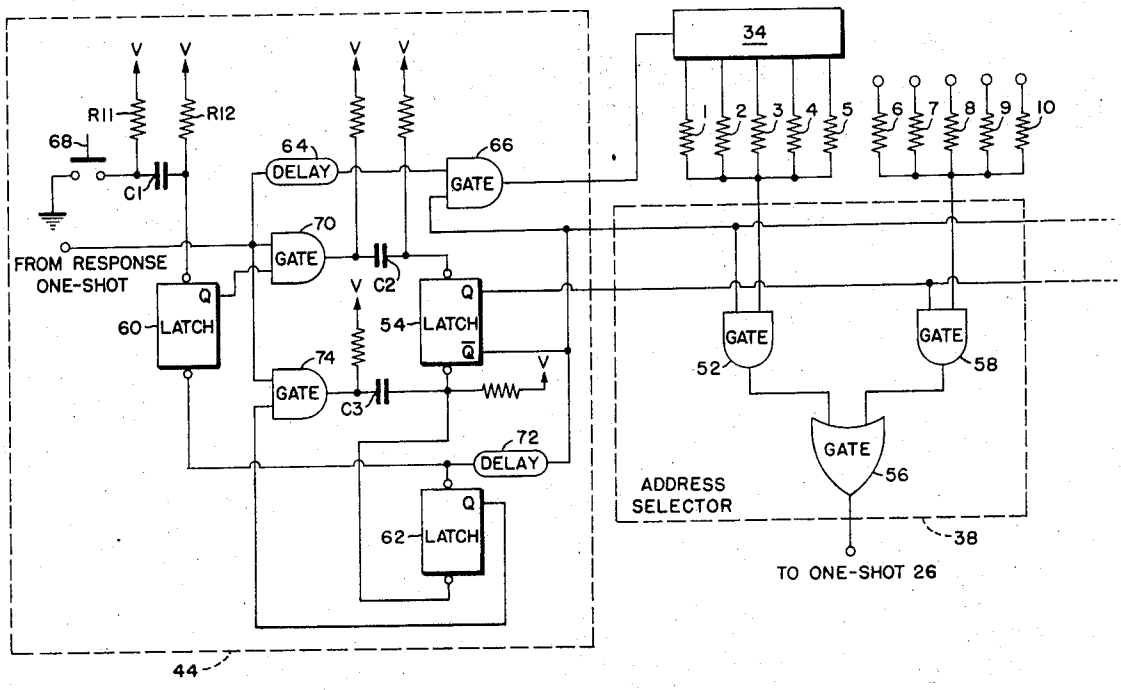
3,559,177	9/1968	Benson	340/163
3,634,824	1/1972	Zinn	340/147 R
3,689,887	9/1972	La Falce et al.	340/163

Primary Examiner—Donald J. Yusko
Attorney, Agent, or Firm—Charles M. Hogan; Irwin P. Garfinkle

[57] **ABSTRACT**

A signaling system located at a central station sequentially interrogates a plurality of remotely located transponders. Means are provided for interrupting the normal addressing sequence and for interrogating any particular remote station, and for then displaying the current status of such station.

12 Claims, 7 Drawing Figures



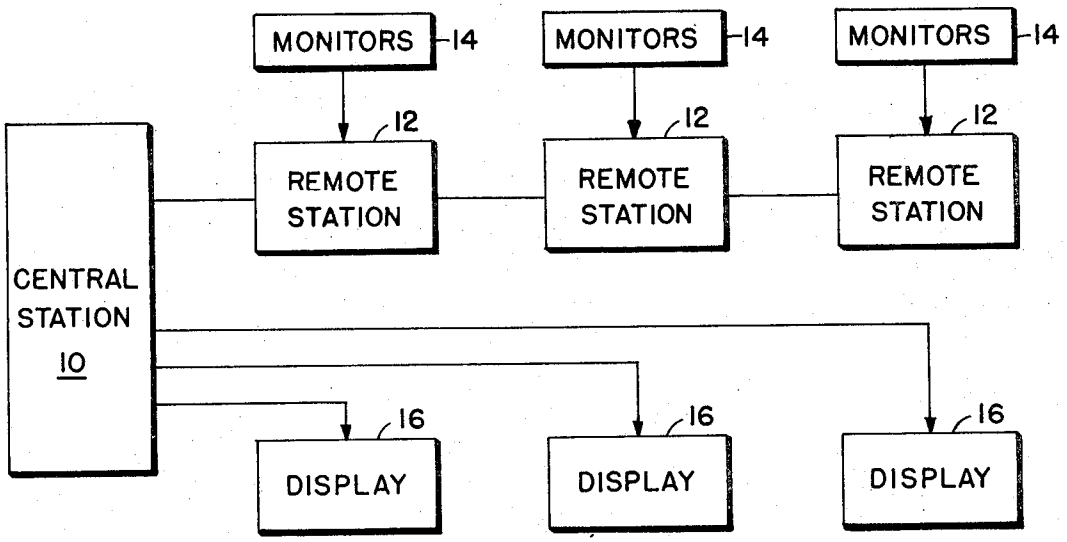


Fig 1

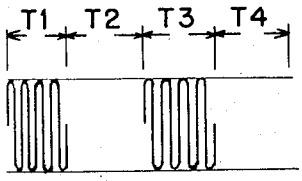


Fig 2

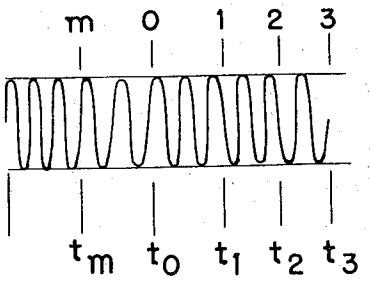


Fig 3

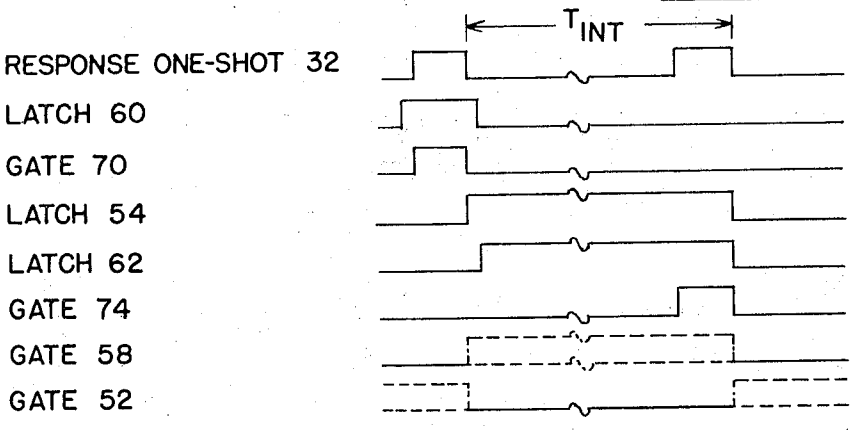


Fig 6

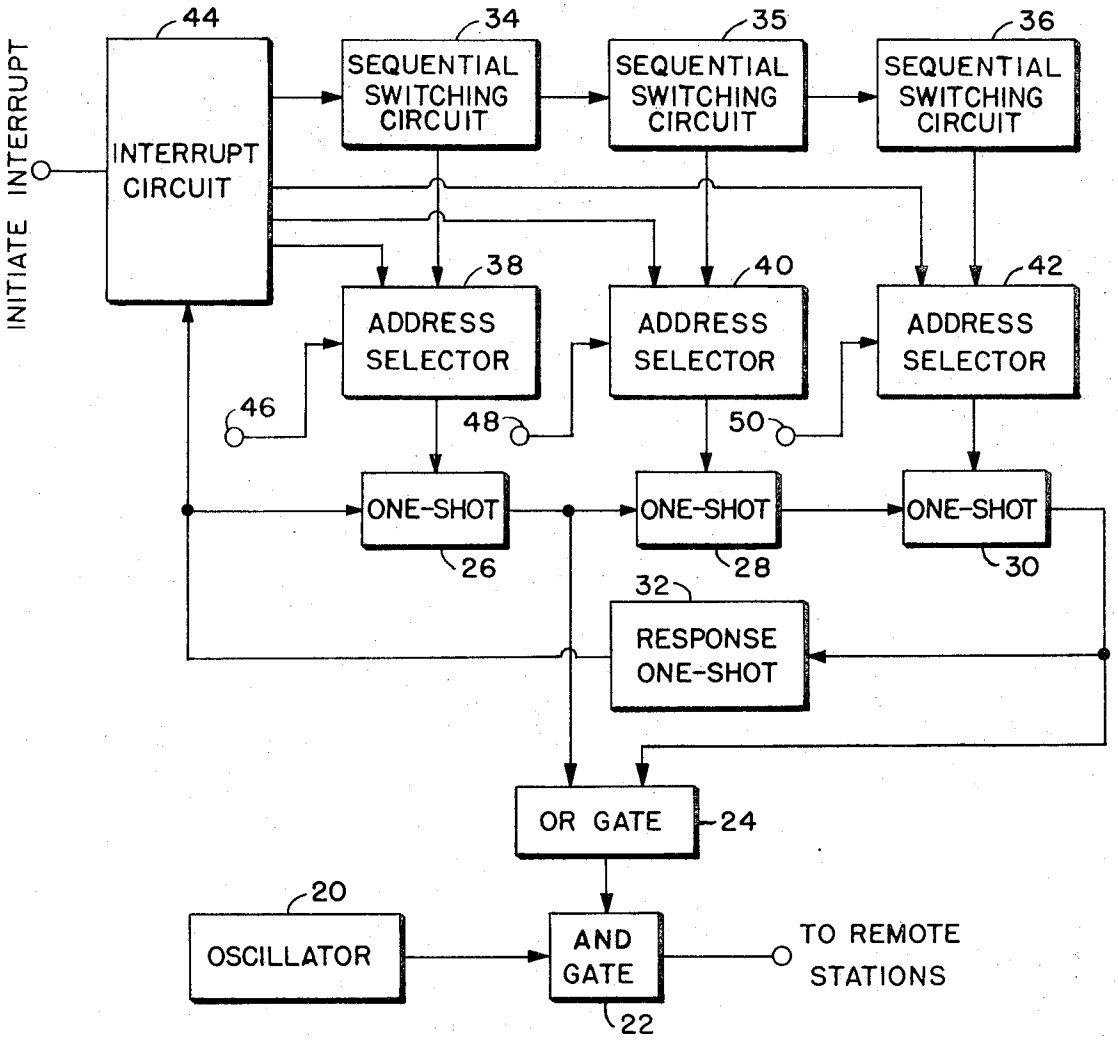

INITIATE INTERRUPT
44
INTERRUPT CIRCUIT
34
SEQUENTIAL SWITCHING CIRCUIT
35
SEQUENTIAL SWITCHING CIRCUIT
36
SEQUENTIAL SWITCHING CIRCUIT
38
ADDRESS SELECTOR
40
ADDRESS SELECTOR
42
ADDRESS SELECTOR
46
48
50
ONE-SHOT
26
ONE-SHOT
28
ONE-SHOT
30
32
RESPONSE ONE-SHOT
OR GATE
24
20
OSCILLATOR
AND GATE
22
TO REMOTE STATIONS

Fig 4

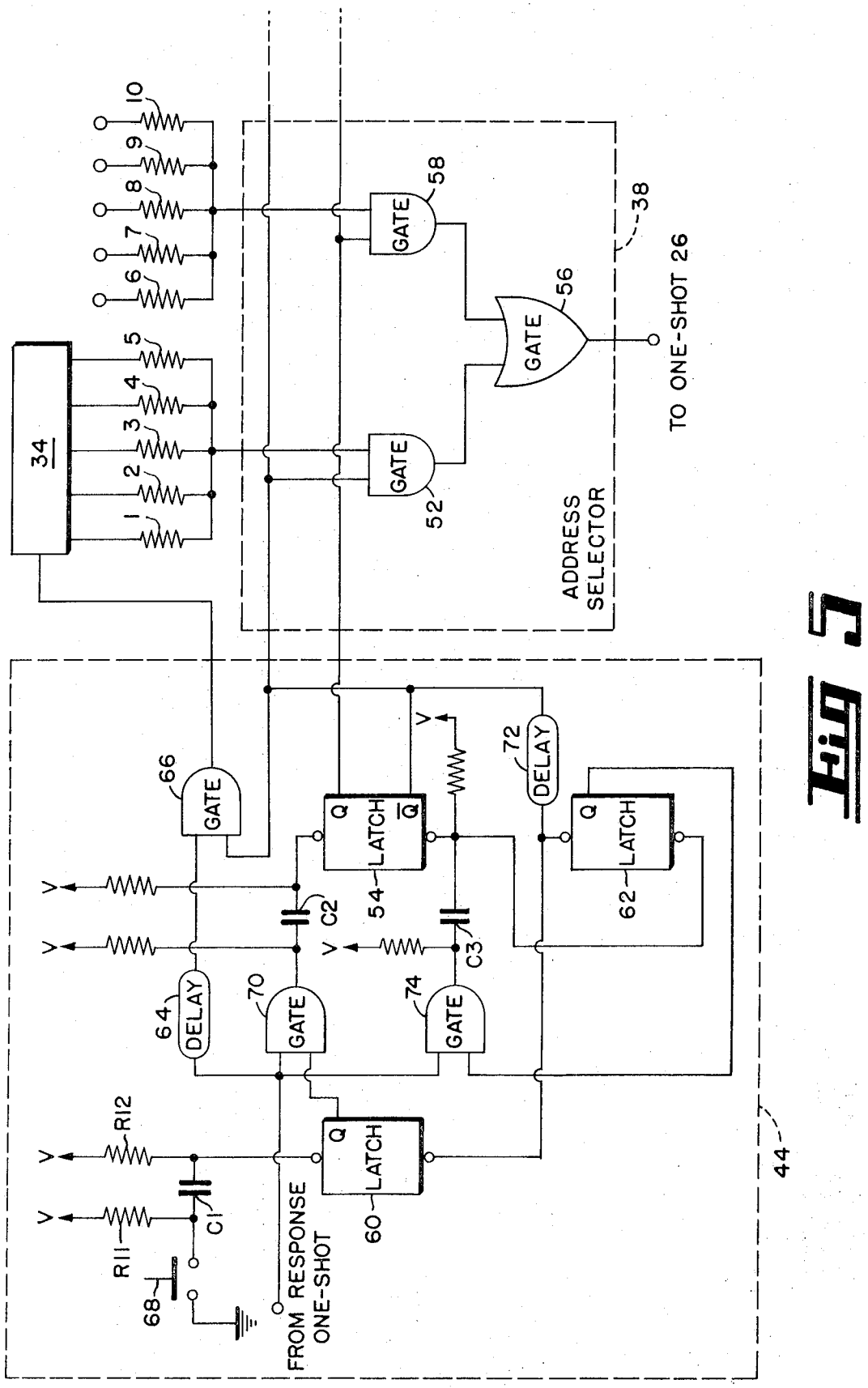

34
1
2
3
4
5
6
7
8
9
10
GATE
58
GATE
56
GATE
52
38
ADDRESS SELECTOR
TO ONE-SHOT 26
66
GATE
Q
LATCH
Q
54
72
DELAY
Q
LATCH
62
V
C2
C3
64
DELAY
70
GATE
74
GATE
R12
R11
C1
68
Q
LATCH
60
FROM RESPONSE ONE-SHOT
44

Fig 5

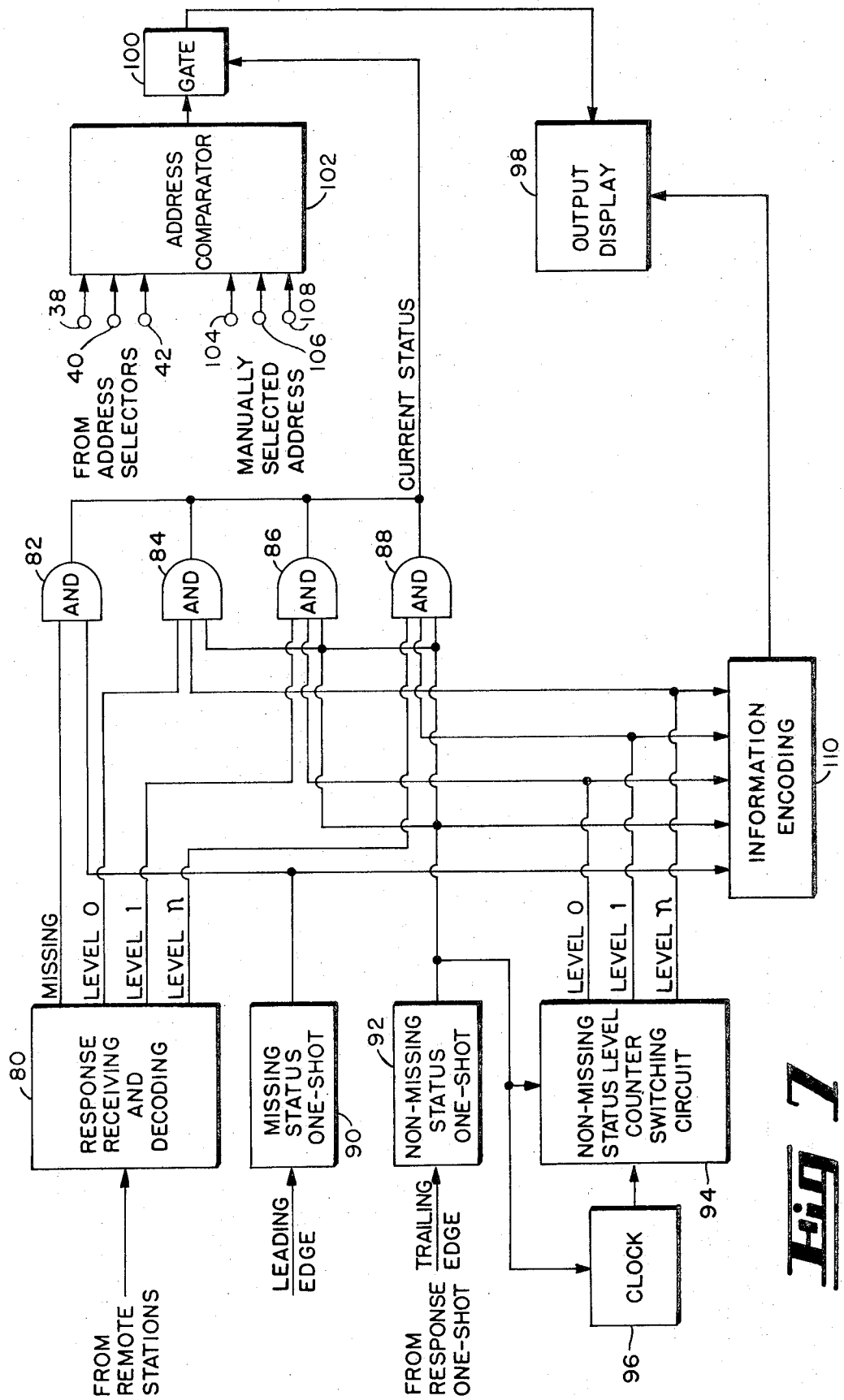

100
GATE
ADDRESS COMPARATOR
102
98
OUTPUT DISPLAY
38
40
42
104
106
108
FROM ADDRESS SELECTORS
MANUALLY SELECTED ADDRESS
CURRENT STATUS
82
84
86
88
AND
INFORMATION ENCODING
110
MISSING
LEVEL 0
LEVEL 1
LEVEL n
80
RESPONSE RECEIVING AND DECODING
MISSING STATUS ONE-SHOT
90
92
NON-MISSING STATUS ONE-SHOT
NON-MISSING STATUS LEVEL COUNTER SWITCHING CIRCUIT
94
CLOCK
96
FROM REMOTE STATIONS
LEADING EDGE
FROM RESPONSE ONE-SHOT
TRAILING EDGE

Fig 7

ADDRESS INTERRUPT AND CURRENT STATUS DISPLAY

BACKGROUND OF THE INVENTION

The invention involves a transponder security system of the type disclosed in U.S. Pat. No. 3,634,824 and which includes a signaling system having a plurality of remote stations and a central station. The central station has the capability of interrogating the remote stations in sequence, the address of the remote stations being time coded into the interrogating pulse transmissions. In a practical system, the time required to transmit **25** separate interrogations requires 39 seconds. This invention provides means for interrupting the normal sequence and interrogating a selected station, displaying the response from the selected station, and then continuing with the normal interrogating sequence.

THE DRAWINGS

FIG. **1** is a block diagram showing a transponder system in which the disclosed invention is utilized;

FIG. **2** is a curve showing the nature of the coded transmitted signal;

FIG. **3** is a curve showing the nature of the coded transpondered signal;

FIG. **4** is a block diagram showing the interrupter system utilized in accordance with this invention;

FIG. **5** is a schematic drawing showing certain of the details of the interrupter circuits and the address selector circuits;

FIG. **6** is a series of curves showing the time relationships occurring within the interrupt circuit; and

FIG. **7** is a block diagram showing the processing of the coded transponded signals from the remote stations.

The overall system is shown schematically in FIG. **1.** A central station **10** sends to the remote station address. Each of the particular remote stations **12** (of which there may be any number within the time capabilities of the system) responds to a particular interrogation by transmitting back to the central station tone pulses of lengths that are determined by the status and changes of status of the respective monitors **14** connected to it. Having received the responses from the remote station, the central station decodes the response, processes the information and displays it in displays **16** in a manner described in U.S. Pat. No. 3,634,824.

The addresses of the remote stations are contained in a fixed frequency signal of the type shown in FIG. **2.** As shown, the central station transmits a first fixed frequency signal having a duration **T1.** This is followed by a space which occurs for a period **T2.** The space **T2** is then followed by another signal of the same fixed frequency and having a time period **T3** which is then followed by a space having a period **T4.** The address of the remote station is coded into the transmission by varying each of the time periods **T1, T2,** and **T3.** The time period **T4** is a fixed period during which the remote station transponds. Theoretically the number of addresses may be multiplied by adding additional time periods, all of which may be variable. In a practical system, only the times **T1** and **T2** were variable to provide a combination of **25** addresses.

As indicated in FIG. **1,** each of the remote stations may contain a number of monitors. Certain of the monitors may, for example, be arranged to detect the opening of a window, the breaking of a window, the walking on a floor, a fire, or the opening of a door. Each of these conditions is given a priority level. As shown in FIG. **3,** a remote station transmits a single frequency back to the central station and it will have a duration determined by the highest level alarm that is causing a transmission. The first period t_m of the transmission occurs at every interrogation to give a positive indication that the transponder is operative. A level **0** priority alarm has a duration t_0, a level **1** priority alarm will have a duration t_1, and so forth, so that the highest level alarm signal will dominate all transponded signals.

When an indication appears at the central station that an alarm is being transmitted by the remote station, it is desirable to interrupt the normal sequence, and re-interrogate the station from which an alarm is indicated and then display or otherwise read out the particular cause of the alarm. The block diagram in FIG. **4** shows schematically how the addresses to the remote stations are sequentially coded and transmitted, and also how the normal sequence is interrupted.

The system includes a fixed frequency oscillator **20** which transmits a signal to the remote stations whenever its associated AND gate **22** is enabled. The AND gate **22** is enabled only when it receives the output from an OR gate **24** in addition to the output signal from the oscillator **20.**

To control the output from the OR gate **24,** and therefore to permit the introduction of the appropriate addresses for the remote stations, a plurality of one-shots **26, 28, 30,** and **32** are connected in series, that is, the one-shots are arranged so that the trailing edge of one triggers the next. The output of each of the one-shots is a square wave having a duration determined by the time constants which are set in. The one-shot **32,** referred to as the response one-shot, has a fixed time constant so that the duration **T4** of its output remains fixed. The time constants of the one-shots **26, 28,** and **30** are alterable, sequentially or manually, and the durations of the outputs from these one-shots determine the time periods **T1, T2,** and **T3** shown in FIG. **2.**

Under normal conditions, the time constants of the one-shots **26, 28,** and **30** are changed by sequentially and cyclically introducing different values of resistance into their respective R-C circuits. This is accomplished by means of conventional sequential switching circuits **34, 35,** and **36.**

The sequential switching circuits **34, 35,** and **36** have a number of stages, each one of which sequentially connects a different resistor value into a respective one-shot R-C network through an associated address selector circuit **38, 40,** and **42.** The update clock for the sequential switching circuit **34** is the output pulse from the response one-shot **32.** After the last stage of the switching circuit **34** is activated, the next update pulse resets it to the first stage and updates sequential switching circuit **35.** Similarly, the resetting of the sequential switching circuit **35** updates the switching circuit **36.** This means that if there are five stations in each switching circuit, there is a possibility of having **125** different addresses. In a system as reduced to practice, there were five stages in the circuit **34** and five stages in the circuit **35** and only a single stage in the circuit **36,** so that a total of **25** addresses were possible. The particular resistor selected by the switching circuit **34** is connected into the one shot **26** through address selector **38,** the resistor selected by the circuit **35** is connected to one-shot **28** through the address selector **40,**

and the resistor selected by the switching circuit **36** is connected into the one-shot **30** by the address selector **42.**

The response one-shot **32** provides the update pulse for the sequential switching circuit **34** through an interrupt circuit **44** hereinafter to be described along with the address selectors **38–42.** A particular address is manually set into the address selectors **38, 40,** and **42** through address interrupt terminals **46, 48,** and **50.** The interrupt circuit **44** and the address selectors **38, 40,** and **42** are shown in more detail in FIG. **5,** to which reference is now made.

The address selectors **38, 40,** and **42** are identical so that only selector **38** and its associated switching circuit **34** are described. Each of the address selectors includes an AND gate **52** having one input terminal connected to the resistors **R1–R5** selected by its respective sequential switching cirucit **34, 35,** and **36** for connection into the R-C network of a selected one-shot. The other terminal of AND gate **52** is connected to the $\overline{Q}$ output of a latch **54.** Under normal sequential operation the AND gate **52** is enabled by a logical **1** on the $\overline{Q}$ output of latch **54,** and an output is provided to the associated one-shot through an OR gate **56.**

The address selectors each includes a second AND gate **58** having one input connected to the manually selected resistors **R6–R10,** any one of which may be manually switched into the R-C circuit of its associated one-shot. The other input terminal of of the gate **58** is connected to the $\overline{Q}$ output terminal of the latch **54.** Under normal sequential operating conditions the Q output of latch **54** is at logical **0,** and the AND gate **58** is disabled. The latch **54** is a part of the interrupt circuit **44** which also includes latches **60** and **62,** each of which has a Q output terminal. Under sequential operating conditions the Q output of all the latches are set to a logical **0,** while the $\overline{Q}$ output of latch **54** is set to a logical **1.** The pulse from the response one-shot **32** is applied to the sequential switching circuit **34** through a delay **64** and through the first terminal of AND gate **66,** the other terminal of which is enabled bt the logical **1** appearing at the $\overline{Q}$ output of latch **54.**

When it is desired to interrupt the sequential updating of the switching circuit **34,** an interrupt pulse is generated by the circuit which includes a capacitor **C1,** resistors **R11** and **R12,** and an interrupt switch **68.** The pulse generated by the discharging of capacitor **C1** sets the Q output of latch **60** to a logical 1 condition. The logical **1** at the Q output of the latch **60** enables AND gate **70** for passing the output pulses from the response one-shot **32** to a capacitor **C2** which serves to provide a spike on the trailing edge of the one-shot pulse for setting the Q output of the latch **54** to a logical **1** and for setting its $\overline{Q}$ output to a logical **0.** The condition of the Q and $\overline{Q}$ outputs of latch **54** disables AND gate **52** and enables AND gate **58** so that one of the manually preselected resistors **R6–R10** is connected through the AND gate **58** and the OR gate **56** to its respective one-shot **26.**

The $\overline{Q}$ output of latch **54** is also applied through a delay **72** to reset the Q output of latch **60** to a logical **0** and to set the Q output of latch **62** to a logical **1.** The output from latch **62** is used to enable an AND gate **74** so that the pulse from the response one-shot **32** resets latches **54** and **62** through a capacitor **C3,** which serve to provide a pulse on the trailing edge of the next response one-shot pulse. The resetting of the latches **54** and **62** returns the central station to its normal addressing sequence beginning again at the point where it was interrupted. The delay **64** is a short time delay which is used for the purpose of preventing the pulse generated by the response one-shot **32** from passing through gate **66** while latch **54** is being set.

The operation of the interrupt and address selector circuits is summarized as follows: Momentary closing of the switch **68** causes the discharge of capacitor **C1** to generate a pulse which is used to set the Q output of latch **60** to a logical **1.** The Q output of latch **60** is gated with the pulse from the response one-shot **32** to set the Q output of latch **54** to a logical **1** and its $\overline{Q}$ output to a logical **0.** The capacitor **C2** assures that the setting and resetting of latch **54** is on the trailing edge of the response one-shot pulse. This interrupts the normal addressing sequence of the central station in time for the generation of a manually selected address, and the $\overline{Q}$ output of latch **54** is used to prevent the sequential switching circuits from being updated by disabling gate **66.**

The Q output of latch **54** is used to enable the manually selected address through gates **58** and **56** while the $\overline{Q}$ output of latch **54** disables the normal address line at gate **52.** The output at gate **56** represents the manually selected address and is used to control the timing of the one-shot **26.**

The $\overline{Q}$ output of latch **54** is applied through delay **72** to reset the Q output of latch **60** back to a logical **0** and to set the Q output of latch **62** to a logical **1.** The Q output from latch **62** is used to enable the AND gate **74** so that the next pulse from the response one-shot resets latches **54** and **62** on the trailing edge. This means that the normal sequencing circuits have been interrupted for one complete cycle but are then free to return to their normal sequencing.

The timing frequencies for the various latches are shown in FIG. **6.** It will be seen that the interrupt occurs during the period T_{int}, i.e., from the trailing edge of one response one-shot pulse to the trailing edge of a succeeding one response one-shot pulse.

Referring now to FIG. **7,** the transponded signals from each selected remote station are applied to a response receiving and decoding circuit **80** which serves to provide a logical **1** or a logical **0** output on a particular line, depending on the code level transponded by the remote station. Thus, if no signal is received from the selected remote station, a logical **1** would appear on the line labeled "missing;" otherwise if a signal of a duration t_m, as shown in FIG. **3** is decoded, a logical **1** would appear on the "level **0**" line, and so on through the "level *n*" line.

Each of the level lines *m* through *n* is connected to a first input terminal of a respective one of a plurality of AND gates **82, 84, 86,** and **88.** The current status of the received signals from the remote stations is determined by sequentially scanning these AND gates. For this purpose a "missing status" one-shot **90,** triggered on the leading edge of the response one-shot pulse, is used to enable AND gate **82.** A "non-missing status" one-shot **92,** triggered on the trailing edge of the response one-shot pulse plus an additional signal from a status level switching circuit **94** enables AND gate **84.** The status level switching circuit **94,** enabled by the leading edge of the output pulse of the one-shot **92** and updated from level **0** through level *n* by means of a system clock **96,** sequentially enables AND gates **84, 86,**

and **88.** The time for generation of the current status output must, of course, occur within one complete cycle of the transmitted and received signals.

The current status appearing at the outputs of the AND gates **82–88** is applied to an output display **98** through an AND gate **100.** The AND gate **100** is enabled by an address-comparator **102** which develops an enabling output signal whenever its two inputs, one from the address selectors **38, 40,** and **42** and the other manually selected addresses set in at the terminals **104, 106,** and **108** are identical. The address-comparator may comprise two logic circuits, one which is set by the outputs of the address selectors **38–42,** and one which is manually set in at the display. The comparator provides an output when there is coincidence between the logic circuits.

As previously noted in connection with FIGS. **4** and **5,** the output from each address selector **38, 40,** and **42** is a resistor **R1–R5** or a resistor **R6–R10,** depending on whether the sequencing is to be interrupted. Thus, the AND gate **100** is enabled when the address appearing in the address selectors coincides with that set in at the terminals **104, 106,** and **108.** The display **98** is enabled when the output from an information and coding circuit **110** is applied. The information and coding circuit **110** sets up the timing for current status which is displayed.

It will be apparent to persons skilled in the art that the disclosed system is subject to various modifications and adaptations, all within the scope of the invention. For example, while three address selectors are shown, it is apparent that the system will work with any number, depending on the number of addresses required by the system and the amount of time sharing which is permitted. In certain circumstances only one address selector may be required.

Furthermore, while the system shown utilizes only four alarm levels including a missing level, it is apparent that any number may be used. While reference is made to a practical system having 25 addresses, it will be understood that in the embodiment as reduced to practice, four remote stations at the same address are transponded simultaneously but at different frequencies and that the system has capabilities, not a part of this invention, for separating and processing the information from four transponders simultaneously.

I claim:

1. In a signaling system having a central station and a plurality of remote stations, said central station having means for sequentially transmitting time coded address signals to each of said remote stations in a preestablished sequence, each of said remote stations transponding to said central station upon receipt of a respective time coded address signal, the combination comprising:

a fixed frequency oscillator having a fixed frequency output;

a gate having an output terminal and first and second input terminals, said fixed frequency output being applied to the first input terminal, said fixed frequency output being coupled to said remote stations through the output terminal of said gate when said gate is enabled, said gate being enabled when an enabling pulse is applied to said second terminal, the duration of each enabling pulse establishing said time coded address signals;

enabling pulse generating means for sequentially generating enabling pulses of different durations, the output of said enabling pulse generating means being applied to said second terminal;

a first plurality of duration determining means connectable into said enabling pulse generating means for establishing the duration of said enabling pulse;

sequential switching means for sequentially connecting each of said duration determining means into said enabling pulse generating means for establishing the durations of said enabling pulse in said preestablished sequence;

a second plurality of selectable duration determining means;

means for interrupting said sequential switching means and for substituting one of said selectable duration determining means for transmitting a selected new time coded address signal; and

means after receiving a signal from a remote station transponding to said selected new time coded address signal for continuing the operation of said sequential switching means.

2. The invention as defined in claim **1** wherein said enabling pulse generating means is a one-shot multivibrator.

3. The invention as defined in claim **2** wherein said first and second pluralities of duration determining means are first and second pluralities of resistors, said resistors being connectable into the R-C network of said one-shot multivibrator for establishing the duration of its output pulse.

4. The invention as defined in claim **3** wherein said sequential switching means is an electronic switch having a stage for each of said first plurality of resistors, each of said stages of said switch sequentially establishing one of said connections in response to an update pulse, said switch recycling to the first stage after the last stage is disconnected.

5. The invention as defined in claim **4,** and a second one-shot multivibrator for generating an update pulse, the trailing edge of the output of said first one-shot multivibrator triggering said second one-shot multivibrator, said update pulse being connected to said sequential circuit means for updating said switch.

6. The invention as defined in claim **5** wherein said means for interrupting the updating of said sequential switching means and for substituting one of said selectable duration determinging means comprises:

a first normally closed switch for connecting the output from said second one-shot multivibrator to said sequential switching means for updating said sequential switching means;

a second normally closed switch connecting sequentially selected ones of said first duration determining means into the R-C network of said first one-shot multivibrator;

a third switch for connecting a selected one of said second plurality of duration determining means, said second switch being normally open;

means for opening said first and second switches and for closing said third switch; and

means for subsequently closing said first and second switches and for opening said third switch.

7. The invention as defined in claim **6** wherein an addressed remote station transponds during the period of said update pulse;

and means during the period of said update pulse for displaying a received signal from a remote station.

8. The invention as defined in claim **7** wherein said means for displaying a received signal includes a gate having an output terminal and first and second input terminals, said first input terminal being supplied with decoded received signals, said second terminal enabling said gate when supplied with a comparator output;

a comparator having first and second inputs, said first input being a manually selected numerically coded address, said second input being supplied with a numerical coded address representing a selected new time coded address signal, the output of said address comparator being applied to said terminal of said gate and enabling said gate when the numerical addresses in said comparator are in coincidence.

9. In a signaling system having a central station and a plurality of remote stations, said central station having means for sequentially transmitting time coded address signals to each of said remote stations in a pre-established sequence, each of said remote stations transponding to said central station upon receipt of a respective time coded address signal, said time coded address comprising the combination including a fixed frequency signal having a duration **T1** followed by a space having a duration **T2,** in turn followed by a fixed frequency signal having a duration **T3,** durations **T1** and **T2** being variable in accordance with a program to generate said time coded signals in said pre-established sequence, said duration **T3** being constant, the combination comprising:

a fixed frequency oscillator having a fixed frequency output;

a gate having an output terminal and first and second input terminals, said fixed frequency output being applied to said first input terminal, said fixed frequency output being coupled to said remote stations through the output terminal of said gate when said gate is enabled, said gate being enabled when an enabling pulse is applied to said second terminal;

first, second, third and fourth serially connected one-shot multivibrators, the trailing edge of the output pulse of each of said multivibrators triggering a succeeding multivibrator, the trailing edge of the output of said fourth multivibrator triggering said first multivibrator, each of said multivibrators having an R-C network, the duration of the output pulse of each multivibrator being a function of the parameters of a respective R-C network, the parameters of said third and fourth multivibrators being fixed, the parameters of said first and second one-shot multivibrators being sequentially alterable in accordance with said program, the duration of the outputs of said first, second, and third one-shot multivibrators being equal to **T1, T2,** and **T3,** respectively, the output of the fourth one-shot multivibrator having a fixed duration **T4;**

a first plurality of duration determining means connectable into the R-C network of said first one-shot multivibrator for establishing the durations of the output pulses therefrom;

a second plurality of duration determining means connectable into the R-C network of said second one-shot multivibrator for selectively re-establishing the durations of the output pulses therefrom;

sequential switching means for sequentially connecting each of said duration determining means of said first and second pluralities into the R-C networks of said first and second one-shot multivibrators in accordance with said program, said sequential switching means being updated by said fourth one-shot multivibrator;

a third and fourth plurality of selectable duration determining means;

means for interrupting the updating of said sequential switching means and for substituting one of said selectable duration determining means of each of said third and fourth pluralities for re-establishing a selected new time coded address signal;

means during the generation of the output pulse of said fourth one-shot multivibrator for displaying a received signal from a remote station; and

means after receiving a signal from said remote station transponding to said selected new time coded address signal for continuing the operation of said sequential switching means.

10. The invention as defined in claim **9** wherein said means for interrupting the updating of said sequential switching means and for substituting one of said selectable duration determining means comprises;

a first normally closed switch for connecting the output from said second one-shot multivibrator to said sequential switching means for updating said sequential switching means;

a second normally closed switch connecting sequentially selected ones of said first duration determining means into the R-C network of said first one-shot multivibrator;

a third switch for connecting a selected one of said second plurality of duration determining means, said second switch being normally open;

means for opening said first and second switches and for closing said third switch; and

means for subsequently closing said first and second switches and for opening said third switch.

11. The invention as defined in claim **10** wherein an addressed remote station transponds during the period of said update pulse;

and means during the period of said update pulse for displaying a received signal from a remote station.

12. The invention as defined in claim **11** wherein said means for displaying a received signal includes a gate having an output termianl and first and second input terminals, said first input terminal being supplied with decoded received signals, said second terminal enabling said gate when supplied with a comparator output;

a comparator having first and second inputs, said first input being a manually selected numerically coded address, said second input being supplied with a numerically coded address representing a selected new time coded address signal, the output of said address comparator being applied to said terminal of said gate and enabling said gate when the numerical addresses in said comparator are in coincidence.

* * * * *

PO-1050
(5/69)

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,806,872 Dated April 23, 1974

Inventor(s) James T. Odom

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 1, line 37, after "sends to" insert --- the remote stations a series of tone pulses which represent ---.

Column 3, line 29, delete one occurrence of "of".

Column 3, line 30, "$\overline{Q}$" should read --- Q ---.

Column 6, line 49, "determinging" should read --- determining --.

Column 8, line 53, "termianl" should read --- terminal ---.

Signed and sealed this 1st day of October 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents