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(54) Title: SELECTIVE ENABLEMENT OF OPERATING MODES OR FEATURES VIA HOST TRANSFER RATE DETECTION

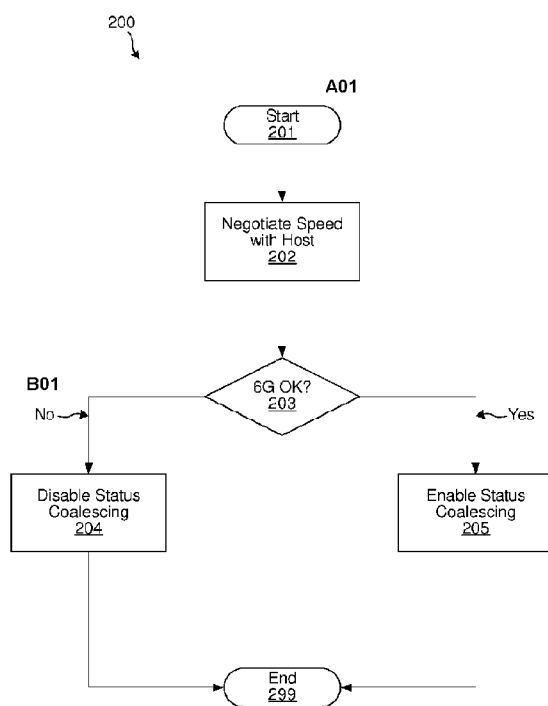


Fig. 2

(57) Abstract: Selective enablement of operating modes or features of a storage system via host transfer rate detection enables, in some situations, enhanced performance. For example, a Solid-State Disk (SSD) having a serial interface compatible with a particular serial interface standard selectively enables coalescing of status information for return to a host based on detecting a particular host transfer rate capability. Some hosts are not fully compliant with the particular standard, being unable to properly process the coalesced status information. The selective enablement disables status coalescing for a non-compliant host and enables status coalescing for at least some compliant hosts, without the SSD having prior knowledge of coupling to a non-compliant/compliant host. The SSD conservatively determines the host is non-compliant/compliant based on a negotiated speed of the serial interface, and selectively disables/enables status coalescing in response to the negotiated speed.





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**SELECTIVE ENABLEMENT OF OPERATING MODES OR FEATURES VIA  
HOST TRANSFER RATE DETECTION**

**CROSS REFERENCE TO RELATED APPLICATIONS**

**[0001]** Priority benefit claims for this application are made in the accompanying Application Data Sheet, Request, or Transmittal (as appropriate, if any). To the extent permitted by the type of the instant application, this application incorporates by reference for all purposes the following applications, all commonly owned with the instant application at the time the invention was made:

U.S. Provisional Application (Docket No. SF-11-05 and Serial No. 61/440,710), filed 08-FEB-2011, first named inventor Andrew John TOMLIN, and entitled **Selective Enablement of Status Coalescing via Host Transfer Rate Detection.**

**BACKGROUND**

**[0002]** Field: Advancements in interfacing hosts with storage systems/sub-systems are needed to provide improvements in performance, efficiency, and utility of use.

**[0003]** Related Art: Unless expressly identified as being publicly or well known, mention herein of techniques and concepts, including for context, definitions, or comparison purposes, should not be construed as an admission that such techniques and concepts are previously publicly known or otherwise part of the prior art. All references cited herein (if any), including patents, patent applications, and publications, are hereby incorporated by reference in their entireties, whether specifically incorporated or not, for all purposes.

## SYNOPSIS

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**[0004]** The invention may be implemented in numerous ways, including as a process, an article of manufacture, an apparatus, a system, a composition of matter, and a computer readable medium such as a computer readable storage medium (e.g. media in an optical and/or magnetic mass storage device such as a disk, or an integrated circuit having non-volatile storage such as flash storage) or a computer network wherein program instructions are sent over optical or electronic communication links. In this specification, these implementations, or any other form that the invention may take, may be referred to as techniques. The Detailed Description provides an exposition of one or more embodiments of the invention that enable improvements in performance, efficiency, and utility of use in the field identified above. The Detailed Description includes an Introduction to facilitate the more rapid understanding of the remainder of the Detailed Description. The Introduction includes Example Embodiments of one or more of systems, methods, articles of manufacture, and computer readable media in accordance with the concepts described herein. As is discussed in more detail in the Conclusions, the invention encompasses all possible modifications and variations within the scope of the issued claims.

## Brief Description of Drawings

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**[0005]** Fig. 1A illustrates selected details of an embodiment of a Solid-State Disk (SSD) including an SSD controller providing selective enablement of one or more operating modes and/or one or more features (such as status coalescing) via host transfer rate detection for managing an interface with a (computing) host, as well as circuitry for managing non-volatile storage, such as flash memories.

**[0006]** Fig. 1B illustrates selected details of various embodiments of systems including one or more instances of the SSD of Fig. 1A.

**[0007]** Fig. 1C illustrates selected details of an embodiment of a system including the SSD of Fig. 1A.

**[0008]** Fig. 1D illustrates selected details of an embodiment of a system including the SSD of Fig. 1A.

**[0009]** Fig. 2 illustrates a flow diagram of selected details of an embodiment of selective enablement of status coalescing via host transfer rate detection.

## List of Reference Symbols in Drawings

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[0010]

| Ref. Symbol | Element Name                                                                     |
|-------------|----------------------------------------------------------------------------------|
| 100         | SSD Controller                                                                   |
| 101         | SSD                                                                              |
| 102         | Host                                                                             |
| 102A        | Host-6G                                                                          |
| 102B        | Host-3G/1.5G                                                                     |
| 102C        | Host-3G/1.5G                                                                     |
| 103         | (optional) Switch / Fabric / Intermediate Controller                             |
| 104         | Intermediate Interfaces                                                          |
| 105         | OS                                                                               |
| 106         | FirmWare (FW)                                                                    |
| 107         | Driver                                                                           |
| 107D        | dotted-arrow (Host Software $\leftrightarrow$ I/O Device Communication)          |
| 109         | Application                                                                      |
| 109D        | dotted-arrow (Application $\leftrightarrow$ I/O Device Communication via driver) |
| 109V        | dotted-arrow (Application $\leftrightarrow$ I/O Device Communication via VF)     |
| 110         | External Interfaces                                                              |
| 111         | Host Interfaces                                                                  |
| 112C        | (optional) Card Memory                                                           |
| 113         | Tag Tracking                                                                     |
| 114         | Multi-Device Management Software                                                 |
| 115         | Host Software                                                                    |
| 116         | I/O Card                                                                         |
| 117         | I/O & Storage Devices/Resources                                                  |
| 118         | Servers                                                                          |
| 119         | LAN/WAN                                                                          |
| 121         | Data Processing                                                                  |
| 123         | Engines                                                                          |
| 131         | Buffer                                                                           |
| 133         | DMA                                                                              |
| 135         | ECC-X                                                                            |

| <b>Ref. Symbol</b> | <b>Element Name</b>       |
|--------------------|---------------------------|
| <b>137</b>         | Memory                    |
| <b>141</b>         | Map                       |
| <b>143</b>         | Table                     |
| <b>151</b>         | Recycler                  |
| <b>161</b>         | ECC                       |
| <b>171</b>         | CPU                       |
| <b>172</b>         | CPU Core                  |
| <b>173</b>         | Command Management        |
| <b>175</b>         | Buffer Management         |
| <b>177</b>         | Translation Management    |
| <b>179</b>         | Coherency Management      |
| <b>180</b>         | Memory Interface          |
| <b>181</b>         | Device Management         |
| <b>182</b>         | Identity Management       |
| <b>190</b>         | Device Interfaces         |
| <b>191</b>         | Device Interface Logic    |
| <b>192</b>         | Flash Device              |
| <b>193</b>         | Scheduling                |
| <b>194</b>         | Flash Die                 |
| <b>199</b>         | NVM                       |
| <b>200</b>         | Flow Diagram              |
| <b>201</b>         | Start                     |
| <b>202</b>         | Negotiate Speed with Host |
| <b>203</b>         | 6G OK?                    |
| <b>204</b>         | Disable Status Coalescing |
| <b>205</b>         | Enable Status Coalescing  |
| <b>299</b>         | End                       |
| <b>1100DA</b>      | Negotiation               |
| <b>1100DB</b>      | Negotiation               |
| <b>1100DC</b>      | Negotiation               |
| <b>1100IA</b>      | Negotiation               |
| <b>1100IB</b>      | Negotiation               |
| <b>1100IC</b>      | Negotiation               |

## DETAILED DESCRIPTION

[0011] A detailed description of one or more embodiments of the invention is provided below along with accompanying figures illustrating selected details of the invention. The invention is described in connection with the embodiments. The embodiments herein are understood to be merely exemplary, the invention is expressly not limited to or by any or all of the embodiments herein, and the invention encompasses numerous alternatives, modifications, and equivalents. To avoid monotony in the exposition, a variety of word labels (including but not limited to: first, last, certain, various, further, other, particular, select, some, and notable) may be applied to separate sets of embodiments; as used herein such labels are expressly not meant to convey quality, or any form of preference or prejudice, but merely to conveniently distinguish among the separate sets. The order of some operations of disclosed processes is alterable within the scope of the invention. Wherever multiple embodiments serve to describe variations in process, method, and/or program instruction features, other embodiments are contemplated that in accordance with a predetermined or a dynamically determined criterion perform static and/or dynamic selection of one of a plurality of modes of operation corresponding respectively to a plurality of the multiple embodiments. Numerous specific details are set forth in the following description to provide a thorough understanding of the invention. The details are provided for the purpose of example and the invention may be practiced according to the claims without some or all of the details. For the purpose of clarity, technical material that is known in the technical fields related to the invention has not been described in detail so that the invention is not unnecessarily obscured.

## INTRODUCTION

[0012] This introduction is included only to facilitate the more rapid understanding of the Detailed Description; the invention is not limited to the concepts presented in the introduction (including explicit examples, if any), as the paragraphs of any introduction are necessarily an abridged view of the entire subject and are not meant to be an exhaustive or restrictive description. For example, the introduction that follows provides overview information limited by space and organization to only certain embodiments. There are many other embodiments, including those to which claims will ultimately be drawn, discussed throughout the balance of the specification.

1 Acronyms

2

3 **[0013]** Elsewhere herein various shorthand abbreviations, or acronyms, sometimes  
 4 refer to certain elements. The descriptions of at least some of the acronyms follow.

| <u>Acronym</u> | <u>Description</u>                              |
|----------------|-------------------------------------------------|
| AHCI           | Advanced Host Controller Interface              |
| API            | Application Program Interface                   |
| ATA            | Advanced Technology Attachment                  |
| ATAPI          | Advanced Technology Attachment Packet Interface |
| BCH            | Bose Chaudhuri Hocquenghem                      |
| CD             | Compact Disk                                    |
| CF             | Compact Flash                                   |
| CMOS           | Complementary Metal Oxide Semiconductor         |
| CPU            | Central Processing Unit                         |
| CRC            | Cyclic Redundancy Check                         |
| DAS            | Direct Attached Storage                         |
| DDR            | Double-Data-Rate                                |
| DMA            | Direct Memory Access                            |
| DNA            | Direct NAND Access                              |
| DRAM           | Dynamic Random Access Memory                    |
| DVD            | Digital Versatile/Video Disk                    |
| DVR            | Digital Video Recorder                          |
| ECC            | Error-Correcting Code                           |
| eMMC           | Embedded MultiMediaCard                         |
| eSATA          | external Serial Advanced Technology Attachment  |
| GPS            | Global Positioning System                       |
| HDD            | Hard Disk Drive                                 |
| I/O            | Input / Output                                  |
| IC             | Integrated Circuit                              |
| IDE            | Integrated Drive Electronics                    |
| JPEG           | Joint Photographic Experts Group                |
| LAN            | Local Area Network                              |
| LBA            | Logical Block Address                           |
| LDPC           | Low-Density Parity-Check                        |
| LPN            | Logical Page Number                             |

| <u>Acronym</u> | <u>Description</u>                                            |
|----------------|---------------------------------------------------------------|
| MLC            | Multi-Level Cell                                              |
| MMC            | MultiMediaCard                                                |
| MPEG           | Moving Picture Experts Group                                  |
| NAS            | Network Attached Storage                                      |
| NCQ            | Native Command Queuing                                        |
| NVM            | Non-Volatile Memory                                           |
| ONA            | Optimized NAND Access                                         |
| ONFI           | Open NAND Flash Interface                                     |
| OS             | Operating System                                              |
| PC             | Personal Computer                                             |
| PCIe           | Peripheral Component Interconnect express (PCI express)       |
| PDA            | Personal Digital Assistant                                    |
| POS            | Point Of Sale                                                 |
| RAID           | Redundant Array of Inexpensive/Independent Disks              |
| RASIE          | Redundant Array of Silicon Independent Elements               |
| RS             | Reed-Solomon                                                  |
| SAN            | Storage Attached Network                                      |
| SAS            | Serial Attached Small Computer System Interface (Serial SCSI) |
| SATA           | Serial Advanced Technology Attachment (Serial ATA)            |
| SCSI           | Small Computer System Interface                               |
| SD             | Secure Digital                                                |
| SDR            | Single-Data-Rate                                              |
| SLC            | Single-Level Cell                                             |
| SMART          | Self-Monitoring Analysis and Reporting Technology             |
| SRAM           | Static Random Access Memory                                   |
| SSD            | Solid-State Disk/Drive                                        |
| UFS            | Unified Flash Storage                                         |
| USB            | Universal Serial Bus                                          |
| VF             | Virtual Function                                              |
| WAN            | Wide Area Network                                             |

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3 **[0014]** In some situations, such as a host coupled to storage, for example a Solid-State  
4 Disk (SSD) having a serial interface compatible with a particular serial interface standard, status

1 coalescing by the SSD for returning status information to the host enables enhanced  
2 performance. Some hosts are not fully compliant with the particular serial interface standard,  
3 being unable to properly process coalesced status information. Selective enablement of status  
4 coalescing via host transfer rate detection disables status coalescing when a non-compliant host  
5 is unable to properly process coalesced status and enables status coalescing for at least some  
6 compliant hosts that are enabled to properly process coalesced status, without the SSD having  
7 prior knowledge of coupling to a non-compliant/compliant host. The SSD conservatively  
8 determines the host is non-compliant/compliant based on a negotiated speed of the serial  
9 interface, and selectively disables/enables status coalescing in response to the negotiated speed.  
10 An example of the serial interface is a Serial Advanced Technology Attachment (SATA)  
11 interface.  
12

13 **[0015]** In various embodiments, an SSD controller includes a host interface for  
14 interfacing with a computing host, a flash interface for interfacing with flash memory (used, e.g.,  
15 to provide non-volatile storage that retains information without application of power), and  
16 circuitry for controlling the interfaces and performing (and/or controlling various aspects of the  
17 performing) selective enablement of status coalescing via host transfer rate detection.  
18

19 **[0016]** According to various embodiments, some host interfaces are compatible with  
20 one or more of a USB interface standard, a CF interface standard, an MMC interface standard,  
21 an eMMC interface standard, a Thunderbolt interface standard, a UFS interface standard, an SD  
22 interface standard, a Memory Stick interface standard, an xD-picture card interface standard, an  
23 IDE interface standard, a SATA interface standard, a SCSI interface standard, a SAS interface  
24 standard, and a PCIe interface standard. According to various embodiments, the computing host  
25 is all or any portions of a computer, a workstation computer, a server computer, a storage server,  
26 a SAN, a NAS device, a DAS device, a storage appliance, a PC, a laptop computer, a notebook  
27 computer, a netbook computer, a tablet device or computer, an ultrabook computer, an electronic  
28 reading device (such as an e-reader), a PDA, a navigation system, a (handheld) GPS device, an  
29 automotive control system, an automotive media control system or computer, a printer, copier or  
30 fax machine or all-in-one device, a POS device, a cash-register, a media player, a television, a  
31 media recorder, a DVR, a digital camera, a cellular handset, a cordless telephone handset, and an  
32 electronic game. In some embodiments, an interfacing host (such as an SAS/SATA bridge)  
33 operates as a computing host and/or as a bridge to a computing host.  
34

35 **[0017]** In various embodiments, the SSD controller includes one or more processors.  
36 The processors execute firmware to control and/or perform operation of the SSD controller. The

1 SSD controller communicates with the computing host to send and receive commands and/or  
2 status as well as data. The computing host executes one or more of an operating system, a  
3 driver, and an application. Communication by the computing host with the SSD controller is  
4 optionally and/or selectively via the driver and/or via the application. In a first example, all  
5 communication to the SSD controller is via the driver, and the application provides higher-level  
6 commands to the driver that the driver translates into specific commands for the SSD controller.  
7 In a second example, the driver implements a bypass mode and the application is enabled to send  
8 specific commands to the SSD controller via the driver. In a third example, a PCIe SSD  
9 controller supports one or more Virtual Functions (VFs), enabling an application, once  
10 configured, to communicate directly with the SSD controller, bypassing the driver.

11  
12 **[0018]** According to various embodiments, some SSDs are compatible with form-  
13 factors, electrical interfaces, and/or protocols used by magnetic and/or optical non-volatile  
14 storage, such as HDDs, CD drives, and DVD drives. In various embodiments, SSDs use various  
15 combinations of zero or more parity codes, zero or more RS codes, zero or more BCH codes,  
16 zero or more Viterbi or other trellis codes, and zero or more LDPC codes.

## 17 18 19 EXAMPLE EMBODIMENTS

20  
21 **[0019]** In concluding the introduction to the detailed description, what follows is a  
22 collection of example embodiments, including at least some explicitly enumerated as “ECs”  
23 (Example Combinations), providing additional description of a variety of embodiment types in  
24 accordance with the concepts described herein; these examples are not meant to be mutually  
25 exclusive, exhaustive, or restrictive; and the invention is not limited to these example  
26 embodiments but rather encompasses all possible modifications and variations within the scope  
27 of the issued claims.

28  
29 **[0020]** EC1) A system comprising:  
30 a means for serially interfacing a host with storage;  
31 a means for determining if the means for serially interfacing is operating at a nominal  
32 serial data transfer rate that is greater/less than a threshold; and  
33 a means for selectively enabling/disabling an operating mode and/or feature, the means  
34 for selectively enable/disabling being dependent at least in part on the means for  
35 determining.

- 1   **[0021]**           EC2) The system of EC1, wherein the means for serially interfacing is  
2   compatible with at least one version of a Serial Advanced Technology Attachment (SATA)  
3   standard.  
4
- 5   **[0022]**           EC3) The system of EC1, wherein the threshold is 6Gb.  
6
- 7   **[0023]**           EC4) The system of EC1, wherein the storage comprises a storage system/sub-  
8   system.  
9
- 10   **[0024]**           EC5) The system of EC1, wherein the storage comprises one or more Solid  
11   State Disks (SSDs), Hard Disk Drives (HDDs), Compact Disk (CD) and/or Digital  
12   Versatile/Video Disk (DVD) drives, and tape drives.  
13
- 14   **[0025]**           EC6) The system of EC1, wherein the means for serially interfacing is  
15   comprised in a Solid State Disk (SSD), and the storage comprises flash memory comprised in  
16   the SSD.  
17
- 18   **[0026]**           EC7) The system of EC1, wherein the means for serially interfacing is  
19   compatible with at least one version of a Serial Advanced Technology Attachment (SATA)  
20   standard, the threshold is 6Gb, the means for serially interfacing is comprised in a Solid State  
21   Disk (SSD), and the storage comprises flash memory comprised in the SSD.  
22
- 23   **[0027]**           EC8) The system of EC1, wherein the host is an interfacing host.  
24
- 25   **[0028]**           EC9) The system of EC8, wherein the interfacing host comprises one or more of  
26   a storage bridge and a storage expander.  
27
- 28   **[0029]**           EC10) The system of EC1, wherein the host is a computing host.  
29
- 30   **[0030]**           EC11) The system of EC10, further comprising all or any portions of the  
31   computing host.  
32
- 33   **[0031]**           EC12) The system of EC1, wherein the means for serially interfacing is  
34   compatible with a storage interface standard.  
35

1   **[0032]**           EC13) The system of EC1, wherein the storage comprises one or more flash  
2   memories and further comprising a means for interfacing with the flash memories.

3

4   **[0033]**           EC14) The system of EC13, wherein the means for interfacing with the flash  
5   memories comprises a flash memory interface.

6

7   **[0034]**           EC15) The system of EC13, further comprising at least one of the flash  
8   memories.

9

10   **[0035]**           EC16) The system of EC13, wherein the means are collectively implemented in  
11   a single Integrated Circuit (IC).

12

13   **[0036]**           EC17) The system of EC13, wherein the means are comprised in a Solid-State  
14   Disk (SSD).

15

16   **[0037]**           EC18) The system of EC13, wherein the means are comprised in a controller of  
17   a Solid-State Disk (SSD).

18

19   **[[0038]**           EC19) The system of EC1, wherein a first version of a serial interface standard  
20   specifies operation at a maximum nominal serial data transfer rate that is at or above the  
21   threshold and the first version of the serial interface standard specifies the operating mode and/or  
22   feature.

23

24   **[[0039]**           EC20) The system of EC19, wherein a second version of the serial interface  
25   standard specifies operation at a maximum nominal serial data transfer rate that is below the  
26   threshold.

27

28   **[[0040]**           EC21) The system of EC19, wherein a second version of the serial interface  
29   standard lacks any specification of the operating mode and/or feature.

30

31   **[[0041]**           EC22) The system of EC19, wherein a second version of the serial interface  
32   standard specifies operation at a maximum nominal serial data transfer rate that is below the  
33   threshold and lacks any specification of the operating mode and/or feature.

34

- 1   **[0042]**           EC23) A method comprising:  
2           serially interfacing a host with storage;  
3           determining if the serially interfacing is operating at a nominal serial data transfer rate  
4           that is greater/less than a threshold; and  
5           selectively enabling/disabling an operating mode and/or feature, the selectively  
6           enable/disabling being dependent at least in part on the determining.  
7
- 8   **[0043]**           EC24) The method of EC23, wherein the serially interfacing is compatible with  
9   at least one version of a Serial Advanced Technology Attachment (SATA) standard.  
10
- 11   **[0044]**           EC25) The method of EC23, wherein the threshold is 6Gb.  
12
- 13   **[0045]**           EC26) The method of EC23, wherein the storage comprises a storage  
14   system/sub-system.  
15
- 16   **[0046]**           EC27) The method of EC23, wherein the storage comprises one or more Solid  
17   State Disks (SSDs), Hard Disk Drives (HDDs), Compact Disk (CD) and/or Digital  
18   Versatile/Video Disk (DVD) drives, and tape drives.  
19
- 20   **[0047]**           EC28) The method of EC23, wherein the serially interfacing is performed in a  
21   Solid State Disk (SSD), and the storage comprises flash memory comprised in the SSD.  
22
- 23   **[0048]**           EC29) The method of EC23, wherein the serially interfacing is compatible with  
24   at least one version of a Serial Advanced Technology Attachment (SATA) standard, the  
25   threshold is 6Gb, the serially interfacing is performed in a Solid State Disk (SSD), and the  
26   storage comprises flash memory comprised in the SSD.  
27
- 28   **[0049]**           EC30) The method of EC23, wherein the host is an interfacing host.  
29
- 30   **[0050]**           EC31) The method of EC30, wherein the interfacing host comprises one or  
31   more of a storage bridge and a storage expander.  
32
- 33   **[0051]**           EC32) The method of EC23, wherein the host is a computing host.  
34
- 35   **[0052]**           EC33) The method of EC32, further comprising operating all or any portions of  
36   the computing host.

1  
2 **[0053]** EC34) The method of EC23, wherein the serially interfacing is compatible with  
3 a storage interface standard.

4  
5 **[0054]** EC35) The method of EC23, wherein the storage comprises one or more flash  
6 memories and further comprising interfacing with the flash memories.

7  
8 **[0055]** EC36) The method of EC35, wherein the interfacing with the flash memories  
9 comprises operating a flash memory interface.

10  
11 **[0056]** EC37) The method of EC35, further comprising operating at least one of the  
12 flash memories.

13  
14 **[0057]** EC38) The method of EC35, wherein the serially interfacing with the host is at  
15 least in part via operating a host interface, the interfacing with the flash memories is at least in  
16 part via operating a flash memory interface, and the host interface and the flash memory  
17 interface are collectively implemented in a single Integrated Circuit (IC).

18  
19 **[0058]** EC39) The method of EC35, wherein the serially interfacing with the host is at  
20 least in part via operating a host interface, the interfacing with the flash memories is at least in  
21 part via operating a flash memory interface, and the host interface and the flash memory  
22 interface are comprised in a Solid-State Disk (SSD).

23  
24 **[0059]** EC40) The method of EC35, wherein the serially interfacing with the host is at  
25 least in part via operating a host interface, the interfacing with the flash memories is at least in  
26 part via operating a flash memory interface, and the host interface and the flash memory  
27 interface are comprised in a controller of a Solid-State Disk (SSD).

28  
29 **[[0060]** EC41) The method of EC23, wherein a first version of a serial interface  
30 standard specifies operation at a maximum nominal serial data transfer rate that is at or above  
31 the threshold and the first version of the serial interface standard specifies the operating mode  
32 and/or feature.

33  
34 **[[0061]** EC42) The method of EC41, wherein a second version of the serial interface  
35 standard specifies operation at a maximum nominal serial data transfer rate that is below the  
36 threshold.

1  
2 **[[0062]** EC43) The method of EC41, wherein a second version of the serial interface  
3 standard lacks any specification of the operating mode and/or feature.

4  
5 **[[0063]** EC44) The method of EC41, wherein a second version of the serial interface  
6 standard specifies operation at a maximum nominal serial data transfer rate that is below the  
7 threshold and lacks any specification of the operating mode and/or feature.

8  
9 **[0064]** EC45) A system comprising:  
10 host interface circuitry enabled to serially interface a host with storage;  
11 serial data rate determining circuitry enabled to determine if the host interface circuitry  
12 is operating at a nominal serial data transfer rate that is greater/less than a  
13 threshold; and  
14 operating mode and/or feature control circuitry enabled to selectively enable/disable an  
15 operating mode and/or feature, the operating mode and/or feature control  
16 circuitry being dependent at least in part on the serial data rate determining  
17 circuitry.

18  
19 **[0065]** EC46) The system of EC45, wherein the host interface circuitry is compatible  
20 with at least one version of a Serial Advanced Technology Attachment (SATA) standard.

21  
22 **[0066]** EC47) The system of EC45, wherein the threshold is 6Gb.

23  
24 **[0067]** EC48) The system of EC45, wherein the storage comprises a storage  
25 system/sub-system.

26  
27 **[0068]** EC49) The system of EC45, wherein the storage comprises one or more Solid  
28 State Disks (SSDs), Hard Disk Drives (HDDs), Compact Disk (CD) and/or Digital  
29 Versatile/Video Disk (DVD) drives, and tape drives.

30  
31 **[0069]** EC50) The system of EC45, wherein the host interface circuitry is comprised in  
32 a Solid State Disk (SSD), and the storage comprises flash memory comprised in the SSD.

33

- 1   **[0070]**           EC51) The system of EC45, wherein the host interface circuitry is compatible  
2   with at least one version of a Serial Advanced Technology Attachment (SATA) standard, the  
3   threshold is 6Gb, the host interface circuitry is comprised in a Solid State Disk (SSD), and the  
4   storage comprises flash memory comprised in the SSD.  
5
- 6   **[0071]**           EC52) The system of EC45, wherein the host is an interfacing host.  
7
- 8   **[0072]**           EC53) The system of EC52, wherein the interfacing host comprises one or more  
9   of a storage bridge and a storage expander.  
10
- 11   **[0073]**           EC54) The system of EC45, wherein the host is a computing host.  
12
- 13   **[0074]**           EC55) The system of EC54, further comprising all or any portions of the  
14   computing host.  
15
- 16   **[0075]**           EC56) The system of EC45, wherein the host interface circuitry is compatible  
17   with a storage interface standard.  
18
- 19   **[0076]**           EC57) The system of EC45, wherein the storage comprises one or more flash  
20   memories and further comprising flash interface circuitry enabled to interface with the flash  
21   memories.  
22
- 23   **[0077]**           EC58) The system of EC57, wherein the flash interface circuitry comprises a  
24   flash memory interface.  
25
- 26   **[0078]**           EC59) The system of EC57, further comprising at least one of the flash  
27   memories.  
28
- 29   **[0079]**           EC60) The system of EC57, wherein the host interface circuitry and the flash  
30   interface circuitry are collectively implemented in a single Integrated Circuit (IC).  
31
- 32   **[0080]**           EC61) The system of EC57, wherein the host interface circuitry and the flash  
33   interface circuitry are comprised in a Solid-State Disk (SSD).  
34
- 35   **[0081]**           EC62) The system of EC57, wherein the host interface circuitry and the flash  
36   interface circuitry are comprised in a controller of a Solid-State Disk (SSD).

1  
2 **[[0082]** EC63) The system of EC45, wherein a first version of a serial interface standard  
3 specifies operation at a maximum nominal serial data transfer rate that is at or above the  
4 threshold and the first version of the serial interface standard specifies the operating mode and/or  
5 feature.

6  
7 **[[0083]** EC64) The system of EC63, wherein a second version of the serial interface  
8 standard specifies operation at a maximum nominal serial data transfer rate that is below the  
9 threshold.

10  
11 **[[0084]** EC65) The system of EC63, wherein a second version of the serial interface  
12 standard lacks any specification of the operating mode and/or feature.

13  
14 **[[0085]** EC66) The system of EC63, wherein a second version of the serial interface  
15 standard specifies operation at a maximum nominal serial data transfer rate that is below the  
16 threshold and lacks any specification of the operating mode and/or feature.

17  
18 **[0086]** EC67) A tangible computer readable medium having a set of instructions stored  
19 therein that when executed by a processing element cause the processing element to perform  
20 operations comprising:

21 managing serially interfacing a host with storage;  
22 managing determining if the serially interfacing is operating at a nominal serial data  
23 transfer rate that is greater/less than a threshold; and  
24 managing selectively enabling/disabling an operating mode and/or feature, the  
25 selectively enable/disabling being dependent at least in part on the determining.

26  
27 **[0087]** EC68) The tangible computer readable medium of EC67, wherein the serially  
28 interfacing is compatible with at least one version of a Serial Advanced Technology Attachment  
29 (SATA) standard.

30  
31 **[0088]** EC69) The tangible computer readable medium of EC67, wherein the threshold  
32 is 6Gb.

33  
34 **[0089]** EC70) The tangible computer readable medium of EC67, wherein the storage  
35 comprises a storage system/sub-system.

36

1   **[0090]**           EC71) The tangible computer readable medium of EC67, wherein the storage  
2   comprises one or more Solid State Disks (SSDs), Hard Disk Drives (HDDs), Compact Disk  
3   (CD) and/or Digital Versatile/Video Disk (DVD) drives, and tape drives.

4  
5   **[0091]**           EC72) The tangible computer readable medium of EC67, wherein the serially  
6   interfacing is performed in a Solid State Disk (SSD), and the storage comprises flash memory  
7   comprised in the SSD.

8  
9   **[0092]**           EC73) The tangible computer readable medium of EC67, wherein the serially  
10   interfacing is compatible with at least one version of a Serial Advanced Technology Attachment  
11   (SATA) standard, the threshold is 6Gb, the serially interfacing is performed in a Solid State Disk  
12   (SSD), and the storage comprises flash memory comprised in the SSD.

13  
14   **[0093]**           EC74) The tangible computer readable medium of EC67, wherein the host is an  
15   interfacing host.

16  
17   **[0094]**           EC75) The tangible computer readable medium of EC74, wherein the  
18   interfacing host comprises one or more of a storage bridge and a storage expander.

19  
20   **[0095]**           EC76) The tangible computer readable medium of EC67, wherein the host is a  
21   computing host.

22  
23   **[0096]**           EC77) The tangible computer readable medium of EC76, further comprising  
24   managing operating all or any portions of the computing host.

25  
26   **[0097]**           EC78) The tangible computer readable medium of EC67, wherein the serially  
27   interfacing is compatible with a storage interface standard.

28  
29   **[0098]**           EC79) The tangible computer readable medium of EC67, wherein the storage  
30   comprises one or more flash memories and further comprising managing interfacing with the  
31   flash memories.

32  
33   **[0099]**           EC80) The tangible computer readable medium of EC79, wherein the managing  
34   interfacing with the flash memories comprises managing operating a flash memory interface.

35

1   **[0100]**           EC81) The tangible computer readable medium of EC79, further comprising  
2   managing operating at least one of the flash memories.

3

4   **[0101]**           EC82) The tangible computer readable medium of EC79, wherein the managing  
5   serially interfacing with the host is at least in part via managing operating a host interface, the  
6   managing interfacing with the flash memories is at least in part via managing operating a flash  
7   memory interface and the host interface, and the flash memory interface are collectively  
8   implemented in a single Integrated Circuit (IC).

9

10   **[0102]**           EC83) The tangible computer readable medium of EC79, wherein the managing  
11   serially interfacing with the host is at least in part via managing operating a host interface, the  
12   managing interfacing with the flash memories is at least in part via managing operating a flash  
13   memory interface and the host interface, and the flash memory interface are comprised in a  
14   Solid-State Disk (SSD).

15

16   **[0103]**           EC84) The tangible computer readable medium of EC79, wherein the managing  
17   serially interfacing with the host is at least in part via managing operating a host interface, the  
18   managing interfacing with the flash memories is at least in part via managing operating a flash  
19   memory interface and the host interface, and the flash memory interface are comprised in a  
20   controller of a Solid-State Disk (SSD).

21

22   **[[0104]**           EC85) The tangible computer readable medium of EC67, wherein a first version  
23   of a serial interface standard specifies operation at a maximum nominal serial data transfer rate  
24   that is at or above the threshold and the first version of the serial interface standard specifies the  
25   operating mode and/or feature.

26

27   **[[0105]**           EC86) The tangible computer readable medium of EC85, wherein a second  
28   version of the serial interface standard specifies operation at a maximum nominal serial data  
29   transfer rate that is below the threshold.

30

31   **[[0106]**           EC87) The tangible computer readable medium of EC85, wherein a second  
32   version of the serial interface standard lacks any specification of the operating mode and/or  
33   feature.

34

- 1    [[0107]           EC88) The tangible computer readable medium of EC85, wherein a second  
2    version of the serial interface standard specifies operation at a maximum nominal serial data  
3    transfer rate that is below the threshold and lacks any specification of the operating mode and/or  
4    feature.  
5
- 6    [0108]           EC89) Any of the foregoing ECs having or referring to a storage interface  
7    standard, wherein the storage interface standard comprises one or more of  
8           a Universal Serial Bus (USB) interface standard,  
9           a Compact Flash (CF) interface standard,  
10          a MultiMediaCard (MMC) interface standard,  
11          an embedded MMC (eMMC) interface standard,  
12          a Thunderbolt interface standard,  
13          a UFS interface standard,  
14          a Secure Digital (SD) interface standard,  
15          a Memory Stick interface standard,  
16          an xD-picture card interface standard,  
17          an Integrated Drive Electronics (IDE) interface standard,  
18          a Serial Advanced Technology Attachment (SATA) interface standard,  
19          an external SATA (eSATA) interface standard,  
20          a Small Computer System Interface (SCSI) interface standard,  
21          a Serial Attached Small Computer System Interface (SAS) interface standard,  
22          a Fibre Channel interface standard,  
23          an Ethernet interface standard, and  
24          a Peripheral Component Interconnect express (PCIe) interface standard.  
25

1    **[0109]**           EC90) Any of the foregoing ECs having or referring to a computing host,  
2    wherein the computing host comprises all or any portions of one or more of  
3           a computer,  
4           a workstation computer,  
5           a server computer,  
6           a storage server,  
7           a Storage Attached Network (SAN),  
8           a Network Attached Storage (NAS) device,  
9           a Direct Attached Storage (DAS) device,  
10          a storage appliance,  
11          a Personal Computer (PC),  
12          a laptop computer,  
13          a notebook computer,  
14          a netbook computer,  
15          a tablet device or computer,  
16          an ultrabook computer,  
17          an electronic reading device (an e-reader),  
18          a Personal Digital Assistant (PDA),  
19          a navigation system,  
20          a (handheld) Global Positioning System (GPS) device,  
21          an automotive control system,  
22          an automotive media control system or computer,  
23          a printer, copier or fax machine or all-in-one device,  
24          a Point Of Sale (POS) device,  
25          a cash-register,  
26          a media player,  
27          a television,  
28          a media recorder,  
29          a Digital Video Recorder (DVR),  
30          a digital camera,  
31          a cellular handset,  
32          a cordless telephone handset, and  
33          an electronic game.  
34

1   **[0110]**           EC91) Any of the foregoing ECs having or referring to a at least one flash  
2   memory, wherein at least a portion of the at least one flash memory comprises one or more of  
3           NAND flash technology storage cells, and  
4           NOR flash technology storage cells.

5

6   **[0111]**           EC92) Any of the foregoing ECs having or referring to a at least one flash  
7   memory, wherein at least a portion of the at least one flash memory comprises one or more of  
8           Single-Level Cell (SLC) flash technology storage cells, and  
9           Multi-Level Cell (MLC) flash technology storage cells.

10

11   **[0112]**           EC93) Any of the foregoing ECs having or referring to a at least one flash  
12   memory, wherein at least a portion of the at least one flash memory comprises one or more of  
13           polysilicon technology-based charge storage cells, and  
14           silicon nitride technology-based charge storage cells.

15

16   **[0113]**           EC94) Any of the foregoing ECs having or referring to a at least one flash  
17   memory, wherein at least a portion of the at least one flash memory comprises one or more of  
18           two-dimensional technology-based flash memory technology, and  
19           three-dimensional technology-based flash memory technology.

20

21   **[0114]**           EC95) Any of the foregoing ECs having or referring to a flash memory  
22   interface, wherein the flash memory interface is compatible with one or more of  
23           an Open NAND Flash Interface (ONFI),  
24           a Toggle-mode interface,  
25           a Double-Data-Rate (DDR) synchronous interface,  
26           a DDR2 synchronous interface,  
27           a synchronous interface, and  
28           an asynchronous interface.

29

30

1 SYSTEM

2

3 **[0115]** Fig. 1A illustrates selected details of an embodiment of an SSD including an  
4 SSD controller providing various techniques for selective enablement of one or more operating  
5 modes and/or one or more features (such as status coalescing) via host transfer rate detection for  
6 managing an interface with a (computing) host, as well as circuitry for managing non-volatile  
7 storage, such as flash memories. The SSD controller is for managing non-volatile storage, such  
8 as implemented via NVM elements (e.g., flash memories). SSD Controller **100** is  
9 communicatively coupled via one or more External Interfaces **110** to a host (not illustrated).  
10 According to various embodiments, External Interfaces **110** are one or more of: a SATA  
11 interface; a SAS interface; a PCIe interface; a Fibre Channel interface; an Ethernet Interface  
12 (such as 10 Gigabit Ethernet); a non-standard version of any of the preceding interfaces; a  
13 custom interface; or any other type of interface used to interconnect storage and/or  
14 communications and/or computing devices. For example, in some embodiments, SSD  
15 Controller **100** includes a SATA interface and a PCIe interface.

16

17 **[0116]** SSD Controller **100** is further communicatively coupled via one or more Device  
18 Interfaces **190** to NVM **199** including one or more storage devices, such as one or more of Flash  
19 Device **192**. According to various embodiments, Device Interfaces **190** are one or more of: an  
20 asynchronous interface; a synchronous interface; a single-data-rate (SDR) interface; a double-  
21 data-rate (DDR) interface; a DRAM-compatible DDR or DDR2 synchronous interface; an ONFI  
22 compatible interface, such as an ONFI 2.2 or ONFI 3.0 compatible interface; a Toggle-mode  
23 compatible flash interface; a non-standard version of any of the preceding interfaces; a custom  
24 interface; or any other type of interface used to connect to storage devices.

25

26 **[0117]** Each Flash Device **192** has, in some embodiments, one or more individual Flash  
27 Die **194**. According to type of a particular one of Flash Device **192**, a plurality of Flash Die **194**  
28 in the particular Flash Device **192** is optionally and/or selectively accessible in parallel. Flash  
29 Device **192** is merely representative of one type of storage device enabled to communicatively  
30 couple to SSD Controller **100**. In various embodiments, any type of storage device is usable,  
31 such as an SLC NAND flash memory, MLC NAND flash memory, NOR flash memory, flash  
32 memory using polysilicon or silicon nitride technology-based charge storage cells, two- or three-  
33 dimensional technology-based flash memory, read-only memory, static random access memory,  
34 dynamic random access memory, ferromagnetic memory, phase-change memory, racetrack  
35 memory, or any other type of memory device or storage medium.

36

1     **[0118]**           According to various embodiments, Device Interfaces **190** are organized as:  
2     one or more busses with one or more of Flash Device **192** per bus; one or more groups of busses  
3     with one or more of Flash Device **192** per bus, where busses in a group are generally accessed in  
4     parallel; or any other organization of one or more of Flash Device **192** onto Device Interfaces  
5     **190**.

6  
7     **[0119]**           Continuing in Fig. 1A, SSD Controller **100** has one or more modules, such as  
8     Host Interfaces **111**, Data Processing **121**, Buffer **131**, Map **141**, Recycler **151**, ECC **161**, Device  
9     Interface Logic **191**, and CPU **171**. The specific modules and interconnections illustrated in Fig.  
10    1A are merely representative of one embodiment, and many arrangements and interconnections  
11    of some or all of the modules, as well as additional modules not illustrated, are conceived. In a  
12    first example, in some embodiments, there are two or more Host Interfaces **111** to provide dual-  
13    porting. In a second example, in some embodiments, Data Processing **121** and/or ECC **161** are  
14    combined with Buffer **131**. In a third example, in some embodiments, Host Interfaces **111** is  
15    directly coupled to Buffer **131**, and Data Processing **121** optionally and/or selectively operates  
16    on data stored in Buffer **131**. In a fourth example, in some embodiments, Device Interface Logic  
17    **191** is directly coupled to Buffer **131**, and ECC **161** optionally and/or selectively operates on  
18    data stored in Buffer **131**.

19  
20    **[0120]**           Host Interfaces **111** sends and receives commands and/or data via External  
21    Interfaces **110**, and, in some embodiments, tracks progress of individual commands via Tag  
22    Tracking **113**. For example, the commands include a read command specifying an address (such  
23    as an LBA) and an amount of data (such as a number of LBA quanta, e.g., sectors) to read; in  
24    response the SSD provides read status and/or read data. For another example, the commands  
25    include a write command specifying an address (such as an LBA) and an amount of data (such  
26    as a number of LBA quanta, e.g., sectors) to write; in response the SSD provides write status  
27    and/or requests write data and optionally subsequently provides write status. For yet another  
28    example, the commands include a de-allocation command (e.g. a trim command) specifying one  
29    or more addresses (such as one or more LBAs) that no longer need be allocated; in response the  
30    SSD modifies the map accordingly and optionally provides de-allocation status. In some  
31    contexts an ATA compatible TRIM command is an exemplary de-allocation command. For yet  
32    another example, the commands include a super capacitor test command or a data hardening  
33    success query; in response, the SSD provides appropriate status. In some embodiments, Host  
34    Interfaces **111** is compatible with a SATA protocol and, using NCQ commands, is enabled to  
35    have up to 32 pending commands, each with a unique tag represented as a number from 0 to 31.  
36    In some embodiments, Tag Tracking **113** is enabled to associate an external tag for a command

received via External Interfaces **110** with an internal tag used to track the command during processing by SSD Controller **100**.

**[0121]** According to various embodiments, one or more of: Data Processing **121** optionally and/or selectively processes some or all data sent between Buffer **131** and External Interfaces **110**; and Data Processing **121** optionally and/or selectively processes data stored in Buffer **131**. In some embodiments, Data Processing **121** uses one or more Engines **123** to perform one or more of: formatting; reformatting; transcoding; and any other data processing and/or manipulation task.

**[0122]** Buffer **131** stores data sent to/from External Interfaces **110** from/to Device Interfaces **190**. In some embodiments, Buffer **131** additionally stores system data, such as some or all map tables, used by SSD Controller **100** to manage one or more of Flash Device **192**. In various embodiments, Buffer **131** has one or more of: Memory **137** used for temporary storage of data; DMA **133** used to control movement of data to and/or from Buffer **131**; and ECC-X **135** used to provide higher-level error correction and/or redundancy functions; and other data movement and/or manipulation functions. An example of a higher-level redundancy function is a RAID-like capability (e.g. RASIE), where redundancy is at a flash device (e.g., multiple ones of Flash Device **192**) level and/or a flash die (e.g., Flash Die **194**) level instead of at a disk level.

**[0123]** According to various embodiments, one or more of: ECC **161** optionally and/or selectively processes some or all data sent between Buffer **131** and Device Interfaces **190**; and ECC **161** optionally and/or selectively processes data stored in Buffer **131**. In some embodiments, ECC **161** is used to provide lower-level error correction and/or redundancy functions, such as in accordance with one or more ECC techniques. In some embodiments, ECC **161** implements one or more of: a CRC code; a Hamming code; an RS code; a BCH code; an LDPC code; a Viterbi code; a trellis code; a hard-decision code; a soft-decision code; an erasure-based code; any error detecting and/or correcting code; and any combination of the preceding. In some embodiments, ECC **161** includes one or more decoders (such as LDPC decoders).

**[0124]** Device Interface Logic **191** controls instances of Flash Device **192** via Device Interfaces **190**. Device Interface Logic **191** is enabled to send data to/from the instances of Flash Device **192** according to a protocol of Flash Device **192**. Device Interface Logic **191** includes Scheduling **193** to selectively sequence control of the instances of Flash Device **192** via Device Interfaces **190**. For example, in some embodiments, Scheduling **193** is enabled to queue operations to the instances of Flash Device **192**, and to selectively send the operations to

individual ones of the instances of Flash Device **192** (or Flash Die **194**) as individual ones of the instances of Flash Device **192** (or Flash Die **194**) are available.

**[0125]** Map **141** converts between data addressing used on External Interfaces **110** and data addressing used on Device Interfaces **190**, using Table **143** to map external data addresses to locations in NVM **199**. For example, in some embodiments, Map **141** converts LBAs used on External Interfaces **110** to block and/or page addresses targeting one or more Flash Die **194**, via mapping provided by Table **143**. For LBAs that have never been written since drive manufacture or de-allocation, the map points to a default value to return if the LBAs are read. For example, when processing a de-allocation command, the map is modified so that entries corresponding to the de-allocated LBAs point to one of the default values. In various embodiments, there are various default values, each having a corresponding pointer. The plurality of default values enables reading some de-allocated LBAs (such as in a first range) as one default value, while reading other de-allocated LBAs (such as in a second range) as another default value. The default values, in various embodiments, are defined by flash memory, hardware, firmware, command and/or primitive arguments and/or parameters, programmable registers, or various combinations thereof.

**[0126]** In some embodiments, Map **141** uses Table **143** to perform and/or to look up translations between addresses used on External Interfaces **110** and data addressing used on Device Interfaces **190**. According to various embodiments, Table **143** is one or more of: a one-level map; a two-level map; a multi-level map; a map cache; a compressed map; any type of mapping from one address space to another; and any combination of the foregoing. According to various embodiments, Table **143** includes one or more of: static random access memory; dynamic random access memory; NVM (such as flash memory); cache memory; on-chip memory; off-chip memory; and any combination of the foregoing.

**[0127]** In some embodiments, Recycler **151** performs garbage collection. For example, in some embodiments, instances of Flash Device **192** contain blocks that must be erased before the blocks are re-writeable. Recycler **151** is enabled to determine which portions of the instances of Flash Device **192** are actively in use (e.g., allocated instead of de-allocated), such as by scanning a map maintained by Map **141**, and to make unused (e.g., de-allocated) portions of the instances of Flash Device **192** available for writing by erasing them. In further embodiments, Recycler **151** is enabled to move data stored within instances of Flash Device **192** to make larger contiguous portions of the instances of Flash Device **192** available for writing.

1   **[0128]**           In some embodiments, instances of Flash Device **192** are selectively and/or  
2   dynamically configured, managed, and/or used to have one or more bands for storing data of  
3   different types and/or properties. A number, arrangement, size, and type of the bands are  
4   dynamically changeable. For example, data from a computing host is written into a hot (active)  
5   band, while data from Recycler **151** is written into a cold (less active) band. In some usage  
6   scenarios, if the computing host writes a long, sequential stream, then a size of the hot band  
7   grows, whereas if the computing host does random writes or few writes, then a size of the cold  
8   band grows.

9  
10   **[0129]**           CPU **171** controls various portions of SSD Controller **100**. CPU **171** includes  
11   CPU Core **172**. CPU Core **172** is, according to various embodiments, one or more single-core or  
12   multi-core processors. The individual processors cores in CPU Core **172** are, in some  
13   embodiments, multi-threaded. CPU Core **172** includes instruction and/or data caches and/or  
14   memories. For example, the instruction memory contains instructions to enable CPU Core **172**  
15   to execute programs (e.g. software sometimes called firmware) to control SSD Controller **100**.  
16   In some embodiments, some or all of the firmware executed by CPU Core **172** is stored on  
17   instances of Flash Device **192** (as illustrated, e.g., as Firmware **106** of NVM **199** in Fig. 1B).

18  
19   **[0130]**           In various embodiments, CPU **171** further includes: Command Management  
20   **173** to track and control commands received via External Interfaces **110** while the commands are  
21   in progress; Buffer Management **175** to control allocation and use of Buffer **131**; Translation  
22   Management **177** to control Map **141**; Coherency Management **179** to control consistency of  
23   data addressing and to avoid conflicts such as between external data accesses and recycle data  
24   accesses; Device Management **181** to control Device Interface Logic **191**; Identity Management  
25   **182** to control modification and communication of identify information, and optionally other  
26   management units. None, any, or all of the management functions performed by CPU **171** are,  
27   according to various embodiments, controlled and/or managed by hardware, by software (such  
28   as firmware executing on CPU Core **172** or on a host connected via External Interfaces **110**), or  
29   any combination thereof.

30  
31   **[0131]**           In some embodiments, CPU **171** is enabled to perform other management tasks,  
32   such as one or more of: gathering and/or reporting performance statistics; implementing  
33   SMART; controlling power sequencing, controlling and/or monitoring and/or adjusting power  
34   consumption; responding to power failures; controlling and/or monitoring and/or adjusting clock  
35   rates; and other management tasks.

36

1   **[0132]**        Various embodiments include a computing-host flash memory controller that is  
2    similar to SSD Controller **100** and is compatible with operation with various computing hosts,  
3    such as via adaptation of Host Interfaces **111** and/or External Interfaces **110**. The various  
4    computing hosts include one or any combination of a computer, a workstation computer, a  
5    server computer, a storage server, a SAN, a NAS device, a DAS device, a storage appliance, a  
6    PC, a laptop computer, a notebook computer, a netbook computer, a tablet device or computer,  
7    an ultrabook computer, an electronic reading device (such as an e-reader), a PDA, a navigation  
8    system, a (handheld) GPS device, an automotive control system, an automotive media control  
9    system or computer, a printer, copier or fax machine or all-in-one device, a POS device, a cash-  
10   register, a media player, a television, a media recorder, a DVR, a digital camera, a cellular  
11   handset, a cordless telephone handset, and an electronic game.

12  
13   **[0133]**        In various embodiments, all or any portions of an SSD controller (or a  
14    computing-host flash memory controller) are implemented on a single IC, a single die of a multi-  
15    die IC, a plurality of dice of a multi-die IC, or a plurality of ICs. For example, Buffer **131** is  
16    implemented on a same die as other elements of SSD Controller **100**. For another example,  
17    Buffer **131** is implemented on a different die than other elements of SSD Controller **100**.

18  
19   **[0134]**        Fig. 1B illustrates selected details of various embodiments of systems including  
20    one or more instances of the SSD of Fig. 1A. SSD **101** includes SSD Controller **100** coupled to  
21    NVM **199** via Device Interfaces **190**. The figure illustrates various classes of embodiments: a  
22    single SSD coupled directly to a host, a plurality of SSDs each respectively coupled directly to a  
23    host via respective external interfaces, and one or more SSDs coupled indirectly to a host via  
24    various interconnection elements.

25  
26   **[0135]**        As an example embodiment of a single SSD coupled directly to a host, one  
27    instance of SSD **101** is coupled directly to Host **102** via External Interfaces **110** (e.g. Switch /  
28    Fabric / Intermediate Controller **103** is omitted, bypassed, or passed-through). As an example  
29    embodiment of a plurality of SSDs each coupled directly to a host via respective external  
30    interfaces, each of a plurality of instances of SSD **101** is respectively coupled directly to Host  
31    **102** via a respective instance of External Interfaces **110** (e.g. Switch / Fabric / Intermediate  
32    Controller **103** is omitted, bypassed, or passed-through). As an example embodiment of one or  
33    more SSDs coupled indirectly to a host via various interconnection elements, each of one or  
34    more instances of SSD **101** is respectively coupled indirectly to Host **102**. Each indirect  
35    coupling is via a respective instance of External Interfaces **110** coupled to Switch / Fabric /  
36    Intermediate Controller **103**, and Intermediate Interfaces **104** coupling to Host **102**.

1  
2 **[0136]** Some of the embodiments including Switch / Fabric / Intermediate Controller  
3 **103** also include Card Memory **112C** coupled via Memory Interface **180** and accessible by the  
4 SSDs. In various embodiments, one or more of the SSDs, the Switch / Fabric / Intermediate  
5 Controller, and/or the Card Memory are included on a physically identifiable module, card, or  
6 pluggable element (e.g. I/O Card **116**). In some embodiments, SSD **101** (or variations thereof)  
7 corresponds to a SAS drive or a SATA drive that is coupled to an initiator operating as Host **102**.  
8

9 **[0137]** Host **102** is enabled to execute various elements of Host Software **115**, such as  
10 various combinations of OS **105**, Driver **107**, Application **109**, and Multi-Device Management  
11 Software **114**. Dotted-arrow **107D** is representative of Host Software  $\leftrightarrow$  I/O Device  
12 Communication, e.g. data sent/received to/from one or more of the instances of SSD **101** and  
13 from/to any one or more of OS **105** via Driver **107**, Driver **107**, and Application **109**, either via  
14 Driver **107**, or directly as a VF.  
15

16 **[0138]** OS **105** includes and/or is enabled to operate with drivers (illustrated  
17 conceptually by Driver **107**) for interfacing with the SSD. Various versions of Windows (e.g.  
18 95, 98, ME, NT, XP, 2000, Server, Vista, and 7), various versions of Linux (e.g. Red Hat,  
19 Debian, and Ubuntu), and various versions of MacOS (e.g. 8, 9 and X) are examples of OS **105**.  
20 In various embodiments, the drivers are standard and/or generic drivers (sometimes termed  
21 “shrink-wrapped” or “pre-installed”) operable with a standard interface and/or protocol such as  
22 SATA, AHCI, or NVMe Express, or are optionally customized and/or vendor specific to enable  
23 use of commands specific to SSD **101**. Some drives and/or drivers have pass-through modes to  
24 enable application-level programs, such as Application **109** via Optimized NAND Access  
25 (sometimes termed ONA) or Direct NAND Access (sometimes termed DNA) techniques, to  
26 communicate commands directly to SSD **101**, enabling a customized application to use  
27 commands specific to SSD **101** even with a generic driver. ONA techniques include one or  
28 more of: use of non-standard modifiers (hints); use of vendor-specific commands;  
29 communication of non-standard statistics, such as actual NVM usage according to  
30 compressibility; and other techniques. DNA techniques include one or more of: use of non-  
31 standard commands or vendor-specific providing unmapped read, write, and/or erase access to  
32 the NVM; use of non-standard or vendor-specific commands providing more direct access to the  
33 NVM, such as by bypassing formatting of data that the I/O device would otherwise do; and other  
34 techniques. Examples of the driver are a driver without ONA or DNA support, an ONA-enabled  
35 driver, a DNA-enabled driver, and an ONA/DNA-enabled driver. Further examples of the driver

1 are a vendor-provided, vendor-developed, and/or vendor-enhanced driver, and a client-provided,  
2 client-developed, and/or client-enhanced driver.

3  
4 **[0139]** Examples of the application-level programs are an application without ONA or  
5 DNA support, an ONA-enabled application, a DNA-enabled application, and an ONA/DNA-  
6 enabled application. Dotted-arrow **109D** is representative of Application  $\leftrightarrow$  I/O Device  
7 Communication (e.g. bypass via a driver or bypass via a VF for an application), e.g. an ONA-  
8 enabled application and an ONA-enabled driver communicating with an SSD, such as without  
9 the application using the OS as an intermediary. Dotted-arrow **109V** is representative of  
10 Application  $\leftrightarrow$  I/O Device Communication (e.g. bypass via a VF for an application), e.g. a  
11 DNA-enabled application and a DNA-enabled driver communicating with an SSD, such as  
12 without the application using the OS or the driver as intermediaries.

13  
14 **[0140]** One or more portions of NVM **199** are used, in some embodiments, for  
15 firmware storage, e.g. Firmware **106**. The firmware storage includes one or more firmware  
16 images (or portions thereof). A firmware image has, for example, one or more images of  
17 firmware, executed, e.g., by CPU Core **172** of SSD Controller **100**. A firmware image has, for  
18 another example, one or more images of constants, parameter values, and NVM device  
19 information, referenced, e.g. by the CPU core during the firmware execution. The images of  
20 firmware correspond, e.g., to a current firmware image and zero or more previous (with respect  
21 to firmware updates) firmware images. In various embodiments, the firmware provides for  
22 generic, standard, ONA, and/or DNA operating modes. In some embodiments, one or more of  
23 the firmware operating modes are enabled (e.g. one or more APIs are “unlocked”) via keys or  
24 various software techniques, optionally communicated and/or provided by a driver.

25  
26 **[0141]** In some embodiments lacking the the Switch / Fabric / Intermediate Controller,  
27 the SSD is coupled to the host directly via External Interfaces **110**. In various embodiments,  
28 SSD Controller **100** is coupled to the host via one or more intermediate levels of other  
29 controllers, such as a RAID controller. In some embodiments, SSD **101** (or variations thereof)  
30 corresponds to a SAS drive or a SATA drive and Switch / Fabric / Intermediate Controller **103**  
31 corresponds to an expander that is in turn coupled to an initiator, or alternatively Switch / Fabric  
32 / Intermediate Controller **103** corresponds to a bridge that is indirectly coupled to an initiator via  
33 an expander. In some embodiments, Switch / Fabric / Intermediate Controller **103** includes one  
34 or more PCIe switches and/or fabrics.

35

1     **[0142]**           In various embodiments, such as some of the embodiments where Host **102** is a  
2     computing host (e.g. a computer, a workstation computer, a server computer, a storage server, a  
3     SAN, a NAS device, a DAS device, a storage appliance, a PC, a laptop computer, a notebook  
4     computer, and/or a netbook computer), the computing host is optionally enabled to communicate  
5     (e.g. via optional I/O & Storage Devices/Resources **117** and optional LAN/WAN **119**) with one  
6     or more local and/or remote servers (e.g. optional Servers **118**). The communication enables, for  
7     example, local and/or remote access, management, and/or usage of any one or more of SSD **101**  
8     elements. In some embodiments, the communication is wholly or partially via Ethernet. In  
9     some embodiments, the communication is wholly or partially via Fibre Channel. LAN/WAN  
10    **119** is representative, in various embodiments, of one or more Local and/or Wide Area  
11    Networks, such as any one or more of a network in a server farm, a network coupling server  
12    farms, a metro-area network, and the Internet.

13

14   **[0143]**           In various embodiments, an SSD controller and/or a computing-host flash  
15    memory controller in combination with one or more NVMs are implemented as a non-volatile  
16    storage component, such as a USB storage component, a CF storage component, an MMC  
17    storage component, an eMMC storage component, a Thunderbolt storage component, a UFS  
18    storage component, an SD storage component, a Memory Stick storage component, and an xD-  
19    picture card storage component.

20

21   **[0144]**           In various embodiments, all or any portions of an SSD controller (or a  
22    computing-host flash memory controller), or functions thereof, are implemented in a host that  
23    the controller is to be coupled with (e.g., Host **102** of Fig. 1B). In various embodiments, all or  
24    any portions of an SSD controller (or a computing-host flash memory controller), or functions  
25    thereof, are implemented via hardware (e.g., logic circuitry), software and/or firmware (e.g.,  
26    driver software or SSD control firmware), or any combination thereof. For example,  
27    functionality of or associated with an ECC unit (such as similar to ECC **161** and/or ECC-X **135**  
28    of Fig. 1A) is implemented partially via software on a host and partially via a combination of  
29    firmware and hardware in an SSD controller. For another example, functionality of or  
30    associated with a recycler unit (such as similar to Recycler **151** of Fig. 1A) is implemented  
31    partially via software on a host and partially via hardware in a computing-host flash memory  
32    controller.

33

34   **[0145]**           Fig. 1C illustrates selected details of an embodiment of a system including the  
35    SSD of Fig. 1A. SSD **101** includes SSD Controller **100** coupled to NVM **199** via Device  
36    Interfaces **190**. The SSD is coupled to any combination of Host 6G **102A**, Host 3G/1.5G **102B**,

1 and Host 3G/1.5G **102C** via External Interfaces **110** as indicated conceptually by dashed lines  
2 Negotiation **1100DA**, Negotiation **1100DB**, and Negotiation **1100DC** (as described in more  
3 detail with respect to Fig. 2). In various embodiments, any one or more of Host 6G **102A**, Host  
4 3G/1.5G **102B**, and Host 3G/1.5G **102C** correspond to various implementations of Host **102** of  
5 Fig. 1B. In some embodiments, SSD **101** (or variations thereof) corresponds to a SAS drive or a  
6 SATA drive that is coupled to an initiator operating as any one or more of Host **102**, Host 6G  
7 **102A**, Host 3G/1.5G **102B**, and Host 3G/1.5G **102C**. In various embodiments and/or usage  
8 scenarios, embodiments represented by Fig. 1C correspond to embodiments represented by Fig.  
9 1B when Switch / Fabric / Intermediate Controller **103** is, e.g., omitted, bypassed, or passed-  
10 through.

11  
12 **[0146]** Fig. 1D illustrates selected details of an embodiment of a system including the  
13 SSD of Fig. 1A. As in Fig. 1C, SSD **101** includes SSD Controller **100** coupled to NVM **199** via  
14 Device Interfaces **190**. The SSD is coupled to any combination of Host 6G **102A**, Host 3G/1.5G  
15 **102B**, and Host 3G/1.5G **102C** via External Interfaces **110** in turn coupled to Switch / Fabric /  
16 Intermediate Controller **103** and then to any combination of Host 6G **102A**, Host 3G/1.5G **102B**,  
17 and Host 3G/1.5G **102C** via Intermediate Interfaces **104** as indicated conceptually by dashed  
18 lines Negotiation **1100IA**, Negotiation **1100IB**, and Negotiation **1100IC** (as described in more  
19 detail with respect to Fig. 2). In various embodiments, SSD Controller **100** is coupled to the  
20 host(s) via one or more intermediate levels of other controllers, such as a RAID controller. In  
21 some embodiments, SSD **101** (or variations thereof) corresponds to a SAS drive or a SATA  
22 drive and Switch / Fabric / Intermediate Controller **103** corresponds to an expander that is in turn  
23 coupled to an initiator, or alternatively Switch / Fabric / Intermediate Controller **103** corresponds  
24 to a bridge that is indirectly coupled to an initiator via an expander. In various embodiments  
25 and/or usage scenarios, embodiments represented by Fig. 1D correspond to embodiments  
26 represented by Fig. 1B when Switch / Fabric / Intermediate Controller **103** is, e.g., present and  
27 not bypassed or passed-through.

28  
29 **[0147]** In some embodiments and/or usage scenarios, Host 6G **102A**, Host 3G/1.5G  
30 **102B**, and Host 3G/1.5G **102C** are hosts each with a serial interface (such as a SATA interface).  
31 For example, Host 6G **102A** is enabled to transfer serial data at a maximum rate termed a “6Gb”  
32 rate having a nominal 6Gb rate (and is also enabled to transfer data at lower rates termed “3Gb”  
33 and “1.5Gb” rates having respective 3Gb and 1.5Gb nominal rates), while hosts 3G/1.5G **102B**  
34 and **102C** are enabled to transfer data at a maximum rate of the 3Gb rate (and are also enabled to  
35 transfer data at a lower rate such as the 1.5Gb rate).

36

SELECTIVE ENABLEMENT OF STATUS COALESCING  
VIA HOST TRANSFER RATE DETECTION

**[0148]** In some embodiments and/or usage scenarios (such as some embodiments where a host is coupled to a storage system/sub-system, e.g. a computing host coupled to an SSD via a serial interface), status coalescing enables enhanced performance. However, some hosts, such as some hosts that are not fully compliant with a particular serial interface standard (e.g. some embodiments where the host is not fully compliant with a particular SATA standard), are not enabled to properly process coalesced status information. Selective enablement of status coalescing via detection of host transfer rate of the serial interface disables status coalescing in situations where a non-compliant host is not enabled to properly process coalesced status and enables status coalescing in at least some situations where a compliant host is enabled to properly process coalesced status, without the storage system/sub-system having prior knowledge of coupling to a non-compliant or to a compliant host. The storage system/sub-system conservatively determines the host is non-compliant or compliant based on a negotiated speed of the serial interface with the host (e.g. a nominal serial data rate of a SATA interface).

**[0149]** With respect to Figs. 1C and 1D, in some embodiments and/or usage scenarios, Host 6G **102A** is compliant with a particular SATA standard and enabled to transfer data at a maximum nominal 6Gb rate (as well as nominal 3Gb and 1.5Gb rates), while Host 3G/1.5G **102B** is compliant with the particular SATA standard and enabled to transfer data at 3Gb or 1.5Gb rates (but not at a 6Gb rate). Further, Host 3G/1.5G **102C** is not fully compliant with the particular SATA standard (e.g. is unable to properly process coalesced status information) and is enabled to transfer data at nominal 3Gb or 1.5Gb rates (but not at 6Gb).

**[0150]** Fig. 2 illustrates a flow diagram of selected details of an embodiment of selective enablement of status coalescing via host transfer rate detection. Flow Diagram **200** is an example of operation of an SSD with an included controller (such as SSD **101** with SSD Controller **100** of Figs. 1C and 1D) when coupling to hosts of various transfer rate capabilities (such as Host 6G **102A**, Host 3G/1.5G **102B**, and Host 3G/1.5G **102C** directly as in Fig. 1C or indirectly as in Fig. 1D).

**[0151]** When the controller and the host are coupled, when a system reset occurs, when power is applied, or when any other even occurs that initiates a data rate negotiation between the host and the controller, flow begins (Start, **201**). The host and the controller agree on a data

1 transfer rate (Negotiate Speed with Host, **202**). If the agreed data transfer rate is nominally 6Gb  
2 (6G OK?, **203**), then flow proceeds to turn on status combining (Enable Status Coalescing, **205**),  
3 and flow is complete (End, **299**). If the agreed data transfer rate is not nominally 6Gb, then flow  
4 proceeds to turn off status combining (Disable Status Coalescing, **204**). Flow is then complete  
5 (End, **299**). After flow is complete, then the controller responds to host requests and returns  
6 status in response to certain requests, the returned status being at times coalesced when  
7 coalescing has been enabled and never coalesced when coalescing has been disabled. In various  
8 embodiments, rather than a determination that a transfer rate is a nominal value (e.g. 6Gb), a  
9 determination is made that a transfer rate is above (or below) a nominal value, such as a  
10 predetermined threshold value.

11

12 **[0152]** As a first example of operation of Flow Diagram **200**, consider SSD **101** with  
13 SSD Controller **100** coupling to Host 6G **102A** (as illustrated in Fig. 1C). Host 6G **102A** is  
14 compliant with a particular SATA standard, being enabled to properly process coalesced status  
15 information and further enabled to transfer data at a maximum nominal 6Gb rate. With respect  
16 to Fig. 2, the host and the controller agree on a data transfer rate (Negotiate Speed with Host,  
17 **202**) and the negotiation is indicated conceptually by dashed line Negotiation **1100DA** in Fig.  
18 1C. The host requests and obtains the maximum data rate of 6Gb, and thus the agreed nominal  
19 data transfer rate is 6Gb, so flow proceeds to turn on status combining (Enable Status  
20 Coalescing, **205**). Flow is then complete. The controller then proceeds to operate with status  
21 coalescing enabled, returning status information to the host coalesced in some situations,  
22 enabling enhanced performance in some situations.

23

24 **[0153]** As a second example of operation of Flow Diagram **200**, consider SSD **101** with  
25 SSD Controller **100** coupling to Host 3G/1.5G **102B** (as illustrated in Fig. 1C). Host 3G/1.5G  
26 **102B** is compliant with a particular SATA standard, being enabled to properly process coalesced  
27 status information and further enabled to transfer data at a maximum nominal 3Gb rate. With  
28 respect to Fig. 2, the host and the controller agree on a data transfer rate (Negotiate Speed with  
29 Host, **202**) and the negotiation is indicated conceptually by dashed line Negotiation **1100DB** in  
30 Fig. 1C. The host requests and obtains the maximum data rate of 3Gb, and thus the agreed  
31 nominal data transfer rate is 3Gb, not 6Gb, so flow (conservatively) proceeds to turn off status  
32 combining (Disable Status Coalescing, **204**). Flow is then complete. The controller then  
33 proceeds to operate with status coalescing disabled, returning status information to the host  
34 without coalescing in any situations, even though the host is enabled to properly process  
35 coalesced status information.

36

1   **[0154]**       As a third example of operation of Flow Diagram **200**, consider SSD **101** with  
2   SSD Controller **100** coupling to Host 3G/1.5G **102C** (as illustrated in Fig. 1C). Host 3G/1.5G  
3   **102C** is not fully compliant with a particular SATA standard, being unable to properly process  
4   coalesced status information but is enabled to transfer data at a maximum nominal 3Gb rate.  
5   With respect to Fig. 2, the host and the controller agree on a data transfer rate (Negotiate Speed  
6   with Host, **202**) and the negotiation is indicated conceptually by dashed line Negotiation  
7   **1100DC** in Fig. 1C. The host requests and obtains the maximum data rate of 3Gb, and thus the  
8   agreed nominal data transfer rate is 3Gb, not 6Gb, so flow proceeds to turn off status combining  
9   (Disable Status Coalescing, **204**) . Flow is then complete. The controller then proceeds to  
10   operate with status coalescing disabled, returning status information to the host without  
11   coalescing in any situations, preventing the host from improperly processing coalesced status  
12   information.

13

14   **[0155]**       Fourth, fifth, and sixth examples of operation of Flow Diagram **200** are similar,  
15   respectively, to the aforementioned first, second, and third, examples, but are based on Fig. 1D  
16   instead of Fig. 1C. The negotiations are indirect via Switch / Fabric / Intermediate Controller  
17   **103** and Intermediate Interfaces **104** as indicated conceptually by dashed lines Negotiation  
18   **1100IA**, Negotiation **1100IB**, and Negotiation **1100IC** rather than directly between the host and  
19   the controller. As a result of Negotiation **1100IA** (6Gb) status coalescing is enabled, and as a  
20   result of Negotiations **1100IB** and **1100IC** (3Gb) status coalescing is disabled.

21

22   **[0156]**       In various embodiments, one or more elements of Fig. 1A manage or perform  
23   one or more operations (or portions thereof) illustrated in Fig. 2. For instance, the speed  
24   negotiation and/or the status information return to the host (whether coalesced or not) are in part  
25   via Host Interfaces **111**. For another instance, the enabling/disabling of status coalescing is  
26   managed using a portion of software execution capabilities of CPU **171**.

27

28   **[0157]**       Although Flow Diagram **200** is specific with respect to a SATA interface,  
29   embodiments are contemplated where operation is with respect to a host and a storage  
30   system/sub-system coupled via a host-storage interface of a more general nature. For example,  
31   the host-storage interface is a serial interface that enables host communication with one or more  
32   mass storage devices (e.g. SDDs, HDDs, CD/DVD drives, tape drives, and other storage sub-  
33   systems enabled to store voluminous data). In some embodiments, the host-storage interface is a  
34   serial interface. In various embodiments, the serial interface has two pairs of conductors. In  
35   various embodiments, the serial interface is one or more of: operable with an (optional)  
36   input/output queuing protocol, compatible with native hot swapping, operable with commands

1 that are backward compatible with ATA and ATAPI commands, and compatible with an  
2 industry standard SATA interface. In various embodiments, the serial interface is operable at  
3 various nominal data rates such as 6Gb, 3Gb, and 1.5Gb.

#### 6 OTHER EMBODIMENTS

8 **[0158]** In other various embodiments, host transfer data rate detection by a slave (e.g. a  
9 storage system/sub-system) is used by the slave to optimize and/or improve behavior of the slave  
10 and/or to selectively enable (or disable) one or more operating features of the slave. For  
11 example, a CF card detects a host enabled to transfer data at a rate greater than a predetermined  
12 threshold, and in response the CF card enables (disables) an operating mode and/or a feature that  
13 is otherwise disabled (enabled). For another example, a CF card detects a host enabled to  
14 transfer data at a rate less than a predetermined threshold, and in response the CF card enables  
15 (disables) an operating mode and/or a feature that is otherwise disabled (enabled).

17 **[0159]** In some embodiments and/or usage scenarios, operating speed (e.g. transfer rate  
18 of an interface) implies operation up to a particular revision level of a standard (e.g. interface  
19 standard revision level), and speed detection is usable to infer compliance with the particular  
20 standard revision level. For example, a higher operating speed implies that a higher level of a  
21 standard is being complied with, and that operating modes and/or features described by the  
22 higher level of the standard are properly supported. Therefore the proper support of the  
23 operating modes and/or features is inferable via detection of the higher operating speed. For  
24 another example, a lower operating speed implies that a lower level of a standard is being wholly  
25 or partially complied with, e.g. operation is incompatible with the lower level of the standard.  
26 Therefore possible non-compliance of the proper support of the operating modes and/or features  
27 is inferable via detection of the lower operating speed.

#### 30 EXAMPLE IMPLEMENTATION TECHNIQUES

32 **[0160]** In some embodiments, various combinations of all or portions of operations  
33 performed by a system implementing selective enablement of operating modes or features (such  
34 as status coalescing) via host transfer rate detection for managing an interface with a  
35 (computing) host, as well as circuitry for managing non-volatile storage, e.g. with flash  
36 memories, a computing-host flash memory controller, and/or an SSD controller (such as SSD

1 Controller **100** of Fig. 1A), and portions of a processor, microprocessor, system-on-a-chip,  
2 application-specific-integrated-circuit, hardware accelerator, or other circuitry providing all or  
3 portions of the aforementioned operations, are specified by a specification compatible with  
4 processing by a computer system. The specification is in accordance with various descriptions,  
5 such as hardware description languages, circuit descriptions, netlist descriptions, mask  
6 descriptions, or layout descriptions. Example descriptions include: Verilog, VHDL, SPICE,  
7 SPICE variants such as PSpice, IBIS, LEF, DEF, GDS-II, OASIS, or other descriptions. In  
8 various embodiments, the processing includes any combination of interpretation, compilation,  
9 simulation, and synthesis to produce, to verify, or to specify logic and/or circuitry suitable for  
10 inclusion on one or more integrated circuits. Each integrated circuit, according to various  
11 embodiments, is designable and/or manufacturable according to a variety of techniques. The  
12 techniques include a programmable technique (such as a field or mask programmable gate array  
13 integrated circuit), a semi-custom technique (such as a wholly or partially cell-based integrated  
14 circuit), and a full-custom technique (such as an integrated circuit that is substantially  
15 specialized), any combination thereof, or any other technique compatible with design and/or  
16 manufacturing of integrated circuits.

17  
18 **[0161]** In some embodiments, various combinations of all or portions of operations as  
19 described by a computer readable medium having a set of instructions stored therein, are  
20 performed by execution and/or interpretation of one or more program instructions, by  
21 interpretation and/or compiling of one or more source and/or script language statements, or by  
22 execution of binary instructions produced by compiling, translating, and/or interpreting  
23 information expressed in programming and/or scripting language statements. The statements are  
24 compatible with any standard programming or scripting language (such as C, C++, Fortran,  
25 Pascal, Ada, Java, VBscript, and Shell). One or more of the program instructions, the language  
26 statements, or the binary instructions, are optionally stored on one or more computer readable  
27 storage medium elements. In various embodiments some, all, or various portions of the program  
28 instructions are realized as one or more functions, routines, sub-routines, in-line routines,  
29 procedures, macros, or portions thereof.

## CONCLUSION

[0162] Certain choices have been made in the description merely for convenience in preparing the text and drawings and unless there is an indication to the contrary the choices should not be construed per se as conveying additional information regarding structure or operation of the embodiments described. Examples of the choices include: the particular organization or assignment of the designations used for the figure numbering and the particular organization or assignment of the element identifiers (the callouts or numerical designators, e.g.) used to identify and reference the features and elements of the embodiments.

[0163] The words “includes” or “including” are specifically intended to be construed as abstractions describing logical sets of open-ended scope and are not meant to convey physical containment unless explicitly followed by the word “within.”

[0164] Although the foregoing embodiments have been described in some detail for purposes of clarity of description and understanding, the invention is not limited to the details provided. There are many embodiments of the invention. The disclosed embodiments are exemplary and not restrictive.

[0165] It will be understood that many variations in construction, arrangement, and use are possible consistent with the description, and are within the scope of the claims of the issued patent. For example, interconnect and function-unit bit-widths, clock speeds, and the type of technology used are variable according to various embodiments in each component block. The names given to interconnect and logic are merely exemplary, and should not be construed as limiting the concepts described. The order and arrangement of flowchart and flow diagram process, action, and function elements are variable according to various embodiments. Also, unless specifically stated to the contrary, value ranges specified, maximum and minimum values used, or other particular specifications (such as flash memory technology types; and the number of entries or stages in registers and buffers), are merely those of the described embodiments, are expected to track improvements and changes in implementation technology, and should not be construed as limitations.

[0166] Functionally equivalent techniques known in the art are employable instead of those described to implement various components, sub-systems, operations, functions, routines, sub-routines, in-line routines, procedures, macros, or portions thereof. It is also understood that many functional aspects of embodiments are realizable selectively in either hardware (i.e.,

generally dedicated circuitry) or software (i.e., via some manner of programmed controller or processor), as a function of embodiment dependent design constraints and technology trends of faster processing (facilitating migration of functions previously in hardware into software) and higher integration density (facilitating migration of functions previously in software into hardware). Specific variations in various embodiments include, but are not limited to: differences in partitioning; different form factors and configurations; use of different operating systems and other system software; use of different interface standards, network protocols, or communication links; and other variations to be expected when implementing the concepts described herein in accordance with the unique engineering and business constraints of a particular application.

[0167] The embodiments have been described with detail and environmental context well beyond that required for a minimal implementation of many aspects of the embodiments described. Those of ordinary skill in the art will recognize that some embodiments omit disclosed components or features without altering the basic cooperation among the remaining elements. It is thus understood that much of the details disclosed are not required to implement various aspects of the embodiments described. To the extent that the remaining elements are distinguishable from the prior art, components and features that are omitted are not limiting on the concepts described herein.

[0168] All such variations in design are insubstantial changes over the teachings conveyed by the described embodiments. It is also understood that the embodiments described herein have broad applicability to other computing and networking applications, and are not limited to the particular application or industry of the described embodiments. The invention is thus to be construed as including all possible modifications and variations encompassed within the scope of the claims of the issued patent.

## WHAT IS CLAIMED IS:

- 1 1. A system comprising:
  - 2 a means for serially interfacing a host with storage;
  - 3 a means for selectively controlling enablement of at least one operating mode or feature,
  - 4 the means for selectively controlling enablement being enabled to selectively
  - 5 enable the at least one operating mode or feature; and
  - 6 wherein the means for selectively controlling enablement is dependent at least in part on
  - 7 a negotiated data transfer rate of the means for serially interfacing.
- 1 2. The system of claim 1, wherein the means for selectively controlling selectively enables the
  - 2 at least one operating mode or feature when the negotiated data transfer rate is greater than a
  - 3 predetermined threshold.
- 1 3. The system of claim 2, wherein the means for selectively controlling enablement is further
  - 2 enabled to selectively disable the at least one operating mode or feature, and the means for
  - 3 selectively controlling enablement selectively disables the at least one operating mode or feature
  - 4 when the negotiated data transfer rate is less than the predetermined threshold.
- 1 4. The system of claim 2, wherein a first version of a serial interface standard specifies
  - 2 operation at a maximum nominal serial data transfer rate that is at or above the predetermined
  - 3 threshold, the first version of the serial interface standard specifies the at least one operating
  - 4 mode or feature, a second version of the serial interface standard specifies operation at a
  - 5 maximum nominal serial data transfer rate that is below the predetermined threshold, the means
  - 6 for serially interfacing is compatible with the first and the second versions of the serial interface
  - 7 standard, and the means for serially interfacing is not compatible with the second version of the
  - 8 serial interface standard when the at least one operating mode or feature is enabled.
- 1 5. The system of claim 4, wherein the first and the second versions of the serial interface
  - 2 standard correspond to respective versions of a Serial Advanced Technology Attachment
  - 3 (SATA) standard.
- 1 6. The system of claim 2, wherein the at least one operating mode or feature comprises
  - 2 coalescing of status information that is to be returned to the host.

- 1 7. The system of claim 6, wherein the means for serially interfacing is compatible with at least  
2 one version of a Serial Advanced Technology Attachment (SATA) standard and the  
3 predetermined threshold is 6Gb.
- 1 8. The system of claim 6, further comprising the host, and wherein the host is enabled to process  
2 the coalesced status information.
- 1 9. The system of claim 1, wherein the means for serially interfacing and the means for  
2 selectively controlling enablement are comprised in one or more Solid State Disks (SSDs), Hard  
3 Disk Drives (HDDs), Compact Disk (CD) and/or Digital Versatile/Video Disk (DVD) drives,  
4 and tape drives.
- 1 10. The system of claim 1, wherein the means for serially interfacing and the means for  
2 selectively controlling enablement are comprised in one or more Solid State Disks (SSDs), and  
3 the storage comprises flash memory comprised in at least one of the SSDs.
- 1 11. A method comprising:  
2 serially interfacing a host with storage;  
3 selectively controlling enablement of at least one operating mode or feature, the  
4 selectively controlling enablement selectively enabling the at least one operating  
5 mode or feature; and  
6 wherein the selectively controlling enablement is dependent at least in part on a  
7 negotiated data transfer rate of the serially interfacing.
- 1 12. The method of claim 11, wherein the selectively controlling enablement selectively enables  
2 the at least one operating mode or feature when the negotiated data transfer rate is greater than a  
3 predetermined threshold.
- 1 13. The method of claim 12, wherein the selectively controlling enablement selectively disables  
2 the at least one operating mode or feature when the negotiated data transfer rate is less than the  
3 predetermined threshold.

1 14. The method of claim 12, wherein a first version of a serial interface standard specifies  
2 operation at a maximum nominal serial data transfer rate that is at or above the predetermined  
3 threshold, the first version of the serial interface standard specifies the at least one operating  
4 mode or feature, a second version of the serial interface standard specifies operation at a  
5 maximum nominal serial data transfer rate that is below the predetermined threshold, the serially  
6 interfacing is compatible with the first and the second versions of the serial interface standard,  
7 and the serially interfacing is not compatible with the second version of the serial interface  
8 standard when the at least one operating mode or feature is enabled.

1 15. The method of claim 14, wherein the first and the second versions of the serial interface  
2 standard correspond to respective versions of a Serial Advanced Technology Attachment  
3 (SATA) standard.

1 16. The method of claim 12, wherein the at least one operating mode or feature comprises  
2 coalescing of status information that is to be returned to the host.

1 17. The method of claim 16, wherein the serially interfacing is compatible with at least one  
2 version of a Serial Advanced Technology Attachment (SATA) standard and the predetermined  
3 threshold is 6Gb.

1 18. The method of claim 16, further comprising the host processing the coalesced status  
2 information.

1 19. The method of claim 11, wherein the serially interfacing and the selectively controlling  
2 enablement are implemented in one or more Solid State Disks (SSDs), Hard Disk Drives  
3 (HDDs), Compact Disk (CD) and/or Digital Versatile/Video Disk (DVD) drives, and tape  
4 drives.

1 20. The method of claim 11, wherein the serially interfacing and the selectively controlling  
2 enablement are implemented in one or more Solid State Disks (SSDs), and the storage comprises  
3 flash memory comprised in at least one of the SSDs.

- 1   21. A method comprising:
  - 2           negotiating a nominal data transfer rate of a serial interface coupling a computing host
  - 3           and a Solid State Disk (SSD);
  - 4           determining if the nominal data transfer rate is less than a predetermined threshold; and
  - 5           based at least in part on the determining, selectively disabling coalescing of status
  - 6           information that is to be returned to the computing host.
- 1   22. The method of claim 21, wherein the serial interface is compatible with at least one version
- 2   of a Serial Advanced Technology Attachment (SATA) standard.
- 1   23. The method of claim 21, wherein the predetermined threshold is 6Gb.
- 1   24. The method of claim 23, wherein the serial interface is compatible with at least one version
- 2   of a Serial Advanced Technology Attachment (SATA) standard.
- 1   25. The method of claim 21, further comprising selectively enabling, based at least in part on
- 2   the determining, coalescing of status information that is to be returned to the computing host.
- 1   26. The method of claim 21, wherein the serial interface is compatible with at least one version
- 2   of a Serial Advanced Technology Attachment (SATA) standard and the predetermined threshold
- 3   is 6Gb; and further comprising disabling coalescing of status information that is to be returned to
- 4   the computing host in response to the nominal data transfer rate being less than the
- 5   predetermined threshold.

1 27. The method of claim 26, wherein the computing host comprises all or any portions of one or  
2 more of  
3 a computer,  
4 a workstation computer,  
5 a server computer,  
6 a storage server,  
7 a Personal Computer (PC),  
8 a laptop computer,  
9 a notebook computer,  
10 a netbook computer,  
11 a Personal Digital Assistant (PDA),  
12 a media player,  
13 a media recorder,  
14 a digital camera,  
15 a cellular handset,  
16 a cordless telephone handset, and  
17 an electronic game.

1 28. The method of claim 26, further comprising enabling coalescing of status information that is  
2 to be returned to the computing host in response to the nominal data transfer rate being greater  
3 than or equal to the predetermined threshold.

1 29. The method of claim 26, wherein the SSD comprises a controller that is enabled to perform  
2 one or more of all or any portions of the negotiating, the determining, and the selectively  
3 disabling.

1 30. The method of claim 29, further comprising operating the computing host to perform at least  
2 a portion of the negotiating.

1 31. The method of claim 29, further comprising operating the computing host to process  
2 coalesced status information.

1 32. The method of claim 21, wherein the serial interface is compatible with at least one version  
2 of a serial interface standard that specifies the coalescing of status information.

- 1 33. The method of claim 32, wherein the serial interface standard is compatible with at least one
- 2 version of a Serial Advanced Technology Attachment (SATA) standard.

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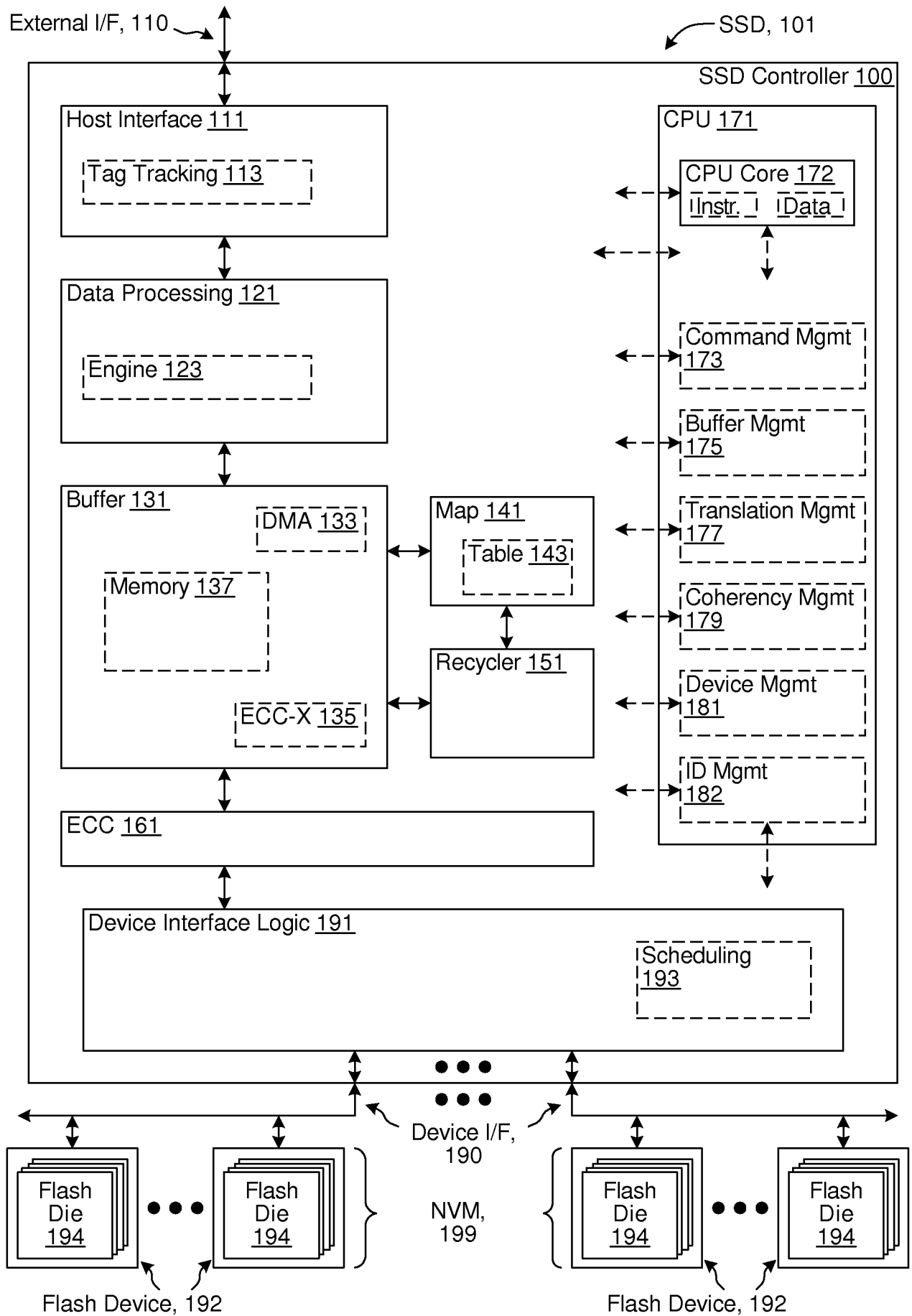


Fig. 1A

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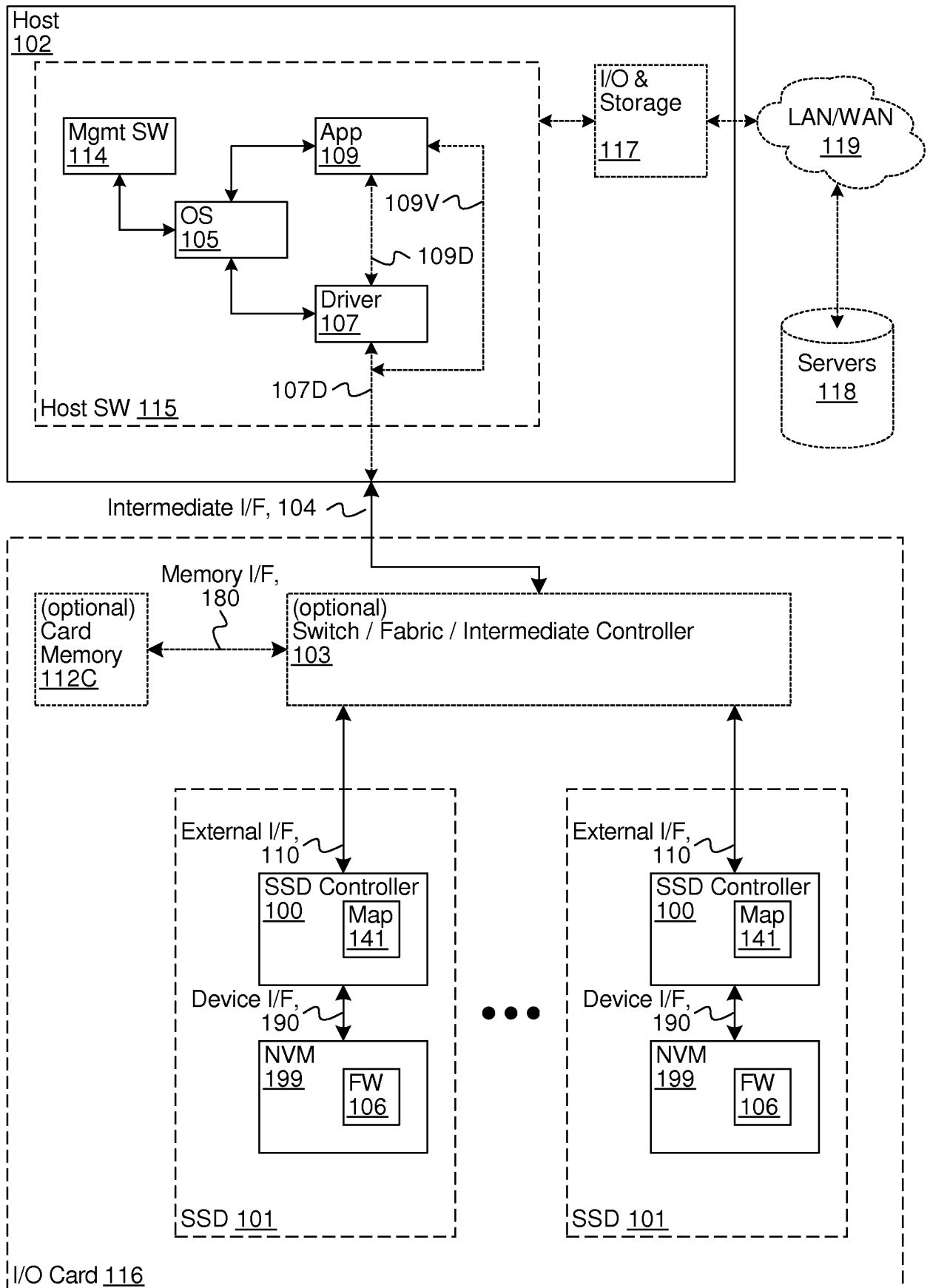


Fig. 1B

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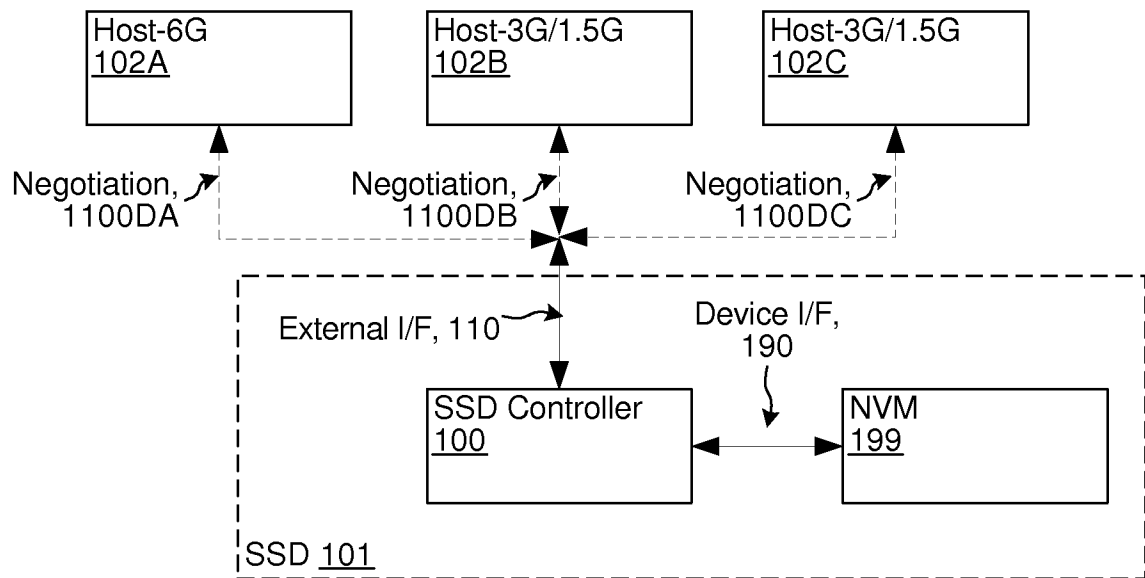


Fig. 1C

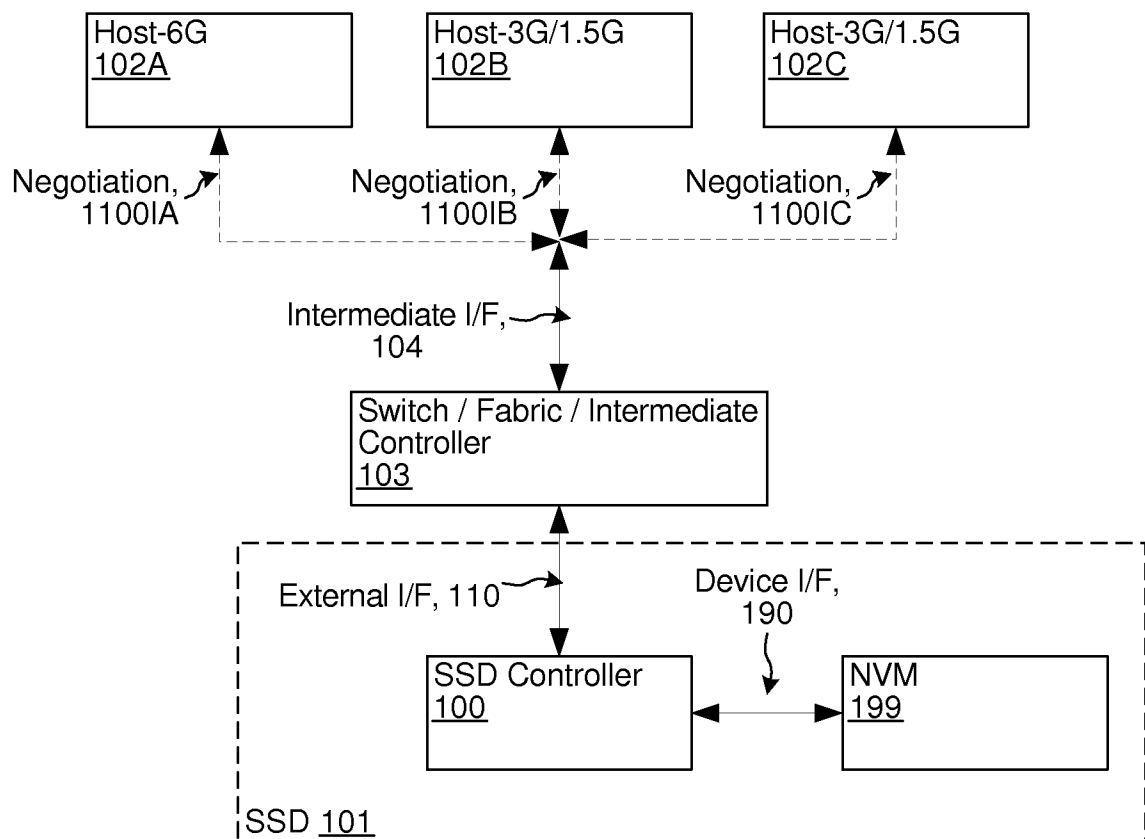


Fig. 1D

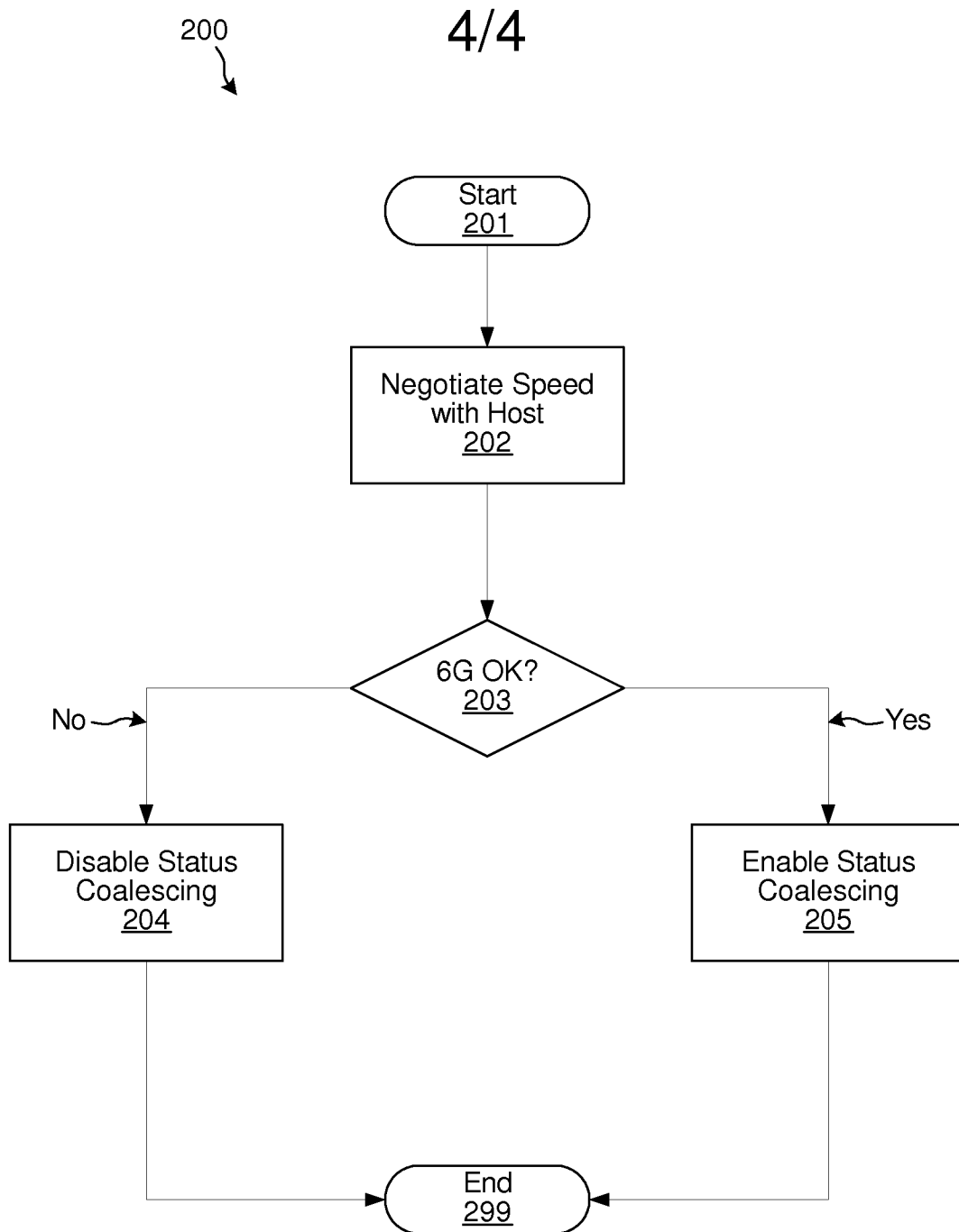


Fig. 2