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Finn

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[54] ELECTRONIC LOCK AND ALARM SYSTEM

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[51] **Int. Cl.** **E05b 47/02,** E05b 49/04

[58] **Field of Search** .....307/10 AT; 317/134; 340/147 R, 340/164 R, 274

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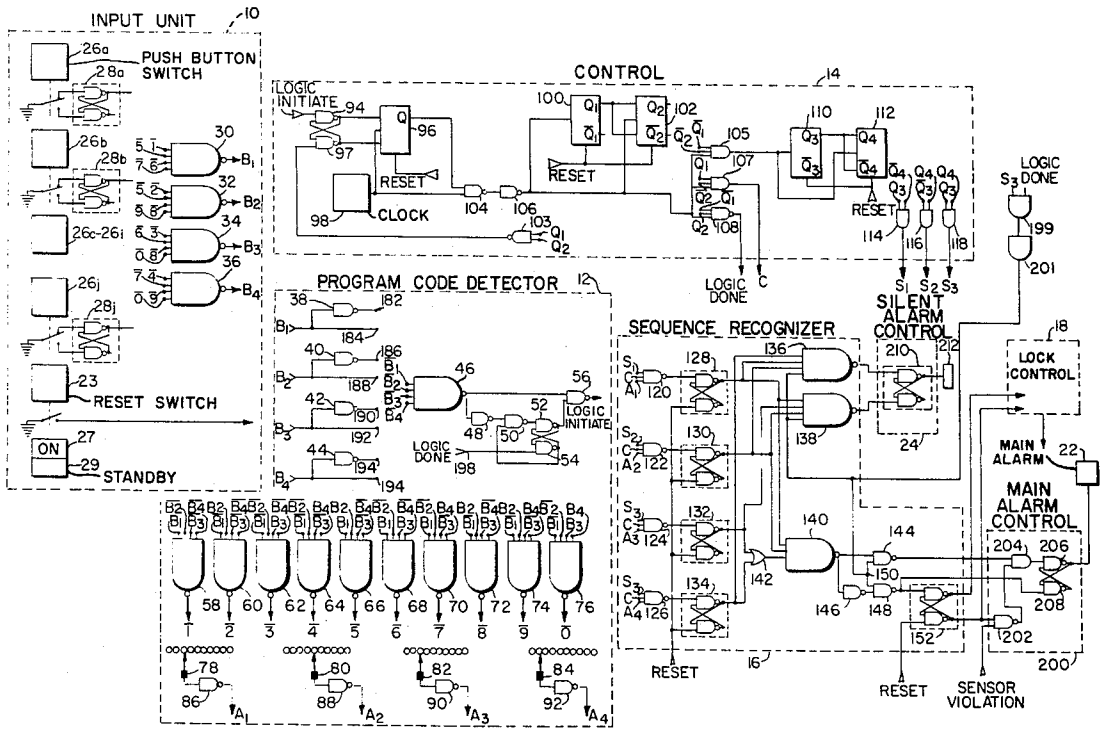
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[57] **ABSTRACT**

In an electronic lock and alarm system, a sequence of digitally coded signals, specified by logically comparing input coded signals from a manually operated selector matrix and preset coded signals from a programmable code detector, is transmitted to a sequence recognizer computer for determining the validity of the coded sequence, and terminals such as door locks, ingnition switches, etc. are operated by the computer in one of several modes specified by a user discriminatingly operating the selector matrix. In a first mode, the terminals are opened for accessibility to the user. In a second mode, the terminals are closed for inaccessibility to the user and a main alarm in the immediate vicinity is energized. In an optional third mode, the terminals are opened for accessibility to the user and a silent alarm is energized at a remote location.

7 Claims, 3 Drawing Figures



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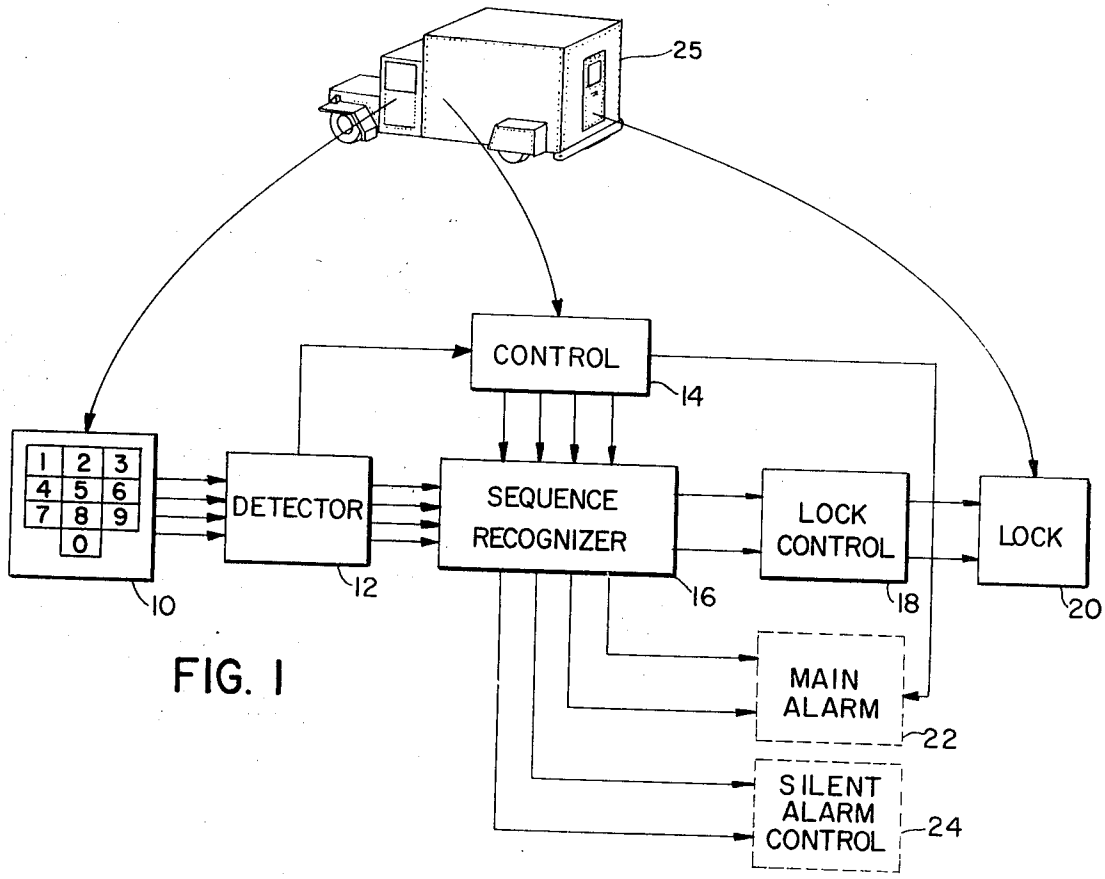


FIG. 1

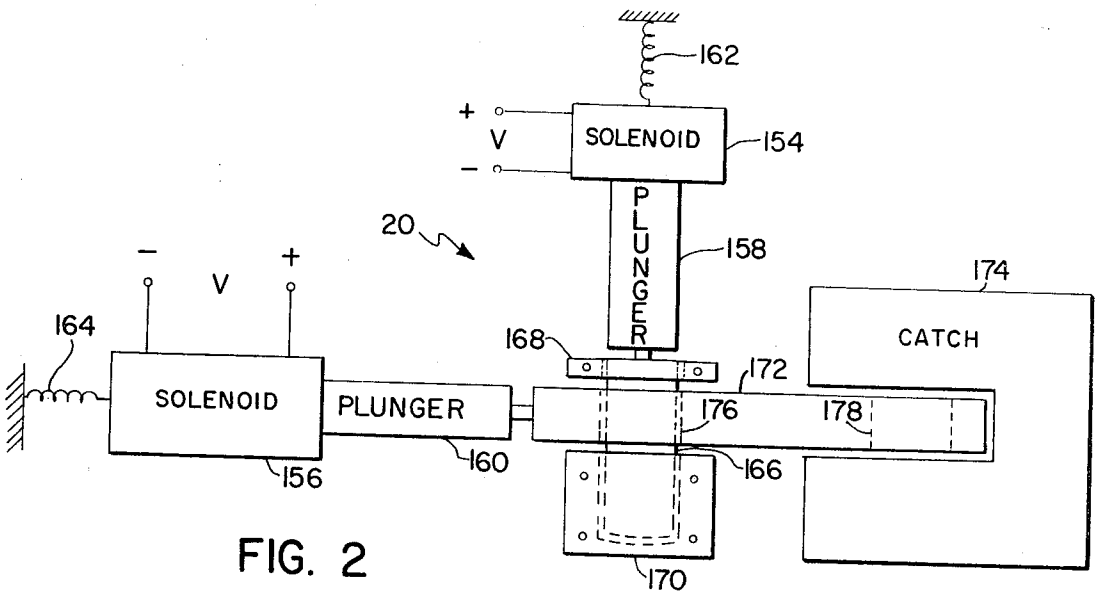


FIG. 2

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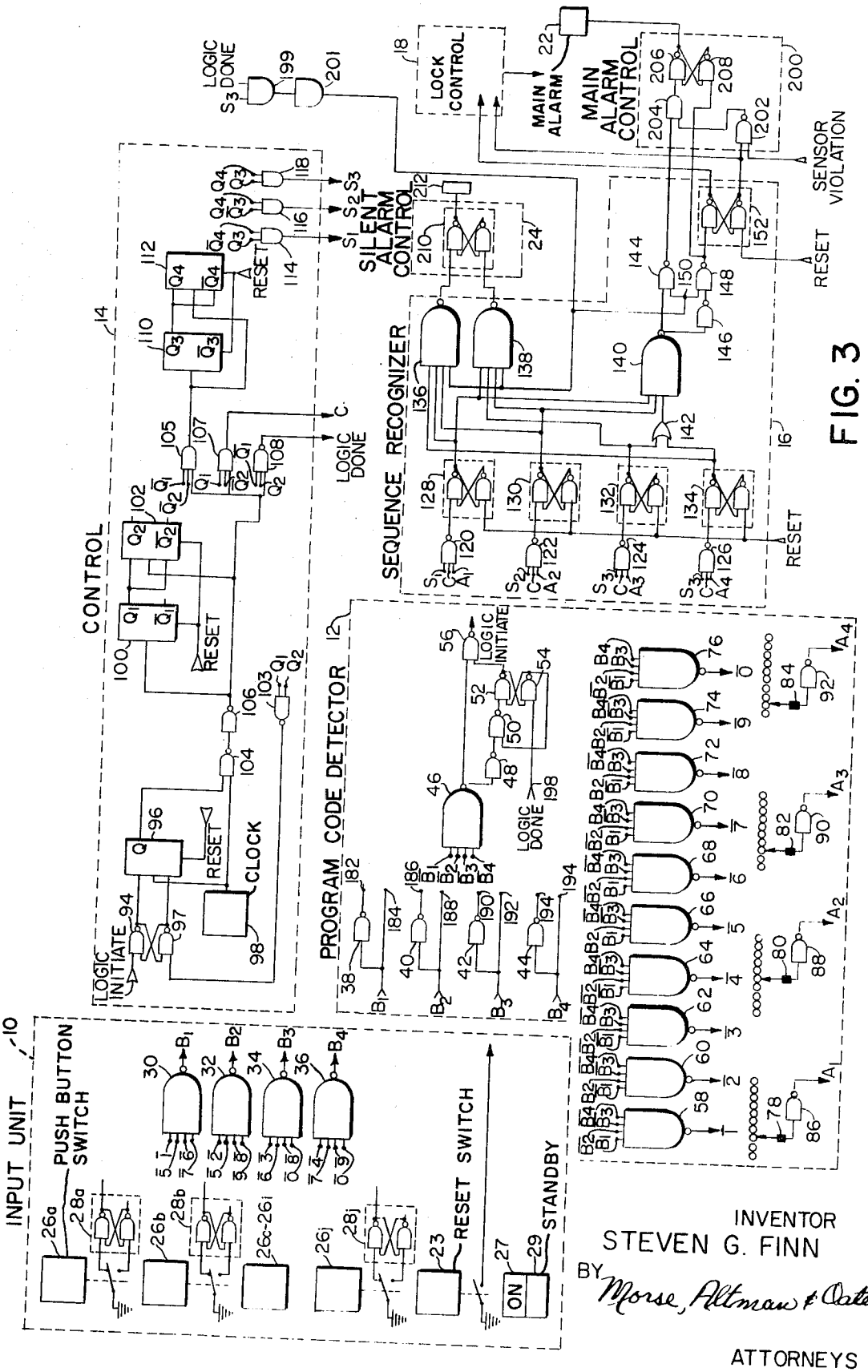


FIG. 3

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ELECTRONIC LOCK AND ALARM SYSTEM

BACKGROUND AND SUMMARY

The present invention relates to security devices and, more particularly, to lock and alarm systems that are actuated manually and operated electronically. Prior systems typically have utilized mechanical keys and locks or mechanical combination locks, in mechanical or electro-mechanical association with mechanical or electro-mechanical controls. In contrast, the present system utilizes manually operable selectors, digitally coded sequences and computer operated controls. Since a system of the present type involves the transfer of much more information than does a system of the prior type, it is capable of much greater functional versatility.

The primary object of the present invention is to provide an electronic lock and alarm system characterized by a manually operated selector for setting a binary coded matrix, a detector for responding with a digitally coded input sequence, a control for providing a digitally coded reference sequence, a sequence recognizer computer for providing output signals logically responsive to a comparison of the input sequence and reference sequence, and locking devices which are actuated or deactuated in electro-magnetic response to the output of the sequence recognizer computer. In the illustrated example, the locking devices include the ignition switch and main safety lock of an armored financial truck.

Another object of the present invention is to provide an alarm system characterized by a main alarm and an optional silent alarm, which are responsive to the signals as at the output of the sequence recognizer computer, for alerting cognizant personnel in the immediate vicinity and at a distant location, respectively, that either an improper code has been set at the binary coded matrix or a security sensor has been activated.

The invention accordingly comprises the apparatus possessing the construction, combination of elements, and arrangements of parts that are exemplified in the following detailed disclosure, the scope of which will be indicated in the appended claims.

BRIEF DESCRIPTION OF DRAWING

For a fuller understanding of the nature and objects of the present invention, reference should be had to the following detailed description, taken in connection with the accompanying drawings, wherein:

FIG. 1 illustrates an electronic combination locking system embodying the present invention;

FIG. 2 illustrates the locking device of FIG. 1; and

FIG. 3 is a schematic diagram of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates an application of the present system to an armored truck. Generally, the system comprises a manually operated code input matrix **10** for providing a selected sequence of binary coded signals, a programmable detector **12** for converting the selected sequence of binary coded signals to a sequence decimal coded signals, a control **14** for providing a sequence of digitally coded signals in response to output signals from detector **12**, a sequence recognizer computer **16** for providing a plurality of output signals which are logically responsive to a comparison of the sequence of decimal coded signals and the sequence of digitally coded signals, the digitally coded signals controlling the sequence in which computer **16** operates, and a lock control **18** for rending a locking device **20** and an ignition switch (not shown) operative and inoperative in response to the signals as at the output of sequence recognizer computer **16**. In the preferred embodiment of the present invention, output signals from sequence recognizer computer **16** are applied also to a main alarm **22**, for example, a siren, for alerting cognizant personnel in the immediate vicinity and a silent alarm control **24**, for example, a transmitter, for alerting cognizant personnel at a distant location. It is to be understood that the silent alarm system is an optional feature and is included in an alternative embodiment of the present invention. It will be readily appreciated that a plurality of security sensors (not shown) may be provided for activating main alarm control **22** for a variety of unauthorized acts, for example, opening the doors, breaking the windows, tampering with the ignition system, opening the hood compartment and etc. In the illustrated embodiment of the present invention, the combination locking system is installed in an armored truck **25**. Switch matrix **10** is installed in the cab portion thereof; detector **12**, control **14**, sequence recognizer computer **16**, lock control **18**, locking device **20**, main alarm **22**, and silent alarm control **24** are located in the rear compartment of truck **25**; and a silent alarm signaling device (not shown) is situated at a remote location. It is understood that, in alternate embodiments, the present invention is adaptable for other uses, for example, securing a vault.

As shown in FIG. 3, input matrix **10** includes a plurality of like switching devices, for example, push button switches **26***a*, **26***b*, and etc. for providing a sequence of binary coded signals. The push button switches are connected to correlative logic circuits, for example, set-reset flip-flops denoted by reference characters **28***a*, **28***b*, and etc. Push button switch **26***a* is connected to set-reset flip-flop **28***a*, push button switch **26***b* is connected to set-reset flip-flop **28***b* and so on. The signal as at the output of set-reset flip-flop **28***a* is designated as $\overline{1}$, the signal as at the output of set-reset flip-flop **28***b* is designated as $\overline{2}$, and so on. The signals as at the output of the set-reset flip-flops represent the positive switching state of their correlative push button switches, i.e. signals which appear at the output of the push button switches as a result of switch bounce are not present at the output of the set-reset flip-flop. If bounce signals are not present at the output of the switches, the set-reset flip-flops may be eliminated. Selected output terminals of the set-reset flip-flops are electrically connected to a plurality of NAND-gates **30**, **32**, **34**, and **36** in such a manner that the outputs of flip-flops **28***a*, **28***e*, **28***f*, and **28***g* are applied to the input of NAND-gate **30**; the outputs of flip-flops **28***b*, **28***e*, **28***h*, and **28***j* are applied to the input of NAND-gate **32**; the outputs of flip-flops **28***c*, **28***f*, **28***h*, and **28***i* are applied to NAND-gate **34**; and the outputs of **28***d*, **28***g*, **28***i*, and **28***j* are applied to NAND-gate **36**. For convenience, the signal as at the output of NAND-gates **30**, **32**, **34** and **36** will be referred to as B1, B2, B3, and B4, respectively. Input switch matrix **10** includes also a RESET switch **23** for resetting the system from alarm-off and locks open to alarm-on and locks closed and for cancelling partial codes entered into matrix **10**, and ON light **27** for indicating the locking and alarm system operative and a STANDBY light **29** for indicating locking system and alarm system inoperative.

Detector **12**, which produces a sequence of digitally coded signals responsive to the sequence of binary coded signals as at the output of matrix **10** and a preset sequence of decimally coded signals, includes a plurality of NAND-gates **38**, **40**, **42**, and **44** for receiving the signals as at the output of NAND-gates **30**, **32**, **34**, and **36**, respectively. Signals $B\overline{1}$, $B\overline{2}$, $B\overline{3}$, $B\overline{4}$ as at the output of NAND-gates **38**, **40**, **42**, and **44**, respectively, are applied to their respective inputs of NAND-gate **46**. The output of NAND-gate **46** is logically connected to NAND-gates **48**, **50**, **54**, and **56**. The signals as at the output of NAND-gates **30**, **32**, **34**, **36**, **38**, **40**, **42**, and **44** are applied to selective input terminals of NAND-gates **58**, **60**, **62**, **64**, **66**, **68**, **70**, **72**, **74**, and **76** in such a manner that the signals at the output of each of the NAND-gates is $\overline{1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$, $\overline{5}$, $\overline{6}$, $\overline{7}$, $\overline{8}$, $\overline{9}$, and $\overline{0}$, respectively. The output terminal of each NAND-gate **58**, **60**, **62**, **64**, **66**, **68**, **70**, **72**, **74**, and **76** is connected to each of a plurality of switching devices **78**, **80**, **82**, and **84**, for example, rotary switches; each of the rotary switches receiving one coded signals $\overline{1}$, $\overline{2}$, $\overline{3}$, $\overline{4}$, $\overline{5}$, $\overline{6}$, $\overline{7}$, $\overline{8}$, $\overline{9}$, and $\overline{0}$. The output terminal of rotary switches **78**, **80**, **82**, and **84** are connected to NAND-gates **86**, **88**, **90**, and **92** respectively. For convenience, the signal as at the output of NAND-gates **86**, **88**, **90**, and **92** will be designated as A_1, A_2, A_3, and A_4 respectively.

Control **14**, which produces a sequence of digitally coded signals responsive to an output of NAND-gate **56**, includes a NAND-gate **94** which is electrically connected to the output of NAND-gate **56**, a JK flip-flop **96** the first input of which is connected to the output of NAND-gate **94**, a clock **98**, and a NAND-gate **97** which are connected the second and third inputs of JK flip-flop **96**, respectively. The output of flip-flop **96** is connected to the first inputs of JK flip-flops **100** and **102** via NAND-gates **104** and **106**, respectively. The output terminal of JK flip-flop **100** is connected to second input terminal of JK flip-flop **102**. For convenience, the outputs of JK flip-flops **100** and **102** will be designated Q_1, $\bar{Q}_2$, and Q_2, $\bar{Q}_2$, respectively. $\overline{Q_1 \cdot Q_2}$ as at the output of a NAND-gate **103** is applied to the input of NAND-gate **97** whereby clock **98** is de-energized. The outputs of JK flip-flop **100**, JK flip-flop **102**, and NAND-gate **106** are connected selectively to AND-gate **105**, AND-gate **107**, and NAND-gate **108**. The first input of each AND-gate **105**, AND-gate **107**, and NAND-gate **108** is connected to NAND-gate **106** and $\bar{Q}1$, $\bar{Q}2$; $\bar{Q}_1$, $\bar{Q}_2$; and $\bar{Q}_1$, Q_2 respectively. For convenience, the signal as at the output of NAND-gate **108** will be designated as "logic done pulse" and the signal as at the output of AND-gate **107** will be designated as C. The output of AND-gate **105** is connected to the first inputs of JK flip-flops **110** and **112**. The output terminal of JK flip-flop **110** is connected to the second input of JK flip-flop **112**. The outputs of JK flip-flops **110** and **112** are designated Q3, $\bar{Q}_3$ and Q4, $\bar{Q}_4$, respectively. The output terminals of JK flip-flops **110** and **112** are connected selectively to AND-gates **114**, **116**, and **118** in such a manner that Q3, $\bar{Q}$4 are applied to AND-gate **114**, $\bar{Q}$3, Q4 are applied to AND-gate **116**, and Q3, Q4 are applied to AND-gate **118**. The signals as at the output of AND-gates **114**, **116**, and **118** are designated S1, S2, and S3, respectively.

Sequence recognizer computer **16**, which provides output control signals responsive to the sequence of digitally coded signals as at the outputs of detector **12** and control **14**, includes four NAND-gates **120**, **122**, **124**, and **126**. The inputs of NAND-gates **120**, **122**, **124**, and **126** are connected selectively to the outputs of NAND-gates **86**, **88**, **90**, **92** and gates **107**, **114**, **116**, and **118** in such a manner that each signal S_1, C, and A_1 is applied to one of the inputs of NAND-gate **120**; each signal S_2, C, and A_2 is applied to one of the inputs of NAND-gate **122**; each signal S_3, C, and A_3 is applied to one of the inputs of NAND-gate **124**; and each signal S_3, C, and A_4 is applied to one of inputs of NAND-gate **126**. Each of the output terminals of NAND-gates **120**, **122**, **124**, and **126** are connected to each of the input terminals of a combination of NAND-gates **128**, **130**, **132**, and **134**, respectively. The signals as at the outputs of NAND-gates **128** and **130** are applied to their correlative inputs of NAND-gates **136**, **138**, and **140**, respectively. The outputs of NAND-gates **132** and **134** are connected to their respective inputs as at OR-gate **142**. In addition, the output of NAND-gate **132** is connected to an input of NAND-gate **138** and the output terminal of NAND-gate **140** is connected to each of the inputs of NAND-gate **144** and **146**. The output of NAND-gate **146** is connected to the first input of NAND-gate **148**. The second input of NAND-gates **144** and **148** are joined at a junction **150**. The output of NAND-gate **148** is connected to an input of a set-reset flip-flop **152**.

As shown in FIG. **2**, locking device **20**, which controls accessibility and inaccessibility to the rear compartment of truck **25**, includes solenoids **154** and **156** which are electrically connected to locking control **18**. Each of the solenoids **154** and **156** are provided with plungers **158** and **160** respectively. Plungers **158** and **160** are held in the extended position by springs **162** and **164**, respectively, when their correlative solenoids are de-energized. Firmly affixed to plunger **158** is a locking pin **166** which is slidably seated in a guide **168** and a catch **170**. Firmly affixed to plunger **160** is a bolt **172** which is removably seated in a catch **174**. Bolt **172** is formed with channels **176** and **178** which are slightly larger than locking pin **166** so that bolt **172** is held immovable in the extended and retracted positions by locking pin **166**. When an open lock signal, for example voltage V is applied to lock control **18**, solenoid **154** is energized and plunger **158** is retracted into solenoid **154**, whereby locking pin **166** is withdrawn from channel **176**. In addition, the open lock signal energizers solenoid **156** and plunger **160** is retracted into solenoid **156**, in consequence bolt **172** is withdrawn from catch **174** and lock **20** is rendered inoperative. It is noted, lock **20** is a fail safe device in that both solenoids **154** and **156** must be energized in order for bolt **172** to be withdrawn from catch **174**.

In operation of the lock and alarm system, three of the push buttons switches **26** of switch matrix **10** are energized in the proper sequence as specified by position of rotary switches **78**, **80**, **82**, and **84**, whereby an open lock signal is applied to solenoids **154** and **156** and locking device **20** is rendered inoperative. It will be appreciated that, in an alternate embodiment, the number of switches comprising the proper combination is other than three, for example, four. In addition to the proper opening sequence, there are two other modes of operation, namely a main alarm mode and a silent alarm mode. When an improper code sequence is received from switches **26** or if locking device **20** is tampered with, main alarm **22** is activated, whereby personnel in the immediate vicinity are alerted and locking device **20** is rendered operative. If the armored truck personnel are under duress and forced to open the locking system, a special sequence code is selected and the silent alarm mode is energized. In the silent alarm mode locking device **20** is rendered inoperative (open) and silent alarm **24** is activated, in consequence cognizant personnel at a remote location are alerted.

As previously stated, locking device **20** is rendered inoperative when the proper sequence of binary coded signals, as specified by the position of rotary switches **78**, **80**, **82**, and **84**, are selected at input switch matrix **10**. When push button switches **26** are energized sequentially, correlative flip-flop **28** is locked in a set state and the energized push button switches **26** are disabled. The signal as at the output of the correlative flip-flops **28** are applied to the respective NAND-gates **30**, **32**, **34**, and **36**, in consequence signals B1, B2, B3, and B4 are applied to detector **12**. Signals B1, B2, B3, and B4 are applied to their correlative NAND gates in detector **12** whereby coded signals B1, $\bar{B}$1, B2, $\bar{B}$2, B_3, $\bar{B}_3$, B_4, and $\bar{B}_4$ are presented at terminals **182**, **184**, **186**, **188**, **190**, **192**, **194**, and **196**, respectively. The $\bar{B}$1, $\bar{B}_2$ $\bar{B}_3$, and $\bar{B}_4$ signals are applied to their respective inputs of NAND-gate **46**, in consequence a ZERO logic initiate signal, for example, is presented at the output of NAND-gate **56**. When the ZERO logic initiate pulse is applied to JK flip-flop **96** via NAND-gates **94** and **97**, flip-flop **96** changes state and clock **98** is activated. The change of state of JK flip-flop **96**, designated Q, is applied to JK flip-flops **100** and **102** via NAND-gates **104** and **106**, whereby Q_1, $\bar{Q}_1$, and Q_2, $\bar{Q}_2$ signals are presented at the outputs of JK flip-flops **100** and **102**, respectively. Signals $\bar{Q}_1$, Q_2 and the signals as at the output of NAND-gate **106** are applied to the input of NAND-gate **108**, whereby a logic done pulse is presented at the output thereof. The logic done pulse, a ZERO, is applied to a terminal **198** at the input of NAND-gate **54**, in consequence the signal as at the output of NAND-gate **54** is ONE, the signal as at the output of NAND-gate **52** is ZERO, and the logic initiate pulse as at output of NAND-gate **56** is ONE. A ONE as at the output of NAND-gate **56** releases the first energized push button switch **26**, in consequence the coded signal representing the second energized push button switch **26** is applied to the input of NAND-gates **38**, **40**, **42**, and **44** of detector **12**. During the time that the logic initiate pulse is ZERO, the B1, $\bar{B}_1$, B_2, $\bar{B}_2$, B_3, $\bar{B}_3$, B_4, and $\bar{B}_4$ binary coded signals as at the output of NAND-gates **38**, **40**, **42**, and **44** are applied selectively to the inputs of NAND-gates **58**, **60**, **62**, **64**, **66**, **68**, **70**, **72**, **74**, and **76** wherein the binary coded signals are converted to decimal coded signals. All the decimal coded number $\bar{1}$, $\bar{2}$, $\bar{3}$, $\bar{4}$, $\bar{5}$, $\bar{6}$, $\bar{7}$, $\bar{8}$, $\bar{9}$, $\bar{0}$ as at the output of NAND-gates **58**, **60**, **62**, **64**, **66**, **68**, **70**, **72**, **74**, and **76**, respectively, are applied to each of the rotary switches **78**, **80**, **82**, and **84**. Signals A_1, A_2, A_3, and A_4, specified by the preset position of their corresponding rotary

switch, are presented at the output of NAND-gates **86**, **88**, **90**, and **92**, respectively. During the time the logic initiate pulse is ZERO, the signal as at the output of NAND-gate **106** is applied also to AND-gates **105** and **107**, whereby JK flip-flops **110** and **112** change state in response to the signal as at their inputs. JK flip-flops **110** and **112** provide a sequence of signals S_1, S_2, and S_3, each of which is specified by the sequence in which push button switches **26** are energized. That is, the first logic initiate pulse, which is specified by the first energized push button switch **26**, causes a JK flip-flop **110** to be in a state ONE (designated Q_3), at this time JK flip-flop **112** is in state ZERO (designated $\overline{Q}_4$); the second logic initiate pulse, which is specified by the second energized push button switch **26**, causes JK flip-flop **110** to be in a state ZERO (designated as $\overline{Q}_3$) and JK flip-flop **112** to be in a state ONE (designated as Q_4); and the third initiate pulse, which is specified by the third energized push button switch **26**, causes a JK flip-flop **110** to be in a state ONE and JK flip-flop **112** remains in state ONE. The Q_3, $\overline{Q}_3$, Q_4, and $\overline{Q}_4$ signals as at the output terminals of their correlative JK flip-flops **110** and **112** are selectively applied to AND-gates **114**, **116**, and **118** in such a manner that their respective output specify the sequence in which push button switches **26** are energized.

Signals S_1, S_2, S_3, A_1, A_2, A_3, A_4, and C are applied selectively to the inputs of NAND-gates **120**, **122**, **124**, and **126** of sequence recognizer computer **16**. When the signals S_1 and A_1 as at the input of NAND-gate **120** are both ONE, application of signal C causes NAND-gate **128** to latch. Similarly, when the correlative A and S signals as at the input of NAND-gates **122**, **124**, and **126** are ONES, application of signals C thereat causes NAND-gate **130**, **132**, and **134**, respectively to latch. The signals as at the output of NAND-gates **128**, **130**, and **132** or **134** are applied to NAND-gate **140**. When the complete three digit code has been entered, the logic done pulse is applied to junction **150** via NAND-gates **199** and **201**, thereby setting the inputs of NAND-gates **144** and **148**. In addition, the signal as at the output of NAND-gate **201** is applied to the input of NAND-gates **136** and **138**. If push button switches **26** are energized in the proper sequence, the signal is at the output of NAND-gate **140** is applied as an open signal to the input of lock control **18** via NAND-gates **146**, **148** and **152**. If the push button switches are energized in an improper sequence, the output of NAND-gate **140** is applied as a close signal to the input of lock control **18** and as an alarm signal to a main alarm control **200**, in consequence an alarm signal is applied to main alarm **22** via a NAND-gate **202**, an AND-gate **204**, and NAND-gates **206** and **208**. In addition, if locking device **20** is tampered with a sensor violation signal is applied to NAND-gate **202** and main alarm **22** is activated. When the push button switches **26** are energized in the silent alarm mode sequence, the signal as at the output of NAND-gate **134** is applied to the first input of NAND-gate **136** and the signals as at the output of NAND-gates **128**, **130**, and **132** are applied to their respective inputs of NAND-gates **136** and **138**. The signals as at the output of **136** and **138** are applied to a NAND-gate **210** in silent alarm control **24**, in consequence a silent alarm **212** activates an alarm signaling device (not shown) at a distant location. In addition to activating the silent alarm signaling device, the silent alarm mode renders locking device **20** inoperative, i.e. open.

Since certain changes may be made in the foregoing disclosure without departing from the scope of the invention herein involved, it is intended that all matter contained in the above description and shown in the accompanying drawings be construed in an illustrative and not in a limiting sense.

I claim:

1. A locking system comprising:

a. input matrix means including a plurality of first switch means for generating coded signals;

b. detector means including a plurality of first gate means and second switch means, said first gate means operatively connected to said first switch means, said first gate means operatively connected to said second switch means, said detector means generating first signals responsive to said signals generated by said input matrix means and governed by said second switch means;

c. control means, including a plurality of flip-flop means for generating second signals, operatively connected to said detector means, said control means responsive to said detector means;

d. sequence recognizer computer means, including a plurality of second gate means, operatively connected to said second switch means, and flip-flop means for generating third signals, the output signal of said sequence recognizer computer means responsive to said first and second signals of said detector means and control means, respectively; and

e. locking means operatively connected to said sequence recognizer computer means, said locking means being rendered operative and inoperative in response to selected third signals as at the output of said sequence recognizer computer means.

2. The locking system of claim **1** wherein said system includes main alarm means operatively connected to said sequence recognizer computer means and responsive to selected signals as at the output of said sequence recognizer computer means, said main alarm means alerting cognizant personnel in the immediate vicinity of said locking system.

3. The locking system of claim **1** wherein said system includes silent alarm means operatively connected to said sequence recognizer computer means and responsive to selected third signals as at the output of said sequence recognizer computer means, said silent alarm means alerting cognizant personnel at a distant location from said locking system.

4. The locking system of claim **1** wherein said first switch means is a plurality of push button switches, each said push button switch providing a specified binary code.

5. The locking system of claim **1** wherein said second switch means is a plurality of rotary switch means for specifying a sequence of signals which renders said locking means operative and inoperative.

6. A locking and alarm system comprising:

a. input switch means for generating coded signals;

b. detector means including first gate means and switch means, for generating first signals, said first gate means operatively connected to said input switch means, said switch means operatively connected to said first gate means, said detector means first signals responsive to said coded signals of said input switch means and said switch means;

c. control means including flip-flop means for generating control signals, said flip-flop means operatively connected to said detector means, said control means responsive to said detector means;

d. sequence recognizer computer means operatively connected to said switch means and flip-flop means for generating second signals, said second signals responsive to said first and control signals of said detector means and control means, respectively;

e. locking means operatively connected to said sequence recognizer computer means, said locking means being rendered operative and inoperative in response to selected second signals as at the output of said sequence recognizer computer means; and

f. alarm means operatively connected to said sequence recognizer computer means and responsive to selected second signals as at the output of said sequence recognizer computer means.

7. The locking and alarm system of claim **6** wherein said detector means includes a plurality of rotary switch means operatively connected to said input switch means for specifying a sequence of coded signals which renders said locking means operative and inoperative and activates and deactivates said alarm means.

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