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(54) Title: ELECTRONIC IDENTIFICATION SYSTEM WITH IMPROVED SENSITIVITY

(57) Abstract

The electronic identification system provides two-way communications between reader (1) and tags (3) using alternating magnetic fields established by the reader (1) and tag (3). Communications is accomplished by utilizing either a one-step or a two-step modulation process in which the information to be communicated either modulates an alternating magnetic field directly or modulates a periodic signal which modulates an alternating magnet field. The coil (5), capacitors (9), and coupling circuitry are maintained in a tuned condition by continually adjusting either the driving frequency, the coil inductance, or the capacitor capacitance during communications. A tag (3) utilizes a coil (50) to couple with the reader's alternating magnetic field and a capacitor (55) to resonate the coil (50), thereby extracting power from the field more efficiently. The coil (50), capacitor (55), and coupling circuitry can be maintained in a turned condition by continually adjusting either the coil inductance, or the capacitor capacitance during communications.

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ELECTRONIC IDENTIFICATION SYSTEM WITH IMPROVED SENSITIVITY

BACKGROUND OF INVENTION

This invention relates to cooperative identification systems (which had their electronic beginnings in World War II as Identification - Friend or Foe Systems) in which the identifying agency and the object to be identified cooperate in the identification process according to a prearranged scheme. More specifically, the invention relates to systems consisting generically of an interrogator (or "reader") inductively coupled to a transponder (or "tag") where the reader is associated with the identifying agency and the tag is associated with the object to be identified.

Such systems are being used or have the potential of being used for identifying fish, birds, animals, or inanimate objects such as credit cards. Some of the more interesting applications involve objects of small size which means that the transponder must be minute. In many cases it is desirable to permanently attach the tag to the object which means implantation of the device in the tissues of living things and somewhere beneath the surfaces of inanimate objects. In this cases, implantation of the tag within the object forecloses the use of conventional power sources for powering the tag. Sunlight will usually not penetrate the surface of the object. Chemical sources such as batteries wear out and cannot easily be replaced. Radioactive sources might present unacceptable risks to the object subject to identification. One approach to powering the tag that has been successfully practiced for many years is to supply the tag with power from the reader by means of an alternating magnetic field generated by the reader. This approach results in a small, highly-reliable tag of indefinite life and is currently the approach of choice.

For many applications, convenience and utility dictate that the reader be hand-portable which translates into the use of batteries to power the unit. However, the size and weight of batteries having the requisite capacity to perform the identification function at reasonable ranges without interruption challenge the very concept of hand-portability. The twin goals of ease of use and system

performance have been the subject of uneasy compromise in the past. There is a need to harness the recent advances in technology to the design of energy efficient systems in order to realize the full potential of identification systems based on inductive coupling.

As identification systems of this type proliferate and users multiply, it becomes important to recognize this changing environment in the design of next-generation identification apparatus. Newer-model readers should be able to read older-model tags. Users' privacy and security interests must be respected - one user should not be able to read another user's tags. And finally, in this computer-driven world, it must be possible to conveniently interface readers with computer.

BRIEF SUMMARY OF INVENTION

The electronic identification system with improved sensitivity provides two-way communication between reader and tag by a one-step or two-step modulation process in which the information to be communicated either modulates an alternating magnetic field directly or modulates a periodic signal which modulates an alternating magnetic field.

Generally, in order to obtain the highest possible communication sensitivity, the coil and capacitor in both reader and tag are maintained at or near a state of resonance while communications are taking place by adjusting either intermittently or continually the frequency of the coil driving signal, the inductance of the coil, or the capacitance of the capacitor in the reader and the inductance of the coil or the capacitance of the capacitor in the tag. It may be desirable in certain situations, in order to realize the best communication performance, to maintain the coil and capacitor near resonance but not in a state of resonance.

In order to maximize the alternating magnetic field produced by the reader coil, the driving signal is tailored to the characteristics of the resonant circuit so that the highest possible coil current is achieved. In this regard, the coil is driven push-pull by means of high-power field-effect transistors connected in a bridge

arrangement. Highly effective impedance matching is achieved by transformer coupling of the coil and the driver and capacitors.

Transformer coupling of the tag coil to the other devices and circuits in the tag is used in order to satisfy the diverse matching requirements imposed by these other devices and circuits.

The system utilizes maximum-likelihood procedures for identifying the bits represented by the signals transmitted by reader and tag. The maximum-likelihood procedures requires a precise knowledge of the beginning and ending of each bit period which is accomplished by a bit-timing clock signal which originates in a reader and is communicated by the reader to each tag with which it communicates. Both the reader and the tag utilize this common bit-timing clock signal for timing their bit transmissions.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is the block diagram of the identification reader and tag.

FIG. 2 is the schematic drawing of the direct-connection embodiment of the coupling means that is used in the reader.

FIG. 3 is the schematic drawing of the first embodiment of the two-winding-transformer coupling means that is used in the reader.

FIG. 4 is the schematic drawing of the second embodiment of the two-winding-transformer coupling means that is used in the reader.

FIG. 5 is the schematic drawing of the three-winding transformer embodiment of the coupling means that is used in the reader.

FIG. 6 is the block diagram of the first embodiment of the resonance-tracking demodulator in the reader.

FIG. 7 is the block diagram of the second embodiment of the resonance-tracking demodulator in the reader.

FIG. 8 is the block diagram of the preferred embodiment of the driver in the reader.

FIG. 9 is the flow diagram of the preferred embodiment of the subroutine that controls the operations of the microprocessor in the reader when the reader is sending a message to the tag.

FIG. 10 is the flow diagram of the first embodiment of the subroutine that controls the operations of the microprocessor in the reader when the reader is receiving a message from the tag.

FIG. 11 is the flow diagram of the second embodiment of the subroutine that controls the operations of the microprocessor in the reader when the reader is receiving a message from the tag.

FIG. 12 is the schematic drawing of the direct-connection embodiment of the coupling means that is used in the tag.

FIG. 13 is the schematic drawing of the first embodiment of the two-winding-transformer coupling means that is used in the tag.

FIG. 14 is the schematic drawing of the second embodiment of the two-winding-transformer coupling means that is used in the tag.

FIG. 15 is the schematic drawing of the three-winding transformer embodiment of the coupling means that is used in the tag.

FIG. 16 is the schematic drawing of the four-winding transformer embodiment of the coupling means that is used in the tag.

FIG. 17 is the schematic drawing of the five-winding transformer embodiment of the coupling means that is used in the tag.

FIG. 18 is the block diagram of the preferred embodiment of the resonance-tracking modem in the tag.

FIG. 19 is the flow diagram for a method of determining the frequency of a single cycle of a frequency-shift-keyed signal.

FIG. 20 is the flow diagram for a method of determining the frequency of a frequency-shift-keyed signal during a bit period.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The functional block diagram for the preferred embodiment of the electronic identification system with improved sensitivity is shown in Fig. 1. The basis of communications between the reader 1 and the tag 3 is an alternating magnetic field established by the coil 5 of the reader. In order to maximize the magnetic field and the range of communication, the coil is connected by means of the coupling circuit 7 to capacitors 9 to form a series-resonant circuit. Two capacitors are used so as to facilitate the use of a push-pull driver 11 which supplies alternating current to the series-resonant circuit.

The frequency of the alternating current supplied by the driver 11, typically between 100 and 400 kHz, is derived from the frequency of the signal supplied by the voltage-controlled oscillator/clock generating circuit (VCO/CGC) 13 which in turn is controlled by a signal supplied by the resonance-tracking demodulator 15. Overall control of the resonance-tracking demodulator is exercised by the microprocessor 17.

The resonance-tracking demodulator 15 performs two functions. One function is to maintain the series-resonant circuit comprising coil 5 and capacitors 9 in a state of resonance or near to a state of resonance. When the reader ages or experiences environmental changes as when the temperature changes or when the reader is moved about in search of a tag, the resonant frequency of the coil/capacitor circuit can change. If the driving frequency is fixed, the circuit may be operating in a non-optimum tuning condition thereby adversely affecting the communication range of the system.

In order to achieve improved performance, the resonancetracking demodulator 15 maintains the coil/capacitor circuit in a resonant or near-resonant condition by either (1) adjusting the frequency of the signal supplied to the driver 11 by the VCO/CGC 13 so that the driving frequency of the coil/capacitor circuit is the same or nearly the same as the resonant frequency of the circuit or (2) adjusting the inductance of coil 5 or the capacitance of capacitors 9 (as indicated

by the dashed control lines) to maintain the resonant frequency of the coil/capacitor circuit the same or nearly the same as the driving frequency.

The resonance-tracking demodulator 15 determines the state of resonance of the coil/capacitor circuit by varying either the frequency of the VCO in the VCO/CGC 13, the inductance of the coil 5, or the capacitance of the capacitors 9 and observing the amplitude and/or the phase of the signals appearing at terminals 1 and 4 of the coupling circuit 7.

The second function of the resonance-tracking demodulator 15 is to extract the amplitude or phase variations of the signal appearing across the coil 5, the extracted information being used in maintaining the coil/capacitor circuit in resonance or near resonance and in extracting the data transmitted by the tag 3 to the reader 1.

The tag 3 transmits data to the reader 1 by modulating the magnetic field produced by coil 5 in accordance with the data to be transmitted. This modulation is manifested at terminals 1 and 4 of the coupling circuit 7 and demodulation is accomplished by the resonance-tracking demodulator 15 using the signals at terminals 1 and 4 and signals supplied by the VCO/CGC 13.

A user exercises overall control of the reader 1 by means of an RS-232C interface to the microprocessor 17 or by means of a user-exercised tactile interface to the control unit 21 which interfaces with the microprocessor.

A display unit 23 driven by the microprocessor 17 provides information to the user as to the status of the system and displays the data received from a tag.

The circuit structure of the tag 3 parallels in many respects that of the reader 1. The coil 50 is coupled through the coupling circuit 53 to the capacitor 55, thereby forming a resonant circuit.

When the tag 3 is transmitting data to the reader 1 the resonance-tracking modem 57 supplies signals to the driver 59 which drives the coil/capacitor resonant circuit at the frequency of the alternating magnetic field in accordance with the data supplied to the resonance-tracking modem by the microprocessor 61.

When the tag 3 is receiving data from the reader 1, the resonance-tracking modem 57 demodulates the signals appearing at terminals 5 and 10 of the coupling circuit 53 and supplies the resulting binary signal to the microprocessor 61.

For best performance in either the transmit or receive mode, the coil/capacitor circuit in the tag should be operating at or near resonance. This condition is achieved by means of the resonance-tracking modem 57 which monitors the reader-originated signal appearing at terminals 5 and 10 of the coupling circuit 53, thereby determining the appropriate correction to be made in coil inductance or capacitor capacitance to achieve a condition of resonance.

A computer interface terminal is provided on the tag for the purpose of installing programs and data in the microprocessor 61 and testing the tag circuitry.

The AC/DC power converter 63 converts the received reader signal appearing at terminals 1 and 4 of the coupling circuit 53 to DC which is used to power all of the other active circuits in the tag 3.

Four alternative embodiments of the reader coupling circuit 7 are shown in Figs. 2 through 5. The terminal numbers correspond to the terminal numbers shown on the coupling circuit 7 in Fig. 1.

The coupling circuit of Fig. 2 directly connects the coil 5 and the capacitors 9. The resonance-tracking demodulator 15 is connected directly across the coil 5.

The coupling circuits of Figs. 3 and 4 utilize a transformer to achieve a better match between the driver 11 and the load represented by the tag 3 when the field generated by reader coil 5 couples with the tag coil 50, thereby achieving a greater transfer of power, between the reader 1 and the tag 3. The resonance--tracking demodulator 15 can be connected to either the transformer primary winding (Fig. 3) or the secondary winding (Fig. 4), depending on the voltage requirement of the resonance-tracking demodulator.

The coupling circuit of Fig. 5 provides a separate winding for driving the resonance-tracking demodulator 15 thereby permitting the voltage across coil 5 to be tailored in magnitude to the needs of the device.

An embodiment of the resonance-tracking demodulator 15 which utilizes a frequency-modulating, zero-average, square-wave signal C_{fm} applied to the frequency-control terminal of the VCO/CGC 13 to discover the state of resonance of the coil/capacitor circuit 5, 7, and 9 is shown in Fig. 6. The VCO/CGC supplies C_{fm} to the analog signal summer 73 which passes it through to the frequency control terminal of the VCO/CGC with the result that the frequency of the VCO alternates between two values at the modulating frequency f_{fm} that is a submultiple of the frequency f_{drive} of the driving signal supplied by the driver 11 to the coil/capacitor circuit 5, 7, and 9. The difference between the two VCO frequency values typically equals the VCO frequency f_{VCO} divided by 2Q where Q is the Q of the coil/capacitor circuit 5, 7, and 9.

The amplitude demodulator 75 extracts a signal proportional to the amplitude of the signal appearing across coil 5, and the extracted signal is processed together with the C_{fm} supplied by the VCO/CGC 13 in the balanced mixer 77 wherein the extracted signal is reversed in sign each time C_{fm} takes on a particular one of its two values.

The output signal from the balanced mixer 77 is offset by the fixed bias voltage prior to being fed into the sampled integrator 79.

The sampled integrator 79 continually integrates the signal from the balanced mixer 77, samples the integration in accordance with the bit rate clock C_{br} supplied by the VCO/CGC 13, and maintains each sampled integration value at its output port until the next sample is obtained. The bit rate clock C_{br} has a frequency f_{br} equal to the rate at which bits are transmitted between the reader 1 and a tag 3. The quantities f_{fm} and f_{br} are chosen such that f_{fm}/f_{br} is an integer.

The output of the sampled integrator 79 is combined with C_{fm} in the analog signal summer 73 and the sum signal controls the instantaneous frequency of the VCO in the VCO/CGC 13. The sampled integrator component of the output of the analog signal summer controls the average frequency of the VCO. The steady-state value of the sampled integration corresponds to the VCO control voltage for which the driver 11 frequency f_{drive} is offset from the resonant

frequency of the coil/capacitor circuit by an amount determined by the magnitude of the bias voltage and in a direction determined by the sign of the bias voltage.

If the resonant frequency of the coil/capacitor circuit 5, 7, and 9 changes as a result of a change in coupling of the field of reader coil 5 to tag coil 50, the sampled integration will change so as to bring about an equivalent change in the driver 11 average frequency.

In an alternative arrangement, the signal from the sampled integrator 79, instead of entering the analog signal summer 73 and controlling the frequency of the VCO in the VCO/CGC 13, maintains the coil/capacitor circuit 5, 7, and 9 in resonance by controlling either the inductance of coil 5 or the capacitance of capacitors 9. Under these circumstances, the average frequency of the VCO is continually maintained at some constant value.

In still another alternative arrangement, C_{fm} modulates either the inductance of coil 5 (e.g. by means of a saturable reactor in the field of the coil) or the capacitances of capacitors 9 (e.g. by selectively connecting individual capacitors in parallel or by a plurality of voltage-controlled capacitors) instead of the frequency of the VCO.

A tag may use either phase shift keying or frequency shift keying for transmitting data to a reader. In the case of phase shift keying, the data transmitted by a tag appears as amplitude modulation of the signal from the coupling circuit 7 at a frequency f_{dm0} which, like f_{fm}, is also a submultiple of the driving frequency f_{drive}. The quotient f_{dm0}/f_{br}, like f_{fm}/f_{br}, is also an integer. A bit is identified by determining the phase of the amplitude modulation with reference to the beginning of the bit period. A "0"bit is associated with zero-phase amplitude modulation--amplitude modulation that is high for the first half-period of the modulation waveform. A "1" bit is associated with a 180-degree-phase amplitude modulation--amplitude modulation that is low for the first half-period of the modulation waveform.

In the case of frequency shift keying, the data transmitted by a tag appears as amplitude modulation of the signal from the coupling circuit 7 at a frequency f_{dm0} when a "0"bit is being transmitted and at a frequency f_{dm1} when a "1"bit is

being transmitted. The frequencies f_{dm0} and f_{dm1}, like f_{fm}, are also submultiples of the driving frequency f_{drive}. The quotients f_{dm0}/f_{br} and f_{dm1}/f_{br}, like f_{fm}/f_{br}, are also integers. A bit is identified by determining the frequency of the amplitude modulation with reference to the beginning of the bit period. A "0"bit is associated with the frequency f_{dm0} and a "1" bit is associated with the frequency f_{dm1}.

The determination of phase is made by multiplying in the balanced mixer 81 the signal from the amplitude demodulator 75 by a zero-phase, zero-average square wave C_{dm0} of frequency f_{dm0} supplied by the VCO/CGC 13 and integrating the product over each bit period in the sampled integrator 83, the integration value for each bit period being maintained at the output port of the sampled integrator until the integration for the next bit period becomes available. The beginning and ending of the integration periods are indicated by the bit rate clock C_{br} since the tag transmits its bits in synchronism with the bit-rate clock C_{br}.

The use of frequency modulation requires two balanced mixers 81 and 82 and two sampled integrators 83 and 84. The determination of frequency is made by multiplying in the balanced mixer 81 the signal from the amplitude demodulator 75 by a zero-phase, zero-average square wave C_{dm0} of frequency f_{dm0} supplied by the VCO/CGC 13 and integrating the product over each bit period in the sampled integrator 83, the integration value for each bit period being maintained at the output port of the sampled integrator until the integration for the next bit period becomes available. Also, the signal from the amplitude demodulator 75 is multiplied in the balanced mixer 82 by a zero-phase, zero-average square wave C_{dm1} of frequency f_{dm1} supplied by the VCO/CGC 13 and integrating the product over each bit period in the sampled integrator 84, the integration value for each bit period being maintained at the output port of the sampled integrator until the integration for the next bit period becomes available. The beginning and ending of the integration periods are indicated by the bit rate clock C_{br} since the tag transmits its bits in synchronism with the bit-rate clock C_{br}.

The clock signals C_{dm0} and C_{dm1} are square waves with zero average values, and consequently, a signal with frequency f_{dm0} from the amplitude demodulator 75

will result in a positive value at the sampled integrator 83 output port and a zero value at the sampled integrator 84 output port. Similarly, a signal with frequency f_{dm1} from the amplitude demodulator 75 will result in a zero value at the sampled integrator 83 output port and a positive value at the sampled integrator 84 output port. Thus, the microprocessor 17 can identify a received bit from the magnitudes of the signals at the outputs of the sampled integrators 83 and 84.

The frequencies f_{fm}, f_{dm0}, and f_{dm1} are chosen such that the quotients f_{fm}/f_{br}, f_{dm0}/f_{br}, and f_{dm1}/f_{br} differ by an integer so that the resonance tracking process and the data extraction processes will not interfere.

There are many existing tags that utilize frequency-shiftkeying for sending data to a reader and are not bit-synchronized with the reader. The zero-crossing detector 85 together with software routines in the microprocessor 17 serve to extract the data from such signals. The zero-crossing detector produces a square wave signal wherein the zero crossings coincide with those of the signal out of the amplitude demodulator 75. The software demodulation routines will be discussed later.

An alternative embodiment of the resonance-tracking modem 15 which utilizes a phase-locked loop to maintain a state of resonance or near-resonance in the coil/capacitor circuit is shown in Fig. 7.

When the coil/capacitor circuit 5, 7, and 9 is not in resonance, the voltage across the coil 5 is approximately in phase or a half-cycle out of phase with the driving voltage from driver 11. This situation is recognized by passing the signal at terminals 1 and 4 of the coupling circuit 7 through a hard limiter 95 which removes any amplitude variations and then mixing the result with the zero-average, square-wave clock signal C_{drive} having the same frequency f_{drive} as and synchronized with the driving signal in the balanced mixer 97. The output of the balanced mixer is either positive or negative depending on whether the resonant frequency of the coil/capacitor circuit is above or below the driving signal frequency.

The output of the balanced mixer, offset by the bias voltage, is integrated in the sampled integrator 99 which produces at its output port a sample of the

integration at intervals of the bit period and maintains each sample at its output port until a new sample becomes available. The output from the sampled integrator controls the frequency of the VCO in the VCO/CGC 13 thereby causing the VCO frequency and the driving signal frequency (which is derived from the VCO frequency) to either increase or decrease until the driving signal frequency is offset from the coil/capacitor resonant frequency by an amount determined by the magnitude of the bias voltage and in a direction determined by the sign of the bias voltage.

When the coil/capacitor circuit reaches a state of resonance or near-resonance, the coil signal is approximately a quarter-cycle out of phase with the driving signal, the output of the balanced mixer is zero, and the output of the sampled integrator remains constant until the resonant frequency of the coil/capacitor circuit changes.

Data transmitted from a tag 3 to the reader 1 is extracted from the signal appearing at terminals 1 and 4 of the coupling circuit 7 by devices 103, 105, 106, 107, 108 and 109 in exactly the same way as the same function was accomplished by devices 75, 81, 82, 83, 84, and 85 in Fig. 6.

The preferred embodiment of the driver 11 is shown in Fig. 8. This embodiment utilizes the microprocessor 113, the four level shifters 115, 116, 117, and 118, and the driving circuit 119 to generate a stepped waveform. The generated waveform can be a simple two-level square wave or a more complicated three-level waveform. The preferred waveform is the three-level waveform for which regions centered on the zero crossings of a sine wave are represented by a zero level, the negative-value regions of the sine wave are represented by a negative level, and the positive-value regions of the sine wave are represented by a positive level, the absolute values of the negative and positive levels being equal.

The levels of four two-level waveforms $F_{P1}(n\Delta t)$, $F_{N1}(n\Delta t)$, $F_{P2}(n\Delta t)$, and $F_{N2}(n\Delta t)$ for one cycle are stored in the microprocessor 113 and retrieved at intervals of Δt and supplied respectively to the level shifters 115, 116, 117, and 118 which convert the two-level input waveforms into two-level output waveforms,

the levels of the two-level output waveforms being such that the associated field-effect transistors in the driving circuit 119 either conduct current or do not conduct. The waveforms with P subscripts drive the P-channel devices and the ones with N subscripts drive the N-channel devices in the driving circuit 119.

One cycle of the two-level waveforms is represented by values of n ranging from 0 to N-1 where N is a predetermined integer. Thus, $N\Delta t$ is the period of the driving signal. The clock signal C_{m1} with frequency f_{m1} is supplied by the VCO/CGC 13 to the microprocessor 113 and causes the microprocessor to produce levels at its output at the f_{m1} rate. The frequency f_{m1} divided by N equals the frequency f_{drive} of the output signal of the driver 11. The address n of a level is obtained by the counter 121 counting modula N the cycles of the clock signal C_{m1}.

The amplitude of the output signal of the driver 11 is governed by the microprocessor 113 in accordance with the clock signals Cdm0 and C_{dm1} supplied by VCO/CGC 13 and the data bit stream D supplied by the microprocessor 17. The reader 1 can use phase shift keying, frequency shift keying, or a combination of the two in transmitting data to the tag.

Phase shift keying is accomplished in the following way. If the low and high values of the clock signals are represented by "0"and "1"respectively, then switches 120 and 122 connect V_{DD1} and V_{SS1} to the driving circuit 119 whenever $(C_{dm0} + D)_{modula\ 2} = 1$. Switches 120 and 122 connect V_{DD2} and V_{SS2} to the driving circuit 119 whenever $(C_{dm} + D)_{modula\ 2} = 0$. Alternatively, C_{dm1} could be used instead of C_{dm0} in implementing phase shift keying. The difference between V_{DD1} and V_{SS1} is approximately 10 volts. The difference between V_{DD2} and V_{SS2} is approximately 12 volts.

Frequency shift keying is accomplished by driving the switches 120 and 122 with either C_{dm0} or C_{dm1} depending on the value of the bit to be transmitted to the tag.

Twice the communication capacity can be realized by selecting either C_{dm0} or C_{dm1} in accordance with a first bit stream and selecting the phase of the selected C_{dm0} or C_{dm1} in accordance with a second bit stream.

The driving circuit 119 consists of the two power-handling P-channel field-effect transistors 125 and 127 and the two powerhandling N-channel field-effect transistors 129 and 131. If the voltages applied to the gates of transistors 125 and 131 permit the transistors to conduct current, current will flow from the V_{DD} supply through transistor 125 to terminal 2 of the coupling and from terminal 3 of the coupling circuit through transistor 131 to the V_{SS} supply.

Similarly, if the voltages applied to the gates of transistors 127 and 129 permit the transistors to conduct current, current will flow from the V_{DD} supply through transistor 127 to terminal 3 of the coupling and from terminal 2 of the coupling circuit through transistor 129 to the V_{SS} supply.

Since the transistors 125, 127, 129, and 131 are all individually controlled, each transistor may be on or off at any particular time.

Field-effect transistors 125, 127, 129, and 131 can be all N-channel devices which are smaller, less expensive, have lower "on" resistance, and are more plentiful on the market than P-channel devices. In order to accommodate the N-channel devices, the gates would be coupled to level shifters 115, 116, 117, and 118 by transformers. It is possible to generate less sophisticated driving signals with a single transformer having one primary winding and four secondary windings, one for each transistor date. One level shifter would be used to drive the primary winding of the transformer.

A class of driving signals can be generated where the waveforms supplied by the microprocessor 113 to level shifters 116 and 117 are simply inverted versions of the waveforms supplied to level shifters 115 and 118 respectively. In fact, there are many possible alternatives for generating the signals to be applied to the gates of field-effect transistors 125, 127, 129, and 131 and achieve the objectives of the present invention.

The resistors 133, 135, 137, and 139 prevent ringing in the gate circuits on turn-on of the transistors and slow down the turn-on time. The diodes 141, 143, 145, and 147 protect the gates of the power-handling field-effect transistors from voltage spikes which could cause progressive gate damage and eventual failure.

The microprocessor 17 is a commercially-available microprocessor having a performance level equal to or greater than an 80C51 or 87C51. Data and/or commands are entered into the microprocessor by means of a keyboard or switches in the control unit 21 or by means of a RS-232C interface with the microprocessor. A message entered for transmission to a tag is stored in the microprocessor memory. When a command to "send message" is entered, the subroutine shown in Fig. 9 is performed by the microprocessor.

In the absence of commands from microprocessor 17, the microprocessor 113 in the driver 11, provides inputs to the level shifters 115, 116, 117, and 118 that result in voltages at their output ports that prevent any current from flowing through terminals 2 and 3 of the coupling circuit 7. The microprocessor 17, upon receiving the "send message" command, performs step 161 in Fig. 9 thereby causing the microprocessor 113 in the driver 11 to clear the counter 121 and then to generate the two- or three-level waveforms. The microprocessor 17 transmits a synchronization pattern consisting of alternating "0's" and "1's" during step 163 for a period of time sufficient for the tag to achieve bit synchronization. Then, in step 165, the microprocessor 17 starts sending the message data D stored in memory to the microprocessor 113 in the driver 11. The microprocessor 17 continually performs the "send message" program for as long as the "send message" command is entered into the microprocessor by the user. The microprocessor 17 shuts the driver down after the message transmission has been completed if the "send message" command no longer appears at the input port of the microprocessor.

Tag synchronization and validation, as described in the material that follows, permits tag data to be received that may contain embedded sync patterns. This capability is important in that it allows the full tag data space to be utilized for the transmission of arbitrary data. Without this capability, other means would have to be used such as bit stuffing or sync filtering to remove sync patterns from the transmitted tag data. Such processes are undesirable in that they restrict the possible tag data space or impose a high penalty in the number of bits available for the transmission of data.

When the "receive message" command is entered into the microprocessor 17 by the user, the microprocessor performs the operations indicated either in Fig. 10 or Fig. 11.

The process of Fig. 10 begins with step 167 where the microprocessor 17 activates the driver 11 and establishes an alternating magnetic field by means of coil 5 and transmits the bit synchronization pattern for a period of time sufficient for the tag to achieve bit synchronization. The tag 3, if it determines that the alternating magnetic field carries no data after the transmission of the bit synchronization pattern ceases, repeatedly transmits a 96-bit message stored in the microprocessor 61 memory until the alternating magnetic field is no longer generated by the reader 1. The 96 bits are comprised of a 2-bit preamble (01), an 8-bit synchronization sequence (01111110), a 6-bit protocol, and an 80-bit encrypted version of 64 bits of tag data and a 16-bit checksum for the tag data that allows error detection by the reader. The protocol word identifies the process to be used in converting the 80-bit encrypted tag data-and-checksum sequence into meaningful tag data. The checksum is determined in accordance with the CCITT V.41 code-independent error-control system.

The microprocessor 17 waits in step 169 for a 01 combination (which may or may not be the 2-bit preamble) to be received from the sampled integrator 83 in the resonance-tracking, modem 15, indicating that bit synchronization has been achieved by the tag and that data is being received. Then, in step 171, the microprocessor 17 accumulates another 94 bits, for a total of 96 bits including the initial 01 combination, (numbered from 0 to 95 according to order of arrival) and stores them in memory.

In step 173, bits 2-9 are compared with the synchronization sequence. If there is a match, bits 10-15 are compared with the protocol sequence in step 175. If there is a match, the 80-bit tag data sequence is decrypted in step 177 and a cyclic redundancy check (CRC) is made in step 179 by dividing the polynomial

$$D_{79}X^{79} + D_{78}X^{78} + D_{77}X^{77} + \ldots D_0X^0$$

by the generating polynomial

$$x^{16} + X^{12} + X^5 + 1.$$

If there is a zero remainder, the CRC indicates an absence of errors, in which case the microprocessor 17 terminates the generation of the alternating magnetic field and causes the tag data to be displayed on display 23.

If the results of any of the steps 173, 175, and 181 is negative, then the microprocessor 17 waits in step 185 for the next bit to be determined by the phase-shift-keying demodulator comprising the balanced mixer 81 and the sampled integrator 83 or the frequency-shift-keying demodulator comprising the balanced mixers 81 and 82 and the sampled integrators 83 and 84, assigns this bit the number 96, discards the bit numbered 0, and reduces the numbers of all of the remaining bits by 1. The microprocessor then repeats the steps beginning with step 173 unless the number of bits received exceeds 192 (step 189) in which case the microprocessor returns to the beginning of the program.

The alternative process shown in Fig. 11 is more complex than the one shown in Fig. 10 but is less demanding insofar as real-time processing is concerned. The process begins with step 201 where the microprocessor 17 activates the driver 11 and establishes an alternating magnetic field by means of coil 5.

The microprocessor 17 waits in step 203 for a 01 combination to be received from the sampled integrator 83 in the resonancetracking modem 15, indicating that bit synchronization has been achieved by the tag and that data is being received. Then, in step 205, the microprocessor 17 accumulates the next 8 bits (numbered from 0 to 7) and compares them in step 207 with the synchronization sequence. If there is not a match, the microprocessor waits in step 209 for the next bit to become available. In step 211, the bit numbers are increased by 1, the oldest bit (numbered 8) is discarded, the newest bit is added and assigned the number 0, and the process beginning with step 207 is repeated unless the total number of bits received exceeds 96 (step 213) in which case the microprocessor returns to the beginning of the program.

If at step 207 there is a match between bits 0-7 and the synchronization sequence, then an additional 88 bits, numbered from 8 to 95, is accumulated in step 217. Bits 8-13 are compared with the protocol sequence in step 219. If there

is a match, the following 80 bits are decrypted in step 221, and the cyclic redundancy check is made in step 223. If the remainder is zero (indicating no errors), the microprocessor terminates the generation of the alternating magnetic field and causes the tag data to appear on display 23.

If either of the steps 219 or 225 give negative results, then in step 227 the numbers associated with the 96 bits being processed are increased by 1 except for the bit numbered 95 which is renumbered 0. If the total number of passes through step 227 is less than 96 (step 229), bits 0-7 are compared with the synchronization sequence in step 231, and if there is a match, the process is repeated beginning with step 219.

If at step 229 the total number of passes through step 227 is not less than 96, then the microprocessor returns to the beginning of the program.

The preferred embodiment of the coupling circuit 53 in the tag 3 depends on the characteristics of the components to which it connects, the need for achieving the greatest possible transfer of power from the source to the sinks, and the sensitivity of tag customers to the costs of tags and readers.

The simplest embodiment is shown in Fig. 12 where all terminals shown at the left of the coupling circuit 53 in Fig. 1 are connected together and all terminals at the right are connected together. There are few means of optimization with this arrangement and communication range between reader and tag is likely to be sacrificed as a result. On the other hand, it is the least costly embodiment of the coil/coupling circuit/capacitor circuit 50, 53, and 55.

The embodiments shown in Figs. 13 and 14 provide a means of improving the power transfer efficiency between reader and tag by utilizing the impedance transforming characteristics of a transformer. In addition, the impedance transforming properties of a transformer allows a greater latitude in designing the coil 50 and selecting the capacitor 55.

Adding a third winding to the transformer, as shown in Fig. 15, provides additional opportunities for optimization of the coil/coupling circuit/capacitor circuit 50, 53, and 55. It is still necessary with this circuit for the resonance-

tracking modem 57 and the AC/DC power converter 63 to share a transformer winding and similarly for the capacitor 55 and the driver 59.

Adding a fourth winding to the transformer, as shown in Fig. 16, permits the disparate requirements of the resonance tracking modem 57 and the AC/DC power converter 63 to be satisfied.

Finally, adding a fifth winding to the transformer, as shown in Fig. 17, allows each device drawing power from the coil 50 to have its own individual winding tailored to its own needs.

The choice of an embodiment of the coupling circuit 53 is made on the basis of availability of components, performance requirements imposed by the application, and cost. The design of multi-winding transformers for the purpose of optimizing power transfer or achieving other goals is well understood by those knowledgeable in the art.

The resonance-tracking modem 57 performs three functions. It extracts the data transmitted by the reader 1 from the signal appearing on the coil 50 and supplies this data to the microprocessor 61. It accepts data from the microprocessor for transmission to the reader and generates appropriate waveforms for this purpose that are supplied to the driver 59. And it maintains the coil/coupling circuit/capacitor combination 50, 53, and 55 in resonance or near resonance.

The preferred embodiment of the resonance-tracking modem 57 is shown in Fig. 18. The signal appearing on terminals 5 and 10 of the coupling circuit 53 enters the amplitude demodulator 251, frequency divider 253, frequency divider 255, and frequency divider 285. The amplitude demodulator removes the amplitude modulation from the arriving signal, blocks the DC component, and feeds the resulting DC-blocked amplitude modulation into the two balanced mixers 257 and 259.

The frequency divider 253 generates a DC-blocked square wave signal of frequency f_{fm} by dividing down the input signal which has the frequency f_{drive}. This square wave is synchronized with amplitude modulation from amplitude

demodulator 251 as a result of the signals introduced at the bottom of the frequency divider 253 block.

The square wave produced by the frequency divider 253 constitutes the second input to the balanced mixer 257 and causes the DC-blocked amplitude modulation to be reversed in sign whenever the square wave is negative. The output of the balanced mixer 257, offset by the bias voltage, enters the sampled integrator 261 which continually integrates the incoming signal and provides at its output port the value of the integration at intervals of the bit period. Bit synchronizing signals are introduced at the bottom of the sampled integrator 261 block.

The sampled integrator 261 maintains the most recent integration value at its output terminal until a new integration value is determined. The output of the sampled integrator controls the capacitance of capacitor 55 or, alternatively, the inductance of coil 50, the capacitance or the inductance, as the case may be, being a monotonically increasing or decreasing function of the control signal magnitude.

If the capacitor 55 comprises a plurality of capacitors selectively connected in parallel to obtain a desired capacitance value, then the output of the sampled integrator 261 is converted to a plurality of binary signals, each of which controls a switch associated with each of the plurality of capacitors that may be connected into a parallel configuration. The values of the individual capacitors are so chosen and the switching signals are so designed that the total capacitance of the capacitors connected in parallel is an increasing or decreasing function of the output of the sampled integrator.

The operations performed by the balanced mixer 257 and the sampled integrator 261 result in a change in the integration quantity over a bit period of KA/f_{br} where K is a positive constant, A is the value (a positive or negative number) of the DC-blocked amplitude modulation when the DC-blocked square wave from the frequency divider 253 is positive, and f_{br} is the bit rate.

When the reader 1 initiates a transmission, it frequency modulates the driving signal at a frequency of f_{fm} which also results in an f_{fm} component in the

amplitude modulation if the coil 5, coupling circuit 7, and capacitors 9 in the reader are not in resonance. However, the resonance-tracking demodulator 15 in the reader quickly adjusts the driving frequency to match the resonant frequency of the circuit and by the time the tag 3 is powered up and ready to operate there is essentially no f_{fm} component in the amplitude modulation of the alternating magnetic field produced by the reader coil 5.

If the coil 50, coupling circuit 53, and capacitor 55 in the tag 3 are not in resonance, the square-wave modulation of the driving frequency by the reader will cause an f_{fm} component to appear in the amplitude modulation of the signal appearing across terminals 5 and 10 of the coupling circuit 53. As a result, the output from the sampled integrator 261 will increase if A is positive and decrease if A is negative, thereby causing the capacitance of capacitor 55 or the inductance of coil 50 to change in a way that brings coil 50, coupling circuit 53, and capacitor 55 into resonance or near to resonance, depending upon the value of the bias voltage applied to the balanced mixer 257. At steady-state, the f_{fm} component appearing in the amplitude modulation of the signal across terminals 5 and 10 of the coupling circuit 53 equals the bias voltage and the output from the sampled integrator no longer increases or decreases.

If the coil, coupling circuit, and capacitor start to drift out of resonance or from the chosen point of near-resonance, the f_{fm} component in the amplitude modulation changes, and the sampled integrator automatically changes the capacitance or inductance to bring the circuit back into resonance or to the desired point of near-resonance.

When the reader 1 initiates a transmission, it also begins modulating the alternating magnetic field in amplitude with the square wave of frequency f_{dm0} and shifting the phase by 180 degrees at the beginning of each bit period. The amplitude modulation resulting from the f_{dm0} signal is greater than the amplitude modulation resulting from the frequency modulation by a factor of at least two or three.

The output signal from the amplitude demodulator 251 passes through switch 262 and enters pulse generator 263. Each time the signal crosses the zero

axis, the pulse generator 263 generates a pulse having a duration equal to about $1/2f_{dm0}$. The DC-blocked square wave of frequency f_{dm0} from frequency divider 255 passes through pulse switch 265 and enters pulse generator 267. The pulse generator 267 generates a pulse having a duration equal to about $1/2f_{dm0}$ for each negative-to-positive transition of the square wave from frequency divider 255.

The pulses from pulse generators 263 and 267 are ANDed in AND gate 269 and the pulse from pulse generator 263 and the inverse of the pulse from pulse generator 267 are ANDed in AND gate 271. An uninterrupted succession of coincident pulses from the two pulse generators cause the counter 273 to count up to four at which point the counter produces a signal which passes through switch 275 and sets the flip-flop 277 causing the Qbar output of the flip-flop to go to zero and the switches 262, 265, 275, and 279 to connect to the other terminals. The counter output provides reasonable assurance that the square wave of frequency f_{dm0} produced by frequency divider 255 is in synchronism with the square-wave clock signal of frequency f_{dm0} generated in the reader 1.

If, however, a pulse produced by pulse generator 263 is not accompanied by a pulse from pulse generator 267, a pulse is produced by AND gate 271 since the flip-flop 280 is reset when a tag 3 is first activated and Qbar remains equal to 1 until the counter 273 sets the flip-flop. The output pulse from the AND gate 271 clears the counter of any counts that have been accumulated and also passes through switch 279 and clears the frequency divider 255 so that the next pulse generated by the pulse generator 267 should coincide with the next pulse generated by the pulse generator 263 and result in f_{dm0} synchronization.

The frequency divider 255 generates a DC-blocked square wave of frequency f_{dm0} from the incoming signal and this square wave causes the DC-blocked amplitude modulation extracted by amplitude demodulator 251 from the incoming signal to be reversed in sign in balanced mixer 259 whenever the DC-blocked square wave is negative. The result is a square wave signal at the output port of the balanced mixer 259 which crosses the zero axis at the bit rate f_{br}.

The square wave signal from the balanced mixer 259 passes through switch 262 and enters pulse generator 263 after f_{dm0} synchronization has been achieved.

Each time the square wave from the balanced mixer 259 crosses the zero axis, the pulse generator 263 generates a pulse having a duration equal to about $1/2f_{dm}$.

The DC-blocked square wave of frequency f_{dm} from frequency divider 255 is further divided in frequency divider 281 to give a square wave of frequency f_{br}. The f_{br} square wave passes through switch 265 and enters pulse generator 267 which generates a pulse having a duration equal to about $1/2f_{dm0}$ for each negative-to-positive transition of the square wave from frequency divider 281.

The pulses from pulse generators 263 and 267 are ANDed in AND gate 269 and the pulse from pulse generator 263 and the inverse of the pulse from pulse generator 267 are ANDed in AND gate 271. An uninterrupted succession of coincident pulses from the two pulse generators cause the counter 273 to count up to four at which point the counter produces a signal which passes through switch 275 and sets the flip-flop 280 causing the Qbar output of the flip-flop to go to zero. The counter output provides reasonable assurance that the square wave of frequency f_{br} produced by frequency divider 281 is in synchronism with the square-wave clock signal of frequency f_{br} generated in the reader 1. In other words, an output from counter 273 indicates bit synchronization between the reader 1 and a tag 3.

If, however, a pulse produced by pulse generator 263 is not accompanied by a pulse generator 267, a pulse is produced by AND gate 271 since the flip-flop 280 is reset when a tag 3 is first activated and Qbar remains equal to 1 until the counter 273 sets the flip-flop. The output pulse from the AND gate 271 clears the counter of any counts that have been accumulated and also passes through switch 279 and clears the frequency divider 281 so that the next pulse generated by the pulse generator 267 should coincide with the next pulse generated by the pulse generator 263 and result in bit synchronization.

The pulses that clear frequency divider 281 also clear frequency divider 253. As a result, the last pulse that clears frequency divider 281 and brings about bit synchronization also brings about f_{fm} synchronization by clearing frequency divider 253.

The pulses that clear frequency divider 281 also clear the frequency divider 285 which generates a DC-blocked square wave of frequency f_{dm1} from the incoming signal that is synchronized with the f_{dm1} signal in the reader 1. This square wave causes the DCblocked amplitude modulation extracted by amplitude demodulator 251 from the incoming signal to be reversed in sign in balanced mixer 260 whenever the DC-blocked square wave is negative.

After allowing time for a tag 3 to achieve bit synchronization, the reader 1 begins sending data. The incoming bits are identified by means of the balanced mixers 259 and 260 and the sampled integrators 282 and 284 in the same way as the similar task was accomplished in the reader with balanced mixers 81 and 82 and sampled integrators 83 and 84 (see Fig. 6).

The pulses from pulse generator 267 are used by the sampled integrator 261 as indices of the beginnings and endings of the integration periods before bit synchronization is achieved.

After bit synchronization is achieved and data is not being transmitted by the reader 1, a tag 3 transmits data to the reader. The data is stored in the microprocessor 61 and supplied to the resonance-tracking modem 57 in accordance with the bit rate clock signal generated by frequency divider 281.

The microprocessor 61 can be programmed to use either phase shift keying, frequency shift keying, or a combination of the two. Phase shift keying is accomplished by maintaining switch 287 in the position shown in Fig. 18 and the phase of the f_{dm0} signal from the frequency divider 255 is shifted in phase by 0 or 180 degrees by balanced modulator 283 depending on whether the bit supplied by microprocessor 61 is a "0" or "1" respectively. The signal out of switch 287 provides the input to the driver 59.

Frequency shift keying is accomplished by maintaining the microprocessor 61 inputs to the balanced modulators 283 and 289 at positive levels and changing the position of switch 285 in accordance with the bit value to be transmitted.

Twice the communication capacity can be realized by utilizing phase shift keying and frequency shift keying simultaneously by supplying a first bit stream to the balanced modulators 283 and 289 and a second bit stream to the switch 287.

It was mentioned earlier that a means is provided in the reader 1 of Fig. 1 for demodulating the frequency-shift-keyed (FSK) signals that are produced by many existing tags. The demodulation process is accomplished by the microprocessor 17 in accordance with the routines shown in Figs. 19 and 20.

In Fig. 19 is shown the routine for determining the period of the amplitude modulation of the signal received by the reader 1. The zero-crossing detector 85 (Fig. 6) produces an interrupt of the microprocessor 17 (Fig. 1) each time a positive zero crossing occurs in the amplitude modulation of the received signal. This interrupt causes the routine of Fig. 19 to be executed.

In step 301 the time since the last interrupt occurred is copied from the free running timer register 303 into the temporary register 305 and the timer register is then cleared.

The value in the temporary register is compared with a predetermined high value high_L for the low FSK frequency L in step 307. If the value is less than or equal to high_L, the value is compared with the predetermined low value low_H of the high FSK frequency H in step 309. If the value is greater than low_H, an error is declared in step 311 and the routine returns to the beginning in step 313 to wait for the next interrupt.

If the value is found to be greater than high_L in step 307, the value is compared with the predetermined high value high_H of the high FSK frequency H in step 315. If the value is greater than high_H, an error is declared in step 311 and the routine returns to the beginning in step 313 to wait for the next interrupt.

If the value is found to be less than or equal to low_H in step 309 and less than or equal to the predetermined low value low_L of the low FSK frequency L in step 317, an error is declared in step 311 and the routine returns to the beginning in step 313 to wait for the next interrupt.

If the value is found to be less than or equal to high_H in step 315, it is concluded that the high FSK frequency was transmitted by the tag and the FSK bit variable is set to ONE in step 319. The ONEs counter 321 and the

SAMPLES counter 323 are incremented in step 325 and the routine returns to the beginning in step 313 to wait for the next interrupt.

If the value is found to be greater than low-L in step 317, it is concluded that the low FSK frequency was transmitted by the tag and the FSK bit variable is reset to ZERO in step 319. The SAMPLES counter 323 is incremented in step 329 and the routine returns to the beginning in step 313 to wait for the next interrupt.

The routine shown in Fig. 20 starts when the reader initiates an interrogation of a tag. The microprocessor waits in step 331 until the FSK variable is ZERO and then waits in step 333 until the FSK variable is ONE. A transition from ZERO to ONE indicates the beginning of a bit period and the bit rate timer 335 is started when this occurs.

The microprocessor waits in step 337 for the beginning of the next bit period as indicated by the bit-rate tinier 335 and then proceeds in step 339 to compare half the value in the SAMPLES counter 323 of Fig. 19 with the value in the ONEs counter 321 of Fig. 19. If the SAMPLES value divided by two is greater than the ONEs value, the bit received during the current bit period is recorded as a ZERO in step 341. If the SAMPLES value divided by two is less than or equal to the ONEs value, the bit received during the current bit period is recorded as a ONE in step 343.

The ONEs counter 321 and the SAMPLES counter 321 are cleared in step 345 and the routine returns in step 347 to step 337 to wait for the beginning of the next pit period.

The preferred embodiment has been described in terms of a tag 3 that receives its power from the alternating magnetic field generated by the reader 1. The reader-tag system described herein also functions satisfactorily if the tag is powered by an independent power source such as a battery. It is also not essential that the tag transmit its information while the reader is generating an alternating magnetic field. For example, the reader may trigger a tag by generating an alternating magnetic field for a time period long enough for the tag

to obtain timing information. Then the reader ceases to generate its alternating magnetic field and listens for a response from the tag.

In the preferred embodiment, the reader 1 and the tag 3 communicate data to each other by phase shift keying and/or frequency shift keying a periodic signal which in turn modulates the amplitude of a carrier signal. Other acceptable ways of communicating data are by phase shift keying and/or frequency shift keying a periodic signal which in turn modulates the phase or frequency of the carrier signal and by phase shift keying and/or frequency shift keying the carrier signal directly.

CLAIMS

1. A radio frequency reader for use in obtaining a signal from a remote tag, the reader comprising:

a resonating circuit including a coil coupled to at least one capacitor, the resonating circuit having a resonant frequency;

means for outputting a coupling signal from the resonant circuit;

means for generating a driving signal to drive the coil of the resonating circuit through the at least one capacitor at a driving frequency; and

resonating means for automatically maintaining the resonating circuit in a tuned condition wherein the difference between the resonant frequency and the driving frequency is maintained within a predetermined range.

2. A radio frequency reader for use with a tag that communicates data to the reader, the reader comprising:

a circuit including a coil coupled to at least one capacitor through a transformer;

a generator for generating a driving signal to drive the coil of the circuit;

means for outputting a coupling signal from the circuit;

means for extracting data from the coupling signal.

3. A reader for use with a tag that transmits a periodic signal having a first frequency when a "0" bit is to be communicated and a second frequency when a "1" bit is to be communicated, the reader comprising:

means for receiving the periodic signal;

means for measuring the period of each cycle of the periodic signal received from the tag during a bit period.

4. A reader for use with a tag that communicates data to the reader by repeating a message a plurality of times, the message comprising a preamble consisting of a sync sequence of S bits, a tag data group consisting of T bits, and

an error-detecting group consisting of E bits, the data group and the error-detecting group possibly including false-sync sequences, the reader comprising:

means for receiving the message transmitted by the tag;

means for detecting each sync sequence in the received message;

means for identifying the preamble;

means for extracting the tag data from the received message utilizing the identification of the preamble.

5. A tag for use with a radio frequency reader, the reader establishing an alternating magnetic field in the proximity of the tag, the tag comprising:

a resonating circuit including a coil coupled to at least one capacitor;

means for outputting a coupling signal from the resonating circuit; and

a resonating means for automatically maintaining the resonating circuit in a tuned condition wherein the difference between the resonant frequency and the frequency of the alternating magnetic field is maintained in a predetermined range.

6. A tag for use with a data-communicating reader, the tag comprising:

a coil;

a capacitor;

means for driving the coil;

a transformer means for coupling the capacitor and the driving means and for outputting a coupling signal;

means for extracting data communicated by the reader from the coupling signal; and

means for extracting power from the coupling signal to operate the tag.

7. A tag for use with a reader, the reader communicating a sequence of bits to the tag by transmitting a first signal during a bit period when a "0" bit is to be communicated and a second signal during a bit period when a "1" is to

be communicated, the reader embedding a bit-timing clock signal in the transmitted signals, the tag comprising:

a resonating circuit including a coil, a capacitor, and a coupling means for coupling the coil to the capacitor;

means for generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the transmitted signals;

means for identifying the bit being transmitted during each bit period, the beginning and ending of each bit period being indicated by the bit-timing clock signal.

8. A tag for use with a reader, the reader transmitting a bit-timing clock signal to the tag, the tag comprising:

a coil;

a capacitor;

means for coupling the capacitor to the coil;

means for generating a driving signal to drive the coil;

means for generating a bit-timing clock signal synchronized to the reader bit-timing clock signal;

means for embedding a sequence of bits to be communicated to the reader in the driving signal, the start of each bit being controlled by the bit-timing clock signal.

9. A method for interrogating a tag, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

generating a driving signal;

driving the coil through the capacitor(s) with the driving signal; and

maintaining the coil and the capacitor(s) near resonance.

10. A method for interrogating a tag comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to a tag in the alternating magnetic field.

11. A method for interrogating a tag, the tag responding to an interrogation by transmitting a sequence of bits, the start of each bit being determined by a bit-timing clock signal generated by the tag and synchronized with a bit-timing clock signal originating with the interrogator, the method comprising the steps:

generating a bit-timing clock signal;

generating an alternating magnetic field in which the bit-timing clock signal is embedded;

extracting data transmitted by the tag utilizing the bit-timing clock signal.

12. A method of receiving a communication from a tag which transmits a repeating message comprising a preamble consisting of a sync sequence of S bits, a tag data group of T bits, and an error detecting group of E bits, the data group and the error-detecting group possibly including false-sync sequences, the method comprising the steps:

receiving the data sequence transmitted by the tag;

detecting each sync sequence in the received data sequence; identifying the preamble;

extracting the tag data from the received data sequence utilizing the identification of the preamble.

13. A method for responding to an interrogation by a reader, the method utilizing a resonating circuit comprising at least one capacitor coupled to a coil, the method comprising the steps:

driving the resonating circuit with a driving signal;

maintaining the resonating circuit in resonance;

embedding the sequence of bits to be communicated to the reader in the driving signal.

14. A method for responding to the establishment of an alternating magnetic field by a reader, the reader embedding a bit-timing clock signal in the alternating magnetic field and communicating a sequence of bits by modulating the alternating magnetic field, the method comprising the steps:

deriving a signal from the alternating magnetic field;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded in the alternating magnetic field;

performing at least one weighted integration of the derived signal over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

15. A method for responding to the establishment of an alternating magnetic field by a reader, a bit-timing signal being embedded in the alternating magnetic field by the reader, the method comprising the steps:

deriving a signal from the alternating magnetic field;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal embedded by the reader in the alternating magnetic field;

generating an alternating magnetic field;

modulating the alternating field generated by the responder with a sequence of bits to be communicated to a reader, the start of each transmitted bit being governed by the bit-timing clock signal.

16. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

extracting data communicated by the responder from an alternating magnetic field generated by the responder;

the method performed by the responder comprising the steps:

extracting the bit-timing clock signal from the alternating magnetic field generated by the interrogator;

generating a bit-timing clock signal that is synchronized to the bit-timing clock signal originating with the interrogator; generating an alternating magnetic field;

embedding data to be communicated to the interrogator in the alternating magnetic field generated by the responder, the start of each bit being controlled by the bit-timing clock signal generated by the responder.

17. A method of communication between an interrogator and a responder, the method performed by the interrogator comprising the steps:

generating an alternating magnetic field;

embedding a bit-timing clock signal in the alternating magnetic field;

embedding data to be communicated to the responder in the alternating magnetic field;

the method performed by the responder comprising the steps:

extracting a bit-timing clock signal from the alternating magnetic field generated by the interrogator;

performing at least one weighted integration of a signal derived from the alternating magnetic field generated by the interrogator over a bit period using the bit-timing clock signal to identify the beginning and end of a bit period;

identifying the bit being transmitted during each bit period utilizing the weighted integration(s).

18. The reader of claim 1 or 2, further comprising:

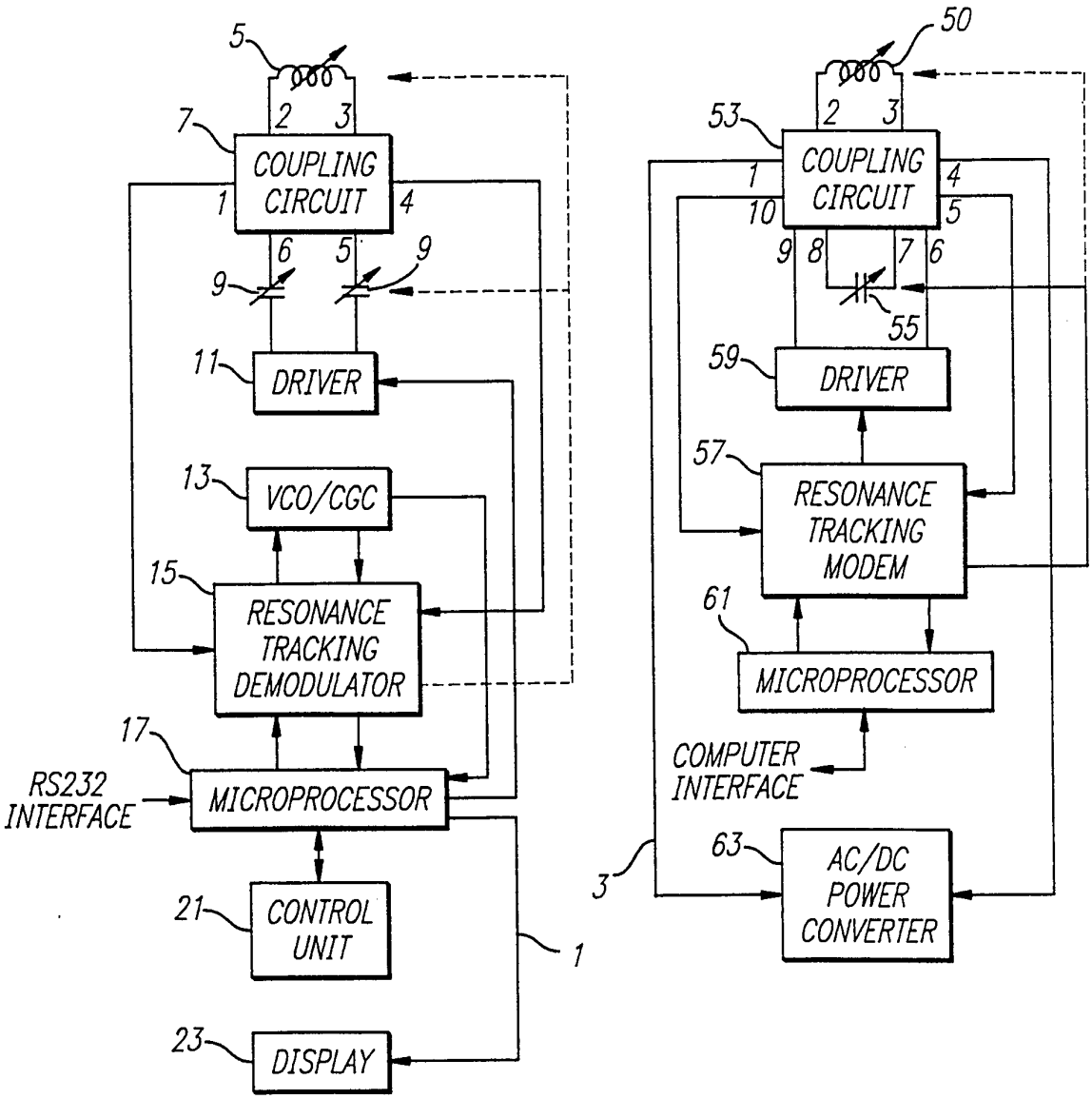
means for embedding a bit-timing clock signal in the driving signal;

means for embedding a sequence of bits to be communicated to a tag in the driving signal.

19. The reader of claim 1 or 2 or 8 or 9 or 13, wherein the driving signal is generated by four transistors connected in a bridge arrangement, two opposing junctions of the bridge being connected to a power supply, the driving signal being available at the remaining two opposing junctions of the bridge, the current flow through the transistors being controlled by a control signal applied to the gate of each transistor.

20. An identification system consisting of a reader and at least one tag, according to any of claims 1-8.

FIG. 1


5
2
3
7
COUPLING CIRCUIT
1
4
6
5
9
9
11
DRIVER
13
VCO/CGC
15
RESONANCE TRACKING DEMODULATOR
17
RS232 INTERFACE
MICROPROCESSOR
21
CONTROL UNIT
23
DISPLAY
1
50
2
3
53
COUPLING CIRCUIT
1
4
10
5
9
8
7
6
55
59
DRIVER
57
RESONANCE TRACKING MODEM
61
MICROPROCESSOR
COMPUTER INTERFACE
63
AC/DC POWER CONVERTER
3

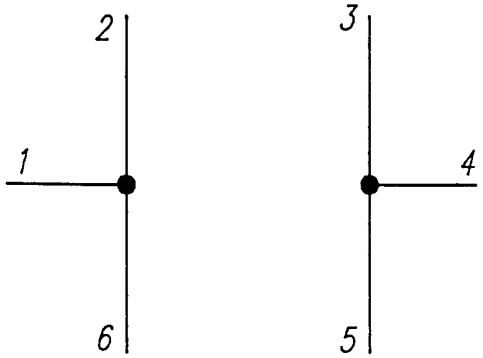


FIG. 2

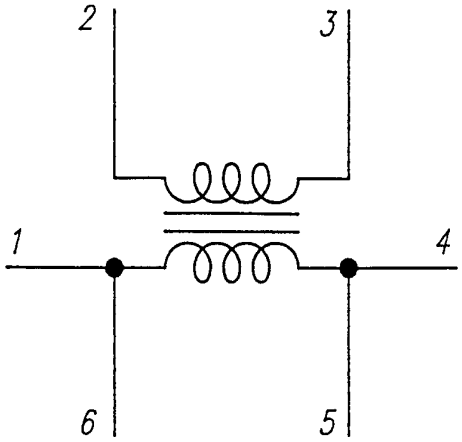


FIG. 3

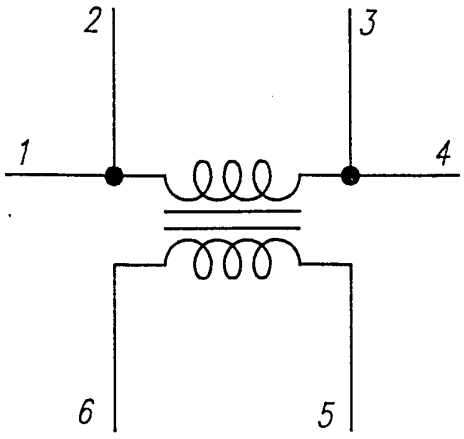


FIG. 4

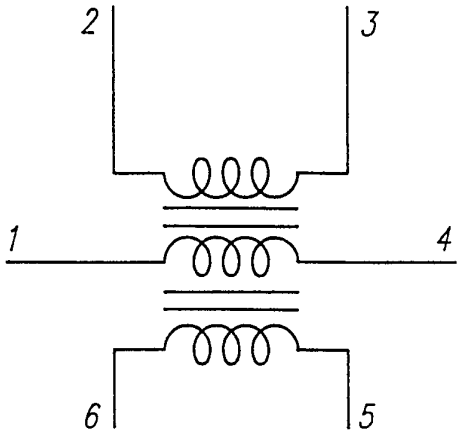


FIG. 5

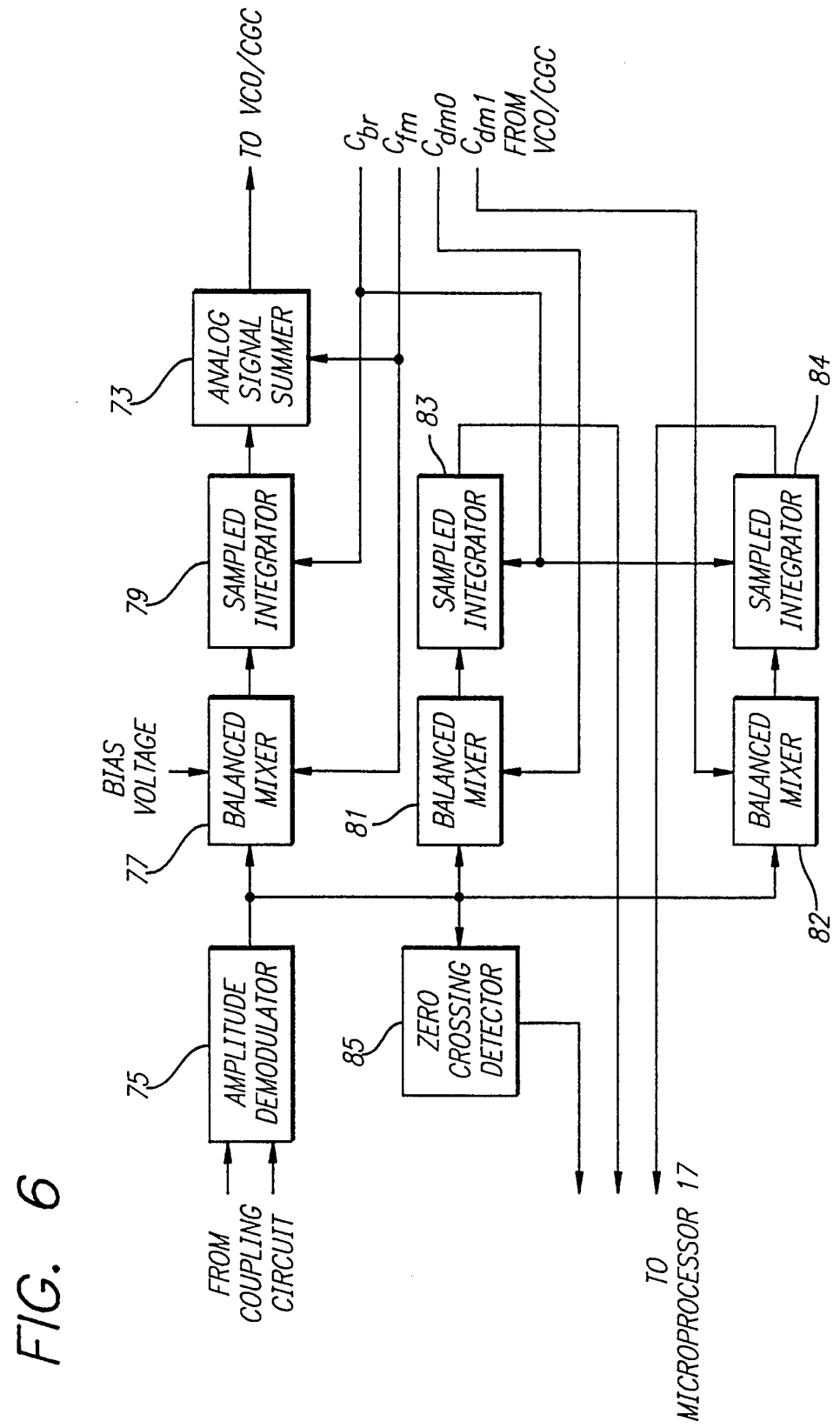

TO VCO/CGC
C_{br}
C_{fm}
C_{dm0}
C_{dm1}
FROM VCO/CGC
ANALOG SIGNAL SUMMER
73
SAMPLED INTEGRATOR
79
83
84
BIAS VOLTAGE
BALANCED MIXER
77
81
82
AMPLITUDE DEMODULATOR
75
ZERO CROSSING DETECTOR
85
FROM COUPLING CIRCUIT
TO MICROPROCESSOR 17

FIG. 6

FIG. 7

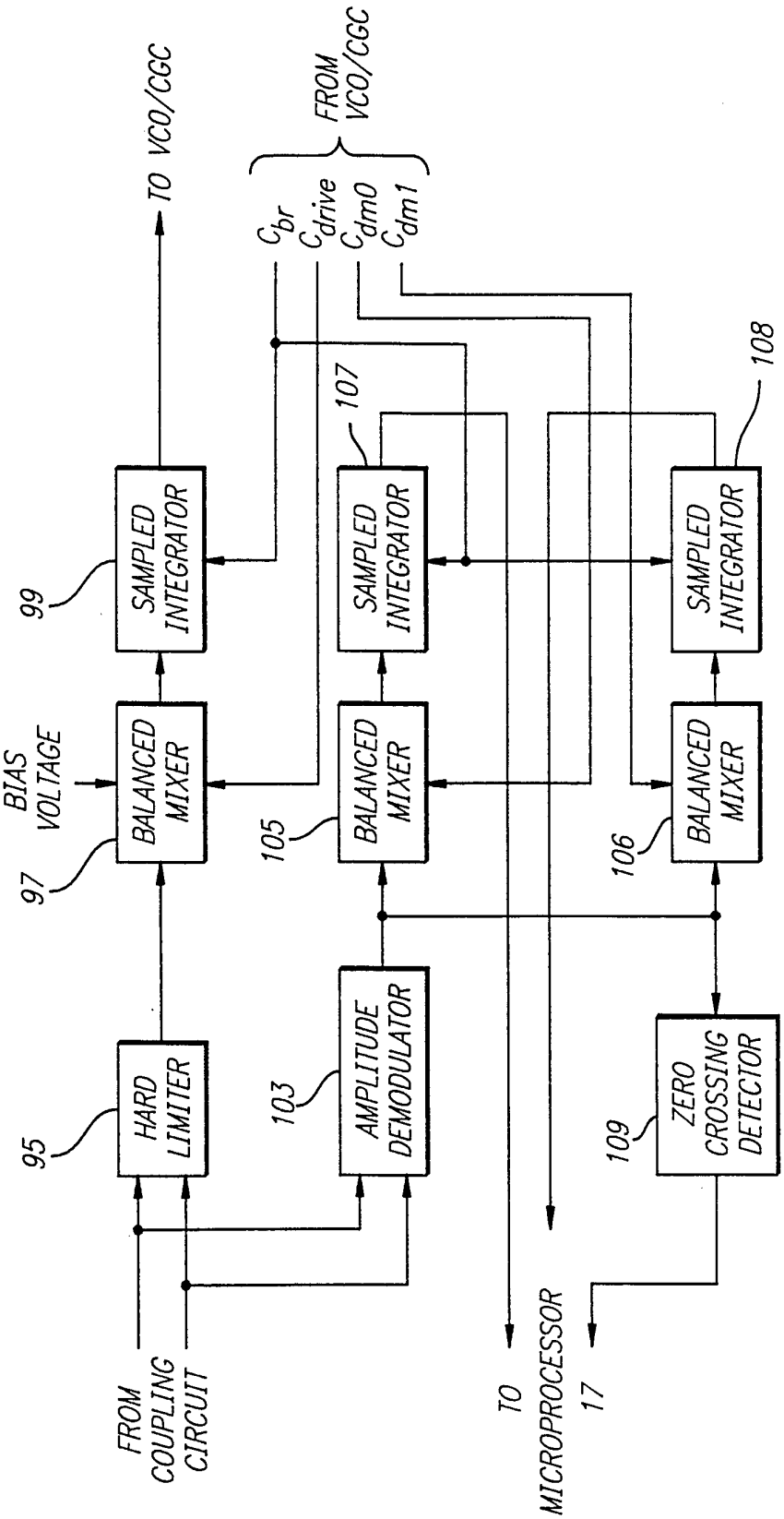

FROM COUPLING CIRCUIT
HARD LIMITER
95
AMPLITUDE DEMODULATOR
103
ZERO CROSSING DETECTOR
109
BIAS VOLTAGE
BALANCED MIXER
97
BALANCED MIXER
105
BALANCED MIXER
106
SAMPLED INTEGRATOR
99
SAMPLED INTEGRATOR
107
SAMPLED INTEGRATOR
108
TO VCO/CGC
FROM VCO/CGC
C_{br}
C_{drive}
C_{dm0}
C_{dm1}
TO MICROPROCESSOR 17

FIG. 8

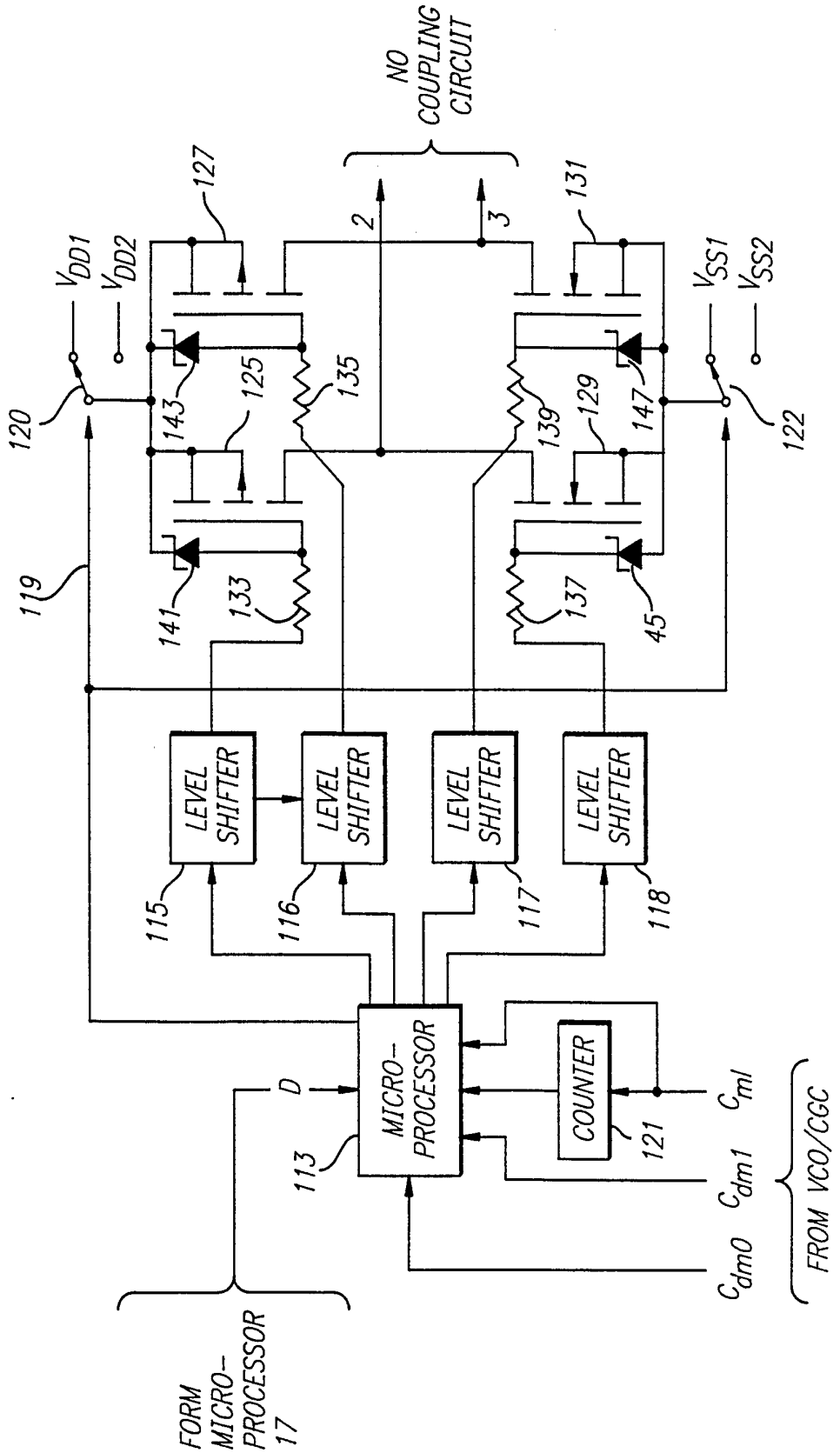

NO COUPLING CIRCUIT
V_{DD1}
V_{DD2}
V_{SS1}
V_{SS2}
120
122
119
127
131
125
135
139
129
143
147
141
133
137
45
2
3
LEVEL SHIFTER
LEVEL SHIFTER
LEVEL SHIFTER
LEVEL SHIFTER
115
116
117
118
MICRO-PROCESSOR
COUNTER
113
121
D
C_{m1}
C_{dm1}
C_{dm0}
FROM VCO/CGC
FORM MICRO-PROCESSOR 17

FIG. 9

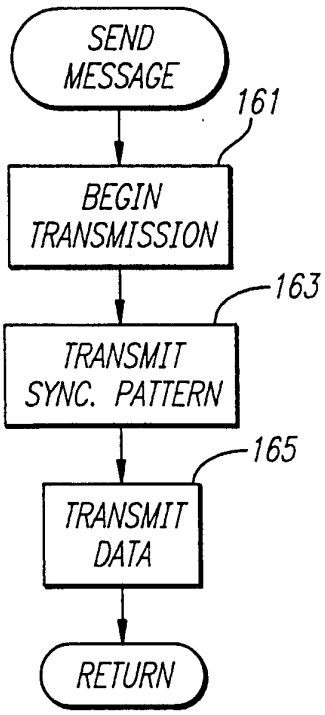
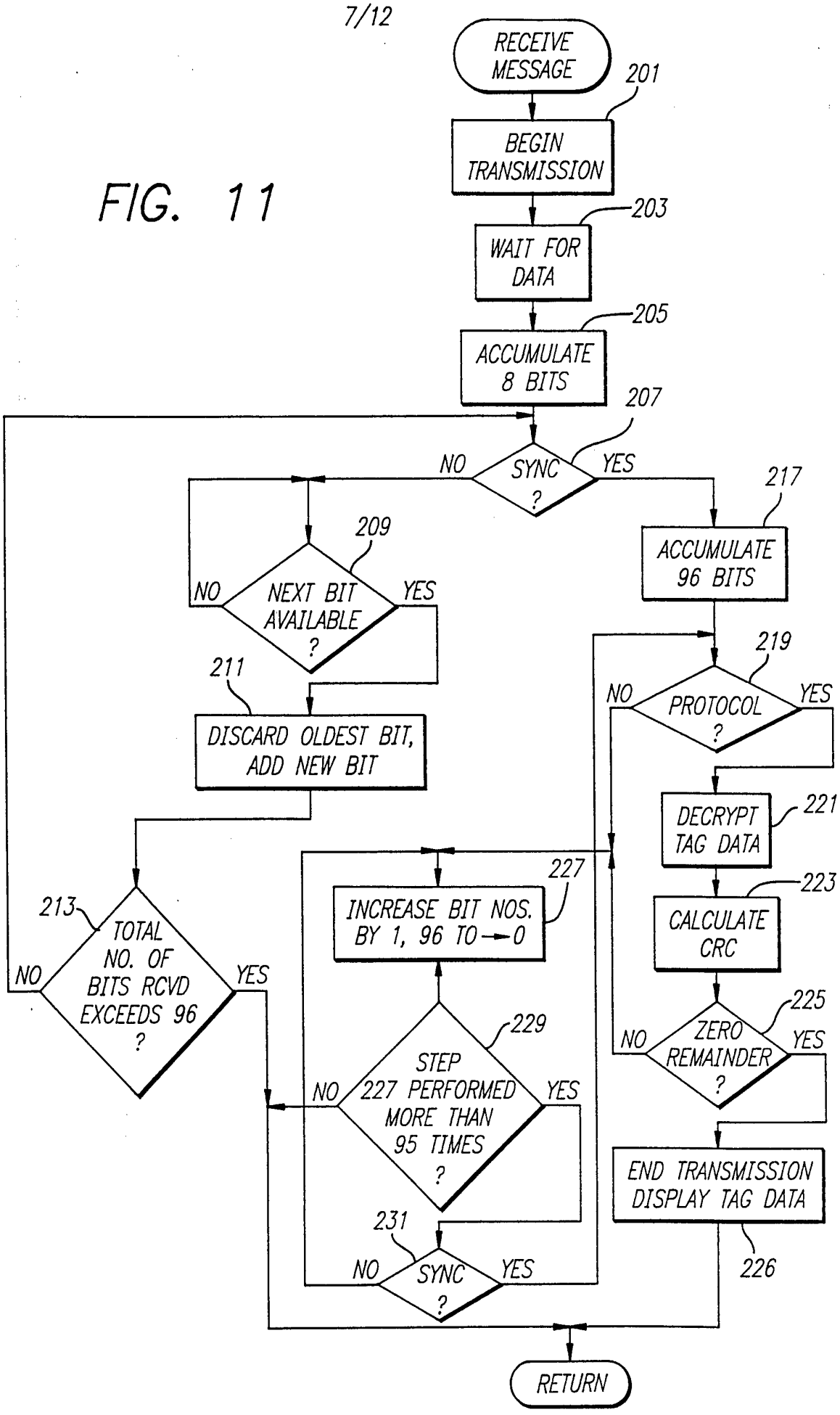

SEND MESSAGE
161
BEGIN TRANSMISSION
163
TRANSMIT SYNC. PATTERN
165
TRANSMIT DATA
RETURN

FIG. 10

RECEIVE MESSAGE
167
BEGIN TRANSMISSION
169
WAIT FOR DATA
171
ACCUMULATE 96 BITS
173
NO
SYNC ?
YES
175
NO
PROTOCOL ?
YES
177
DECRYPT TAG DATA
179
CALCULATE CRC
181
NO
ZERO REMAINDER ?
YES
189
NO
NO. OF BITS RCVD EXCEEDS 191 ?
YES
185
NO
NEXT BIT AVAILABLE ?
YES
END TRANSMISSION DISPLAY TAG DATA
183
DISCARD OLDEST BIT, ADD NEW BIT
187
RETURN

FIG. 11


RECEIVE MESSAGE
201
BEGIN TRANSMISSION
203
WAIT FOR DATA
205
ACCUMULATE 8 BITS
207
SYNC ?
NO
YES
209
NEXT BIT AVAILABLE ?
NO
YES
211
DISCARD OLDEST BIT, ADD NEW BIT
213
TOTAL NO. OF BITS RCVD EXCEEDS 96 ?
NO
YES
217
ACCUMULATE 96 BITS
219
PROTOCOL ?
NO
YES
221
DECRYPT TAG DATA
223
CALCULATE CRC
225
ZERO REMAINDER ?
NO
YES
227
INCREASE BIT NOS. BY 1, 96 TO 0
229
STEP 227 PERFORMED MORE THAN 95 TIMES ?
NO
YES
231
SYNC ?
NO
YES
END TRANSMISSION DISPLAY TAG DATA
226
RETURN

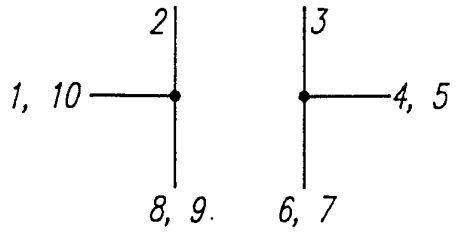


FIG. 12

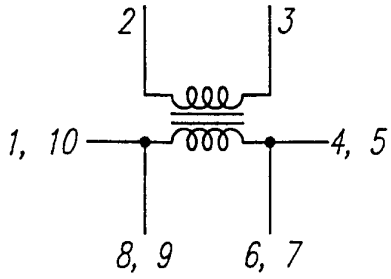


FIG. 13

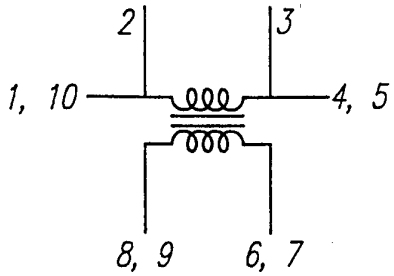


FIG. 14

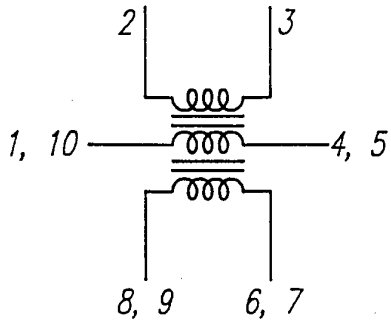


FIG. 15

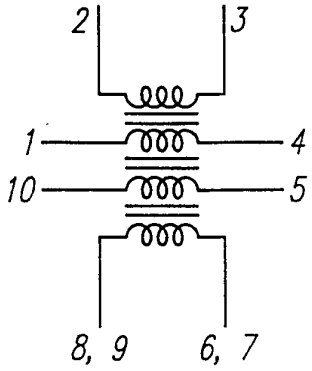


FIG. 16

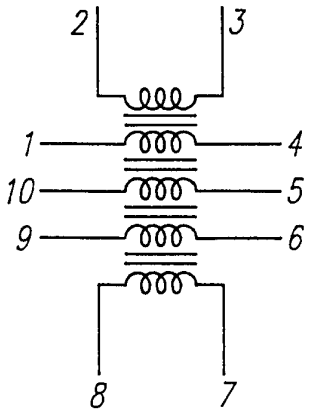


FIG. 17

FIG. 18(A)

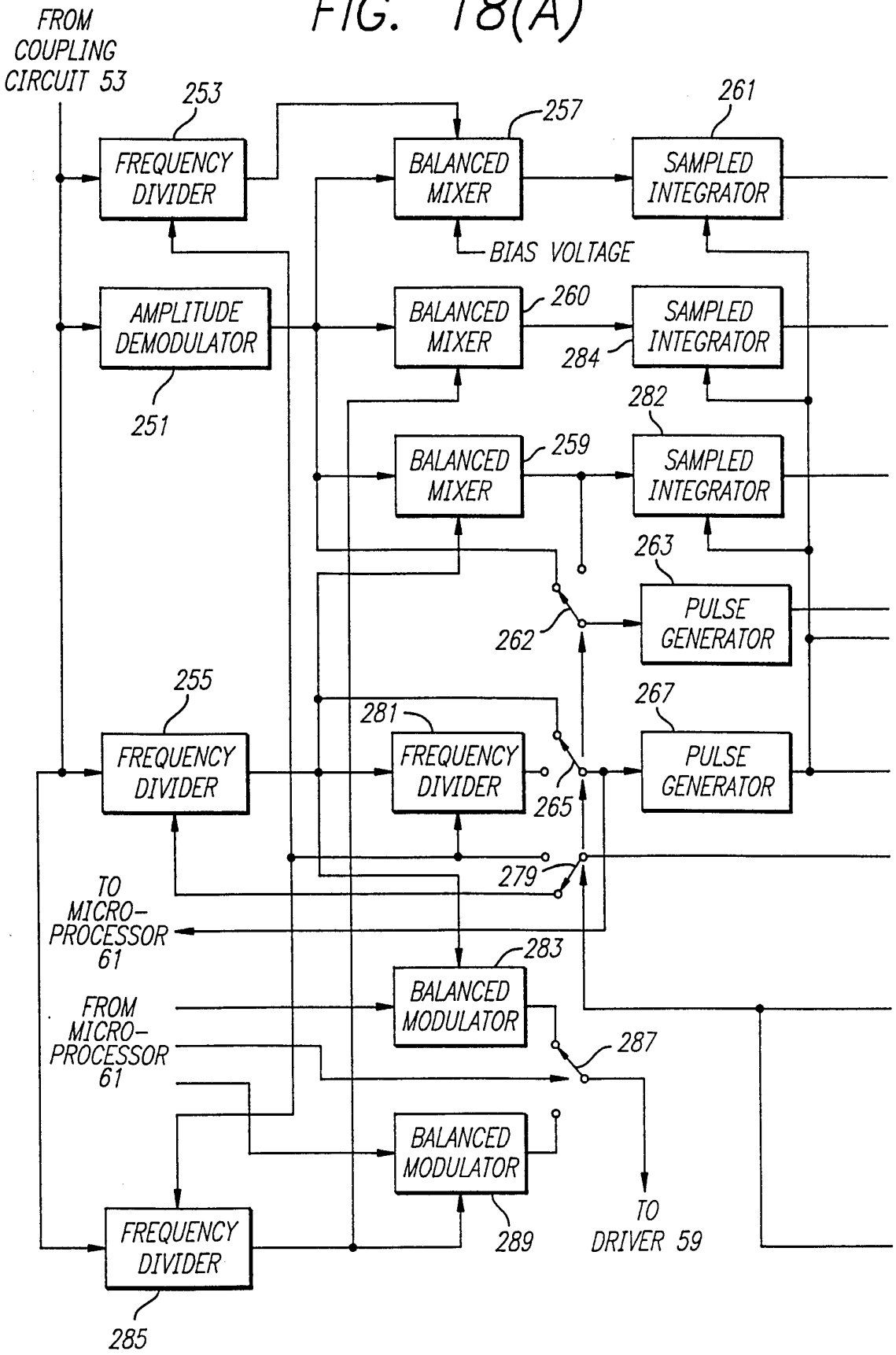

FROM COUPLING CIRCUIT 53
253
FREQUENCY DIVIDER
257
BALANCED MIXER
261
SAMPLED INTEGRATOR
BIAS VOLTAGE
AMPLITUDE DEMODULATOR
251
BALANCED MIXER
260
SAMPLED INTEGRATOR
284
282
BALANCED MIXER
259
SAMPLED INTEGRATOR
263
262
PULSE GENERATOR
255
FREQUENCY DIVIDER
281
FREQUENCY DIVIDER
265
267
PULSE GENERATOR
279
TO MICRO-PROCESSOR 61
283
BALANCED MODULATOR
FROM MICRO-PROCESSOR 61
287
BALANCED MODULATOR
FREQUENCY DIVIDER
285
289
TO DRIVER 59

FIG. 18(B)

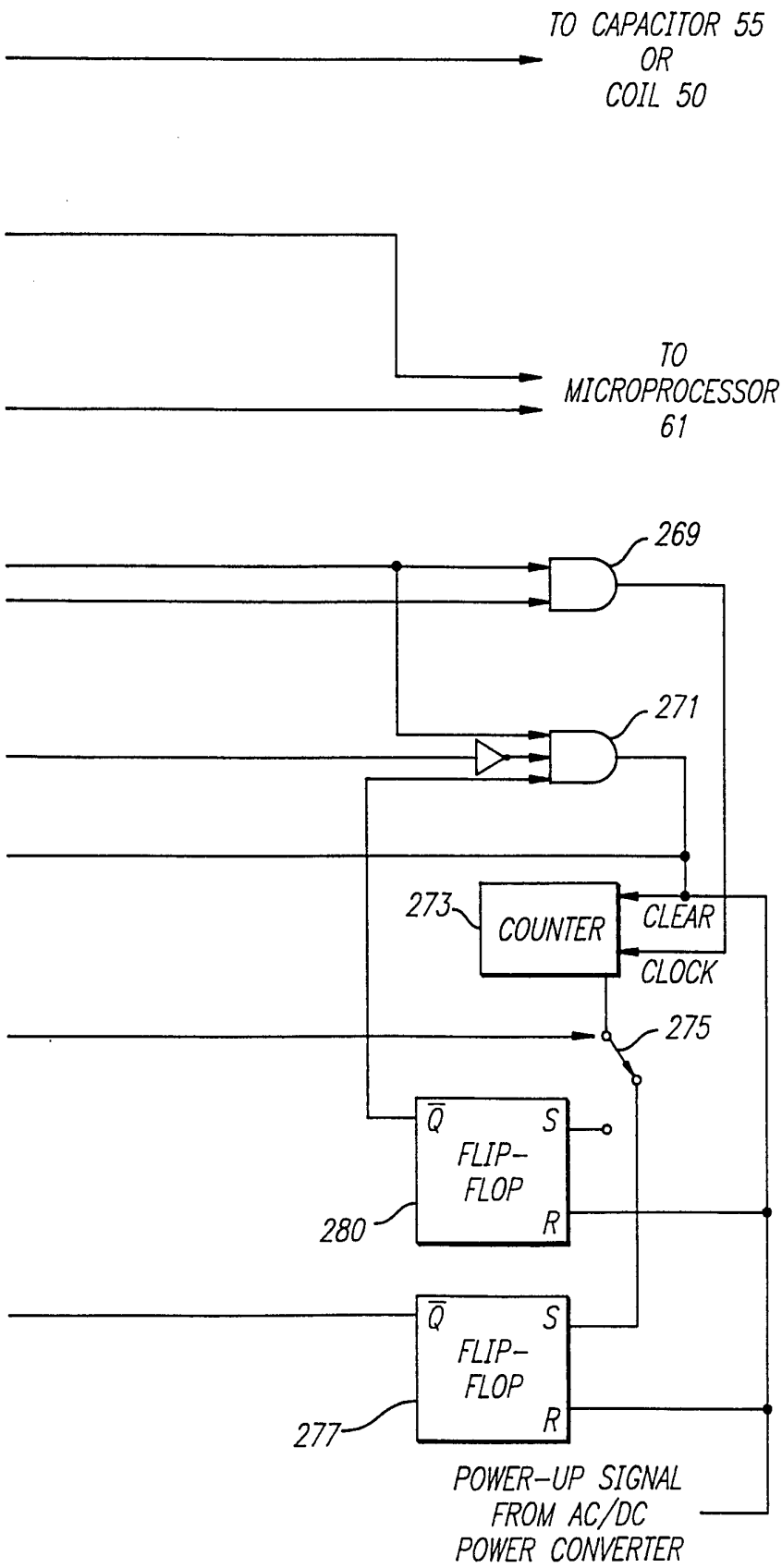

TO CAPACITOR 55
OR
COIL 50
TO
MICROPROCESSOR
61
269
271
273
COUNTER
CLEAR
CLOCK
275
Q
S
FLIP-
FLOP
R
280
Q
S
FLIP-
FLOP
R
277
POWER-UP SIGNAL
FROM AC/DC
POWER CONVERTER

FIG. 19

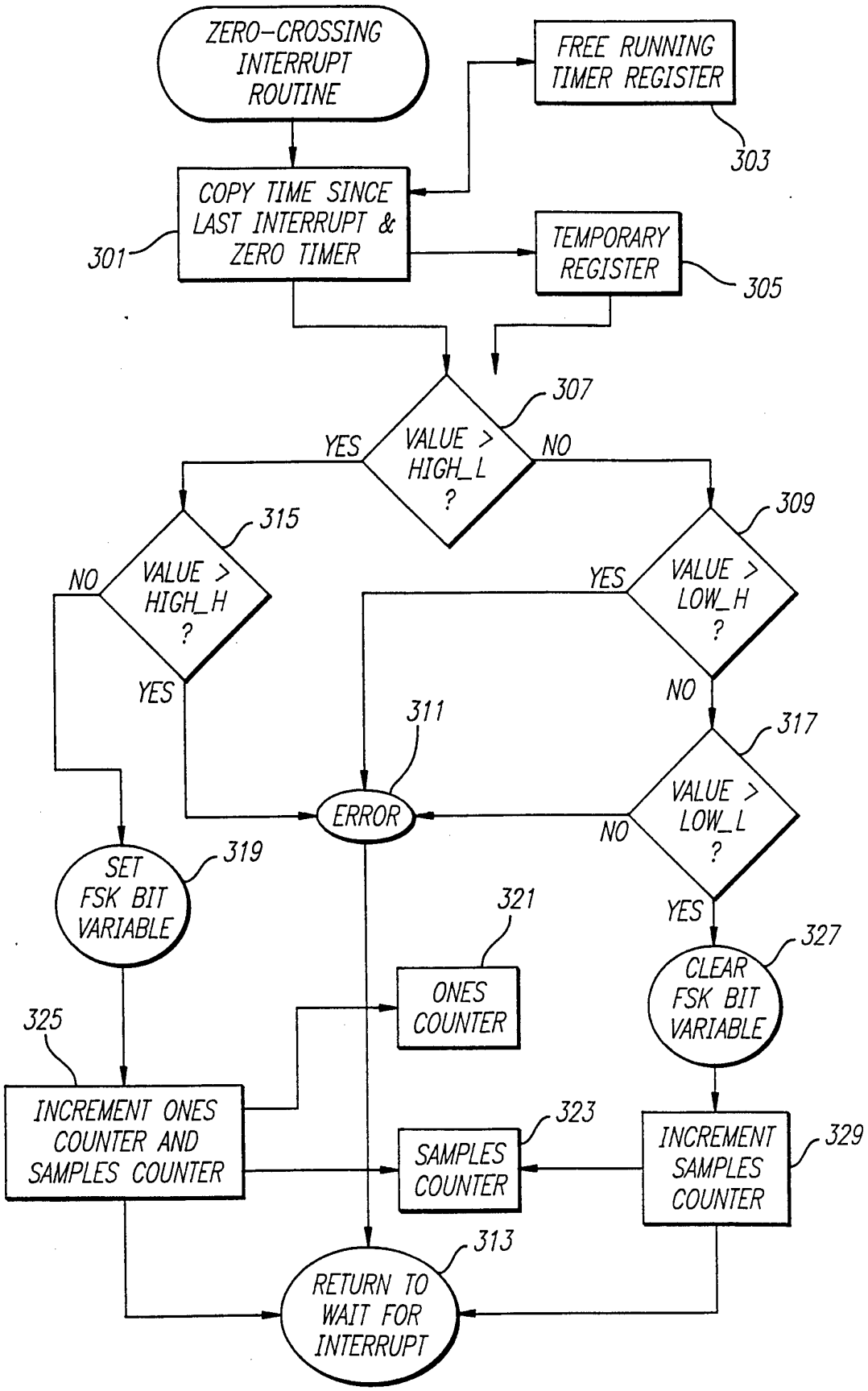
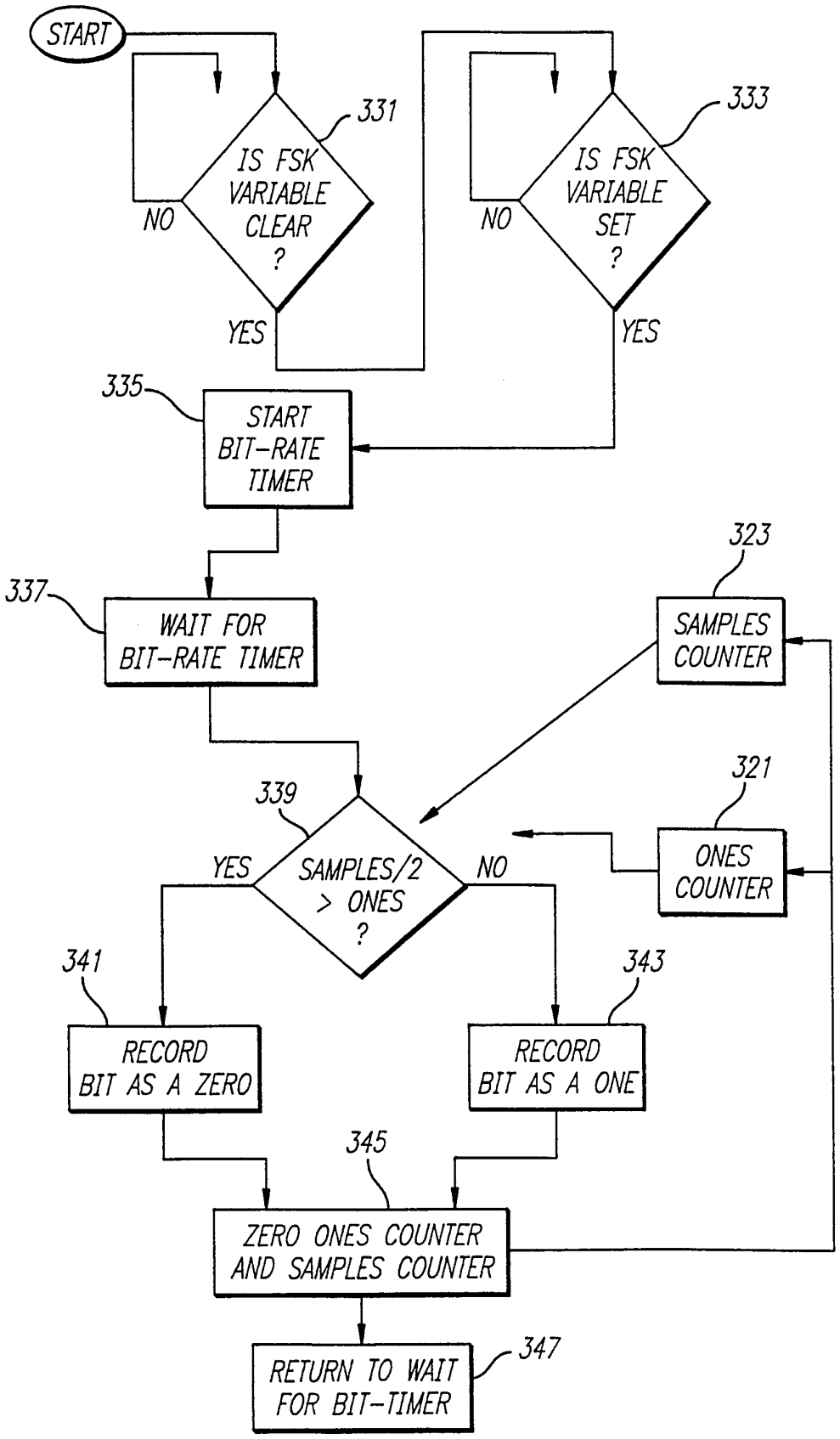

ZERO-CROSSING INTERRUPT ROUTINE
FREE RUNNING TIMER REGISTER
303
COPY TIME SINCE LAST INTERRUPT & ZERO TIMER
301
TEMPORARY REGISTER
305
VALUE > HIGH_L ?
307
YES
NO
VALUE > HIGH_H ?
315
NO
YES
VALUE > LOW_H ?
309
YES
NO
311
ERROR
VALUE > LOW_L ?
317
NO
YES
SET FSK BIT VARIABLE
319
ONES COUNTER
321
CLEAR FSK BIT VARIABLE
327
325
INCREMENT ONES COUNTER AND SAMPLES COUNTER
SAMPLES COUNTER
323
INCREMENT SAMPLES COUNTER
329
RETURN TO WAIT FOR INTERRUPT
313

FIG. 20


START
331
IS FSK VARIABLE CLEAR ?
NO
YES
333
IS FSK VARIABLE SET ?
NO
YES
335
START BIT-RATE TIMER
337
WAIT FOR BIT-RATE TIMER
323
SAMPLES COUNTER
321
ONES COUNTER
339
SAMPLES/2 > ONES ?
YES
NO
341
RECORD BIT AS A ZERO
343
RECORD BIT AS A ONE
345
ZERO ONES COUNTER AND SAMPLES COUNTER
347
RETURN TO WAIT FOR BIT-TIMER

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/07735

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04L 7/027
US CL : 340/572, 825.54, 825.31, 825.71-825.76; 455/41
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 340/572, 825.54, 825.31, 825.71-825.76; 455/41

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,235,326 (BEIGEL ET AL) 10 August 1993 See entire document.	1 ; 2 ; 5 - 9;11;13;16;18/ 1,2;19/1,2,8 ,9,13;20
A	US, A, 5,153,583 (MURDOCH) 06 October 1992	1 ; 2 ; 5 - 9;11;13;16;18/ 1,2;19/1,2,8, 9;13;20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 28 AUGUST 1995	Date of mailing of the international search report 22SEP1995
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer WILLIAM H. WILSON, JR. Telephone No. (703) 308-5459

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/07735

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1;2;5-9;11;13;16;18/1,2;19/1,2,8,9,13 and 20

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/07735

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1; 2; 9; 13; 18/1,2; 19/1,2,9,13 drawn to a radio frequency reader for use in obtaining a signal from a remote tag.

Group II, claim 3, drawn to a reader for use with a tag that shifts frequency to transmit "0" and "1" bits.

Group III, claims 4,12, drawn to a plurality of messages comprising a preamble consisting of a sync sequence of S bits, a tag data group consisting of T bits, and an error-detecting group consisting of E bits.

Group IV, claims 5-8; 11; 16; 19/8, drawn to a tag for use with a reader.

Group V, claims 10, 14, 15, 17 drawn to a method for interrogating a tag.

Claim 20 is associated with any of claims 1-8 with the elected group.

The inventions listed as Groups I, II, III, IV, and V do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Group I, claims 1; 2; 9; 13; 18/1,2; 19/1,2,9,13 specify the technical embodiment of a reader to read signals transmitted from a remote tag wherein resonant tuning is automatically maintained.

Group II, claim 3 specifies the technical embodiment of signalling between a reader and a tag wherein the signalling shifts in frequency to transmit "0" and "1" bits.

Group III, claims 4 and 12 specify the technical embodiment of a plurality of messages transmitted between a reader and a tag wherein the message preamble consists of a sync sequence of S bits, a tag data group consisting of T bits, and an error-detecting group consisting of E bits.

Group IV, claims 5-8; 11; 16; 19/8 specify the technical embodiment of a remote tag to transmit signals to be read by a reading device.

Group V, claims 10, 14, 15, 17 specify a method for interrogating a remote tag by a reading device.

As applicant did not pay any fees, Group I is searched; Group Iv is searched as not requiring additional effort justifying additional fees.