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(54) Abstract Title: Gate in panel (GIP) liquid crystal display device.

(57) A liquid crystal display device includes first and second substrates, 102, 104, having a display area, AA, and a non-display area, NA, and a liquid crystal layer, 160, a seal pattern, 220, in the NA, a driver in the NA on the first substrate, column spacers, 204, in the AA and a first auxiliary spacer, 202, between the driver and the second substrate. The driver may have a signal line, 125, and the first auxiliary spacer may extend between the signal line and the second substrate (Figure 6). The driver signal line and auxiliary spacer may alternatively be located within the seal pattern (Figure 8), with the seal pattern including conductive ball spacers. A second auxiliary spacer may be included along a periphery of the AA (620, Figure 9) where the first and second auxiliary spacers are a honeycomb-like material.

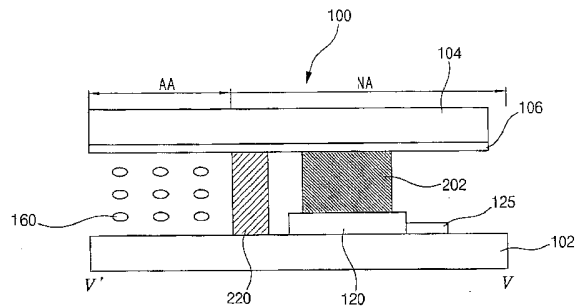
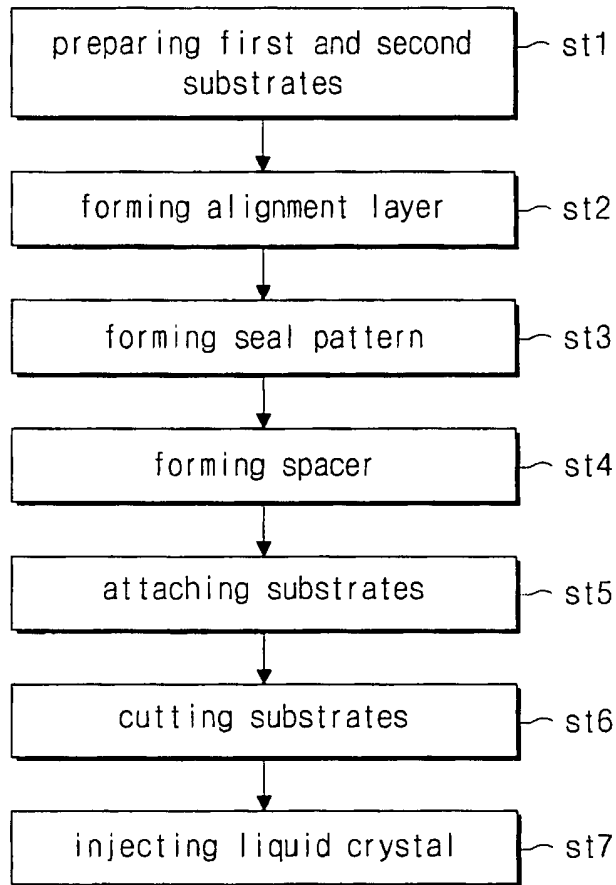
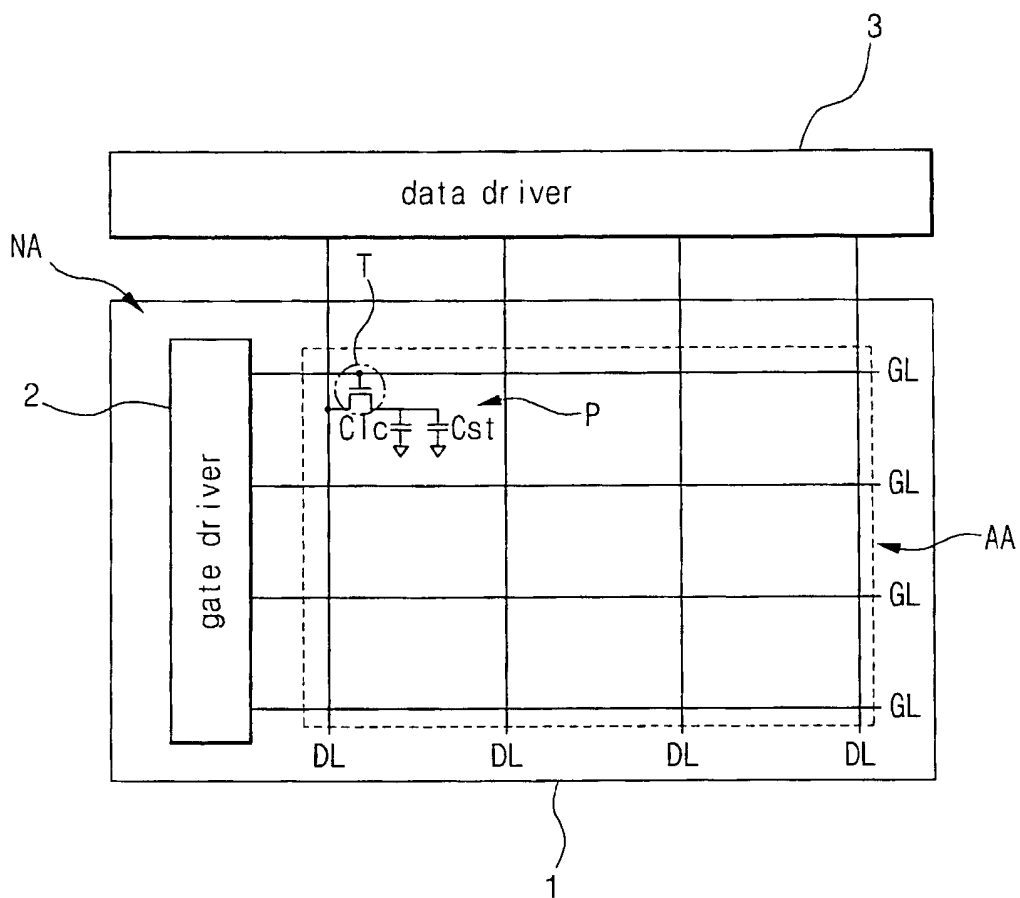


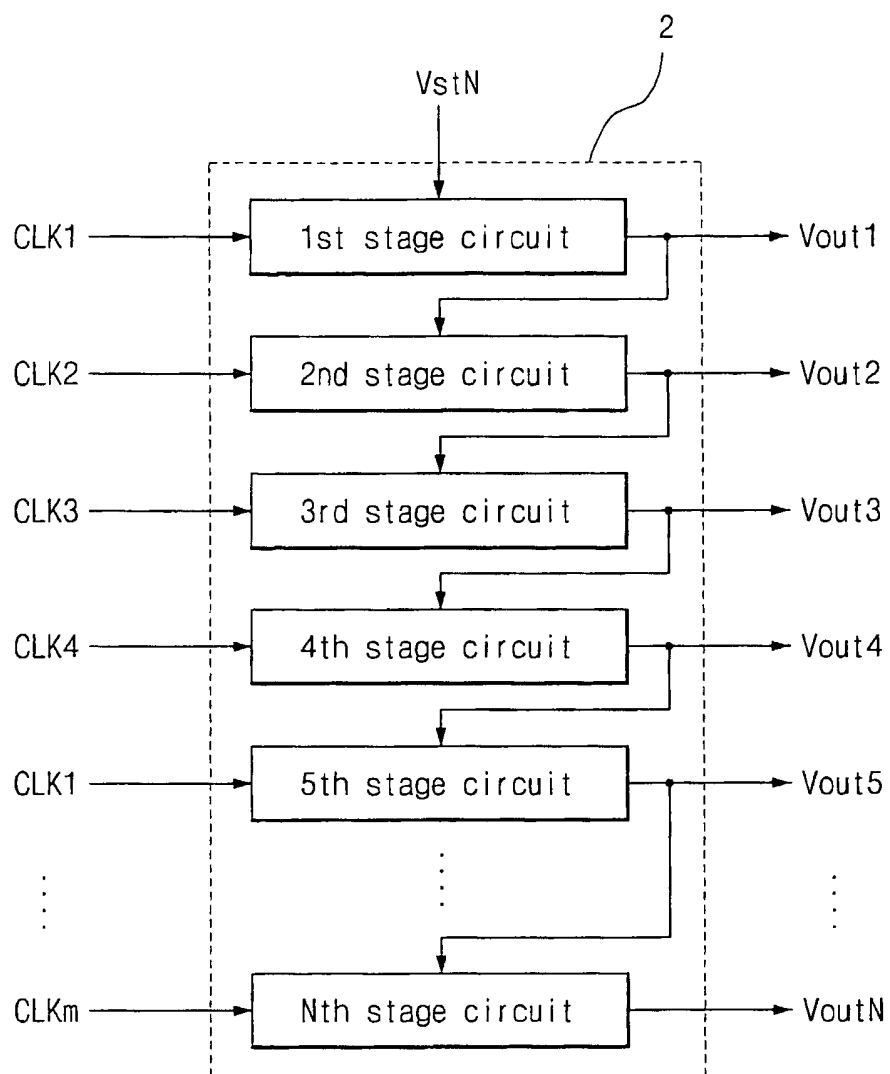
FIG. 5



**FIG. 1**  
Related Art



**FIG. 2**  
Related Art



**FIG. 3**  
Related Art

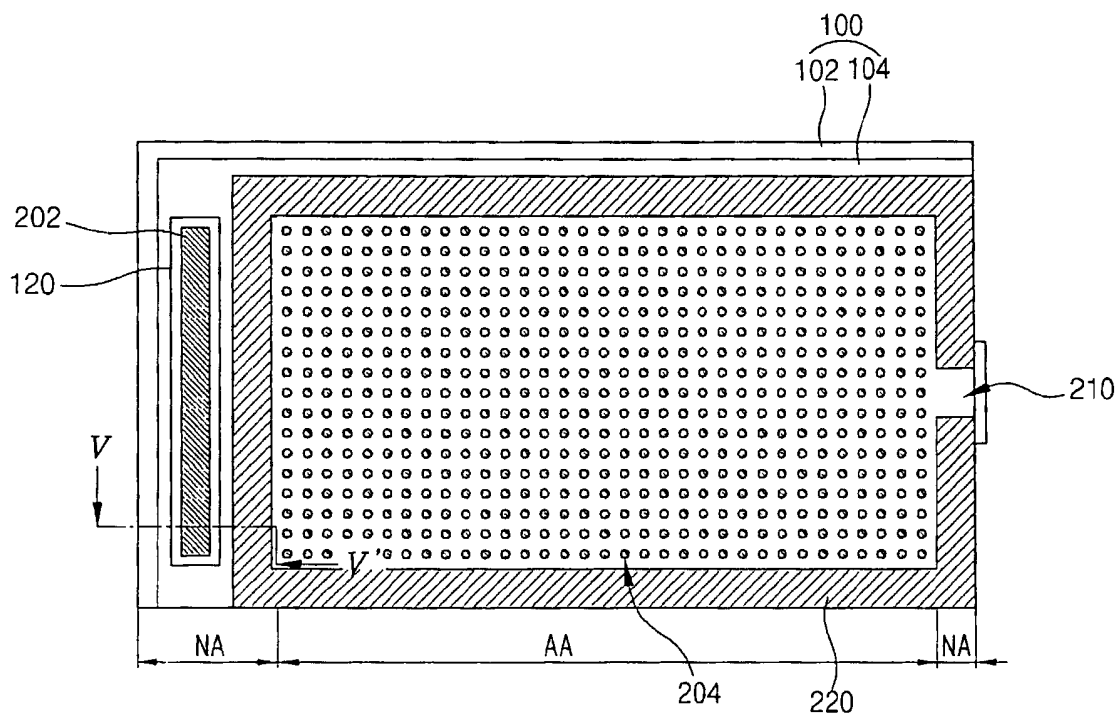


FIG. 4

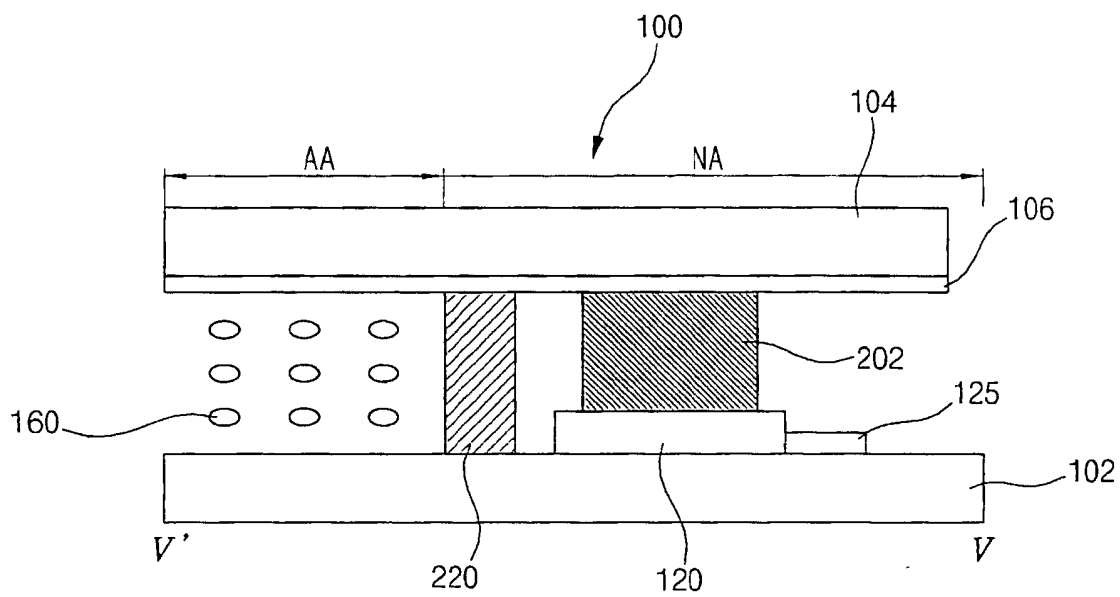


FIG. 5

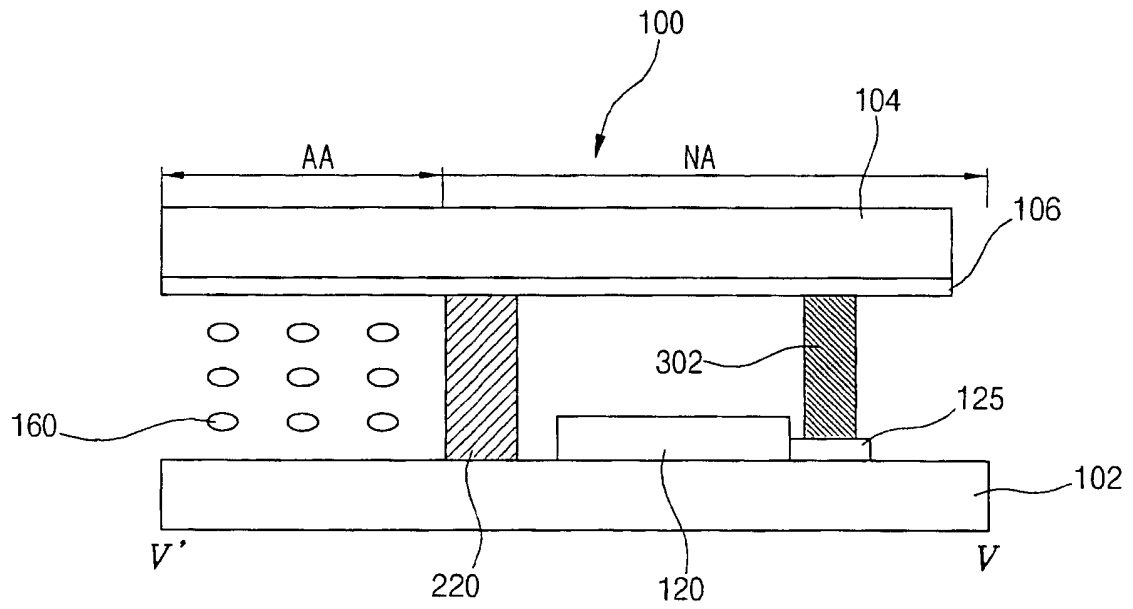


FIG. 6

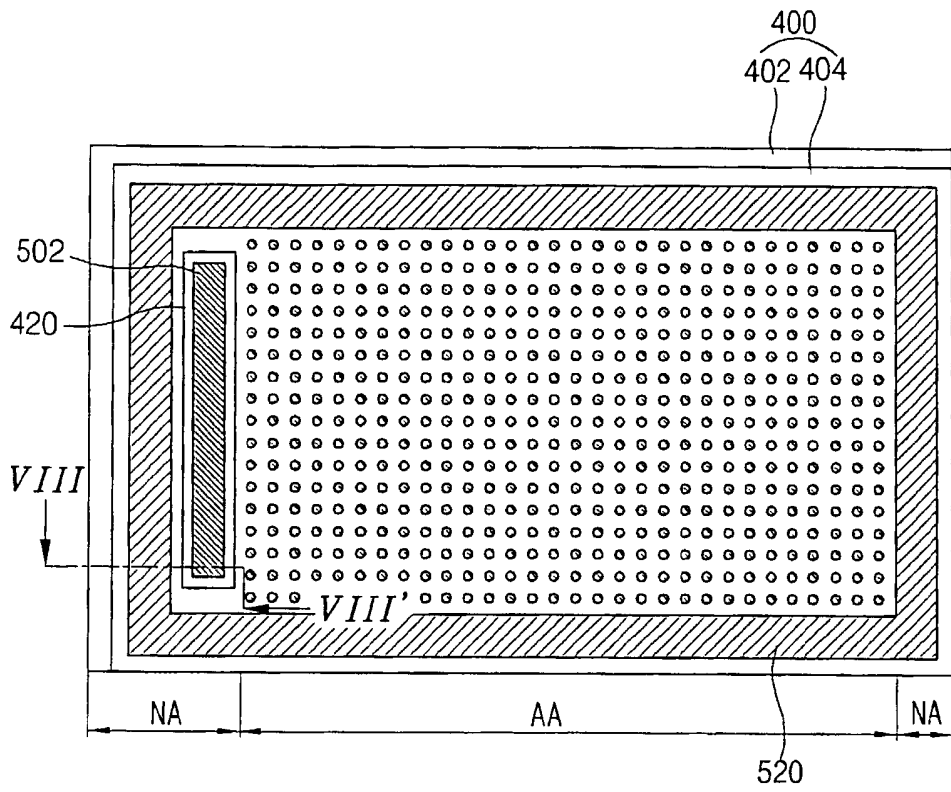


FIG. 7

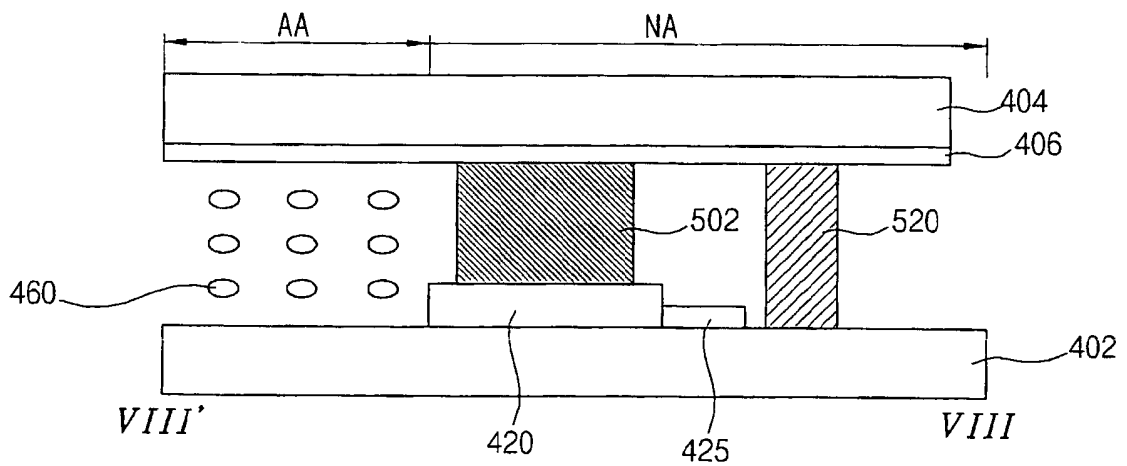


FIG. 8

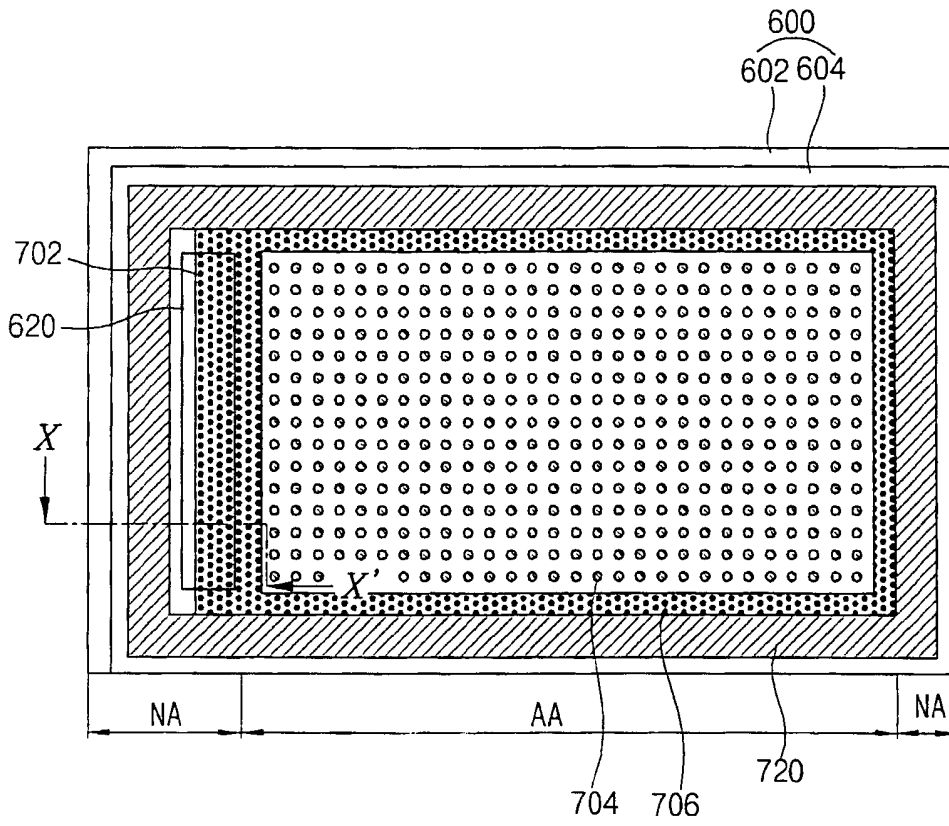


FIG. 9

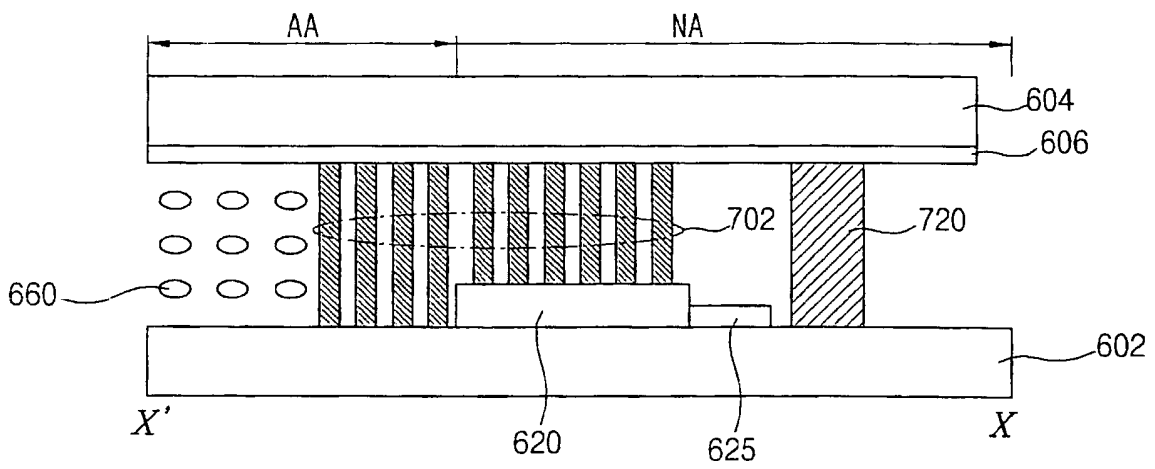


FIG. 10



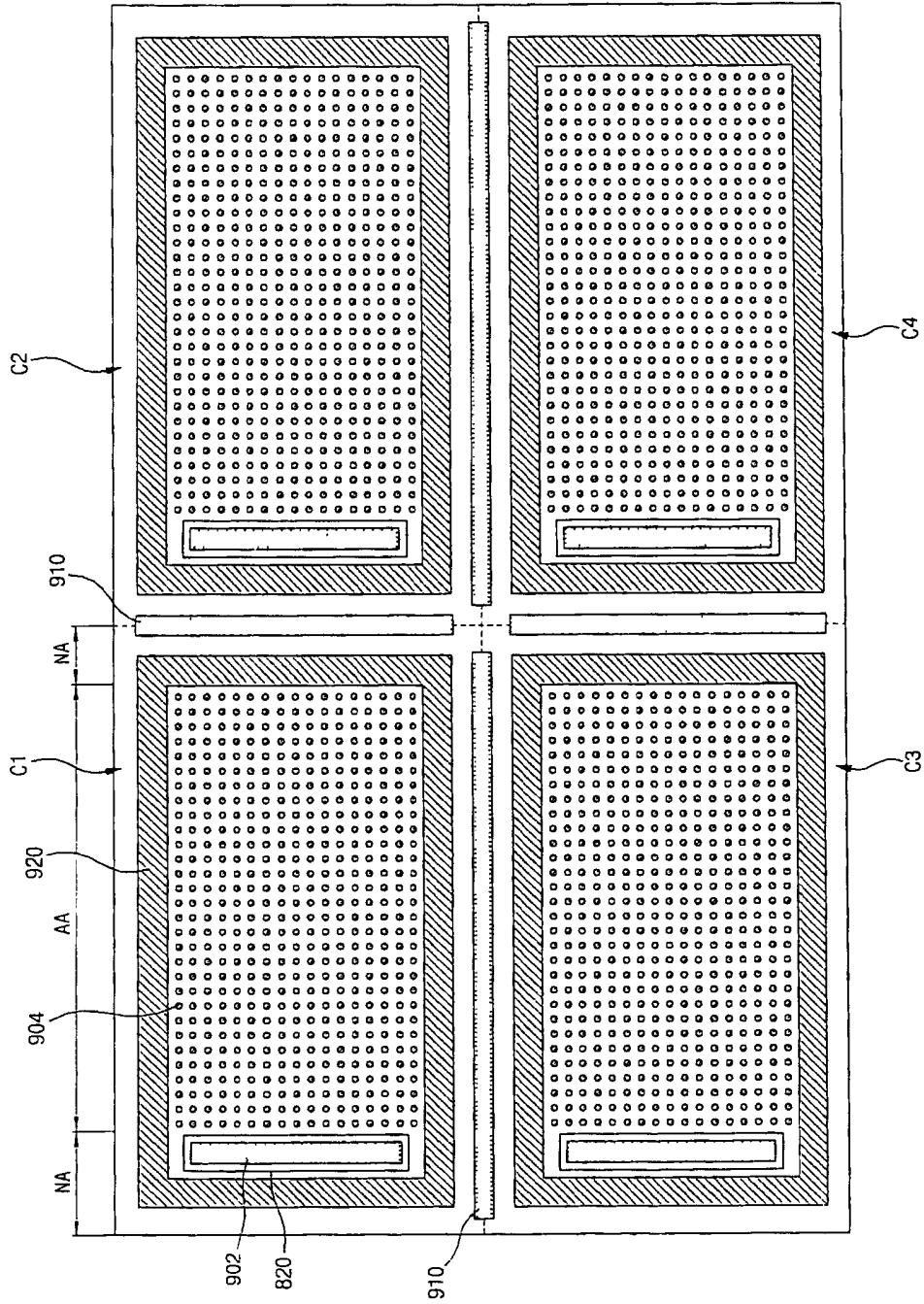


FIG. 11

LIQUID CRYSTAL DISPLAY DEVICE  
AND METHOD OF MANUFACTURING THE SAME

[0001] The invention claims the benefit of Korean Patent Application Nos. 10-2006-0138872 filed in Korea on December 29, 2006 and 10-2007-0039311 on April 23, 2007, which are hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

Field Of The Invention

[0002] Embodiments of the invention relate to a display device, and more particularly, to a liquid crystal display device and a method of manufacturing the same. Although embodiments of the invention are suitable for a wide scope of applications, it is particularly suitable for preventing signal delay within a gate driver and gate lines for a gate-in-panel (GIP) type.

Discussion Of The Related Art

[0003] Generally, liquid crystal display (LCD) devices, as flat panel display devices, change arrangement of liquid crystal molecules, which are initially arranged along a predetermined direction, by applying an electric field to the liquid crystal molecules to control transmittance of light passing through a liquid crystal cell to thereby display images. The liquid crystal cell is fabricated by arranging two substrates such that transparent electrodes of the substrates face each other, interposing a liquid crystal layer between the two substrates, and sealing an injection hole. Polarizing films are attached on the outer surfaces of the substrates. The light transmittance of the liquid crystal cell is controlled by the intensity of a voltage applied to the electrodes such that the liquid crystal cell displays graphic symbols/images by an optical shutter effect.

[0004] FIG. 1 is a flow chart illustrating a fabrication process of the related art liquid crystal cell for an LCD device. As shown in step st1 of FIG. 1, a first substrate and a second substrate are prepared. Thin film transistors and pixel electrodes connected to the thin film transistors are formed on the first substrate. A color filter layer and a common electrode covering the color filter layer are formed on the second substrate.

[0005] As shown in step st2 of FIG. 1, first and second alignment layers are formed on the first and second substrates, respectively. The first alignment layer covers the pixel electrodes, and the second alignment layer covers the common electrode. This step includes forming a polymeric thin film by coating the substrates with polymer and rubbing the polymeric thin film. The polymeric thin film should be deposited substantially over the entire surface of the first and second substrates with a uniform thickness and should be uniformly rubbed.

[0006] The rubbing method includes rubbing the alignment layer along the specific direction by a rubbing cloth, and has advantages such as easy orientation treatment, suitability to mass production, high stability of the orientation and easy controllability of a pre-tilt angle. Other methods, including photo-alignment, are also possible. An organic material of polyimide series is mainly used as the alignment layer, and a rubbing method is mainly used as the aligning method of the alignment layer.

[0007] As shown in step st3 of FIG. 1, a seal pattern, which forms a gap for liquid crystal material injection and prevents leakage of the liquid crystal material, is formed on one substrate. The seal patterning process involves forming a desired pattern by application of a thermosetting resin. A screen print method using a screen mask and a seal dispenser method using a dispenser are used for the seal patterning process. For the simplicity of fabrication, the screen print method has mainly been used. However, since the screen mask is not suitable for a wide substrate and a

contamination by contact between the mask and the alignment layer often occurs, use of the seal dispenser method has gradually increased.

[0008] As shown in step st4 of FIG. 1, a spacer having a specific size to maintain a precise and uniform gap between the first and second substrates is deposited by spraying the spacer onto one of the first and second substrates. The spacer spray method can be divided into two different types: a wet spray method that involves spraying a mixture of alcohol and spacer material and a dry spray method that involves a spraying spacer material alone. The seal pattern and the spacer may be formed on different substrates. For example, the seal pattern may be formed on the second substrate, which has a relatively flat surface, and the spacer may be formed on the first substrate, which functions as a lower substrate.

[0009] As shown in step st5 of FIG. 1, the array and color filter substrates are arranged and attached by pressure-resistant hardening of the seal pattern. The aligning accuracy of the substrates is decided by a margin. If the substrates are attached beyond the margin, there is leakage of light, to thereby decrease the quality of images of the liquid crystal cell. Therefore, the aligning accuracy of several micrometers is required.

[0010] As shown in step st6 of FIG. 1, the attached liquid crystal substrate is divided into unit cells. A cell cutting process includes a scribe process that forms cutting lines on a surface of the substrate using a diamond pen or a cutting wheel of tungsten carbide, a hardness of which is higher than a hardness of the glass substrate, and a break process that divides the unit cells by force.

[0011] As shown in step st7 of FIG. 1, a liquid crystal material is injected into the unit cells. The unit cell has an area of several  $\text{cm}^2$  and a gap of several micrometers. To effectively inject the liquid crystal material into the unit cell, a vacuum injection method using pressure difference

between the inside and outside of the unit cells is commonly used as an effective injection method. Since fine air bubbles included in the liquid crystal material can deteriorate the display property of the unit cells, a bubble-eliminating process, in which the cells are kept in a vacuum state for a long period of time, is required.

[0012] After finishing the liquid crystal material injection, an injection hole is sealed to prevent leakage of the liquid crystal material. Generally, a ultra violet (UV) curable resin is deposited onto the injection hole by use of a dispenser and then ultra violet light is irradiated onto the resin, thereby hardening the resin and sealing the injection hole. The unit cell is then tested. After that, polarization films are attached on outer surfaces of the unit cell, and a driving circuit is connected to the unit cell using an attachment process.

[0013] Recently, a gate-in-panel (GIP) type LCD device has been suggested and developed. The GIP type LCD device, in which a gate driver is formed on a substrate of a liquid crystal panel, decreases manufacturing costs and minimizes power consumption.

[0014] FIG. 2 is a schematic view of a GIP type LCD device according to the related art. As shown in FIG. 2, a liquid crystal panel 1 includes a display area AA for displaying images and a non-display area NA surrounding the display area AA. In the display area AA, gate lines GL and data lines DL cross each other to define pixels P, and each pixel P includes a thin film transistor T, as a switching element, and a pixel electrode (not shown) connected to the thin film transistor T. The thin film transistor T switches on/off according to signals of the gate line GL and electrically connects the pixel electrode and the data line DL. The pixel electrode forms a liquid crystal capacitor Clc with a common electrode. The liquid crystal capacitor Clc is connected to a storage capacitor Cst.

[0015] A gate driver 2 is formed at a side of the non-display area NA, and a data driver 3 is attached at another side of the non-display area NA. The gate driver 2 sequentially provides gate-driving signals to the gate lines GL, so that the pixels P connected to one of the gate lines GL are selected. Whenever the gate lines GL are sequentially selected, the data driver 3 provides RGB data signals to the data lines DL. The data signals are provided to the pixels P, and an electric field is induced between the pixel electrode and the common electrode. The electric field varies according to the data signals. The transmittance of light passing through a liquid crystal layer is controlled by changing the electric field, and thus images are displayed.

[0016] In the GIP type LCD device, the gate driver 2 is formed on a substrate of the liquid crystal panel 1 through the same processes as the thin film transistor T of the pixel P. That is, at the step st1 of FIG. 1, elements of the gate driver 2 are formed when the thin film transistors and the pixel electrodes are formed on the first substrate. The data driver 3 may or may not be formed on the substrate of the liquid crystal panel 1.

[0017] FIG. 3 is a block diagram schematically illustrating a gate drive of a GIP type LCD device according to the related art. In FIG. 3, the gate driver 2 includes a shift register composed of N (N is a natural number) stage circuits. The stage circuits are driven by 4 clock signals.

[0018] A first stage circuit receives a first clock signal CLK1 and a starting signal VstN and outputs a first gate-driving signal Vout1 to a first gate line (not shown). A second stage circuit receives a second clock signal CLK2 and the first gate-driving signal Vout1, as a starting signal, and outputs a second gate-driving signal Vout2. A third stage circuit receives a third clock signal CLK3 and the second gate-driving signal Vout2, as a starting signal, and outputs a third gate-driving signal Vout3. A fourth stage circuit receives a fourth clock signal CLK4 and the third gate-driving signal Vout3, as a starting signal, and outputs a fourth gate-driving signal

Vout4. A fifth stage circuit receives the first clock signal CLK1 and the fourth gate-driving signal Vout4, as a starting signal, and outputs a fifth gate-driving signal Vout5. At last, an Nth stage circuit receives a clock signal CLKm (m is one of 1 to 4) and an (N-1)th gate-driving signal (not shown), as a starting signal, and outputs an Nth gate-driving signal VoutN.

**[0019]** Each stage circuit of the gate driver 2 for the GIP type LCD device includes thin film transistors. Channel widths of the thin film transistors of the stage circuits are several hundred times larger than the thin film transistors formed in the display area AA of the liquid crystal panel 1 of FIG. 2. A parasitic capacitance may be induced between the thin film transistor of the gate driver 2 and a second substrate in the non-display area NA. The parasitic capacitance is larger than that in the display area AA. The parasitic capacitance lowers characteristics of the thin film transistor and affects the gate-driving signals Vout1 to VoutN to thereby cause incorrect operation. In addition, the fabrication process for the liquid crystal cell of FIG. 1 is carried out as the gate driver 2 is formed in the non-display area NA, and thus particles can go into the gate driver 2. Because particles may go into one of the thin film transistors of the gate driver 2, the thin film transistor may be shorted with others, and one stage circuit, which is connected to the shorted thin film transistor, may be totally turned OFF.

#### SUMMARY OF THE INVENTION

**[0020]** Accordingly, embodiments of the invention are directed to a liquid crystal display device and a method of manufacturing the same that seek to substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

**[0021]** Embodiments of the invention seek to provide a liquid crystal display device and a method of manufacturing the same that prevent wrong working of a gate driver due to a parasitic

capacitance between thin film transistors of the gate driver and a common electrode in a gate-in-panel (GIP) type.

[0022] Embodiments of the invention also seek to provide a liquid crystal display device and a method of manufacturing the same that prevent electrical short due to particles going to the gate driver.

[0023] Embodiments of the invention also seek to provide a liquid crystal display device and a method of manufacturing the same that solve a problem of lowering output of gate-driving signals due to line delay of the gate driver and a signal line connected to the gate driver.

[0024] Additional features and advantages of embodiments of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of embodiments of the invention. The objectives and other advantages of the embodiments of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0025] To achieve these and other advantages and in accordance with the purpose of embodiments of the invention, as embodied and broadly described, a liquid crystal display device includes first and second substrates spaced apart from each other, on which a display area and a non-display area are defined, a liquid crystal layer interposed between the first and second substrates, a seal pattern in the non-display area between the first and second substrates, a driver in the non-display area on the first substrate, column spacers in the display area between the first and second substrates, and a first auxiliary spacer between the driver and the second substrate.

[0026] In another aspect, a liquid crystal display device includes first and second substrates spaced apart from each other, on which a display area and a non-display area are defined, a liquid crystal layer interposed between the first and second substrates, a seal pattern in the non-



display area between the first and second substrates, a driver with a signal line in the non-display area on the first substrate, column spacers in the display area between the first and second substrates, and an auxiliary spacer between the signal line and the second substrate in the non-display area.

[0027] In another aspect, a method of manufacturing a liquid crystal display device having first and second spaced apart substrates and each having a display area and a non-display area includes forming a seal pattern in the non-display area between the first and second substrates, forming a driver in the non-display area on the first substrate, forming column spacers in the display area between the first and second substrates, forming an auxiliary spacer on a signal line for the driver in the non-display area, and forming a liquid crystal layer interposed between the first and second substrates.

[0028] In yet another aspect, a method of manufacturing a liquid crystal display device includes preparing first and second substrates, on which a display area and a non-display area are defined, forming a driver in the non-display area on the first substrate, forming column spacers in the display area on one of the first and second substrates, forming a first auxiliary spacer in the non-display area on one of the first and second substrates, the first auxiliary spacer corresponding to the driver, forming a seal pattern in the non-display area on one of the first and second substrates, and attaching the first and second substrates.

[0029] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of embodiments of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings, which are included to provide a further understanding of embodiments of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of embodiments of the invention. In the drawings:

[0031] FIG. 1 is a flow chart illustrating a fabrication process of a related art liquid crystal cell for an LCD device;

[0032] FIG. 2 is a schematic view of a GIP type LCD device according to the related art;

[0033] FIG. 3 is a block diagram schematically illustrating a gate drive of a GIP type LCD device according to the related art;

[0034] FIG. 4 is a schematic plan view illustrating a liquid crystal panel for an LCD device according to a first embodiment of the invention;

[0035] FIG. 5 is a cross-sectional view along the line V-V' of FIG. 4;

[0036] FIG. 6 is a cross-sectional view of a liquid crystal panel according to another example of the first embodiment;

[0037] FIG. 7 is a plan view of a liquid crystal panel for an LCD device according to a second embodiment;

[0038] FIG. 8 is a cross-sectional view along the line VIII-VIII' of FIG. 7;

[0039] FIG. 9 is a plan view of a liquid crystal panel for an LCD device according to a third embodiment of the invention;

[0040] FIG. 10 is a cross-sectional view along the line X-X' of FIG. 9; and

[0041] FIG. 11 is a schematic plan view of a liquid crystal panel for an LCD device according to a fourth embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

[0043] FIG. 4 is a schematic plan view illustrating a liquid crystal panel for a liquid crystal display (LCD) device according to a first embodiment of the invention. As shown in FIG. 4, a liquid crystal panel 100 includes a first substrate 102 and a second substrate 104. A display area AA for displaying images and a non-display area NA surrounding the display area AA are defined in the first and second substrates 102 and 104. Column spacers 204 are disposed in the display area AA and are spaced apart from each other with a certain distance. The column spacers 204 keep a cell gap uniform. The column spacers 204 are formed through a photolithographic process patterning a thin film using a photosensitive material, such as photoresist. The column spacers 204 may be formed on the second substrate 104. Acrylic organic materials are used as a material for the column spacers 204. The column spacers 204 may be formed by directly exposing and developing a photosensitive organic material without using photoresist. A seal pattern 220 is formed in the non-display area NA adjacent to the display area AA between the first and second substrates 102 and 104. The seal pattern 220 has a liquid crystal injection hole 210 at a side. A liquid crystal layer (not shown) is interposed inside the seal pattern 220 between the first and second substrates 102 and 104.

[0044] A gate driver 120 is formed on the first substrate 102 in the non-display area NA. An auxiliary spacer 202 is disposed on the gate driver 120 and is formed of an organic material. The auxiliary spacer 202 is on top of the gate driver 120. The auxiliary spacer 202 contacts the second substrate 104. The auxiliary spacer 202 and the column spacers 204 can be formed at the

same time on either the first substrate 102 or the second substrate 104. Thus, the auxiliary spacer 202 can be formed of the same material and through the same process as the column spacers 204. In this case, an additional process to form the auxiliary spacer 202 is not required. Since the auxiliary spacer 202 is on top of the gate driver 120, the particles are prevented from going into the gate driver 120 after attaching the first and second substrates 102 and 104, as described in step st5 of FIG. 1.

[0045] FIG. 5 is a cross-sectional view along the line V-V' of FIG. 4. As shown in FIG. 5, first and second substrates 102 and 104 are spaced apart from each other. A seal pattern 220 is formed between the first and second substrates 102 and 104. An area inside the seal pattern 220 is defined as a display area AA, and an area outside the seal pattern 220 including a region for the seal pattern 220 is defined as a non-display area NA. A liquid crystal layer 160 is interposed in the display area AA between the first and second substrates 102 and 104.

[0046] A gate driver 120 and a signal line 125 for the gate driver 120 are formed on an inner surface of the first substrate 102 in the non-display area NA. A common electrode 106 is formed on an inner surface of the second substrate 104 in the display area AA and in the non-display area NA. An auxiliary spacer 202 is disposed between the second substrate 104 and the gate driver 120. The auxiliary spacer 202 is on the common electrode 106 in the non-display area NA of the second substrate. Accordingly, particles do not enter into the gate driver 2 after attaching the first and second substrates 102 and 104.

[0047] Another example of the first embodiment will be described with reference to the accompanying drawings. As the size of the liquid crystal panel increases, the signal line for the gate driver gets longer, and output of the gate-driving signals may be lowered due to signal delay. Another example of the first embodiment may solve this problem.

[0048] FIG. 6 is a cross-sectional view of a liquid crystal panel according to another example of the first embodiment. For the convenience of explanation, the same parts as the example of FIG. 5 may have the same references. As shown in FIG. 6, first and second substrates 102 and 104 are spaced apart from each other. A seal pattern 220 is formed between the first and second substrates 102 and 104. An area inside the seal pattern 220 is defined as a display area AA, and an area outside the seal pattern 220 including a region for the seal pattern 220 is defined as a non-display area NA.

[0049] A liquid crystal layer 160 is interposed in the display area AA between the first and second substrates 102 and 104. A gate driver 120 and a signal line 125 for the gate driver 120 are formed on an inner surface of the first substrate 102 in the non-display area NA. A common electrode 106 is formed on an inner surface of the second substrate 104 in the display area AA and the non-display area NA.

[0050] In the example of FIG. 6, an auxiliary spacer 302 is disposed in the non-display area NA between the common electrode 106 and the signal line 125 for the gate driver 120. In the alternative, the auxiliary spacer 202 of FIG. 5 or 302 of FIG. 6 may be formed on both the gate driver 120 and the signal line 126, respectively. In this case, the step difference between the gate driver 120 and the signal line 125 may be considered.

[0051] Meanwhile, an Ag-dot, generally, is formed between the first and second substrates 102 and 104 to connect the common electrode 106 on the second substrate 104 to a driver (not shown) packaged on the first substrate 102. However, there are problems in that a process for forming the Ag-dot is very complicated and requires a lot of time. Accordingly, a method of connecting the common electrode to the driver by using a seal pattern, which includes

conductive ball spacers therein, is used. However, the first embodiment can not be used with such a conductive seal pattern since the conductive seal pattern will short out the signal lines.

**[0052]** FIG. 7 and FIG. 8 illustrate a liquid crystal panel using the seal pattern according to a second embodiment of the invention. FIG. 7 is a plan view of a liquid crystal panel for an LCD device according to the second embodiment. FIG. 8 is a cross-sectional view along the line VIII-VIII' of FIG. 7.

**[0053]** As shown in FIG. 7 and FIG. 8, the liquid crystal panel 400 of the second embodiment includes first and second substrates 402 and 404 that overlap each other. A display area AA and a non-display area NA are defined on the first and second substrates 402 and 404. The display area AA displays images, and the non-display area NA surrounds the display area AA. Although not shown in the figures, gate lines and data lines cross one another to define pixel regions on an inner surface of the first substrate 402. A thin film transistor is disposed at each crossing portion of the gate and data lines. A pixel electrode is disposed in each pixel region and is connected to the thin film transistor. A storage capacitor may be formed in the pixel region and may be connected to the pixel electrode.

**[0054]** A black matrix (not shown), a color filter layer (not shown) and a common electrode 406 are formed on an inner surface of the second substrate 404 in the display area AA. The common electrode 406 extends into the non-display area NA. The common electrode 406 and the pixel electrode (not shown) constitute a liquid crystal capacitor.

**[0055]** Column spacers 504 are formed in the display area AA between the first and second substrates 402 and 404. The column spacers 504 keep a cell gap, i.e., a distance between the first and second substrates 402 and 404, uniform.

[0056] A seal pattern 520 is formed in the non-display area NA and surrounds the display area AA. The column spacers 504 and the seal pattern 520 may be formed on different substrates. The column spacers 504 may be formed on the inner surface of the second substrate 404, and the seal pattern 520 may be formed on the inner surface of the first substrate 402. Alternatively, the column spacers 504 and the seal pattern 520 may be formed on the same substrate.

[0057] A gate driver 420 and a signal line 425 for the gate driver 420 are formed on the inner surface of the first substrate 402 in the non-display area NA. The gate driver 420 and the signal line 425 are disposed inside of the seal pattern 520.

[0058] A liquid crystal layer 460 is interposed in the display area AA between the first and second substrates 402 and 404. Here, the seal pattern 520 may have a closed structure, which may be used with a liquid crystal dropping method. In the case of manufacturing an LCD device using the liquid crystal dropping method, a seal pattern is formed on a substrate of the liquid crystal panel, and column spacers are formed on another substrate. Then, liquid crystal is dropped on the substrate, including the column spacers. Next, the substrates are attached, and the attached substrates are cut into unit cells. In the liquid crystal dropping method, since the liquid crystal is directly dropped on the substrate, manufacturing time is relatively short. An amount of the liquid crystal dropped on the substrate is substantially accurately controlled, and little liquid crystal is wasted. The liquid crystal may be dropped on the substrate, including the seal pattern, but it is desirable that the liquid crystal is dropped on the substrate excluding the seal pattern to minimize problems due to contact between the seal pattern and the liquid crystal.

[0059] The seal pattern 520 for the liquid crystal dropping method may have a closed structure. As mentioned above, the seal pattern 520 can include conductive ball spacers therein

and be conductive. Therefore, if the gate driver 420 is formed outside the seal pattern 520, the seal pattern 520 contacts the gate driver 420 or gate lines (not shown). The gate lines may be shorted therebetween or the gate lines may be shorted with the common electrode 406. To prevent this problem, in the second embodiment, the gate driver 420 is disposed inside the seal pattern 520.

**[0060]** In the case that the gate driver 420 may be disposed inside the seal pattern 520, the liquid crystal layer 460 may be also disposed on the gate driver 420, to thereby cause a parasitic capacitance between the gate driver 420 and the common electrode 406 with the liquid crystal layer 460 as a dielectric substance.

**[0061]** In the second embodiment of the invention, by disposing an auxiliary spacer 502 on the gate driver 420, the parasitic capacitance is prevented from being caused between the gate driver 420 and the common electrode 406. Here, the auxiliary spacer 502 is formed of an organic material. To decrease the number of processes, the auxiliary spacer 502 may be formed of the same material and through the same process as the column spacers 504. The auxiliary spacer 502 can cover the top of the gate driver 420.

**[0062]** In addition, as stated in the first embodiment, the auxiliary spacer 502 may be disposed on the signal line 425 or may be disposed on both the gate driver 420 and the signal line 425.

**[0063]** Meanwhile, when the liquid crystal may be dropped on the substrate without the seal pattern, there may be a problem that the dropped liquid crystal flows beyond the display area and outward. To solve the problem, another auxiliary spacer of a honeycomb-like structure may be further formed along a periphery of the display area. A liquid crystal panel including the auxiliary spacer of the honeycomb-like structure according to a third embodiment of the



invention is illustrated in FIG. 9 and FIG. 10. FIG. 9 is a plan view of a liquid crystal panel for an LCD device according to the third embodiment of the invention. FIG. 10 is a cross-sectional view along the line X-X' of FIG. 9.

**[0064]** In FIG. 9 and FIG. 10, the liquid crystal panel 600 of the third embodiment includes first and second substrates 602 and 604 that overlap each other. A display area AA and a non-display area NA are defined on the first and second substrates 602 and 604. The display area AA displays images, and the non-display area NA surrounds the display area AA.

**[0065]** Column spacers 704 are formed in the display area AA between the first and second substrates 602 and 604 and correspond to regions except for pixel regions. The column spacers 704 keep a distance between the first and second substrates 602 and 604 uniform.

**[0066]** A seal pattern 720 is formed in the non-display area NA and surrounds the display area AA. The seal pattern 720 may include conductive ball spacers therein. A gate driver 620 and a signal line 625 for the gate driver 620 are formed in the non-display area NA. The gate driver 620 and the signal line 625 are disposed inside the seal pattern 720.

**[0067]** A first auxiliary spacer 702 is disposed on the gate driver 620. A second auxiliary spacer 706 is formed along a periphery of the display area AA between the first and second substrates 602 and 604. A liquid crystal layer 660 is interposed in the display area AA between the first and second substrates 602 and 604.

**[0068]** The first auxiliary spacer 702 may be in the non-display area NA along a side of the display area AA. The second auxiliary spacer 706 may surround the liquid crystal layer 660 in the display area AA. The first and second auxiliary spacers 702 and 706 can be closely spaced patterns or, alternatively, a honeycomb-like structure. The first and second auxiliary spacers 702 and 706 prevent the dropped liquid crystal from flowing beyond the display area AA.

**[0069]** To reduce the number of processes, the first and second auxiliary spacers 702 and 706 may be formed of the same material and through the same process as the column spacers 704. The first auxiliary spacer 702 may be disposed on the signal line 625 or may be disposed on both the gate driver 620 and the signal line 625.

**[0070]** In the third embodiment, the first auxiliary spacer 702 of the plurality of closely spaced patterns or, alternatively, a honeycomb-like structure is disposed on the gate driver 620 such that parasitic capacitance is not caused between the gate driver 620 and the common electrode 606.

**[0071]** As stated above, the LCD device may be manufactured by forming unit cells for respective liquid crystal panels on large substrates and then cutting the substrates into the unit cells. As the substrates get larger, it is more important to maintain a uniform distance between two substrates. To do this, an additional auxiliary spacer may be further formed between adjacent unit cells.

**[0072]** A liquid crystal panel including an auxiliary spacer between adjacent unit cells according to a fourth embodiment of the invention is illustrated. FIG. 11 is a schematic plan view of a liquid crystal panel for an LCD device according to the fourth embodiment of the invention. FIG. 11 shows two attached substrates including unit cells for respective liquid crystal panels.

**[0073]** In FIG. 11, a display area AA and a non-display area NA are defined in each of unit cells C1, C2, C3 and C4. In the display area AA, column spacers 904 are formed, and a liquid crystal layer (not shown) is disposed. In the non-display area NA, a seal pattern 920 is formed and surrounds the display area AA. A gate driver 820 is formed inside the seal pattern 920 of the non-display area NA. A first auxiliary spacer 902 is disposed on the gate driver 820. A second

auxiliary spacer 910 is formed between adjacent unit cells C1, C2, C3 and C4. The second auxiliary spacer 910 between any two of the unit cells C1, C2, C3 and C4 may be spaced apart from others or may be united with others. The first and second auxiliary spacers 902 and 910 may be formed of the same material and through the same process.

**[0074]** In a GIP type LCD device of embodiments of the invention, the parasitic capacitance is not caused between thin film transistors of the gate driver and the common electrode, and the thin film transistors of the gate driver may be prevented from working wrong. In addition, particles do not enter the gate driver during the manufacturing processes. Moreover, in a GIP type LCD device having a medium or large size, output of the gate-driving signals is prevented from being lowered due to delay of the signal line for the gate driver.

**[0075]** It will be apparent to those skilled in the art that various modifications and variations can be made in the gate-in-panel type liquid crystal display device and the method of manufacturing the same of embodiments of the invention without departing from the spirit or scope of the invention. Thus, it is intended that embodiments of the invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

CLAIMS:

1. A liquid crystal display device, comprising:  
first and second spaced apart substrates, each having a display area and a non-display area;  
a liquid crystal layer interposed between the first and second substrates;  
a seal pattern in the non-display area between the first and second substrates;  
a driver in the non-display area on the first substrate;  
column spacers in the display area between the first and second substrates; and  
a first auxiliary spacer between the driver and the second substrate in the non-display area.
2. A liquid crystal display device according to claim 1, wherein the driver has a signal line and the first auxiliary spacer is on the signal line.
3. A liquid crystal display device according to claim 1, further comprising a common electrode on the second substrate in the non-display area and in the display area,  
wherein the first auxiliary spacer is on the common electrode in the non-display area of the second substrate
4. A liquid crystal display device according to any preceding claim, further comprising a second auxiliary spacer along a periphery of the display area between the first and second substrates.

5. A liquid crystal display device according to claim 4, wherein the first and second auxiliary spacers are one of closely spaced patterns and a honeycomb-like structure.

6. A liquid crystal display device according to claim 4 or 5, wherein the first and second substrates have unit cells and a third auxiliary spacer is positioned between the unit cells.

7. A liquid crystal display device according to any of claims 1 to 3, wherein the first and second substrates have unit cells and a second auxiliary spacer is positioned between the unit cells.

8. A liquid crystal display device according to any preceding claim, wherein the driver is within the seal pattern.

9. A liquid crystal display device according to claim 8, wherein the driver has a signal line and the first auxiliary spacer is on the signal line.

10. A liquid crystal display device according to claim 8, further comprising a common electrode on the second substrate in the non-display area and in the display area, wherein the first auxiliary spacer is on the common electrode in the non-display area of the second substrate.

11. A liquid crystal display device according to any of claims 8 to 10, further comprising a second auxiliary spacer along a periphery of the display area between the first and

second substrates.

12. A liquid crystal display device according to claim 11, wherein the first and second auxiliary spacers are one of closely spaced patterns and a honeycomb-like structure.

13. A liquid crystal display device according to claim 11 or 12, wherein the first and second substrates have unit cells and a third auxiliary spacer is positioned between the unit cells.

14. A liquid crystal display device according to any of claims 8 to 10, wherein the first and second substrates have unit cells and a second auxiliary spacer is positioned between the unit cells.

15. A device according to any of claims 8 to 14, wherein the seal pattern includes conductive ball spacers therein.

16. A device according to any preceding claim, wherein the first auxiliary spacer is formed of a same material as the column spacers.

17. A device according to any preceding claim, wherein the first auxiliary spacer is formed of an organic material.

18. A liquid crystal display device, comprising:  
first and second substrates spaced apart from each other, on which a display area and a

non-display area are defined;

a liquid crystal layer interposed between the first and second substrates;

a seal pattern in the non-display area between the first and second substrates;

a driver with a signal line in the non-display area on the first substrate;

column spacers in the display area between the first and second substrates; and

an auxiliary spacer between the signal line and the second substrate in the non-display area.

19. A liquid crystal display device according to claim 18, further comprising a common electrode on the second substrate in the non-display area and in the display area, wherein the auxiliary spacer is on the common electrode in the non-display area of the second substrate.

20. A method of manufacturing a liquid crystal display device having first and second spaced apart substrates, each having a display area and a non-display area, comprising:

forming a seal pattern in the non-display area between the first and second substrates;

forming a driver in the non-display area on the first substrate;

forming column spacers in the display area between the first and second substrates;

forming an auxiliary spacer on a signal line for the driver in the non-display area; and

forming a liquid crystal layer interposed between the first and second substrates.

21. A method of manufacturing a liquid crystal display device, comprising:

preparing first and second substrates, on which a display area and a non-display area are

defined;

forming a driver in the non-display area on the first substrate;

forming column spacers in the display area on one of the first and second substrates;

forming a first auxiliary spacer in the non-display area on one of the first and second substrates, the first auxiliary spacer corresponding to the driver;

forming a seal pattern in the non-display area on one of the first and second substrates;

and

attaching the first and second substrates.

22. A method according to claim 21, wherein forming the first auxiliary spacer is simultaneously performed with forming the column spacers.

23. A method according to claim 21 or 22, wherein the first auxiliary spacer is formed of an organic material.

24. A method according to any of claims 21 to 23, further comprising forming a second auxiliary spacer along a periphery of the display area, wherein the second auxiliary spacer includes a plurality of patterns and has a honeycomb-like structure.

25. A method according to claim 24, wherein the first auxiliary spacer has a honeycomb-like structure.



26. A method according to any of claims 21 to 23, further comprising:  
forming unit cells on the first and second substrates, each of which includes the seal pattern, the driver, the column spacers, and the first auxiliary spacer;  
forming a second auxiliary spacer between the unit cells; and  
cutting the first and second substrates into the unit cells,  
wherein forming the first auxiliary spacer is simultaneously performed with forming the second auxiliary spacer.
27. A method according to any of claims 21 to 26, wherein forming the driver includes forming a signal line, wherein the first auxiliary spacer corresponds to the signal line.
28. A method according to any of claims 21 to 27, further comprising injecting liquid crystal after attaching the first and second substrates.
29. A method according to any of claims 21 to 28, further comprising dropping liquid crystal on one of the first and second substrates before attaching the first and second substrates.
30. A method according to claim 29, wherein the seal pattern is formed on the second substrate and the liquid crystal is dropped on the first substrate.
31. A liquid crystal display device, substantially as hereinbefore described with reference to any of Figs. 4 to 11 of the accompanying drawings.

32. A method of manufacturing a liquid crystal display, substantially as hereinbefore described with reference to any of Figs. 4 to 11 of the accompanying drawings.

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**Claims searched:** 1-30

**Date of search:** 17 September 2007

**Patents Act 1977: Search Report under Section 17**

**Documents considered to be relevant:**

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1, 4, 6-8 11, 13 & 15-17	JP 08248427 A1 (SEMICONDUCTOR ENERGY LAB) English language abstract WPI AN: 1996-489260. Figures 1 and 6.
A	-	US 2006/0146244 A1 (PARK) Figures 7-10

**Categories:**

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art
Y	Document indicating lack of inventive step if combined with one or more other documents of same category	P	Document published on or after the declared priority date but before the filing date of this invention
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**Field of Search:**

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>X</sup>:

G2F; G5C

Worldwide search of patent documents classified in the following areas of the IPC

G02F; G09G

The following online and other databases have been used in the preparation of this search report

Online: EPODOC, WPI

**International Classification:**

Subclass	Subgroup	Valid From
G02F	0001/1339	01/01/2006
G09G	0003/36	01/01/2006