

(51) International Patent Classification:
H03F 1/32 (2006.01)(21) International Application Number:
PCT/IB2008/053875(22) International Filing Date:
24 September 2008 (24.09.2008)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (for all designated States except US):
FREESCALE SEMICONDUCTOR, INC. [US/US];
6501 William Cannon Drive West, Austin, Texas 78735
(US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **PRATT, Patrick**
[IE/IE]; GortnaGreig, Mallow, 000 (IE). **CHEN, Jau**
Hong [—/US]; 2225 W Frye Rd. #2050, Chandler, Ari-
zona 85224 (US). **NORRIS, George** [US/US]; 23317 S
182nd St, Gilbert, Arizona 85298 (US).(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,
CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ,EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO,
NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG,
SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, US, UZ, VC, VN, ZA, ZM, ZW.(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,
TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI
(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR,
NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

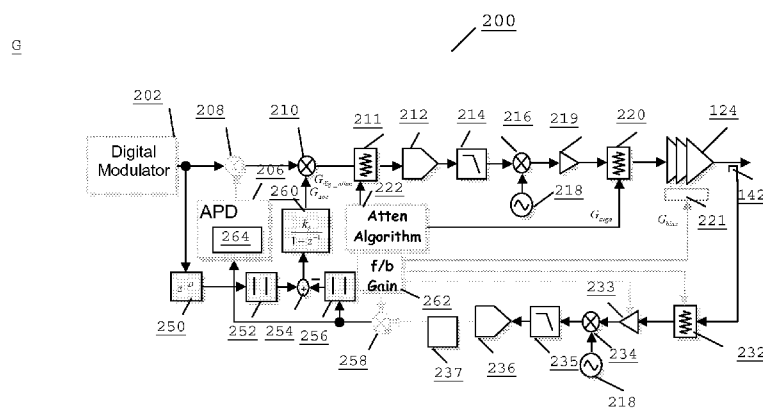
Published:

— with international search report (Art. 21(3))

— with amended claims (Art. 19(1))

(54) Title: WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF POWER CONTROL OF A
POWER AMPLIFIER THEREFOR

FIG. 2



(57) Abstract: A wireless communication unit (100) comprises a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path arranged to feed back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124). The forward path and feedback path form a constant gain tracking (CGT) loop. The feedback path comprises an adaptive predistortion logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path. The CGT loop comprises a controller logic module arranged to determine a gain offset of a signal routed through the forward path and feedback path and in response thereto set a drive level of the PA (124).

**TITLE: WIRELESS COMMUNICATION UNIT, INTEGRATED CIRCUIT AND METHOD OF
POWER CONTROL OF A POWER AMPLIFIER THEREFOR**

TECHNICAL FIELD

5

The technical field relates generally to a wireless communication unit, integrated circuit and method of power control of a power amplifier therefor. The technical field is applicable to, but not limited to, a wireless communication unit, integrated circuit and method of power control of a power amplifier used in an adaptive predistortion transmitter.

10

BACKGROUND

15

Wireless communication systems, for example cellular telephony or private mobile radio communication systems, typically provide for radio telecommunication links to be arranged between a plurality of base transceiver stations (BTS), referred to as Node Bs with regard to a universal mobile telecommunication system (UMTS), and a plurality of subscriber units, often referred to as user equipment (UE) in UMTS.

20

In a cellular network, such as UMTS, the power transmitted by a UE is regulated in order to minimise interference with other UEs. Typically, the output power generated by the radio frequency (RF) power amplifier (PA) in the UE will vary due to any number, or combination, of factors, such as the manufacturing process, operating temperature, supply voltage, antenna loading and other such factors. Thus, it often becomes necessary to measure the radio frequency transmit power at, or after, the PA output and to control a PA gain, typically by controlling the gain of amplifiers located earlier in the amplifier chain, in response to this measurement. This feedback will allow power control regulation to compensate for variations in PA supply voltage, operating temperature & manufacturing process.

25

30

35

Continuing pressure on the limited spectrum available for radio communication systems is forcing the development of spectrally-efficient linear modulation schemes. Since the envelopes of a number of these linear modulation schemes fluctuate, intermodulation products can be generated in the non-linear radio frequency power amplifier. Thus, it is important to ensure any unwanted terms arising from the intermodulation are minimised and stay below a specified value. By modifying the bias to improve efficiency the PA becomes more non-linear, which in turn would lead to increased intermodulation problems. Specifically, in this field, there has been a significant amount of research effort in developing high efficiency topologies capable of providing high performances in the 'back-off' (linear) region of the power amplifier.

Linear modulation schemes require linear amplification of the modulated signal in order to minimise undesired out-of-band emissions. It is also known that non-linearities may also create in-band distortion, which is typically measured by determining an error vector magnitude (EVM). Quantum processes within a typical RF amplifying device are inherently non-linear by nature. Only when a small portion of the consumed DC power is transformed into RF power, can the transfer function of the amplifying device be approximated by a straight line, i.e. as in an ideal linear amplifier case. This mode of operation provides a low efficiency of DC to RF power conversion, which is unacceptable for portable (subscriber) wireless communication units. Furthermore, the low efficiency is also recognised as being problematic for the base stations.

Furthermore, the emphasis in portable (subscriber) equipment is to increase battery life. The emphasis for base station designers is to reduce operating and equipment cost (power consumption, size, power dissipation, etc.). Hence, such operating efficiencies of the amplifiers used must be maximised. To achieve both linearity and efficiency, so called linearisation techniques are used to improve the linearity of the more efficient amplifier classes, for example class 'AB', 'B' or 'C' amplifiers. A number of linearising techniques exist, such as Cartesian Feedback, Feed-forward, and Adaptive Pre-distortion (APD) and these are often used to resolve the inherent trade off of linearity versus efficiency in wireless communication units.

The purpose of an APD system/circuit is to mitigate against any distortion arising from any dynamic amplitude modulation (AM) gain variation. For existing 3rd generation communication standards, such as EDGE, WCDMA, OFDMA, etc., the AM of the signal to be transmitted changes as a result of a variable PA gain. The APD in a sense creates an inverse to this gain so that the total gain is a constant. To fully exploit the advantages of APD, a system that will automatically adjust the power amplifier (PA) supply is also required, so that it may be optimally biased across, say, the 3GPP power target range as well as in the presence of process, temperature and/or load variation. It is known that without such a power tracking or Envelope Tracking (ET) system the PA can become over-compressed, resulting in a poor adjacent channel leakage power ratio (ACLR) and/or error vector magnitude (EVM) failure. Alternatively, the PA may be under-compressed resulting in reduced efficiency performance.

Known techniques using APD have been targeted at base station applications where the requirements on optimally biasing the PA across load and power target variation are less severe compared to a handset wireless communication design. It is known that an adaptive predistortion loop, if operated in isolation, will function under limited operating regions. However, at certain operating corners the adaptive predistortion loop will not function robustly enough, due to the fact that the adaptive predistortion loop may have too much linear gain to adapt out.

US 7203247 B2, titled 'Digital predistortion technique for WCDMA wireless communication system and method of operation thereof' describes a basic adaptive predistortion mechanism, but does not consider any aspect related to power levelling in an

- 3 -

APD-based transmitter. A paper titled 'Adaptive linearization using predistortion-experimental results', authored by M. Faulkner and M. Johansson and published in 'Vehicular Technology, IEEE Transactions on, 1994' describes adaptive predistortion with power levelling. However, the power levelling method is limited to a simple gain modification in the APD feedback path.

- 5 Thus, by facilitating gain modification in the APD feedback path, the APD system becomes much more complex and slower than desired or required.

SUMMARY OF THE INVENTION

- 10 A wireless communication unit, an integrated circuit and a method of performing power control in a transmitter are described, as defined in the accompanying Claims.

Further aspects and features of the invention are as defined in the accompanying dependent Claims and are disclosed in the embodiments of the invention to be described.

15 BRIEF DESCRIPTION OF THE DRAWINGS

- The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to
20 further illustrate various embodiments and to explain various principles and advantages all in accordance with the invention.

FIG. 1 illustrates a block diagram of an example of a wireless communication unit..

FIG. 2 illustrates a more detailed block diagram of an example of a transmitter of a wireless communication unit employing an adaptive predistortion system.

- 25 FIG. 3 illustrates a more detailed block diagram of an automatic output power control arrangement of a wireless communication unit transmitter.

FIG. 4 illustrates a graphical representation of gain versus output power for the transmitter and RF attenuator of a wireless communication unit transmitter.

- 30 FIG. 5 illustrates a more detailed block diagram of another example of an alternative transmitter architecture of a wireless communication unit employing an adaptive predistortion system.

FIG. 6 illustrates a flowchart of an example of a power control algorithm of a transmitter of a wireless communication unit.

35 DESCRIPTION OF EMBODIMENTS OF THE INVENTION

As explained below in more detail, in the shown examples, the power regulation loop functionality is separated from and individually treated, the APD function. In particular, a Constant Gain Tracking (CGT)-specific loop is placed inside an adaptive predistortion (APD)

- 4 -

loop. The CGT-specific loop removes constant gain offsets with respect to the idealised or desired linear gain. The CGT-specific loop may, for example, regulate or set the average or constant root mean square (rms) gain of the loop. The CGT-specific loop is arranged to compare the instantaneous detected amplitude modulated (AM) signal to a delayed
5 synchronised reference AM signal and adjust the transmit gain to drive the mean power towards its target. In doing so the root mean square (RMS) gain around the (APD) loop is normalised.

Concurrently, the APD can regulate the AM-dependent, dynamic, varying gain of the loop. Accordingly, the APD only has to linearise the transmit loop gain around a normalised
10 operating point. Thereby, its rate of convergence may be accelerated and overall system performance may be improved.

Conventional automatic output control (AOC) systems are limited to off line, factory calibration and at most may have temperature and or battery sensors to adapt to environmental changes. The CGT loop may be initialised from the APD Master Gain Table
15 (MGT). Hence, the CGT loop may be adaptive and capable of adapting to changes in the Power amplifier (PA) AM distortion characteristics. As the CGT loop is adaptive it is able to respond to changes in the transmit gain characteristics faster than a conventional (non adaptive) AOC loop.

One purpose of locating the CGT loop within an APD loop is to regulate or 'level' the
20 average or mean power. Thereby, it may be to ensure that the output mean power is set and remains 'close' to a target power value. Thus, the CGT loop may set the gain of the transmit chain line-up to achieve a given average target output power (P_{out}), where:

$$P_{out} = G_{average} \times P_{in},$$

Where:

25 P_{in} is the input average power of the transmit chain line-up, and
 $G_{average}$ is the average gain of the line up).

Thus, in this manner, the CGT loop sets the required $G_{average}$ for a given target P_{out} . Furthermore, the locating of a CGT loop within an APD loop may enable removing constant gain offsets and, thus, enable centering the predistortion (PD) operation around a
30 normalized operating point, thereby accelerating adaptation of the APD logic module.

Before describing in detail examples it should be observed that the apparatus components and method steps have been represented where appropriate by conventional
symbols in the drawings, showing only those specific details that are pertinent to
35 understanding the embodiments of the invention so as not to obscure the disclosure with details that will be readily apparent to those of ordinary skill in the art having the benefit of the description herein.

- 5 -

In the following, a mechanism is described for adjusting the PA supply voltage V_{cc} as an example. However, the same technique may be used to adjust a PA bias voltage. Thus, hereinafter reference to a PA supply voltage in the specification and claims is meant to encompass both.

5 Referring now to FIG. 1, a block diagram of an example of a wireless communication unit 100 adapted to support the inventive concept of the invention, is illustrated. For the sake of clarity, the wireless communication unit 100 is shown as divided into two distinct portions: a receiver chain 105 and a transmitter chain 125.

10 The wireless communication unit 100 contains an antenna 102. In this example, the antenna 102 is coupled to an antenna switch 104 that provides signal control of radio frequency (RF) signals in the wireless communication unit 100, as well as isolation between the receiver chain 105 and transmitter chain 125. The antenna switch 104 may be replaced by a duplex filter, for frequency duplex communication units as is known to those skilled in the art.

15 For completeness, the receiver 105 of the wireless communication unit 100 will be briefly described. The receiver 105 includes a receiver front-end circuit 106 (which provides reception, filtering and intermediate or base-band frequency conversion). The front-end circuit 106 is serially coupled to a signal processing function (generally realised by at least one receiving signal processing unit, such as digital signal processor (DSP)) 108. An output
20 from the at least one digital signal processor 108 is provided to a user interface 111, which in a receiving context may comprise a suitable output device, such as a screen or loudspeaker. A controller 114 is operably coupled to the front-end circuit 106. A memory device 116 stores data, such as data relating to decoding/encoding functions and the like. A timer 118 is operably coupled to the controller 114 to control the timing of operations, namely the
25 transmission or reception of time-dependent signals.

As regards the transmit chain 125, this essentially includes an input device 120, such as a keypad, or microphone operably coupled to signal processing logic 128 and transmitter/modulation circuitry 122 and an up-converter/power amplifier 124. A skilled artisan will appreciate that the signal processing unit 128 in the transmit chain may be implemented as
30 distinct from a receiving signal processing unit in the receive chain. Alternatively, a single unit, e.g. a single DSP may be used to implement processing of both transmit and receive signals, as shown in FIG. 1.

As described hereafter in the examples, the signal processing unit 128, transmitter/modulation circuitry 122 and the up-converter/power amplifier 124 are operationally
35 responsive to the controller 114, with an output from the power amplifier 124 coupled to the antenna switch 104. A feedback circuit includes a detector (not shown) and down-converter 132, which together with the transmitter/modulation circuitry 122, power amplifier 124 and a directional coupler 142, forms a closed feedback loop.

Referring now to FIG. 2, an example of a transmitter architecture 200, is shown. The shown transmitter architecture 200 comprises a digital logic module 202 arranged to provide a digitally modulated input signal to the transmitter chain. The digitally modulated input signal is input to a first multiplier unit 208, where the digitally modulated input signal is multiplied with a predistortion signal provided by an adaptive pre-distortion (APD) logic module 206. The APD logic module 206 provides a complex I/Q signal to the digitally modulated input signal to ensure that the signal output from the power amplifier 124 is linear in nature. The output from the first multiplier unit 208, and therefore the output from the outer APD loop, is input to a second multiplier unit 210, where it is multiplied with a signal provided by a constant gain tracking (CGT) loop.

The second multiplier unit 210 inputs a scaled (i.e. multiplied) I/Q signal to a digital-to-analogue converter (DAC) 212, which converts the input digital signal to an analogue output signal. The scaling is controlled via a digital variable attenuator 211. The DAC 212 outputs the analogue output signal to a low-pass filter (LPF) 214 that rejects high frequency undesired analogue signals. The output from the LPF 214 is input to an up-mixer 216 arranged to frequency up-convert the analogue, filtered signal with a local oscillator (LO) 218 reference signal. The up-converted signal is input to an amplifier 219 and a gain adjustment circuit or element (such as a variable attenuator) 220, which is controlled by an attenuator logic module 222. The gain adjusted signal is then input to a power amplifier chain 124, where it is amplified and routed to an antenna (not shown). The gain of the PA 124 is controlled by a gain_bias signal 221.

A directional coupler 142 is arranged to couple a portion of the amplified transmit signal into a feedback path comprising a further gain adjustment circuit or element 232. The gain adjusted feedback signal is input to a RF gain circuit or element 233 and a down-mixer 234 arranged to frequency down-convert the coupled, gain-adjusted transmit signal with the LO 218 reference signal. The combination of the further gain adjustment circuit or element 232, the RF gain circuit or element 233 and down-mixer 234 may be considered as a feedback detector, which may be implemented as a zero intermediate frequency (ZIF) coherent receiver.

The down-converted signal is input to a LPF 235 to filter out undesirable mixed signals and thereafter to an analogue-to-digital converter (ADC) 236, where it is converted into a digital form. The digital signal from the ADC 236 is then input to a third multiplier unit 258, where the digital signal is multiplied with a gain adjustment value provided by feedback gain control module 262. Feedback gain control module 262 also provides gain control signals to RF amplifier 233 and variable RF attenuator 232 in the feedback path, and controls the DC supply to the PA 124 to control the gain of the PA. The setting of the variable RF attenuator 232 is selected based on the mean output power target of the transmitter and may

- 7 -

be chosen such that signal-to-noise ratio (SNR) and linearity of the transmitter are improved for a given target output power level.

The output from the third multiplier unit 258 is input to APD logic module 206, which corrects for both amplitude and phase distortions caused by the PA 124 in the following manner. It should be noted that if the system was ideal and perfectly linear, then the transmitted amplitude and phase (output from the PA 124) would be identical to the detected amplitude and phase (for example the detected output from the ADC 236 (with the exception of a random but constant phase offset). However, in practice the PA exhibits a nonlinearity that corrupts or distorts the amplitude modulated (AM) and phase modulated (PM) components of the original input signal. Thus, the APD logic module 206 predistorts the transmit signal, such that the detected AM and PM components (as translated by ADC 236 and represented at the output of the PA 124) are as close as possible to the original AM and PM components of the original input signal. In addition to the distortion of the PA corrupting the PM component of the output signal, the PA 124 will in practice also introduce an arbitrary phase offset to the transmitted PM, which is generally known or referred to as Phase Insertion. The amount of phase insertion is random, while dependent on temperature, voltage, loading, etc. The APD logic module 206 attempts to correct for these factors when applying a correction signal to the first multiplier unit 208. To overcome the problems arising from insertion phase offset, quadrature imbalance and DC offset of the feedback signal, a calibration system 237 may be present. In the example of FIG. 2, this calibration operation is performed by the calibration system 237 independently of, and separately to, the APD.

The output from the third multiplier unit 258 is converted into its amplitude or magnitude equivalent (i.e. the magnitude of the complex, I-Q detected signal) by magnitude logic module 256 before being applied to subtracting logic module 254. The input digital signal provided by the digital modulator logic module 202 is delayed in delay element 250, converted to AM by logic module 252 and then applied to subtracting logic module 254. The output from subtracting logic module 254 is provided to gain logic module 260 to provide a multiplication value. The multiplication value from gain logic module 260 is applied to second multiplier unit 210, thereby completing the CGT loop. By selecting an appropriate multiplication value, it is possible to effect and absolutely scale (via the CGT loop) a desired average output power P_{out} of PA 124.

In the shown examples the inner CGT loop is arranged to control the attenuation of variable attenuators, such as variable attenuator 220, based on an evolution of the APD master gain table (MGT) 264. In this manner, the CGT loop is linked to the APD operation so that its initial factory-phased gain settings are adaptive and modified by the particular gain expansion or compression of the PA at the given target power, as determined by the APD MGT 264. The use of the CGT loop closed around the instantaneous AM signal generating elements is therefore able to remove constant gain offsets arising from imperfect factory

phasing and any subsequent drift. This is achieved by the CGT loop attempting to normalize the AM distortion characteristics around the target mean power. In addition, the CGT loop achieves the final, fine gain control or power levelling, to set the mean target power of the transmitter and thereby accelerate speed of convergence of the APD loop.

5 The coarse gain may be partitioned into three stages:

- (i) the PA gain, which can be set via a bias control signal, G_{bias} ;
- (ii) a segmented variable gain attenuator 220, G_{svga} ; and
- (iii) a digital attenuator, G_{dig_atten} as shown in FIG. 2.

10 The particular PA gain and bias settings may, for example, be read from a factory phase look-up table (LUT) (not shown) indexed by the Power Control Level (PCL), modulation mode and frequency band and are programmed in advance of transmitting on a particular cellular communication system, for example a 2nd Generation (2G) transmit multislot and 3rd Generation (3G) Random Access Channel (RACH), or subject major power transition in the case of 3G. The contents of the MGT 264 are not used in determining the PA gain in this
15 example.

Referring now to FIG. 3, a more detailed block diagram of an automatic output power control arrangement of a wireless communication unit transmitter, adapted in accordance with embodiments of the invention, is illustrated. The LUT may for example be phased at, say,
20 three power settings, high power, medium power and low power. Interpolation logic module 322 may be arranged to interpolate between these three phased values to establish the required Segmented Voltage Gain Amplifier (Svga) setting or code for the full range of power control levels. In addition, the CGT logic module 302 may also be arranged to calculate a virtual attenuator setting that is equivalent to the total or combined ideal setting, taking into
25 account the various controllable attenuator and gain settings, such as a digital attenuator and any radio frequency variable gain attenuator (such as the Svga), etc. This gain is referred to here as G_{TX} and can be understood as the combined attenuator setting that would level the mean power exactly at the target value if the phasing conditions (temperature, loading, supply) were still valid. The digital attenuator or back-off may be pre-calculated by the CGT
30 logic module 302 to correct for the finite resolution or quantisation effect of the Svga, as quantized in DAC 308:

$$G_{dig_atten} = G_{TX} / G_{svga}.$$

It should be noted that a 'linear' mode of operation encompassed when the PA is biased such that the PA nonlinearity is deemed negligible (for example when the peak AM is
35 well backed off or below 1dB compression so that the adjacent channel leakage ratio (ACLR) and error voltage magnitude (evm), etc. are within the regulated specification without a need for any linearization systems, such as APD. Thus, in the example the CGT logic module 302

is phased with gain values based on such linear operation. In contrast, a nonlinear mode of operation is where the bias is modified such that the peak AM extends into a soft compression region, thereby resulting in degraded ACLR and EVM unless a linearization technique, such as APD is used.

- 5 In nonlinear mode, the attenuator settings are adjusted to correct for any post-phasing changes to the amount of gain compression or expansion at the target power. For example, supposing that relative to the phasing point, the PA gain is expanded by xdB at the particular target power, then the attenuator gains must be compressed by xdB. In general, this correction may be expressed by:

$$10 \quad G_x = \frac{X_{rms}}{Y_{rms}} \quad [1]$$

where:

X_{rms} represents the transmitted baseband rms for the desired target power; and

Y_{rms} represents the resultant, detected, baseband rms value.

- 15 In essence, G_x is the inverse rms gain of the loop for the given target power. If the loop has not shifted from its phasing point then $G_x = 0\text{dB}$ and no correction is required. Otherwise correction of the phased attenuator settings is desirable to minimize or at least reduce subsequent training of the APD. This inverse rms gain can be evaluated from the MGT 264 at the target power, i.e.

$$20 \quad G_x = |G_{pd}(P_t)| \quad [2]$$

- In the example of FIG. 3, the total attenuation (digital attenuator 314 plus Svga 310) is first read out of the CGT phasing table (MGT 324). This gain (or total attenuation) is then scaled by the predistortion gain, $|G_{pd}(P_t)|$ obtained from MGT 324 (such as an APD LUT) to
 25 produce the total corrected gain required to level the power at the target value. This gain (or total attenuation) is then quantized in a simple forward step to find a Svga setting that is nearest to Gtx, 308 to produce the applied Svga attenuation level 310. The digital attenuator setting 314 can then be calculated from the quantized Svga, in divider module 312 according to:

$$30 \quad G_{dig_atten} = G_{TX} |G_{pd}(P_t)| / G_{svga} \quad [3]$$

The absolute power levelling and accuracy of the CGT loop is determined by the gain of the detector, and is controlled at two points along the detector path, an RF/analogue step attenuator and digital gain stage (not shown).

Referring now to FIG. 4, a graphical representation 400 of gain 405 versus output power 410 is illustrated for a wireless communication unit's transmitter. The graphical representation 400 also illustrates the virtual gain G_{tx} for a linear PA 430 and the corresponding Svga settings (i.e. G_{tx} rounded to the nearest Svga setting) when the transmitter is operating in an APD mode of operation. Similarly, the graphical representation 400 illustrates the equivalent gains 415, 420 when the transmitter is operating with a nonlinear biased PA.

FIG. 5 illustrates a block diagram of another transmitter architecture 500 of a wireless communication unit employing an adaptive predistortion system. In a similar manner to the architecture 200 of FIG. 2, the transmitter architecture 500 comprises a majority of the same circuits and elements, the operation of which will not be replicated here for simplicity purposes only. The primary difference between the architecture 200 of FIG. 2 and the transmitter architecture 500 of FIG. 5 is as follows.

The output from the third multiplier unit 258 is input to unity gain logic module 512 before being applied to subtracting logic module 510. The linearising input digital signal provided by the APD logic module 506 to the first multiplier unit 208 is also applied to subtracting logic module 510 after being passed through an absolute logic module 508, (which may be understood as providing a magnitude of a complex gain of the APD loop converted to absolute gain). As in FIG. 2, the output from subtracting logic module 510 is provided to gain logic module 504 to provide a multiplication value. The multiplication value from gain logic module 504 is applied to second multiplier unit 210, thereby completing the CGT loop. By selecting an appropriate multiplication value, it is possible to effect and absolutely scale (via the CGT loop) a desired average output power P_{out} of PA 124.

In this example, the inner CGT loop is arranged to calculate the gain output of the APD logic module 506. In effect, the instantaneous absolute gain of the APD is compared to unity or '1'. The digital gain is then adjusted so that the average error (where the error is equal to a difference between APD magnitude gain and unity) is minimised. This effectively adjusts the digital gain 212 until the average magnitude APD gain is unity. This is, in effect, the function of the CGT loop, which is to set the gain so that the APD operates around a normalised of unity, i.e. its average or mean gain should be unity.

FIG. 6 illustrates a flowchart 600 of an example of a constant gain tracking mechanism of a transmitter of a wireless communication unit. In this Figure, the flowchart 600 illustrates the operation of a CGT-specific loop located within an adaptive predistortion (APD) loop and arranged to regulate or set the average or constant root mean square (rms) gain of the loop. The CGT-specific loop is arranged to compare the instantaneous detected amplitude modulated (AM) signal to a delayed synchronised reference AM signal and adjust

- 11 -

the transmit gain to drive the mean power towards its target. Thus, the operation of the CGT-specific loop serves to remove any constant gain offsets with respect to the idealised or desired linear gain. In doing so the RMS gain around the (APD) loop is normalised.

The mechanism commences with receiving a target power level (PWR), as shown as
5 indicated with 605. The target power level (PWR) may be an input supplied from a 'higher level' or 'layer' that represents the target (average) power. Next, as indicated with 610, a CGT algorithm calculates the desired attenuator settings, for example dig_atten and Segmented Voltage Gain Amplifier (Svga) settings, for the given PWR value. The dig_atten value refers to a digital, baseband amplifier, i.e. a multiplier that scales the digital baseband
10 I/Q signal and the Svga setting is an RF based step attenuator having non-uniform attenuation steps. The combined gain of the digital attenuator and the Svga would ideally (if the factory phased settings (temp. loading, battery etc) were still applicable) provide the desired power levelling. However, due to temperature, loading, battery and/or process variation within the communication unit the power levelling will be imperfect, thereby resulting
15 in an offset or gain error in either dig_atten and/or the Svga setting. This error is corrected by adjusting either the Svga and/or the digital attenuator, as follows.

The flowchart continues with a calculation of gain error based on PA expansion or compression of PA using MGT at the target power value, as shown as indicated with 615. Due to temperature, battery and/or load variation, the PA gain at the target power will deviate
20 from the original factory gain value. This gain offset will be calculated by the MGT as indicated with 615 and may be used to correct the CGT attenuator/gain settings. For example, the Svga may be first adjusted to correct for 'as much' of this (coarse) error as possible, as shown as indicated with 620. The Svga may have a limited number of settings, for example in a similar manner to the quantisation effect of a digital-to-analogue converter
25 (DAC). To remove as much of the gain error the Svga may be adjusted with the residual (fine) error being corrected by adjusting the digital attenuator setting, as indicated with 625.

The MGT values are then mapped to the localised APD look-up table, as shown as indicated with 630. Ideally if the above adjustments to the CGT settings are correct, the power should be levelled exactly. However, the MGT values may not be updated fast enough
30 to track variations in the transmit gain, with the result that there may be residual gain errors causing an offset in the mean target power. The CGT loop may then dynamically remove this remaining error in an automatic closed loop control fashion, as shown as indicated with 635.

It will be understood that the examples of a wireless communication unit, integrated
35 circuit and method of controlling an output power of a PA in a transmitter, as described above, may facilitate a radio transmitter to run deeper into compression, and hence more efficiently, regardless of process, load and/or temperature variation. In this manner, the radio transmitter is arranged to optimally, or at least improve, bias of a PA for both minimum or at least

- 12 -

reduced current consumption and minimum, or at least reduced, nonlinearity, for example in a variable data rate 3G phone, across power target, process, temperature and load. This ultimately saves current consumption and thereby extends talk time for the radio transmitter. Furthermore, if an operating condition occurs that implies that the switcher voltage is too low, then the system is sufficiently intelligent to automatically back off the target power. In addition, the examples continuously operate a switcher loop, making its performance less susceptible to operating condition variations. Also, the examples are capable of being more aggressive in terms of operating the PA deeper in saturation, while maintaining good spectral performance.

In particular, the shown examples use two separate control loops: a constant gain tracking (CGT) loop arranged to eliminate the constant gain error (that would otherwise need to be taken out by all of the taps on the adaptive predistortion loop). The CGT loop normalizes the system to facilitate a more robust operation of the adaptive predistortion loop around the normalised target mean power level.

Those skilled in the art will realize that the above recognized advantages and other advantages described herein are merely exemplary and that the invention does not require all of these advantages to be obtained.

It will be appreciated that the examples described herein may be comprised of one or more generic or specialized processors (or 'signal processors') such as microprocessors, digital signal processors, customized processors and field programmable gate arrays (FPGAs) and unique stored program instructions (including both software and firmware) that control the one or more processors to implement, in conjunction with certain non-processor circuits, some, most, or all of the functions of the method and apparatus for performing power control described herein. Alternatively, some or all functions could be implemented by a state machine that has no stored program instructions, or in one or more application specific integrated circuits (ASICs), in which each function or some combinations of certain of the functions are implemented as custom logic. Of course, a combination of the two approaches could be used. Both the state machine and ASIC are considered herein as a 'signal processor' for purposes of the foregoing discussion and claim language.

Moreover, an embodiment of the invention can be implemented as a computer-readable storage element having computer readable code stored thereon for programming a computer (e.g., comprising a processing device) to perform a method as described and claimed herein. Examples of such computer-readable storage elements include, but are not limited to, a hard disk, a CD-ROM, an optical storage device, a magnetic storage device, a Read Only Memory (ROM), a Programmable Read Only Memory (PROM), an Erasable Programmable Read Only Memory (EPROM), an Electrically Erasable Programmable Read Only Memory (EEPROM) and a Flash memory. Further, it is expected that one of ordinary

skill, notwithstanding possibly significant effort and many design choices motivated by, for example, available time, current technology, and economic considerations, when guided by the concepts and principles disclosed herein will be readily capable of generating such software instructions and programs and ICs with minimal experimentation.

5 In the foregoing specification, specific embodiments of the invention have been described. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the invention as set forth in the claims below.

10 Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of invention. The benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential features or elements of any or all the claims. The invention is defined solely by the appended claims including any amendments
15 made during the pendency of this application and all equivalents of those claims as issued.

Furthermore, although individual features may be included in different claims, these may possibly be advantageously combined, and the inclusion in different claims does not imply that a combination of features is not feasible and/or advantageous. Also, the inclusion of a feature in one category of claims does not imply a limitation to this category, but rather
20 indicates that the feature is equally applicable to other claim categories, as appropriate.

Moreover in this document, relational terms such as first and second, top and bottom, and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual such relationship or order between such entities or actions.

25 The terms 'comprises', 'comprising', 'has', 'having', 'includes', 'including', 'contains', 'containing' or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises, has, includes, contains a list of elements does not include only those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. An element
30 proceeded by 'comprises ...a', 'has ...a', 'includes ...a', 'contains ...a' does not, without more constraints, preclude the existence of additional identical elements in the process, method, article, or apparatus that comprises, has, includes, contains the element. The terms 'a' and 'an' are defined as one or more, unless explicitly stated otherwise herein.

35 The terms 'substantially', 'essentially', 'approximately', 'about' or any other version thereof, are defined as being close to as understood by one of ordinary skill in the art. The term 'coupled' as used herein is defined as connected, although not necessarily directly and not necessarily mechanically. A device or structure that is 'configured' in a certain way is configured in at least that way, but may also be configured in ways that are not listed.

Claims

1. A wireless communication unit (100) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path arranged to feed back a
5 portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124) wherein the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the CGT loop comprises a controller logic module arranged to determine a gain offset of a
10 signal routed through the forward path and feedback path and in response thereto set a drive level of the PA (124).
2. The wireless communication unit (100) of Claim 1 wherein the controller logic module of the CGT loop is arranged to automatically adapt the drive level of the PA (124) in
15 response to a determination of a gain change.
3. The wireless communication unit (100) of Claim 1 or Claim 2 wherein the controller logic module (114) is arranged to automatically adapt the drive level of the PA (124) to a nominal drive level such that the APD logic module linearises a signal output from the PA
20 around the nominal drive level.
4. The wireless communication unit (100) of any preceding Claim wherein the controller logic module is arranged to set a drive level of the PA (124) by controlling a gain setting of a plurality of attenuators.
25
5. The wireless communication unit (100) of Claim 4 wherein the controller logic module is arranged to set a drive level of the PA (124) by first controlling a coarse gain setting of a radio frequency attenuator located in the forward path.
- 30 6. The wireless communication unit (100) of Claim 4 wherein the controller logic module is arranged to set a drive level of the PA (124) by subsequently controlling a fine gain setting of a digital attenuator located in the forward path.
- 35 7. An integrated circuit for performing power control of a transmitter comprising a power amplifier, PA, (124), the integrated circuit comprising a forward path and a feedback path operably coupleable to the PA (124), wherein the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with

- 15 -

the forward path and feedback path, wherein the CGT loop comprises a controller logic module arranged to determine a gain offset of a signal routed through the forward path and feedback path and in response thereto set a drive level of the PA (124).

- 5 8. A method of power control in a wireless communication unit (100, 200) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path for feeding back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124), such that the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path further comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the method comprises:

 determining a gain offset of a signal routed through the forward path and feedback path in the CGT loop, and
15 in response thereto setting a drive level of the PA (124).

9. The method of Claim 8 further comprising linearising a signal output from the PA (124) around the drive level of the PA (124) set based on the determined gain offset.

- 20 10. A computer-readable storage element having computer readable code stored thereon for programming a computer to perform a method for power control in a wireless communication unit (100, 200) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path for feeding back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124), such that the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path further comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the code is operable for:
- determining a gain offset of a signal routed through the forward path and feedback path in the CGT loop, and
30 in response thereto setting a drive level of the PA (124).

11. The computer-readable storage element of Claim 10 wherein the computer readable storage element comprises at least one of: a hard disk, a CD-ROM, an optical storage device, a magnetic storage device, a Read Only Memory, ROM, a Programmable Read Only Memory, PROM, an Erasable Programmable Read Only Memory, EPROM, an Electrically Erasable Programmable Read Only Memory, EEPROM and a Flash memory.
- 35

AMENDED CLAIMS
received by the International Bureau on
04 September 2009 (04.09.2009)

1. A wireless communication unit (100) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path arranged to feed back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124) wherein the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the CGT loop comprises a controller logic module arranged to determine a gain offset of a signal routed through the forward path and feedback path and in response thereto set a drive level of the PA (124) by controlling a gain setting of a plurality of attenuators.
2. The wireless communication unit (100) of Claim 1 wherein the controller logic module of the CGT loop is arranged to automatically adapt the drive level of the PA (124) in response to a determination of a gain change.
3. The wireless communication unit (100) of Claim 1 or Claim 2 wherein the controller logic module (114) is arranged to automatically adapt the drive level of the PA (124) to a nominal drive level such that the APD logic module linearises a signal output from the PA around the nominal drive level.
4. The wireless communication unit (100) of Claim 1 wherein the controller logic module is arranged to set a drive level of the PA (124) by first controlling a coarse gain setting of a radio frequency attenuator located in the forward path.
5. The wireless communication unit (100) of Claim 1 wherein the controller logic module is arranged to set a drive level of the PA (124) by subsequently controlling a fine gain setting of a digital attenuator located in the forward path.
6. An integrated circuit for performing power control of a transmitter comprising a power amplifier, PA, (124), the integrated circuit comprising a forward path and a feedback path operably coupleable to the PA (124), wherein the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the CGT loop comprises a controller logic module arranged to determine a gain offset of a signal routed through the forward path and feedback path and in response thereto set a drive level of the PA (124) by controlling a gain setting of a plurality of attenuators.

7. A method of power control in a wireless communication unit (100, 200) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path for feeding back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124), such that the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path further comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the method comprises:

determining a gain offset of a signal routed through the forward path and feedback path in the CGT loop, and
in response thereto setting a drive level of the PA (124) by controlling a gain setting of a plurality of attenuators.

8. The method of Claim 7 further comprising linearising a signal output from the PA (124) around the drive level of the PA (124) set based on the determined gain offset.

9. A computer-readable storage element having computer readable code stored thereon for programming a computer to perform a method for power control in a wireless communication unit (100, 200) comprising a transmitter having a forward path comprising a power amplifier, PA, (124) and a feedback path for feeding back a portion of a signal output from the PA (124) to a point in the forward path prior to the PA (124), such that the forward path and feedback path form a constant gain tracking, CGT, loop and the feedback path further comprises an adaptive predistortion, APD, logic module located outside of the CGT loop and arranged to form an APD loop with the forward path and feedback path, wherein the code is operable for:

determining a gain offset of a signal routed through the forward path and feedback path in the CGT loop, and
in response thereto setting a drive level of the PA (124) by controlling a gain setting of a plurality of attenuators.

10. The computer-readable storage element of Claim 9 wherein the computer readable storage element comprises at least one of: a hard disk, a CD-ROM, an optical storage device, a magnetic storage device, a Read Only Memory, ROM, a Programmable Read Only Memory, PROM, an Erasable Programmable Read Only Memory, EPROM, an Electrically Erasable Programmable Read Only Memory, EEPROM and a Flash memory.

FIG. 1

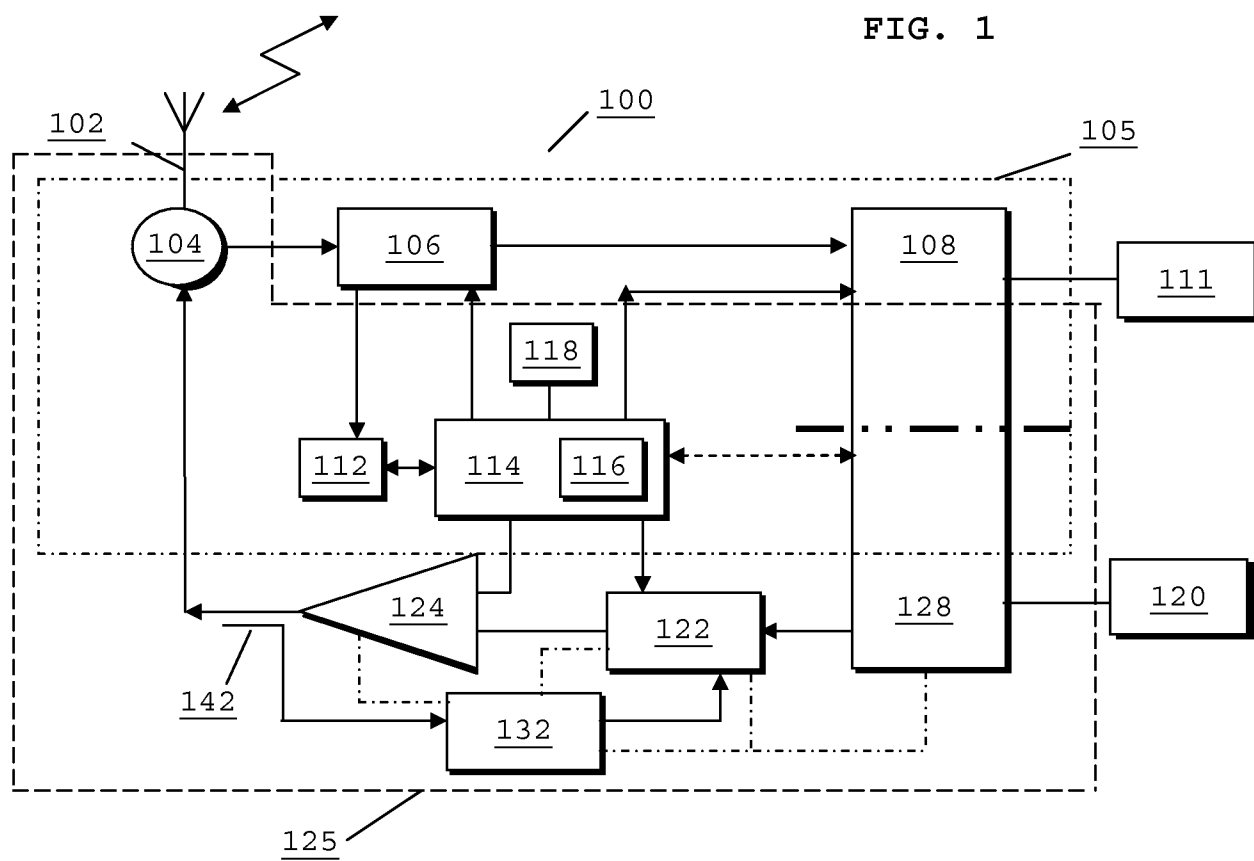
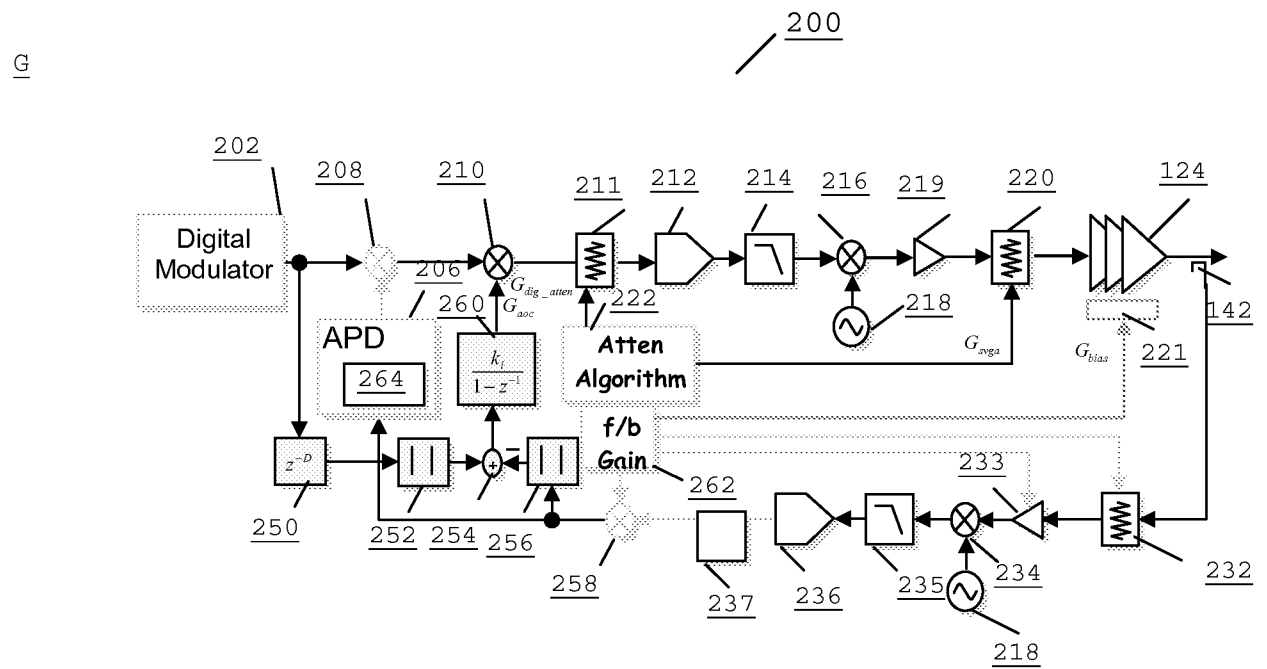


FIG. 2



3/5

FIG. 3

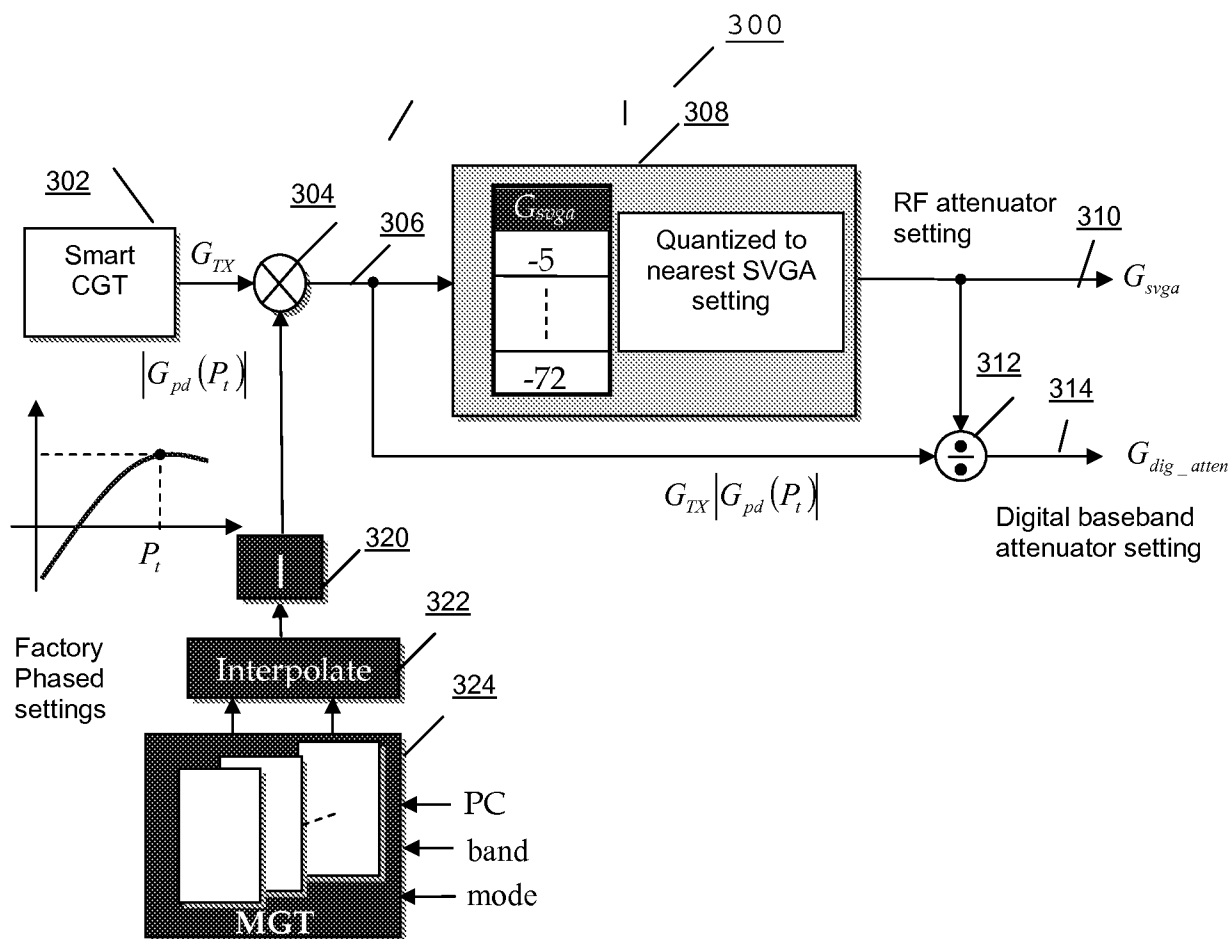
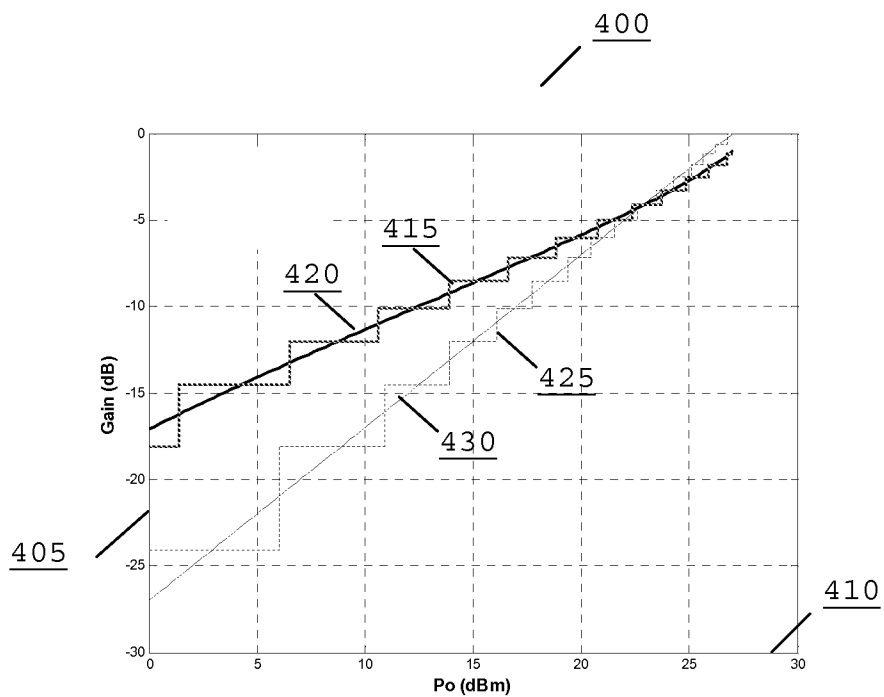
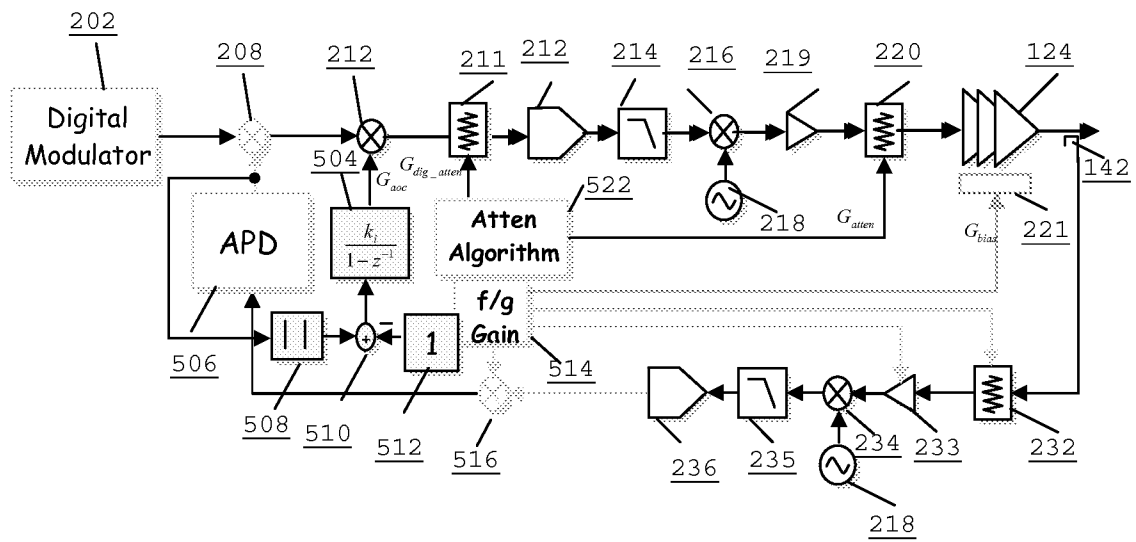


FIG. 4

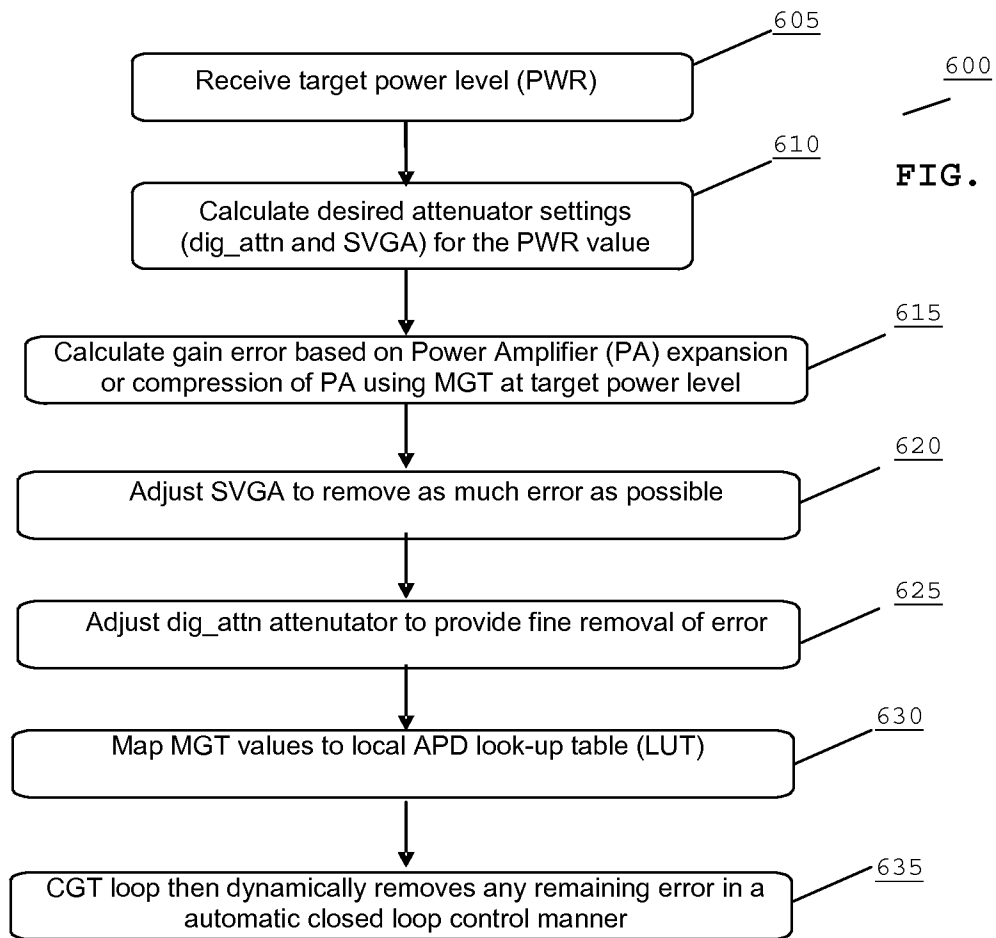


500

FIG. 5



5/5



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/053875

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01/05026 A (DATUM TELEGRAPHIC INC [CA]) 18 January 2001 (2001-01-18) page 62, line 23 - page 63, line 10; figure 51	1-3,7-11
A	EP 1 681 771 A (NORTHROP GRUMMAN CORP [US]) 19 July 2006 (2006-07-19) the whole document	1-10
A	US 7 058 369 B1 (WRIGHT ANDREW S [CA] ET AL) 6 June 2006 (2006-06-06) column 12, line 5 - column 13, line 50; figure 5	1-10
A	US 2007/287393 A1 (NANDIPAKU SANJAY [US] ET AL) 13 December 2007 (2007-12-13) the whole document	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- * & * document member of the same patent family

Date of the actual completion of the international search

9 April 2009

Date of mailing of the international search report

07/05/2009

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Kurzbauer, Werner

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2008/053875

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
WO 0105026	A	18-01-2001	AT 276603 T	15-10-2004
			AU 6009400 A	30-01-2001
			DE 60013852 D1	21-10-2004
			EP 1203445 A1	08-05-2002
			EP 1280273 A2	29-01-2003
			US 6798843 B1	28-09-2004
EP 1681771	A	19-07-2006	US 2006158254 A1	20-07-2006
US 7058369	B1	06-06-2006	US 7260365 B1	21-08-2007
			US 7200367 B1	03-04-2007
			US 7177603 B1	13-02-2007
			US 7340223 B1	04-03-2008
			US 7295815 B1	13-11-2007
US 2007287393	A1	13-12-2007	CN 101361264 A	04-02-2009
			EP 2027649 A2	25-02-2009
			WO 2007146691 A2	21-12-2007