A programmable phase change material (PCM) structure includes a heater element formed at a transistor gate level of a semiconductor device, the heater element further including a pair of electrodes connected by a thin wire structure with respect to the electrodes, the heater element configured to receive programming current passed there through, a layer of phase change material disposed on top of a portion of the thin wire structure, and sensing circuitry configured to sense the resistance of the phase change material.
Fig. 1
(Prior Art)
Fig. 7(a)
Fig. 8(a)  
(Prior Art)

Fig. 8(b)  
(Prior Art)
<table>
<thead>
<tr>
<th>Silicide Property</th>
<th>C54-TiSi₂</th>
<th>CoSi₂</th>
<th>NiSi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thin Film Resistivity (μΩ·cm)</td>
<td>15-25</td>
<td>15-20</td>
<td>10-25</td>
</tr>
<tr>
<td>Silicide Thickness / Si consumption—normalized to metal thickness</td>
<td>2.4 / 2.3</td>
<td>3.5 / 3.6</td>
<td>2.2 / 1.8</td>
</tr>
<tr>
<td>Melting temperature (°C)</td>
<td>1500</td>
<td>1326</td>
<td>992</td>
</tr>
<tr>
<td>Formation Temperature (°C)</td>
<td>750-850</td>
<td>600-750</td>
<td>300-500</td>
</tr>
<tr>
<td>Controlling Formation mechanism</td>
<td>Nucleation</td>
<td>Nucleation / Diffusion</td>
<td>Diffusion</td>
</tr>
<tr>
<td>Diffusing Species</td>
<td>Si</td>
<td>Si &amp; Co (a)</td>
<td>Ni</td>
</tr>
<tr>
<td>Limitations</td>
<td>Transformation C49 → C54</td>
<td>Rise in Rs of narrow lines, roughness, SiGe</td>
<td>High temperature degradation</td>
</tr>
</tbody>
</table>

(a) Co for Co₂Si, Si for CoSi and Co for CoSi₂ if formed at low T. For CoSi₂ at high temperature, both elements diffuse similarly.

Fig. 10
(Prior Art)
PROGRAMMABLE FUSE/NON-VOLATILE MEMORY STRUCTURES USING EXTERNALLY HEATED PHASE CHANGE MATERIAL

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of U.S. patent application Ser. No. 11/672,110, filed Feb. 7, 2007, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present invention relates generally to integrated circuit devices and, more particularly, to programmable fuse/non-volatile memory structures (and arrays) using externally heated phase change material.

[0003] Electrically programmable fuse (eFUSE) devices have many practical applications such as, for example, redundancy implementation in memory arrays, field programmable arrays, voltage trimming resistors/capacitors, RF circuit tuning, electronic chip identification, usage tracking/diagnostic data logging, remote disabling of a device/car that is reported stolen, read only memory (ROM), etc. Existing eFUSE technology is based on various different techniques such as, for example, electromigration (IBM), rupture (Infinion) and agglomeration (Intel). However, each of these existing fuse technologies are "one-shot," in that once the fuse is blown, it cannot be returned to a conducting state. Moreover, such devices occupy relatively large areas, involve large amounts of power/current, and are very slow to program (e.g., several microseconds).

[0004] On the other hand, reprogrammable fuses utilizing chalcogenide materials (and indirect heating through a resistive heater) are described in U.S. Pat. No. 6,448,576 to Davis et al. However, such chalcogenide fuse materials emit large amounts of heat, and it is estimated that switching currents needed to produce the required heating heat are on the order of about 15 mA. Under this assumption, a required heater current of 15 mA would in turn result in a design that is inconveniently large, requiring a driver FET width on the order of about 15 microns.

[0005] Accordingly, as eFUSE technology develops, it will be desirable to be able to address existing concerns pertaining to higher performance, including factors such as: reducing the device area taken up by the fuse, cope with the "sunsetting" of the non-standard high voltages/currents required by existing programmable fuse devices, the desirability of having multi-shot reprogrammable fuses, and enhanced speed, among other aspects.

SUMMARY

[0006] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a programmable phase change material (PCM) structure. In an exemplary embodiment, the structure includes a heater element formed in a transistor gate level of a semiconductor device, the heater element further including a pair of electrodes connected by a thin wire structure with respect to the electrodes, the heater element configured to receive programming current passed therethrough, a layer of phase change material disposed on top of a portion of the thin wire structure, and sensing circuitry configured to sense the resistance of the phase change material.

[0007] In another embodiment, a non-volatile, programmable phase change material (PCM) memory array includes a plurality of memory cells arranged in rows and columns, with each memory cell comprising a heater element formed at a transistor gate level of a semiconductor device; the heater element further including a pair of electrodes connected by a thin wire structure with respect to the electrodes; the heater element configured to receive programming current passed therethrough; a layer of phase change material disposed on top of a portion of the thin wire structure; and sensing circuitry configured to sense the resistance of the phase change material.

[0008] In still another embodiment, a method of forming a programmable phase change material (PCM) structure includes forming a polysilicon layer over a semiconductor substrate, at a location corresponding to a transistor gate level of a semiconductor device; patterning the polysilicon layer so as to define a pair of electrodes and a thin wire structure connecting the electrodes; forming a silicide metal layer over the patterned polysilicon layer so as to define a heater element; and forming a layer of phase change material disposed on top of a portion of the thin wire structure of the heater element; wherein the portions of the silicide metal layer corresponding to the thin wire structure in contact with a portion of the phase change material are configured to selectively heat the portion of phase change material in a manner that programs the phase change material into one of a low resistance crystalline state and a high resistance amorphous state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Referring to the exemplary drawings wherein like elements are numbered alike in the several Figures:

[0010] FIG. 1 is a graph illustrating the exemplary thermal cycling operations of a phase change material;

[0011] FIGS. 2(a) through 2(c) are top and cross-sectional views of a programmable eFUSE device using an externally heated PCM, formed at the gate-level of device processing, in accordance with an embodiment of the invention;

[0012] FIGS. 3 and 4 are schematic diagrams illustrating the operation of the programmable eFUSE structure of FIG. 2, in conjunction with an exemplary sensing circuit, in accordance with a further embodiment of the invention;

[0013] FIGS. 5(a) through 5(c) are top and cross-sectional views of a non-volatile memory cell using an externally heated PCM, formed at the gate-level of device processing, in accordance with a further embodiment of the invention;

[0014] FIG. 6 is a schematic diagram illustrating the operation of the non-volatile memory cell of FIG. 5;

[0015] FIG. 7(a) is a schematic diagram illustrating an array of non-volatile memory cells using an externally heated PCM and associated sensing circuitry, in accordance with a further embodiment of the invention;

[0016] FIGS. 7(b) and 7(c) are alternative embodiments of the sensing circuitry for an array of non-volatile memory cells;

[0017] FIG. 8(a) is a graph illustrating the thermal conductivity properties of silicon as a function of temperature;

[0018] FIG. 8(6) is a graph illustrating the relationship of heater resistance as a function of heater temperature;
FIGS. 9(a) and 9(b) illustrate temperature contours resulting from a PCM heating simulation of a device similar to the embodiment of FIG. 2.

FIG. 10 is a table listing properties of various silicide metals used in CMOS processing.

FIGS. 11 through 14 are top and cross-sectional views illustrating a more detailed, sequential description of an exemplary method of forming the device of FIG. 2.

Detailed Description

Disclosed herein are electrically reprogrammable fuse (eFUSE) devices and non-volatile memory structures such as Phase Change Random Access Memory ("PCM") also referred to as "PRAM"), as well as arrays thereof using externally heated, phase change material. Such devices may be advantageously integrated in a gate-level of device formation (i.e., at the front-end-of-line), thereby involving minimal changes to standard CMOS processing technology.

Certain phase change materials (such as Ge—Sb—Te (GST) alloys) have a programmable electrical resistance that changes with temperature. Other compositions such as GeSbTe, (including substitution/addition of other elements) are also possible for the phase change materials. Individual phase change elements (PCE) are thus used as programmable eFUSEs or as the storage cells of a memory device. The state of an individual PCE is programmed through a heating and cooling process which is electrically controlled by passing a current through the PCE (or a discrete heating element in proximity to the PCE) and the resulting ohmic heating that occurs. Depending upon the specific applied temperature and duration of heating applied to the PCE element, the structure is either "set" to a lower resistance crystalline state or "reset" to an amorphous, higher resistance state. Essentially, there is no practical limit to the number of times a PCE element may be programmed from the crystalline state to the amorphous state and vice versa.

The changing of the phase of a PCE typically requires a high temperature (e.g., considerably above the PCM melting temperature of about 600°C), as can be obtained by Joule heating from current flowing through the phase change material or discrete resistor. When the phase change material is heated above its melting temperature to thereafter be quickly cooled, the phase change material becomes amorphous to result in a severed electrical connection in the case of an eFUSE, or to store a data bit of one logical value in the case of a memory element. Alternatively, when the phase change material is heated above its crystallization temperature and maintained at that temperature for a predetermined time before cooling, the phase change material becomes crystalline to result in a restored electrical connection in the case of an eFUSE, or to store a data bit of the opposite logical value in the case of a memory element.

More specifically, FIG. 1 is a graph illustrating the exemplary thermal cycling operations of a phase change material. As is illustrated, a first thermal cycling operation includes a "RESET" pulse for converting the PCM from crystalline to amorphous form, and a second thermal cycling operation includes a "SET" pulse for converting the PCM from amorphous to crystalline form. During the RESET pulse, the temperature of the PCM is raised above its melting temperature (T_m), followed by a rapid quench over a short time t_1. As a result of the rapid quench, the disordered arrangement of atoms of the PCM due to the melt is retained. Thus, the PCM is left in an amorphous, high resistive state after the RESET pulse. During the SET pulse, the PCM is annealed at a lower temperature with respect to the melting temperature, and for a longer time t_2 with respect to t_1. This process enables the amorphous form to crystallize into a lower resistive state.

From a practical standpoint, some of the design requirements for a PCM-based eFUSE or non-volatile memory device include the capability of functionally perform the SET and RESET operations for a very large number of cycles (e.g., on the order of about 10^11), the capability of reading/sensing the state of the fuses/memories, element, the limitation on the amount of power/current needed to program the PCM, and the need to minimize the cost and time requirements to implement the structure with minimal changes to standard CMOS processing.

Referring now to FIGS. 2(a) through 2(c), there are shown various top and cross-sectional views of a programmable eFUSE device using an externally heated PCM, and which is formed at the gate-level of device processing, in accordance with an embodiment of the invention. In the exemplary single-cell implementation depicted, formation of the eFUSE structure is based upon two gate-level steps in the CMOS process: undoped polycrystalline silicon formation and silicide formation, along with the addition of an additional PCM level and associated vias. The patterned polysilicon (normally used as gate structures in standard CMOS processing) forms a thin wire structure (having a thin silicide layer formed thereupon) connecting two large pads or electrodes. The silicide layer is used as a metalic conductor and forms the heater for the eFUSE device. The PCM is formed so as to overlap the thin wire structure (and silicide material) in a direction transverse thereto. Thus configured, the metallic silicide connects the two electrodes with a low-resistance link, thereby forming the external heater used to program the state of the overlapping PCM. From a thermal standpoint, the polysilicon wire structure is the dominant heat conductor of the external heater structure.

More specifically, FIG. 2(a) is a top view of a programmable eFUSE structure 200, FIG. 2(b) is a cross-sectional view taken along B-B of FIG. 2(a), and FIG. 2(c) is a cross-sectional view taken along C-C of FIG. 2(a). As particularly illustrated in the cross-sectional views of FIGS. 2(b) and 2(c), a substrate 202 (e.g., silicon, silicon-on-insulator, etc.) has an insulating layer 204 formed thereon. During a poly-silicon formation process, polysilicon material formed over the insulating layer 204 is patterned so as to form the heater electrodes 206, as well as the thin wire structure 208 that electrically connects the heater electrodes 206. As also used in CMOS processing, a thin layer of oxide 210 covers the sidewalls of the electrodes 206 and wire structure 208.

As also part of a CMOS process, the polysilicon material is provided with silicide metal contacts for ohmic contact with upper wiring levels. As is known in the art, a silicide layer 212 is formed over polysilicon by deposition of a suitable refractory metal (e.g., cobalt, nickel, titanium, tantalum, tungsten, platinum, erbium, ytterbium, etc.) followed by a high-temperature anneal. The portions of the metal layer in contact with silicon react with the silicon during the anneal to form a conductive silicide metal layer. As this is a self-aligning process with respect to silicon, it is also known in the art as a "salicide" process.

Following the silicide metal formation, a layer of PCM 214 is formed over the heater element in a generally
perpendicular direction with respect to the orientation of the wire structure 208, as best seen in FIG. 2(b). An extended portion 215 of the PCM 214 extends along the insulating layer 204 adjacent the wire structure 208 so as to provide a contact point for the functional portion of the eFUSE device (i.e., a point at which the programmed state of the fuse may be sensed). In particular, the extended portion 215 provides a surface upon which conductive vias 216 may be subsequently defined once an interlevel dielectric (ILD) layer 218 (not shown in FIG. 2(a)) is formed over the structure. Additional vias 216 are also formed on the heater electrodes 206 in order to run heating current through the wire structure 208. Sequential longitudinal views illustrating the formation steps in further detail, as well as exemplary processing conditions, are presented herewith.

[0031] FIG. 3 is a schematic diagram illustrating the operation of the programmable eFUSE structure 200 of FIG. 2, in conjunction with an exemplary sensing circuit 300, in accordance with a further embodiment of the invention. The heater circuit (defined by electrodes 206 and connecting wire structure 208) is connected between a power supply $V_{pp}$ and ground through a programming FET 302, which has a control signal $V_{gate}$ applied to the gate terminal thereof. The PCM layer 214 formed over the wire structure 208 has the extended portion 215 thereof connected (through vias 216) to an input node of a sense inverter 304, as well as to ground through a reference resistor R0.

[0032] In FIG. 3, it is initially assumed that, either through initial formation or specific programming to a crystalline state, the portion of the PCM layer 214 atop the wire structure 218 is in the low resistance state. During sensing of the state of the fuse device 200, FET 302 is deactivated, thus isolating the heater anode from ground. Because the entire PCM layer 214 is in a conductive (low resistance) state, the power supply voltage $V_{pp}$ applied to the heater anode is also coupled to the extended portion 215 of the PCM layer 214, and thus built up across reference resistor R0. Since such a voltage (or other converted voltage suitable for use with the sense logic) represents a logical high voltage at the input node of the inverter 304, the sense output will be a logic low (ground) value.

[0033] In order to convert the PCM layer 214 to the insulating state, the quench or RESET operation, the programming transistor 302 (e.g., an NFET) is activated by a relatively high input voltage on $V_{gate}$ to deliver a high current, followed by a rapid shut off of the transistor 302. Upon turning off the current through the heater, heat is rapidly conducted away from the silicidate material 212 and PCM layer 214, through the polysilicon, resulting in a quench of the PCM 214. Accordingly, as a result of such a RESET operation, the portion of the PCM layer 214 in proximity to the silicide heater (shown in differing shading in FIG. 4) is converted to the amorphous, high resistance state. In this case, since the current path between the power supply $V_{pp}$ and the PCM terminal (extended portion 215) is now blocked, the voltage on the input of the inverter 304 will discharge to ground through R0, thereby driving the sense output high.

[0034] Conversely, in order to restore the PCM layer 214 back to the conducting state, the anneal or SET operation is implemented by turning on transistor 302 with a relatively low input voltage on $V_{gate}$ to deliver a lower current with respect to the RESET operation, and thereafter shutting off transistor 302. The high resistance portion of the PCM layer 214 is annealed back to the low resistance, crystalline state shown in FIG. 3, thereby restoring the electrical connection between the PCM terminal (extended portion 215) and the power supply $V_{pp}$. The voltage of the inverter input node across R0 goes high, and the sense output is driven back to a low value.

[0035] As indicated above, in addition to reprogrammable eFUSEs, the structure of FIG. 2 can also be used as a non-volatile memory storage cell, such as for a PRAM device. Accordingly, FIGS. 5(a) through 5(c) illustrate various top and cross-sectional views of a non-volatile memory cell using an externally heated PCM, and which is formed at the gate-level of device processing, in accordance with a further embodiment of the invention. As will be noted, in comparison with the eFUSE embodiment of FIG. 2, the memory cell 500 in FIGS. 5(a) through 5(c) includes a substantially similar heater and PCM layer configuration, with the addition of a programming transistor 502 in series with one of the heater electrodes 206.

[0036] In particular, the programming transistor 502 includes a polysilicon gate conductor 504 formed over a gate insulating layer 506, which is in turn formed over a non-insulated portion of the substrate 202. Integration of the programming transistor is fairly straightforward with respect to CMOS processing, including doping of the source/drain regions 508. It is noted that during silicidation, silicide contacts 212 are also formed over the silicon containing gate conductor 504 and source/drain regions 508. Also illustrated in FIGS. 5(a) through 5(c) is a first wiring layer 510 that is used, for example, to connect the programming transistor to one of the heater electrodes 206, as well as to connect the other heater electrode to the power source and connect the PCM layer 214 to the associated sense circuitry.

[0037] In contrast to the eFUSE embodiment, the sense circuitry associated with the non-volatile memory cell 500 does not typically rely on the heater supply voltage to supply an input signal thereto. This is schematically depicted in the schematic diagram of FIG. 6, wherein it will be noted that the power supply voltage $V_{pp}$ is separate from the sensing voltage, $V_s$, which is used as the input to the sense circuitry (not shown in FIG. 6). Generally speaking, to sense the state of the PCM memory cell, a non-zero voltage is applied to $V_s$ (the sense terminal) and the gate of the programming transistor 502 is pulsed. The amount of current flowing through the PCM resistor, $R_V$, is dependent on the state of the PCM (i.e., low when it is in the low resistance crystalline state, and very low when it is in the high resistance amorphous state).

[0038] Referring generally to FIGS. 7(a) through 7(c), various embodiments of sensing circuitry for an array of PCM memory cells such as shown in FIG. 5 are depicted. For purposes of simplicity, the arrays are depicted as 2x2; however, it will be appreciated that the principles described herein are applicable to larger arrays.

[0039] FIG. 7(a) illustrates an exemplary sense array circuit 700. In addition to the programming transistors 702, each cell includes an additional sense transistor 704 configured to pass a lower current with respect to the programming transistor 702. This configuration prevents current from circulating between the program lines (PA, PB, etc.) and the sense lines (SA, SB, etc.) through non-selected cells in a given column. As also shown in FIG. 7(a), an adjustable power supply $V_{pp}$ ($V_{ppA}, V_{ppB}$, etc.), and a fixed power supply $708$ ($V_{sa}, V_{sB}$, etc.) is provided for each column, as is a sense current amplifier 710. These devices are connected to the column lines by switches PA, PB, etc., and SA, SB, etc. It will be noted that, for any of the sense circuit embodiments, the power supplies
(e.g., both the adjustable and fixed power supplies 706, 708) may be located on the same circuit board as the sense array circuit 700, or they may be located on a different component altogether. In the latter instance, the off-chip sources would be coupled to corresponding power source nodes on the chip containing the sense array circuit 700.

[0040] In order to program a cell (for example, in column A) the PA switches are closed and the SA switches are opened. A programming (high) voltage is thus applied by the adjustable power supply 706 to the appropriate Vp line connected to the cell, and the gate line (e.g., Vg1, Vg2, etc.) corresponding to the cell to be programmed is pulsed. The magnitude and duration of the pulse is selected between one having a low magnitude and slow ramp down (e.g., low resistance for writing a logical 0) and one having a large magnitude and fast ramp down (e.g., high resistance for writing a logical 1). Optionally, programming can be done for all 0's or all 1's on the same gate line at the same time. In order to sense the state of an array cell, a low voltage (below the programming threshold) is applied to the corresponding Vp line (A, B, etc.) connected to the cell, followed by pulsing the gate line for the cell. A parallel output of all cells attached to the selected gate line is coupled to the corresponding current sense output 710, thus generating, for example, Sense_out_A.

[0045] Notwithstanding the particular application of a PCM device as discussed above (e.g., reprogrammable eFUSE, non-volatile PRAM, etc.), certain key aspects of the operation of a PCM device include the quench time and the quench (RESET) power. For example, the quench time must be short (e.g., on a nanosecond time scale), in order for the melted PCM material to cool to the amorphous state rather than recrystallizing. The power required to melt the material is supplied through a programming transistor, and the length of this transistor scales in accordance with the programming current supplied thereby. In addition, the transistor width is a major factor in the area per stored memory bit. Thus, minimizing programming power is a key factor in minimizing the area per bit.

3D Simulations of Heat Flow

[0046] Thermal simulations are based on solving the thermal diffusion equation:

$$\frac{C_p \partial T}{\partial t} = \nabla \cdot (K \nabla T)$$

[0047] for the temperature T(\(r, t\)), with specific heat at constant volume, C_p, diffusion coefficient, K(\(r\)), and heating rate, H(\(r, t\)). Since the high thermal conductivity of the silicon wire plays a key role in both the thermal time constant and in the required power, it is important to take into account the substantial decrease in this thermal conductivity with increasing temperature, as reflected in the graph of FIG. 8(a). The approximate T-dependence of K over the operating temperature region is given by the expression K = 2113/(T1.258 W/cm K. The heating rate depends on current through the heater resistance, which is also temperature dependent, with the approximate behavior expressed by R = 144+0.35(T)(\(\Omega\)), as shown in FIG. 8(b). Elsewhere, the conductivity and heat capacity are constant and typical for the corresponding materials.

[0048] Referring now to FIGS. 9(a) and 9(b), the results of a 3D simulation of a gate-level PCM eFUSE 900 similar to the embodiment of FIG 2 are illustrated. The cross-sectional view of FIG. 9(a) corresponds to the view seen in FIG. 2(c), while the cross-sectional view of FIG. 9(b) generally corresponds to the view seen in FIG. 2(b). In the specific simulation illustrated, the eFUSE device 900 measured 1.28x 0.58x0.38 mm^3. The cathode and anode in-plane dimensions are 0.3x0.3 mm^2, and the silicide strip (wire structure 208) connecting them is 0.40 microns long and 0.03 microns thick. The PCM 214 is 0.12 microns wide parallel to the silicide strip portion of the wire structure 208, and 0.05 microns thick. For constant current inside the silicide strip, the resistance R = 144+0.35(T) causes the heating rate to vary with temperature in the same manner.

[0049] In the simulations depicted, a temperature dependent heating rate was applied to the silicide for 34 ns, followed by a zero heating rate for an additional 6 ns. The temperature increases at all locations of the device during the heating, causing the melting of all portions of the PCM 214 in contact with the silicide 212. Once the heating rate drops to zero, the temperature correspondingly decreases at all loca-
tions, but in particular, the temperature in the PCM 214 drops very suddenly (to below the melting temperature) within about 1 ns. This is fast enough to quench the PCM and render it non-conducting.

In particular, FIGS. 9(a) and 9(b) depict the temperature distribution just before quenching with an outer temperature contour 904 at about 255°C and an inner temperature contour 902 at the PCM melting temperature, assumed to be 607°C. At this point, all of the PCM within the inner temperature contour 902 is melted. The average power input to the silicide during the heating phase is 2.4 mW. The peak temperature after 34 ns is about 847°C, which sufficiently low to preserve the integrity of the materials. Various other designs, dimensions, and heating rates were simulated as well, demonstrating the desired PCM melting temperatures with reasonably low applied power levels and low peak temperatures in the silicide material.

Materials Issues

In a physical implementation of the disclosed embodiments of the eFUSE and memory cell shown in FIGS. 2 and 5, the silicide material used in forming conductive contacts for FET devices at the substrate level is also used to form the electrodes and wire structure of the heater circuit. An exemplary process of record utilizes nickel mono-silicide (NiSi) doped with about 5% Pt as silicide metal. However, other di-silicide materials, such as CoSi2 or TiSi2, for example, may need to be considered, depending on the required power/temperature rise during the quench/annel cycle. In the case of CoSi2 or TiSi2, existing processes of record for silicide contact formation are also available for ease of integration of the PCM devices into CMOS processing. The relative advantages or disadvantages of these different silicides are illustrated in FIG. 10.

Of the three silicides listed in FIG. 10, the melting temperature of NiSi is the lowest (less than 1000°C), while that of TiSi2 is the highest. The silicide stability at high temperatures (and thus the integrity of the heater/PCM interface during the quench/annel cycle) affects the capability of maximizing the multishot (reprogrammability) feature of the eFUSE/memory cell. As such, it is also contemplated that multiple silicide phases having different resistivities may be formed. However, changing silicide resistivity may be problematic in terms of controlling and managing power inputs during the quench/annel cycles.

With regard to NiSi, certain challenges include more complex phase formation (multiple metal rich phases), the possibility of forming higher resistivity NiSi2 in BEOL anneals, and lower morphological stability. On the other hand, one advantage of NiSi is that it addresses the absence of voiding in narrow polysilicon lines, provided that measures are taken to prevent other silicide phases from forming. This may be achieved by an additional doping (e.g., Re, Rh or Hf, in addition to Pt). Rutherford Backscattering Spectroscopy (RBS) analysis of a GST-225/NiSi (5% Pt) interface indicates stable at least up to about 505°C. This is in part due to a thin native (about 25 Å) SiO2 layer on the surface of the silicide, which acts as a (inter) diffusion barrier. By adding a thin Ti layer at the interface to form GST-225/TiNiSi (5% Pt) stack, some interface reaction is taking place, since Ti is a highly effective oxygen getter (by reducing the SiO2 on the NiSi and/or diffusing into the GST). To maintain the integrity of the interface at high temperatures, a barrier layer of nitride or oxide may be used.

Manufacture

Finally, FIGS. 11 through 14 are top and cross-sectional views illustrating a more detailed, sequential description of an exemplary method of forming the eFUSE device of FIG. 2. As indicated previously, the structures in FIGS. 11(a) through 11(c) are formed in conformance with standard CMOS processing. First, the active areas are defined by forming the STI regions 204 on the substrate. The heating element, comprising the anode, cathode (electrodes 206) and the heater link (wire structure 208) is formed during the polysilicon conductor formation process (material deposition, lithographic patterning and etching) and the subsequent nitride spacer formation process.

FIGS. 12(a) through 12(c) illustrate the device as a result of the salicidation process. In an exemplary embodiment, the device is wet cleaned using 40:1 BHF (buffered hydrofluoric acid) for 45 seconds prior to the sputter deposition of about 8 nm of a NiPt alloy (95% Ni, 5% Pt) and 5 nm of TiN as a salicidation metal material. A short time anneal of about 5 seconds is used to react the Pt+ polysilicon (120 nm) with the deposited NiPt (8 nm) to form about 16 nm NiPt (95% Ni, 5% Pt) silicide layer 212. The unreacted NiPt metal is removed by etching in aqua regia (a mixture of 5 parts concentrated (37%) hydrochloric acid, 1 part concentrated (70%) nitric acid, and 4 parts deionized water) for several minutes. A second, longer duration homogenization anneal completes the salicidation at about 500°C.

In FIGS. 13(a) through 13(c), an additional process for deposition and patterning of the PCM material 214 (e.g., GST) is shown. In FIGS. 14(a) through 14(c), the device is shown after MOL (middle of the line) dielectric deposition 218 and contact (via 216) formation. As known in the art, contact formation is implemented through lithographic patterning and etching of dielectric layer 218, followed by damascene metal (e.g., W) deposition and planarization. Subsequent processing is thereafter continued in accordance with standard logic processing techniques.

While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A programmable phase change material (PCM) structure, comprising:
a heater element formed at a transistor gate level of a semiconductor device;
the heater element further including a pair of electrodes connected by a thin wire structure with respect to the electrodes, the heater element configured to receive programming current passed therethrough;
a layer of phase change material disposed on top of a portion of the thin wire structure; and sensing circuitry configured to sense the resistance of the phase change material.

2. The programmable PCM structure of claim 1, where the sensing circuitry further comprises an input node coupled to an extended portion of the phase change material not in direct contact with the thin wire structure.

3. The programmable PCM structure of claim 2, wherein the sensing circuitry further comprises a reference resistor coupled to the input node such that the input node is discharged to ground when a portion of the phase change material formed on the thin wire structure is programmed to a high resistance state.

4. The programmable PCM structure of claim 3, wherein the input node is maintained at a logic high voltage through coupling to a heater power source when a portion of the phase change material formed on the thin wire structure is programmed to a low resistance state.

5. A non-volatile, programmable phase change material (PCM) memory array, comprising: a plurality of memory cells arranged in rows and columns, with each memory cell comprising a heater element formed at a transistor gate level of a semiconductor device; the heater element further including a pair of electrodes connected by a thin wire structure with respect to the electrodes the heater element configured to receive programming current passed therethrough; a layer of phase change material disposed on top of a portion of the thin wire structure; and sensing circuitry configured to sense the resistance of the phase change material.

6. The memory array of claim 5, wherein the sensing circuitry further comprises: a program line corresponding to each column, the program line configured for selective coupling to an adjustable power source; a programming transistor for each cell, the programming transistor connected in series between the cell heater element and the program line, wherein the programming transistor is activated by a signal applied to a gate line corresponding to a given row; and a sense line corresponding to each column, the sense line configured for selective coupling to a fixed power source; wherein an extended portion of the phase change material not in direct contact with the thin wire structure is configured to receive a sensing voltage applied thereto, the sensing voltage originating from the fixed power source.

7. The memory array of claim 6, wherein each cell further comprises a sense transistor connected in series between the extended portion of the phase change material and the sense line, wherein the sense transistor is activated by a signal applied to the gate line of the cell.

8. The memory array of claim 6, wherein each row further comprises a peripherally located sense transistor which selectively connects each of the heater elements in the row to ground, wherein the sense transistor is activated by a signal applied to the gate line of the row.

9. The memory array of claim 6, wherein a selected cell is programmed through application of a programming voltage to the associated program line and pulsing of the gate line coupled to the programming transistor of the cell, wherein the magnitude and duration of the gate line pulse is selected between one of: a lower magnitude and slower ramp down, and a larger magnitude and faster ramp down, depending upon the logical state of the bit to be programmed into the cell.

10. The memory array of claim 9, wherein a selected cell is sensed through application of a sensing voltage to the associated sense line and pulsing of the gate line coupled to the programming transistor of the cell, wherein the magnitude of current sensed on the programming line corresponds to the logical state of the selected cell, and wherein the sensing voltage is less than a threshold level of the programming voltage.

11. The memory array of claim 5, wherein the sensing circuitry further comprises: a program line corresponding to each column, the program line configured for selective coupling to an adjustable power source; a programming transistor for each cell, the programming transistor connected in series between the cell heater element and ground, wherein the programming transistor is activated by a signal applied to a gate line corresponding to a given row; and a reference resistor connected in parallel with the program line, and in series between an extended portion of the phase change material of each cell of the column and a power source node of the adjustable power source; wherein the resistance value of the reference resistor is selected so as to apply a sensing voltage to the phase change material of each cell of the column.

12. The memory array of claim 11, wherein the resistance value, r, of the reference resistor is selected in accordance with the expression: $r = (R_v + R_h)/N$; wherein $R_v$ represents a low resistance value of the phase change material in a crystalline state, $R_h$ represents the resistance value of the heater element, and $N$ is the total number of rows in the array.

13. The memory array of claim 12, wherein $r$ is from about 1 to about 100 ohms.

14. The memory array of claim 11, wherein a selected cell is programmed through application of a programming voltage to the associated program line and pulsing of the gate line coupled to the programming transistor of the cell, wherein the magnitude and duration of the gate line pulse is selected between one of: a lower magnitude and slower ramp down, and a larger magnitude and faster ramp down, depending upon the logical state of the bit to be programmed into the cell.

15. The memory array of claim 14, wherein a selected cell is sensed through pulsing of the gate line coupled to the programming transistor of the cell, wherein the magnitude of current through the sense resistor corresponds to the logical state of the selected cell, and wherein the sensing voltage is less than a threshold level of the programming voltage.