(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 July 2017 (06.07.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/117362 A2

(51) International Patent Classification:
H01Q 1/22 (2006.01) *H01Q 13/20* (2006.01)

(21) International Application Number:
PCT/US2016/069137

(22) International Filing Date:
29 December 2016 (29.12.2016)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/982,932 29 December 2015 (29.12.2015) US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:
US 14/982,932 (CON)
Filed on 29 December 2015 (29.12.2015)

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku Tokyo 160-8366 (JP).

(72) Inventors: **COOK, Benjamin, Stassen**; 8749 Southwestern Blvd., Dallas, TX 75206 (US). **SANKARAN, Swaminathan**; 1037 Everglades Drive, Allen, TX 75013 (US).

(74) Agent: **DAVIS, Michael A., Jr.**; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR BACKSIDE INTEGRATED CIRCUIT HIGH FREQUENCY SIGNAL RADIATION, RECEPTION AND INTERCONNECTS

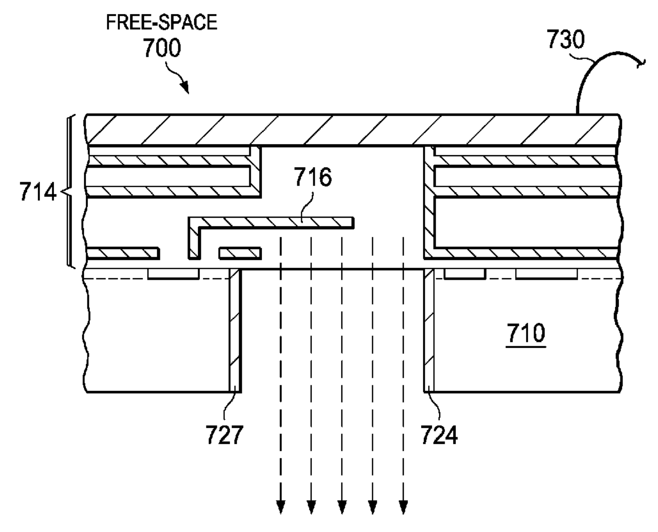


FIG. 7A

(57) Abstract: In described examples of apparatus (700), a semiconductor substrate (710) has a front side surface and a backside surface opposing the front side surface. Metal conductors (714) are formed over the front side surface. At least one cavity opening is etched in the backside surface. A radiating or coupling structure (716) is formed in a portion of the metal conductors (714) and configured to radiate signals through the cavity opening in the backside surface.

WO 2017/117362 A2

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

METHODS AND APPARATUS FOR BACKSIDE INTEGRATED CIRCUIT HIGH FREQUENCY SIGNAL RADIATION, RECEPTION AND INTERCONNECTS

[0001] This relates generally to integrated circuits and integrated wave structures, and more particularly to building backside wave structures for high frequency radiation and reception in semiconductor devices.

BACKGROUND

[0002] As used herein, the term “terahertz” covers electromagnetic transmission with wavelengths of approximately 3000 um to 10um corresponding to the range of frequencies from approximately 0.1 THz to approximately 30.0 THz.

[0003] Coupling millimeter wave, sub-THZ and THz signals from an integrated circuit to an antenna or interconnect can be problematic in conventional solutions due to three key issues.

[0004] The first issue involves the losses that occur in back-end materials due to skin depth in metals, and dielectric losses in oxides and nitrides. To achieve high gain antennas, or to form high frequency inter-chip interconnects, large structures are required in the back end processing with respect to wavelength, which greatly increases conductor and dielectric loss.

[0005] The second issue involves surface waves, which are propagating modes which appear when a dielectric on a metal interface is large with respect to the signal wavelength. The surface waves cause signal loss (efficiency loss) in antennas and interconnects. FIGS. 1A and 1B show a graph of the efficiency (shown on the vertical axis of FIG. 1A) where H is the thickness of the dielectric over the top of a metal M1, and the ratio H/lambda_o is shown on the horizontal axis. A typical back end dielectric is 6 microns thick, which is 0.02 (H/lambda_o) at a 1 THz frequency, as shown in FIG. 1A this leads to 10% power loss due to surface waves in patch antennas (similar in a transmission line in the back end). FIG. 1B illustrates the surface wave effects in an example structure showing the energy being transferred as waves along the surface of the dielectric layer, and thus not being efficiently transmitted away from the structure.

[0006] The third issue involves the top level metal structures and dielectric materials typically in use for conventional semiconductor devices. These materials, when used for radiators or coupling structures, are too lossy for the efficient radiation and reception of THz frequency signals.

[0007] In one conventional approach to address at least some problems in Patent No. US 8,450, 687 (“the ‘687 Patent”), an antenna is integrated directly on the integrated circuit (IC). In the ‘687 Patent, an antenna is formed on the IC with the intent of radiating the energy on the circuit side or top-side of the IC, sometimes referred to as the “front” side. The antenna structure described in the ‘687 Patent is formed in a manner that lowers production costs over prior approaches, in that the antenna build can be incorporated into the IC building process, thus saving additional costs of micromachining as in prior approaches. Another feature of the approach of the ‘687 Patent is that the antenna used improves the radiating efficiency over conventional planar styled integrated antennas. However, additional problems remain.

[0008] FIGS. 2A and 2B illustrate a conventional top-side antenna built within an IC fabrication system. In FIG. 2A, a cross-sectional view 200 shows a semiconductor substrate 210a, the doped surface region forming an active area 212, and the metal conductor stack 214. Within the metal conductor stack, a ground plane 220a and an antenna 222a are formed with the antenna 222a at the uppermost portion of the metal conductor stack 214. The metal conductor stack 214 can be formed from a multiple level metal structure with conductors formed at levels separated by dielectric layers such as are formed over the surface of semiconductor substrates in integrated circuit fabrication. In FIG. 2B, a top view 202 of this structure is illustrated again showing the semiconductor substrate 210b, the ground plane 220b and the antenna structure 222b. Also, a number of bond pads 224 and bond wires 230 are shown to help illustrate that this antenna structure is formed on the top or circuit side of a semiconductor substrate such as a silicon, silicon germanium, gallium arsenide or other semiconductor wafer. With the antenna 222a formed on the top-side of the semiconductor substrate, the energy radiates upwards away from the top side of the wafer or substrate 210b.

[0009] FIG. 3 shows a conventional top-side antenna 300 (such as shown in FIGS. 2A and 2B) in operation radiating signals, and a corresponding balloon graph 340. FIG. 3 shows an arrangement 300 including a wafer or semiconductor substrate 310, a top-side antenna 322, bond pads 324 and bond wires 330. The balloon graph 340 represents the simulated energy radiated by the top-side antenna 322 in operation. In this arrangement 300, the peak gain was found in simulations to be approximately 7 dB as indicated by the graph scale 342 in FIG. 3 and the balloon graph 340.

[0010] Continuing improvements are therefore needed for methods and for couplers or antennas that are compatible with commercial semiconductor processes and that can efficiently transmit and receive signals at THz and sub-THz frequencies. A higher gain antenna is desirable with ability to more efficiently couple the radiated energy to other THz components.

SUMMARY

[0011] In described examples of apparatus, a semiconductor substrate has a front side surface and a backside surface opposing the front side surface. Metal conductors are formed over the front side surface. At least one cavity opening is etched in the backside surface. A radiating or coupling structure is formed in a portion of the metal conductors and configured to radiate signals through the cavity opening in the backside surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIGS. 1A and 1B illustrate signal efficiency showing losses in a conventional structure with a surface wave effect.

[0013] FIGS. 2A and 2B illustrate a conventional top-side antenna integrated with an IC.

[0014] FIG. 3 shows a conventional top-side antenna and a balloon graph illustrating signal strength radiated from the antenna.

[0015] FIGS. 4A, 4B and 4C illustrate an antenna arrangement built within a CMOS process with a cavity formed in the backside of a semiconductor substrate.

[0016] FIGS. 5A, 5B and 5C illustrate another antenna arrangement built with a waveguide formed in the backside of a semiconductor substrate.

[0017] FIG. 6 shows a balloon graph indicating energy radiated by a backside antenna in a system.

[0018] FIGS. 7A, 7B, 7C and 7D show different views of an antenna and waveguide formed in the backside of a semiconductor substrate to illustrate several example arrangements.

[0019] FIGS. 8A, 8B and 8C show cross-sectional views of additional arrangements for antennas and cavities formed on the backside of a semiconductor substrate.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are not necessarily drawn to scale.

[0021] Example embodiments expand an ability to efficiently radiate and detect THz frequency radiated energy from radiators or coupling structures fabricated on integrated circuits, wafers or semiconductor substrates.

[0022] In this description, the term “coupled” includes “directly connected” and connections made with intervening elements. Additional elements and various connections may be used between any elements that are described as "coupled."

[0023] In described examples, an integrated antenna will provide sub-THz and THz radiation for receiving or transmission directed from the backside of a semiconductor substrate or wafer by building the antenna portion with a cavity formed on the backside of the IC.

[0024] Building the antenna within the backside of the substrate allows for uniform parallel orientation of the radiating structure to the ground plane, with accurate spacing between the radiator and a ground plane reflector which intensifies the radiated signal, improving the gain. Also, example embodiments provide antennas and coupling structures for high frequency signals that are mechanically robust and compatible with existing semiconductor fabrication processes.

[0025] Further, example embodiments include waveguides within a wafer or substrate, enabling an efficient coupling of the THz energy to other ICs, to packages, to redistribution layers, to waveguides, or to other points on the same IC.

[0026] At least one example embodiment includes a structure that inverts the antenna structure to radiate energy out of the backside of a semiconductor substrate or wafer. In various arrangements, different etching techniques and processes are used to form various cavities or waveguides in the back side of the wafer or semiconductor substrate and are arranged underneath and proximal to the antenna or coupling structure in different patterns. Example embodiments improve the gain characteristics of the radiated energy over conventional approaches. Also, example embodiments enable additional coupling structures and transmission methods that are not available in conventional approaches to fabricating sub-THz and THz antennas. Example embodiments provide coupling structures for guiding THz signals from one point to another in a non-radiating, waveguide structure. Because the antenna or coupling structure is formed on the backside of the wafer, the losses incurred by conventional top side antennas are avoided. As described hereinbelow, example embodiments achieve further advantages. The cavities can be arranged as waveguides or antenna horns. Redistribution layers or THz beamforming techniques can be achieved by controlling of the spacing between the antenna or coupling structure and electrical or magnetic reflectors, and by varying the shapes of the cavities including by controlled etching of the semiconductor substrate material, and by thinning or controlling the thickness of the semiconductor substrate or wafer. Example embodiments provide an efficient radiator and detector for sub-THz and THz frequency signals that cannot be achieved using conventional approaches. THz signaling using coupling structures and cavities or waveguides can be achieved for on-die, die-to-die, or die-to-package connections at high frequency that were previously unavailable.

[0027] FIGS. 4A-4C illustrate example arrangements of a THz antenna built within a semiconductor process with a cavity opening or waveguide formed in the backside of the wafer substrate. FIG. 4A illustrates a cross-section 400 of a wafer 410a fabricated with conventional CMOS processing with a cavity opening or waveguide 424a. A region 412 at the surface of the substrate 410a can contain active or passive circuit components. In an example arrangement formed using a standard MOS semiconductor process, CMOS components (e.g., active circuitry formed from MOS transistors and, in some arrangements, passive circuitry such as capacitors and resistors) can be formed in active region 412. For example, ion implantation, doping, and diffusion processes can be used to form source and drain regions spaced by a channel to form active MOS devices in region 412. The metal conductor system 414 formed on the surface of the semiconductor substrate 410a contains at least one antenna structure 422a and a corresponding reflecting plane 416a which is separated from the antenna by a distance 420. Other portions of the metal conductor system can be used to couple components formed in or on the wafer, such as transistors and capacitors. The metal conductor system 414 can be formed from multiple level conductors electrically isolated by dielectric layers, such as silicon oxide, silicon nitride, silicon oxynitride, and carbon containing dielectrics. For example, amplifier circuitry can be formed in the active region 412 and can be coupled to the antenna structure 422a, and receiver circuitry can also be formed in the active region 412 and coupled to the antenna 422a for receiving radiated signals.

[0028] Various physical implementations of the antenna 422a are possible where the signal radiates through the cavity opening or waveguide 424a on the backside of the wafer. Two such examples are illustrated in FIGS. 4B and 4C. In FIG. 4B, a bottom view 402 shows an electric field radiator using the metal stack of FIG. 4A. In this example arrangement, a waveguide or cavity opening 424b has been etched into the backside of the wafer substrate 410b at a position corresponding to the antenna 422b. In some additional alternative arrangements, the opening 424b can extend entirely through the semiconductor substrate exposing the antenna to the opening, in other additional arrangements, a portion of the semiconductor substrate 410a or 410b can be retained. In FIG. 4B, 416b illustrates a metal portion of the metal structure formed above (shown beneath the antenna in this bottom view) the antenna 422b which, in this example arrangement, serves as a reflector to direct radiated energy from the antenna 422b out the backside opening. By spacing the reflector formed in metal 416a from the antenna 422a, a constructive interference arrangement can be created. The spacing 420 is determined by the wavelength λ of the signal being radiated. In one arrangement, the reflector 416b is an electrical reflector such as a ground plane, and it will reflect the radiated electromagnetic signals with unity gain and 180 degree phase shift. By spacing the antenna 422a at a distance 420 that corresponds to λ/4, a 90 degree phase shift occurs between the antenna and the reflector 416a. The signal is then reflected with an additional 180 degree phase shift and undergoes another 90 degree phase shift traveling between the reflector 416a/416b and the antenna 422a/422b. In this arrangement the total phase shift is 360 degrees at the antenna, so that the reflected signal is constructively interfering with the radiated signal at the antenna 416a/416b, thus gain is accomplished. The distance 420 can be adjusted for the wavelength (the inverse of the frequency) of the signal being radiated to achieve constructive interference/gain. Achieving gain of THz frequency signals is therefore easily accomplished using example embodiments. This advantageous result is in sharp contrast to conventional approaches, where gain is difficult or impractical to obtain for the sub-Thz and Thz frequencies of interest, so that the radiated signals exhibit loss, and not gain. In the case of a patch antenna arrangement, the radiator can be as close as lambda/100 to the ground plane to still radiate efficiently. Coupling structures which are not radiators or antennas but are instead conductors that transmit signals using the backside cavity structure can also be as close lambda/100 to a ground plane and perform efficient transmission.

[0029] Another example embodiment is illustrated in FIG. 4C. In FIG. 4C, a bottom view 403 of a magnetic field coupled antenna 422c is shown with a cavity opening or waveguide 424c etched in the wafer substrate 410c. The etched opening can extend through the substrate to expose antenna 422c. However, in alternative arrangements, a portion of the semiconductor substrate 410c can be retained at a small thickness. The signal reflector 416c is illustrated beneath the antenna 422c and will be spaced from the antenna as indicated by the distance 420 as in cross-section view 400 in FIG. 4A.

[0030] When a magnetic reflector plane is used instead of an electrical reflector, different phase shifts occur. A perfect magnetic reflector has a reflection that is unity gain and has a zero degree phase shift. In the example of FIG. 4C, when a magnetic reflector is used, the spacing

420 can be quite close because the reflected electromagnetic energy will constructively interfere with the energy radiated from the antenna 422c, and thus gain can again be accomplished using the arrangements. This approach is also applicable to the arrangements of FIGS. 4A and 4B to obtain gain.

[0031] The magnetic reflector 416c can be implemented using an artificial magnetic reflector by patterning a metal pattern above the antenna to create a magnetic reflector. For example, the antenna or coupling structure 422c can be implemented in the first level metal layer in a semiconductor process, so that it is proximal to the surface of the semiconductor substrate, and the electrical reflector 416b in FIG. 4B (or the magnetic reflector 416c of FIG. 4C) can be implemented in an upper level of the metal structure. Various patterns are useful to create the reflector plane, such as if an artificial magnetic reflector is desired.

[0032] In conventional semiconductor processes the metal structure 414 in FIGS. 4A-4C can be formed in the “back end of the line” or “BEOL” phase of the semiconductor processes. The conductors in the metal structure 414 can be formed from copper and copper alloys, such as using single damascene or dual damascene processes. For example, such processes are increasingly used to form metal conductors after the implant, diffusion and anneal processes are used to form the doped regions in the active region 412 in a “front end” process. Also, backside processing is becoming more prevalent, such as to form deep openings for through silicon vias (TSVs). In example embodiments, the cavity openings or waveguide openings formed extending into the semiconductor substrate from the backside are also performed in (or, in an alternative approach, can be performed after) the BEOL processes. Wet etches, such as KOH, TMAH, HF and other chemical wet etches for semiconductor material removal can be used to form cavity openings with sloping sides to form antenna horn structures in various ones of the arrangements. In at least one example, for a silicon substrate, a KOH chemistry can form a sloped sidewall in the opening having an angle of about 57 degrees to the horizontal. In another example arrangement, a TMAH wet etch can be used form a cavity opening having an angle of about 61 degrees.

[0033] As further described below, waveguide or cavity openings with vertical sidewalls can be formed using deep reactive ion etching (DRIE) processes. Simulations can be used to determine horn shapes for antennas, or waveguides that have efficient transmission for radiated energy at a particular frequency. Beamforming techniques can be used to increase the efficiency and output of the antennas. Also, the simulations can indicate shapes that are efficient for receiving radiated signals at a chosen frequency (receiving and transmitting are reciprocal, the radiation and reception pattern are always the same). As another alternative, a stepped opening can be formed by repeating DRIE or wet etch processes with smaller and smaller patterns.

[0034] Further alternative shapes can be achieved by using different wafer thicknesses. Mechanical thinning from the backside of the wafer or "backgrinding" can be used to thin the wafers to further shape the cavities to optimize radiation and detection of electromagnetic energy at the chosen frequencies. Backgrinding can be used to remove a controlled thickness of semiconductor material to thin a wafer. Additional examples of removal methods include using chemical mechanical polishing (CMP) processes or combinations of CMP and mechanical backgrinding.

[0035] The semiconductor substrate can be, in an example arrangement, a wafer as commonly used in semiconductor processing, or a portion thereof. The semiconductor substrate can be silicon in one example arrangement. In more alternative arrangements, the semiconductor substrate can be of other useful materials, such as gallium arsenide, silicon germanium, gallium nitride, indium phosphide, indium arsenide or other "III-V" materials that are used or known for semiconductor processing.

[0036] FIGS. 5A, 5B and 5C illustrate three different views of alternative arrangements that include a THz antenna built within a semiconductor substrate in a semiconductor process, with a waveguide formed in the backside of the wafer substrate. In FIG. 5A, an illustrated cross-sectional view 500 shows a semiconductor substrate 510a with a waveguide 524a. A region 512 in the surface of the semiconductor substrate or wafer contains circuit components for the integrated circuit. The metal system 514 fabricated on the substrate surface contains an antenna structure 522a and a ground plane 518a which is separated from the antenna 522a by a distance 520. In this arrangement, the distance 520 has a range of $\lambda/10$ to $\lambda/8$. By selecting the distance labeled 520 for a particular frequency of interest, destructive interference can be avoided and, in some arrangements, constructive interference can be used to add gain to the signal radiated from the antenna 522a, which is an advantage over conventional approaches. Gain is achievable using example embodiments for frequencies such as THz and sub-THz frequencies where no practical ways exist to attain gain using conventional approaches.

[0037] Various antenna structures and various coupling structures are possible, with the signal radiating through the backside opening or waveguide or being detected through the backside opening or waveguide. Two additional examples are illustrated in FIGS. 5B and 5C. In FIG. 5B a bottom view 502 shows, in one example arrangement, a THz antenna 522b that is viewed through the back side waveguide 524b which is etched in the wafer substrate 510b. The ground plane 516b is shown behind the antenna and is separated by a distance 520 as indicated in cross-section 500 of FIG. 5A. The antenna 522b can also be arranged for other frequencies, such as for millimeter wave or sub-THz frequencies. The antenna 522b can also be arranged to detect or receive signals.

[0038] Another example embodiment is shown in the bottom view 503 in FIG. 5C, where a THz antenna 522c is shown through a waveguide opening 524c etched on the backside of the semiconductor substrate into, or completely through, the substrate 510c. Behind the antenna in FIG. 5C, the ground plane 516c is shown, and it is separated by a distance 520 as indicated in cross-section 500 of FIG. 5A.

[0039] FIG. 6 shows a balloon graph 640 indicating energy radiated by a backside antenna 622 in a system 600. The backside antenna 622 is shown radiating energy through a backside opening or waveguide 624 which was etched in the substrate 610 using conventional processes. The balloon graph 640 represent the simulated energy radiated by the backside antenna thru the waveguide. In this arrangement, the peak gain was simulated to be approximately 14dB as indicated by the graph scale 642. In an unexpected result, signal strength attained using example embodiments can be substantially higher than signal strength attained using conventional solutions. For example, as shown in FIG. 3, a conventional solution provides only a signal strength of about 7dB. Accordingly, example embodiments are suitable for achieving a performance of about twice that of conventional solutions for the frequencies of interest.

[0040] Various arrangements include different cavity openings or waveguide shapes that can be formed on the back side of the semiconductor substrate or wafer. The waveguides will be created using semiconductor processing techniques that are compatible with the semiconductor wafer used for the antenna. For very high aspect ratio etches, the DRIE (Direct Reactive Ion Etch) process can be used. The DRIE etch can be used as a single etch to form a column style waveguide or in multiple steps with increasing area to form a horn style opening or waveguide. In processes where a sloped waveguide is desired, a cavity or wet etch is a common technique used for that shape. Several examples of waveguide shapes and the associated etches are shown in FIGS. 7A-7D and 8A-8C.

[0041] FIGS. 7A-7D show cross-sectional views of an opening or waveguide formed with a DRIE etch and several examples of its use. A portion of an integrated circuit cross-section 700 of FIG. 7A contains an antenna structure 716 within the metal structure 714 with a bond wire 730 that protrudes from the top of the metal structure 714. A vertical cavity or waveguide 724 can be etched in the backside of wafer substrate 710 using a DRIE etch (direct reactive ion etch) process. In some example arrangements, the cavity can be further enhanced by plating with a conductive layer 727 as shown in FIG. 7A using a compatible metallization process. In alternative arrangements, the conductive layer 727 can be omitted. The vertical waveguide 724 formed on the backside of the substrate results in improved directionality and gain over conventional front side solutions. This arrangement enables free-space radiation of the signal, die-to-die signal coupling, inter-die signal coupling, die-to-package and die-to-waveguide signal coupling. For example, redistribution layers can be formed using these structures for Thz signaling.

[0042] In FIG. 7B, a cross-section 704 of a substrate 722 represents an inter-die communication waveguide 724c and can be formed after the etch using compatible processing or by waveguides embedded in a portion of a second substrate or other redistribution layer (RDL) 722. As shown in cross-section 704, the RDL 722 can be used to route signals from one portion of an integrated circuit or wafer to another portion, allowing for THz signal communications through the waveguide 724c without a need for intervening elements such as optical couplers.

[0043] In FIG. 7C, another aspect of the current application is shown. In this arrangement, use of antennas with backside radiation provides electrical isolation of a pair of dies 720a, 710b from each other, yet allows THz communications between them. The space 723 between the two dies of cross-section 702 can be constructed as an isolating air gap. In another example arrangement, the gap 723 may be filled with an insulating material to closely control the antenna spacing while providing electrical isolation between the die pair. In this manner dies that are coupled to different potentials or ground voltages can communicate without being connected to a common potential.

[0044] In FIG. 7D another arrangement is shown in a cross-section 706. In this arrangement, a package substrate 711 contains an embedded waveguide 718 which directs the signal from the die 710c with antenna or coupling structure 716 into the waveguide 718 in the substrate 711.

Not illustrated at the other end of the substrate waveguide, an antenna or other die coupling structure may receive the signal. Because example embodiments enable THz frequency signaling, data or communications signals can be readily transmitted from an integrated circuit directly into a waveguide without the need for opto-couplers or other intervening devices.

[0045] In an alternative arrangement, the waveguide can be a dielectric waveguide; that is, the waveguide 718 can be filled with a dielectric material for constraining and directing the THz frequency signals. For example, in alternative arrangements, the waveguide can include low-loss dielectrics, such as PTFE, PE, PP, quartz and ceramics.

[0046] FIGS. 8A-8C show cross-sectional views of additional alternative arrangements for additional waveguide formations on the backside of a substrate or wafer. In FIG. 8A, a portion of a semiconductor substrate 810 which can include active devices is shown in a cross-section 800 with the metal stack 814 above the substrate. A stepped waveguide horn 824a is shown as etched in the backside of the semiconductor substrate 810 using multiple DRIE etches. For example, a first DRIE etch can provide a shallow opening at the surface of the backside of the substrate. A second DRIE etch that is narrower can then be performed to form a deeper stepped hole within the boundaries of the first opening. The DRIE etches can continue to form the stepped structure 824a.

[0047] FIG. 8B illustrates an alternative arrangement in a cross-section 802. In another aspect, a smooth horn waveguide 824b can be etched in the substrate 810 using wet etch methods as shown in FIG. 8B. The smooth waveguide or cavity 824b can be used to perform die to die, die to RDL, die to substrate, and die to waveguide coupling, and also for free space radiation, similar to the various coupling methods of FIGS. 7A-7D.

[0048] FIG. 8C illustrates a cross-section 804 of another example arrangement. In cross-section 804 of FIG. 8C, a pair of integrated circuit dies having substrates 810a and 810b and metal structures 814a and 814b are arranged for die-to-die coupling via radiation from their smooth waveguide horns 824b. In FIG. 8C, electrical isolation between the two dies can be achieved by leaving the space between the die 823 filled with air. In another alternative approach, electrical isolation between the dies can be achieved by inserting an insulating material between the die in space 823.

[0049] In an example arrangement, an apparatus includes a semiconductor substrate having a front side surface including circuitry and a backside surface opposing the front side surface.

Metal conductors are formed over the front side surface. At least one cavity opening is etched in the backside surface. A radiator (such as a radiating or coupling structure) is formed in a portion of the metal conductors and configured to radiate signals through the cavity opening in the backside surface.

[0050] In another example arrangement, the radiator is formed in a level of the metal conductors overlying the surface of the semiconductor substrate. In a further arrangement, the apparatus further includes a reflective surface formed spaced from and overlying the radiator, and configured to reflect the signals towards the opening in the backside surface. In another arrangement, the reflective surface is an electrical reflector. In still another arrangement, in the apparatus, the reflective surface reflects the radiated signals with a phase shift of 180 degrees.

[0051] In more alternative arrangements, the reflective surface is spaced from the radiator by a distance that is a fraction of the wavelength of the radiated signals between 1/10 and 1/2 of the wavelength. In still another arrangement, the reflective surface is a magnetic reflector. In a further alternative arrangement, the reflective surface reflects the radiated signals with a phase shift of 0 degrees.

[0052] In yet another arrangement, the radiated signals have a frequency between 0.1 THz and 30 THz. In further arrangements, the radiated signals have a frequency of at least about 0.1 THz. In still another alternative arrangement, the cavity opening has sloped sidewalls. In still another alternative arrangement, the semiconductor substrate further comprises active devices. In yet further alternative arrangements, the semiconductor substrate further comprises metal oxide semiconductor transistors. In yet another alternative arrangement, the cavity opening forms a waveguide for the radiated signals. In more alternative arrangements, the cavity opening has vertical sidewalls. In still further alternative arrangement, the cavity opening is coated with a conductive material. In further arrangements, the radiator forms an antenna. In still additional arrangements, the antenna is further configured to receive radiated signals. In still another arrangement, the semiconductor substrate is a silicon substrate.

[0053] In another arrangement, a method includes forming a backside cavity opening on a backside surface semiconductor substrate proximal to a radiator formed in a metal conductor overlying a front side surface of the semiconductor substrate; and radiating signals having a frequency range between 0.1 THz and about 30 THz from the radiator and out of the backside cavity opening. In still another arrangement, forming a backside cavity opening further includes backgrinding the semiconductor substrate to thin the semiconductor substrate to a predetermined thickness. In yet another arrangement, the method includes forming a backside cavity opening further including performing a wet etch to form an opening with sloped sidewalls.

[0054] In still another alternative arrangement, forming the backside cavity opening further comprises performing a KOH wet etch. In yet another alternative arrangement, forming the backside cavity opening further includes performing a TMAH wet etch. In a further alternative arrangement, forming the backside cavity further includes performing a wet etch to form an opening with sloping sidewalls.

[0055] In still another alternative arrangement, forming the backside cavity opening further includes performing a deep reactive ion etch. In a further alternative, the backside cavity opening has vertical sidewalls.

[0056] In another arrangement, a system includes a first integrated circuit having an antenna for radiating THz frequency signals formed in a metal structure overlying the surface of a first semiconductor substrate, and an first opening formed in the backside of the first semiconductor substrate and extending into the semiconductor substrate at a location corresponding to the antenna; and a second integrated circuit having an antenna for receiving THz frequency signals formed in a metal structure overlying the surface of a second semiconductor substrate, and an second opening formed in the backside of the second semiconductor substrate; the first and second openings facing one another and being aligned one to another to facilitate transmission of the THz signals from the first integrated circuit to the second integrated circuit.

[0057] Another arrangement provides a space between the first integrated circuit and the second integrated circuit. In yet another arrangement, an electrical isolation material is disposed between the first integrated circuit and the second integrated circuit. In still another arrangement, the first opening and the second opening further comprise waveguides. In a further arrangement, the first opening and the second opening further comprise openings having sloped sidewalls. In still another arrangement, the first opening and the second opening further comprise openings having vertical sidewalls.

[0058] Various modifications are possible in the order of steps and in the number of steps to form additional arrangements of example embodiments.

[0059] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. Apparatus, comprising:

a semiconductor substrate having a front side surface and a backside surface opposing the front side surface;

metal conductors formed over the front side surface;

at least one cavity opening etched in the backside surface; and

a radiating or coupling structure formed in a portion of the metal conductors and configured to radiate signals through the cavity opening in the backside surface.

2. The apparatus of claim 1, wherein the radiating or coupling structure is formed in a level of the metal conductors that is overlying the front side surface.

3. The apparatus of claim 2, and further comprising a reflective surface formed spaced from and overlying the radiating or coupling structure, and configured to reflect the signals towards the opening in the backside surface.

4. The apparatus of claim 3, wherein the reflective surface is an electrical reflector.

5. The apparatus of claim 4, wherein the reflective surface reflects the radiated signals with a phase shift of 180 degrees.

6. The apparatus of claim 4, wherein the reflective surface is spaced from the radiating or coupling structure by a distance that is a fraction of the wavelength of the radiated signals between 1/100 and 1/2 of the wavelength.

7. The apparatus of claim 3, wherein the reflective surface is a magnetic reflector.

8. The apparatus of claim 7, wherein the reflective surface reflects the radiated signals with a phase shift of 0 degrees.

9. The apparatus of claim 1 wherein the radiated signals have a frequency between 0.1 THz and 30 THz.

10. The apparatus of claim 1, wherein the cavity opening has sloped sidewalls.

11. The apparatus of claim 1, wherein the cavity opening forms a waveguide for the radiated signals.

12. The apparatus of claim 1, wherein the cavity opening has vertical sidewalls.

13. The apparatus of claim 12, wherein the cavity opening is coated with a conductive material.

14. The apparatus of claim 1 wherein the radiating or coupling structure forms an antenna.

15. A method, comprising:

forming a backside cavity opening on a backside surface of a semiconductor substrate proximal to a radiating or coupling structure formed in a metal conductor overlying a front side surface of the semiconductor substrate; and

radiating signals having a frequency range between 0.1 THz and about 30 THz from the radiator and out of the backside cavity opening.

16. The method of claim 15, wherein forming a backside cavity opening further comprises:

backgrinding the semiconductor substrate to thin the semiconductor substrate to a predetermined thickness.

17. The method of claim 15, wherein forming a backside cavity opening further comprises performing a wet etch to form an opening with sloped sidewalls.

18. The method of claim 15, wherein forming the backside cavity opening further comprises performing an etch that is one selected from the group consisting essentially of a KOH wet etch, a TMAH etch, and a deep reactive ion etch.

19. A system, comprising:

a first integrated circuit having an antenna for radiating THz frequency signals formed in a metal structure overlying the surface of a first semiconductor substrate, and an first opening formed in the backside of the first semiconductor substrate and extending into the semiconductor substrate at a location corresponding to the antenna; and

a second integrated circuit having an antenna for receiving THz frequency signals formed in a metal structure overlying the surface of a second semiconductor substrate, and an second opening formed in the backside of the second semiconductor substrate;

the first and second openings facing one another and being aligned one to another to facilitate transmission of the THz signals from the first integrated circuit to the second integrated circuit.

FIG. 1A

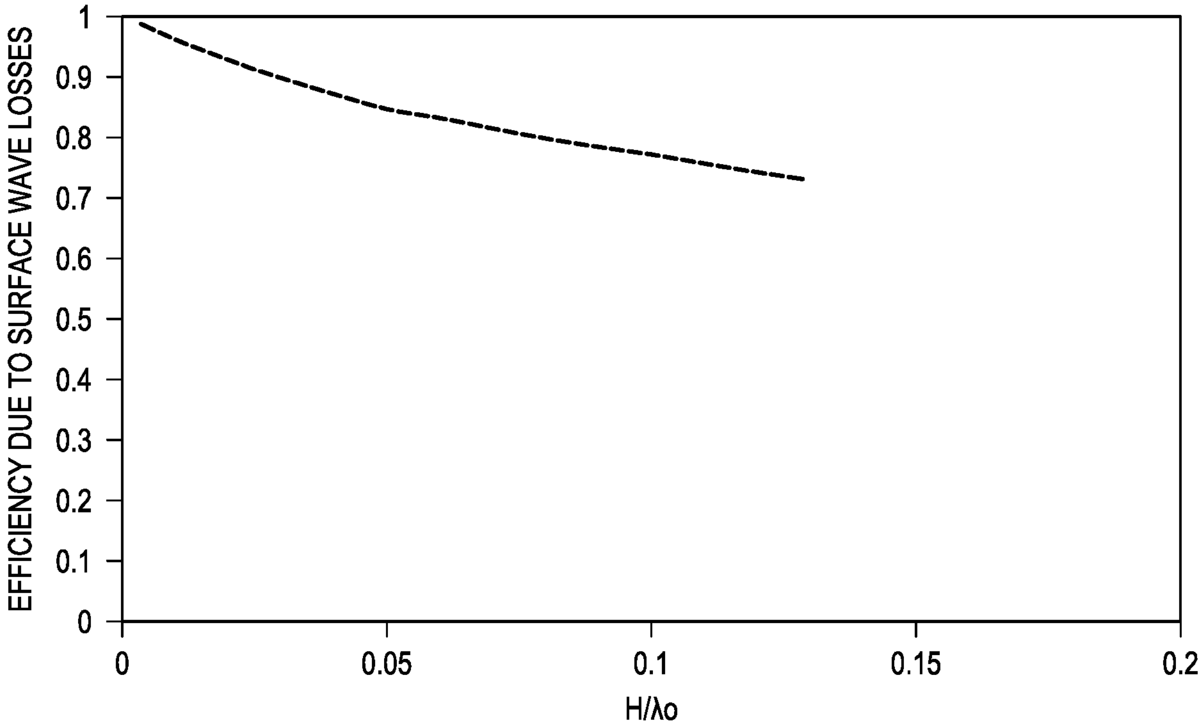
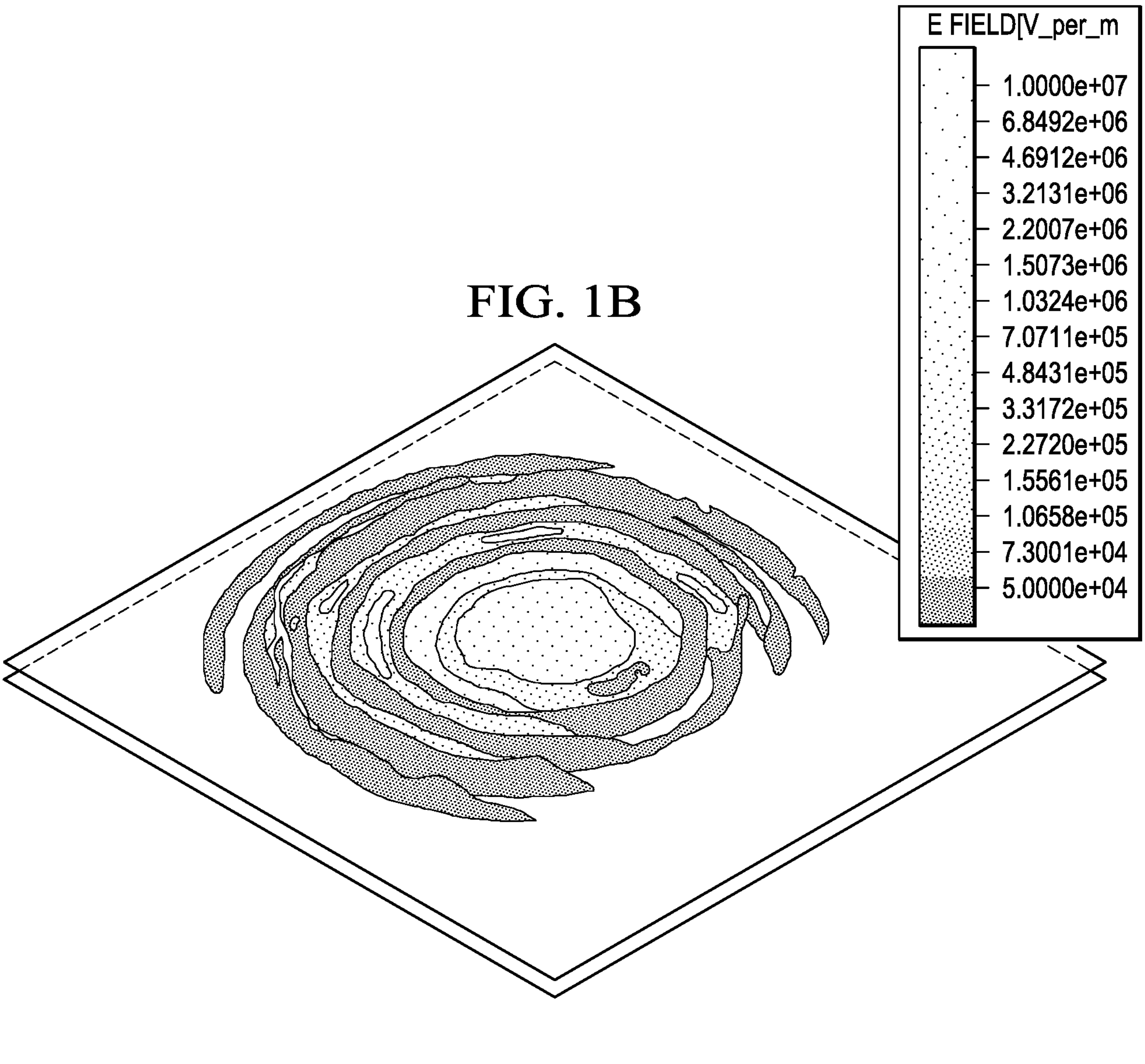

EFFICIENCY DUE TO SURFACE WAVE LOSSES
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
0.05
0.1
0.15
0.2
H/λo

FIG. 1B


E FIELD[V_per_m
1.0000e+07
6.8492e+06
4.6912e+06
3.2131e+06
2.2007e+06
1.5073e+06
1.0324e+06
7.0711e+05
4.8431e+05
3.3172e+05
2.2720e+05
1.5561e+05
1.0658e+05
7.3001e+04
5.0000e+04

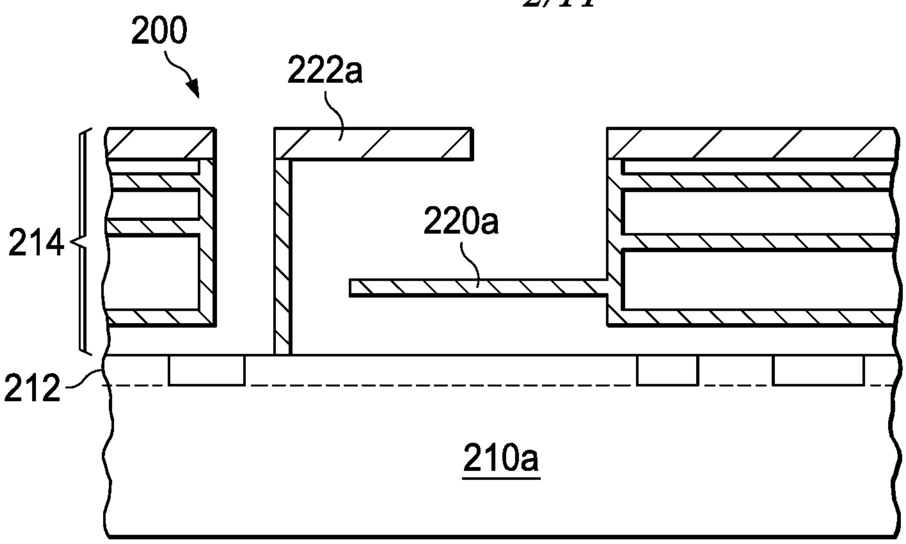


FIG. 2A
(PRIOR ART)

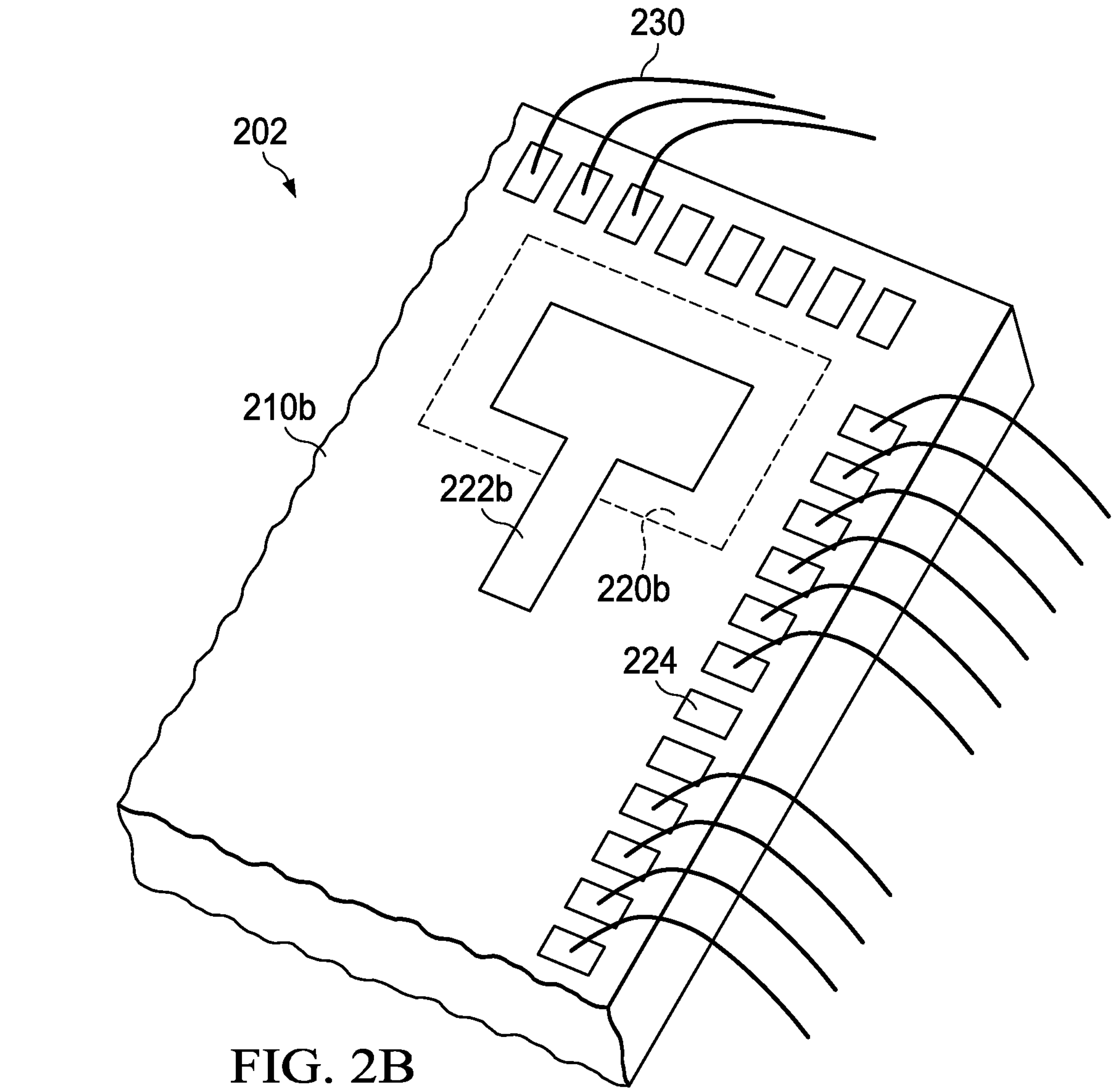


FIG. 2B
(PRIOR ART)

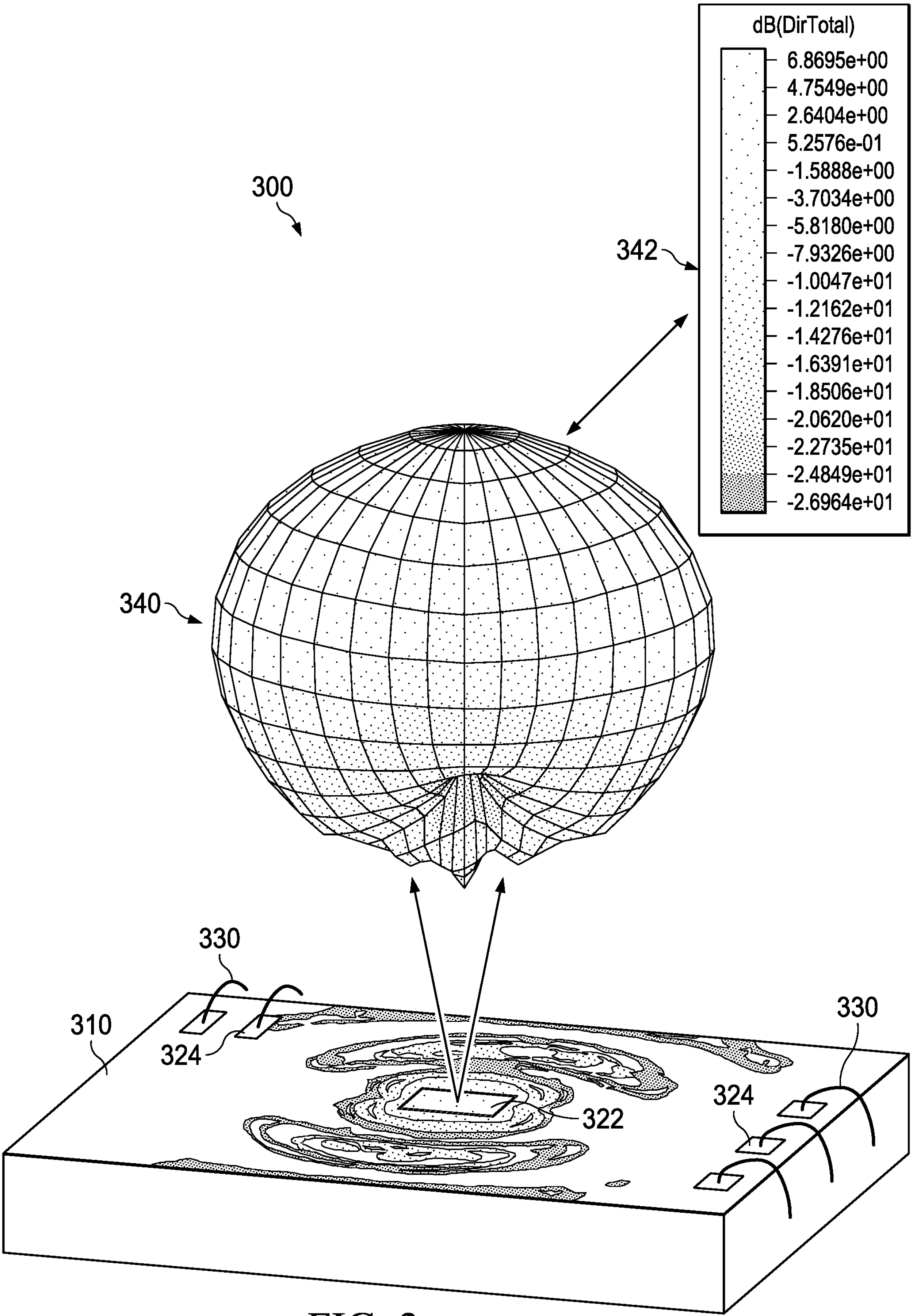


FIG. 3
(PRIOR ART)

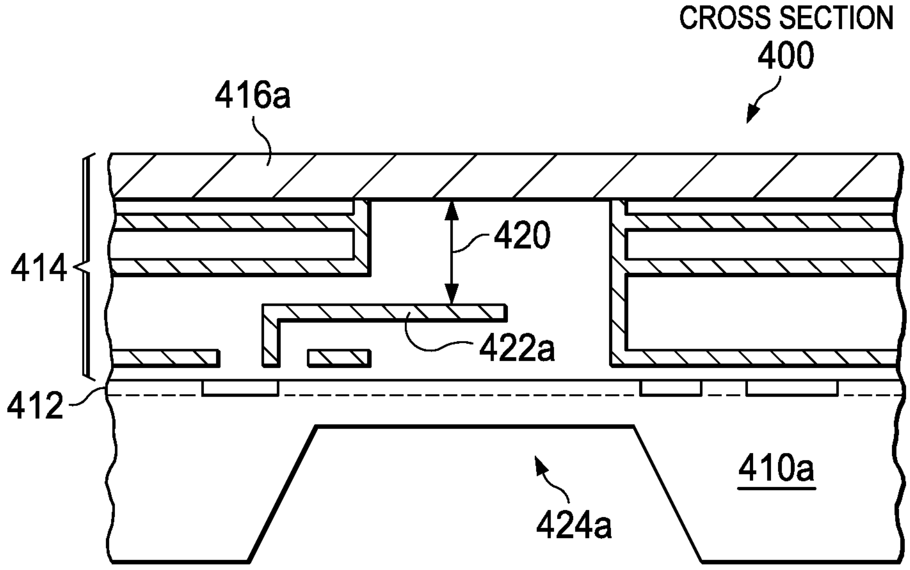


FIG. 4A

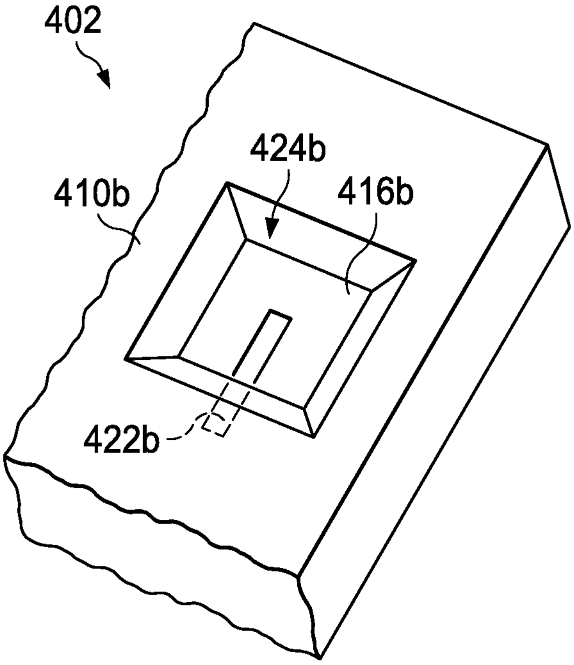


FIG. 4B

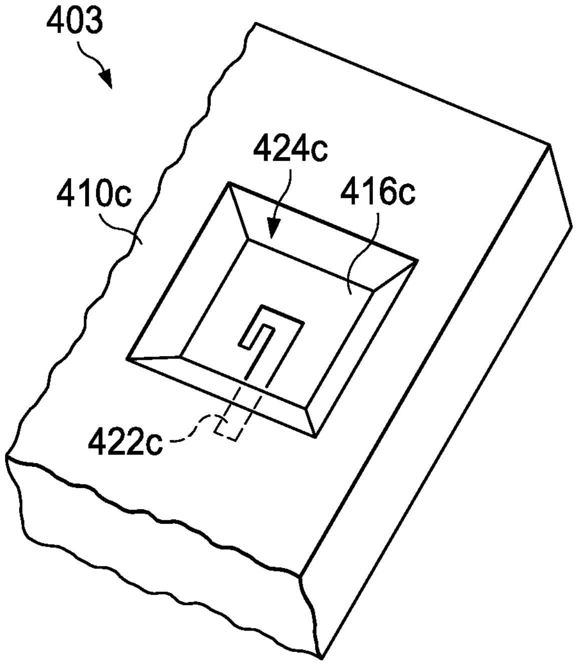


FIG. 4C

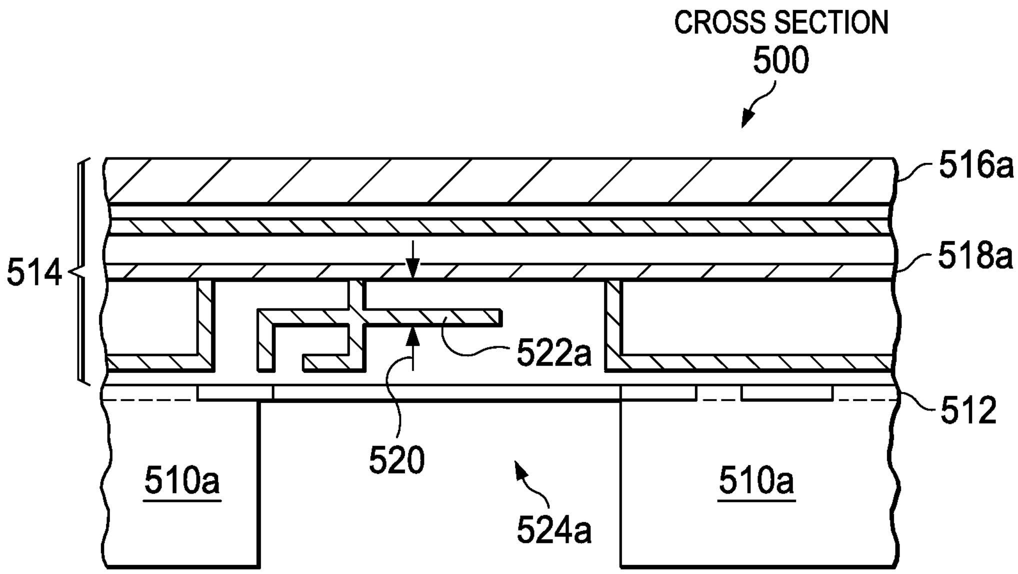


FIG. 5A

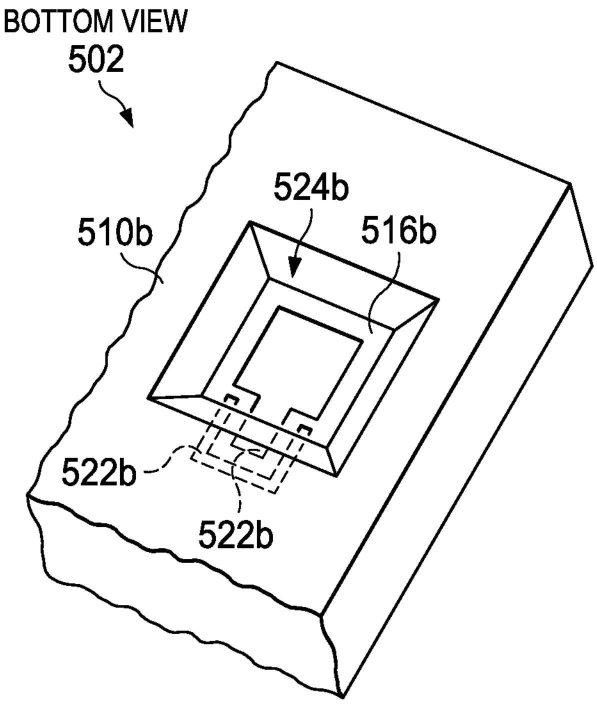


FIG. 5B

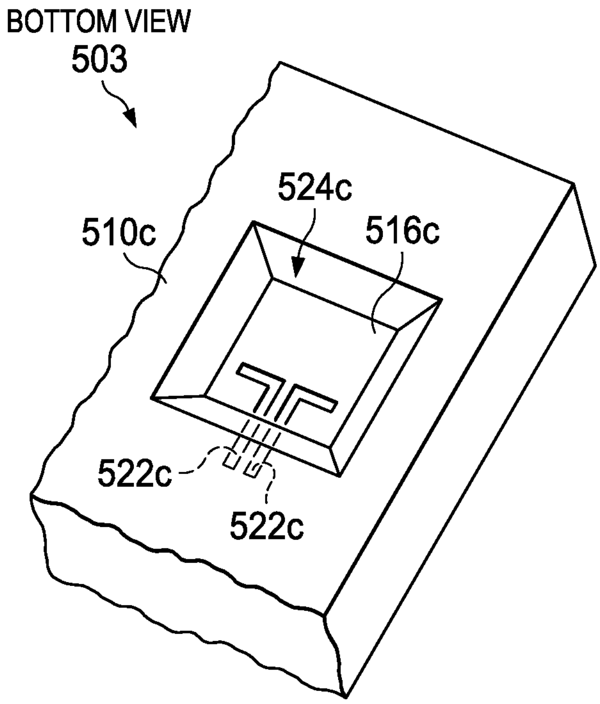


FIG. 5C

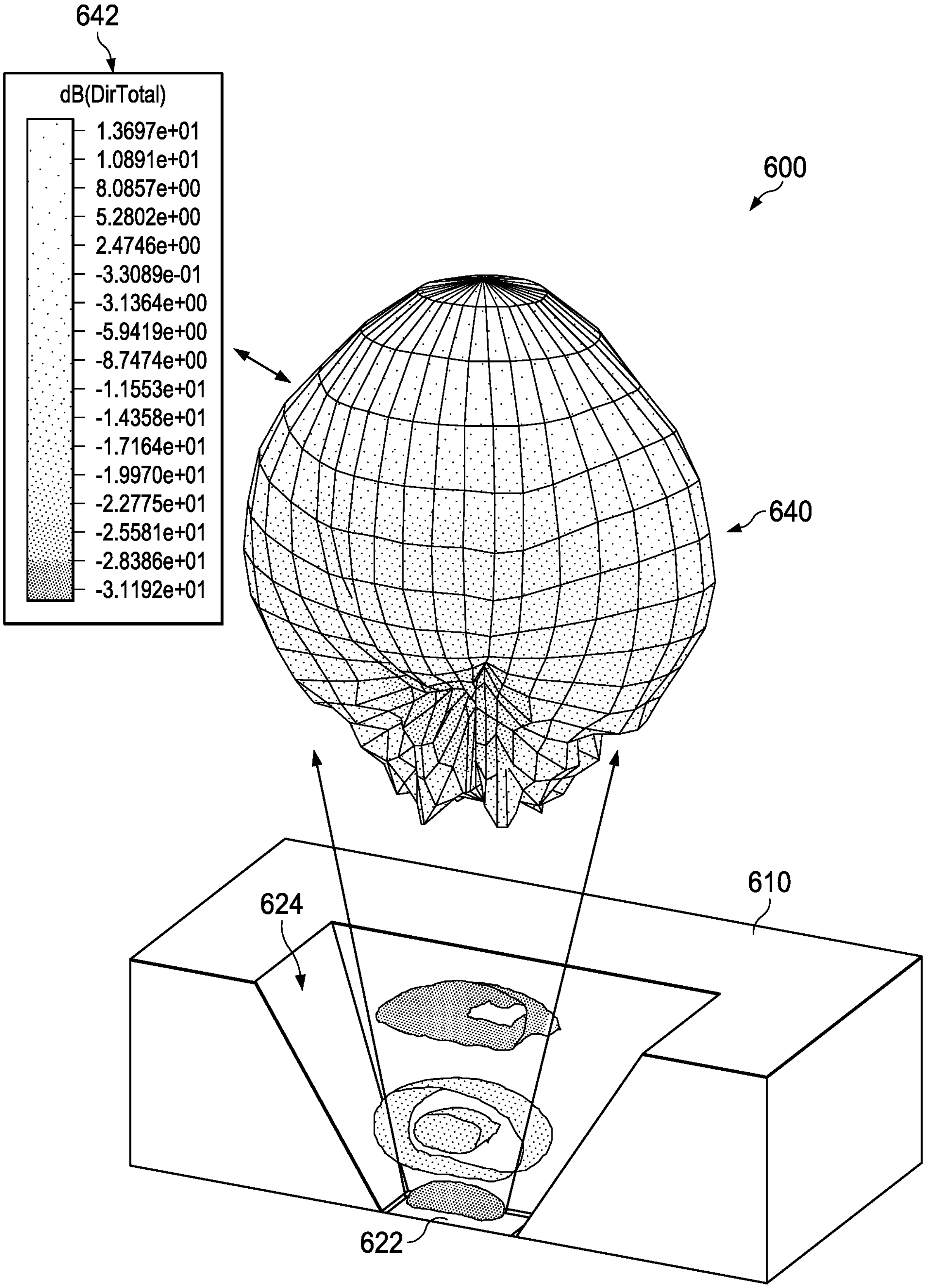

642
dB(DirTotal)
1.3697e+01
1.0891e+01
8.0857e+00
5.2802e+00
2.4746e+00
-3.3089e-01
-3.1364e+00
-5.9419e+00
-8.7474e+00
-1.1553e+01
-1.4358e+01
-1.7164e+01
-1.9970e+01
-2.2775e+01
-2.5581e+01
-2.8386e+01
-3.1192e+01
600
640
610
624
622

FIG. 6

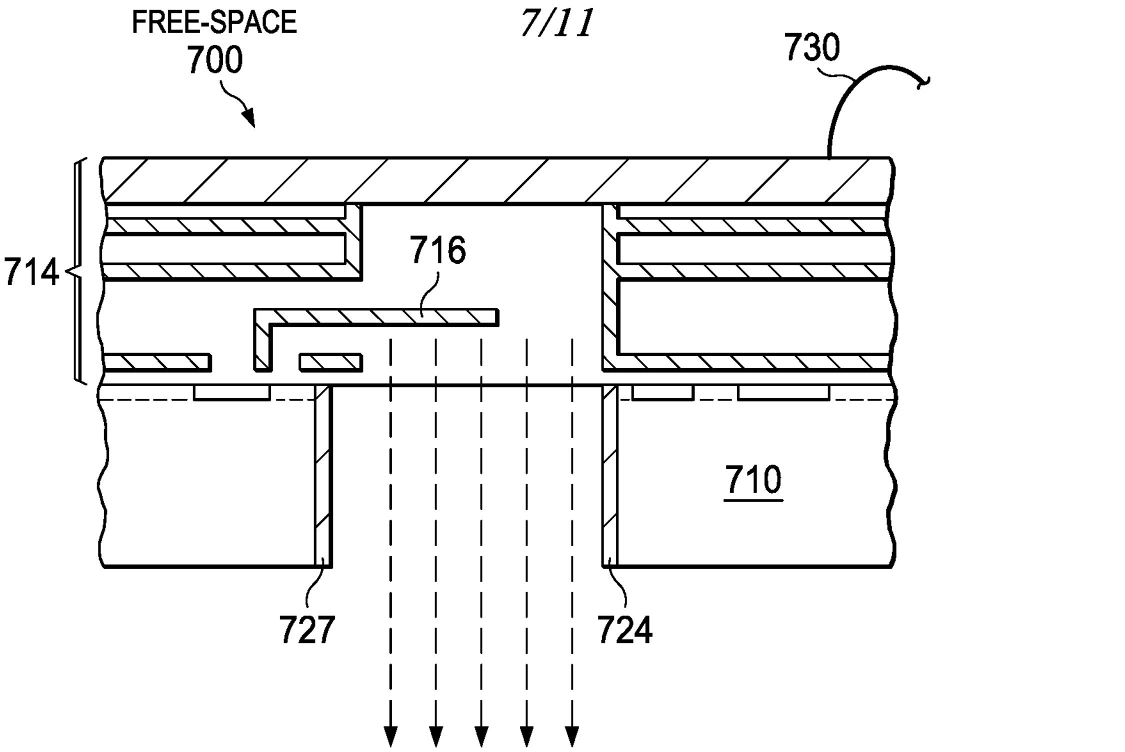

FREE-SPACE
700
730
714
716
710
727
724

FIG. 7A

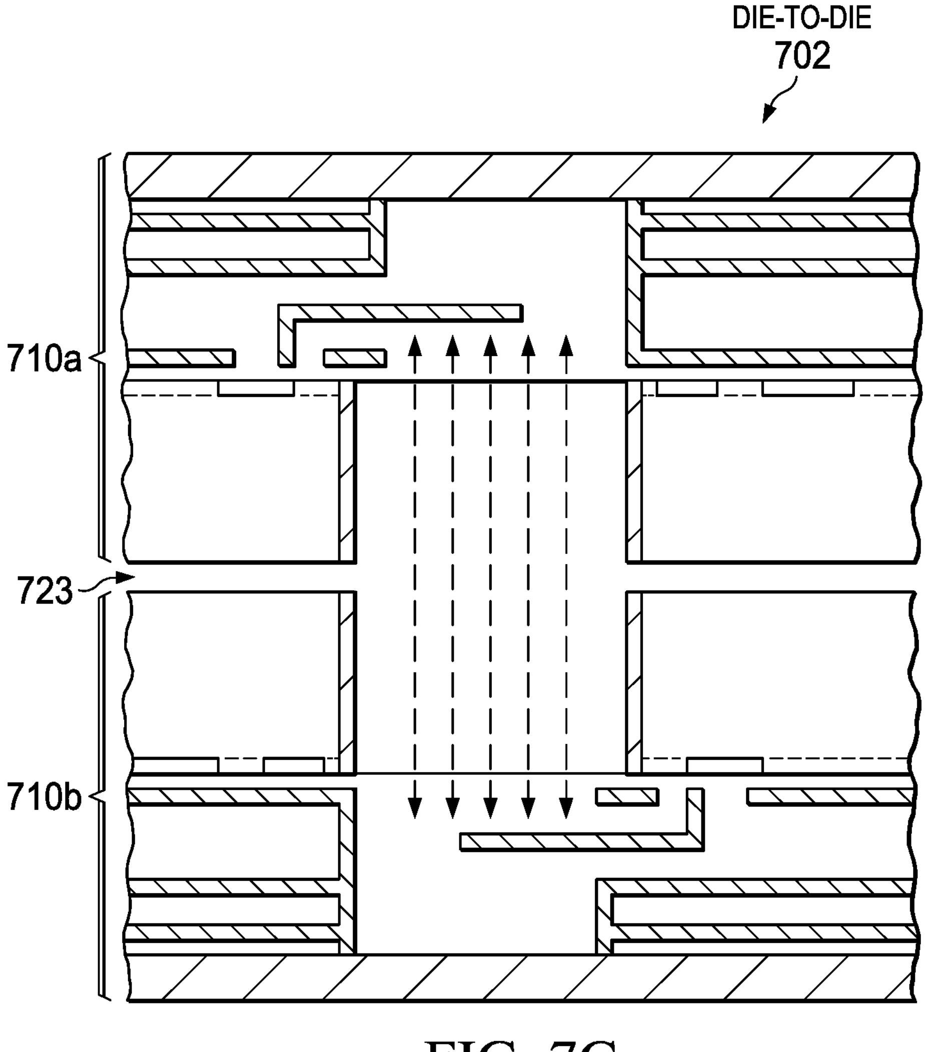

DIE-TO-DIE
702
710a
723
710b

FIG. 7C

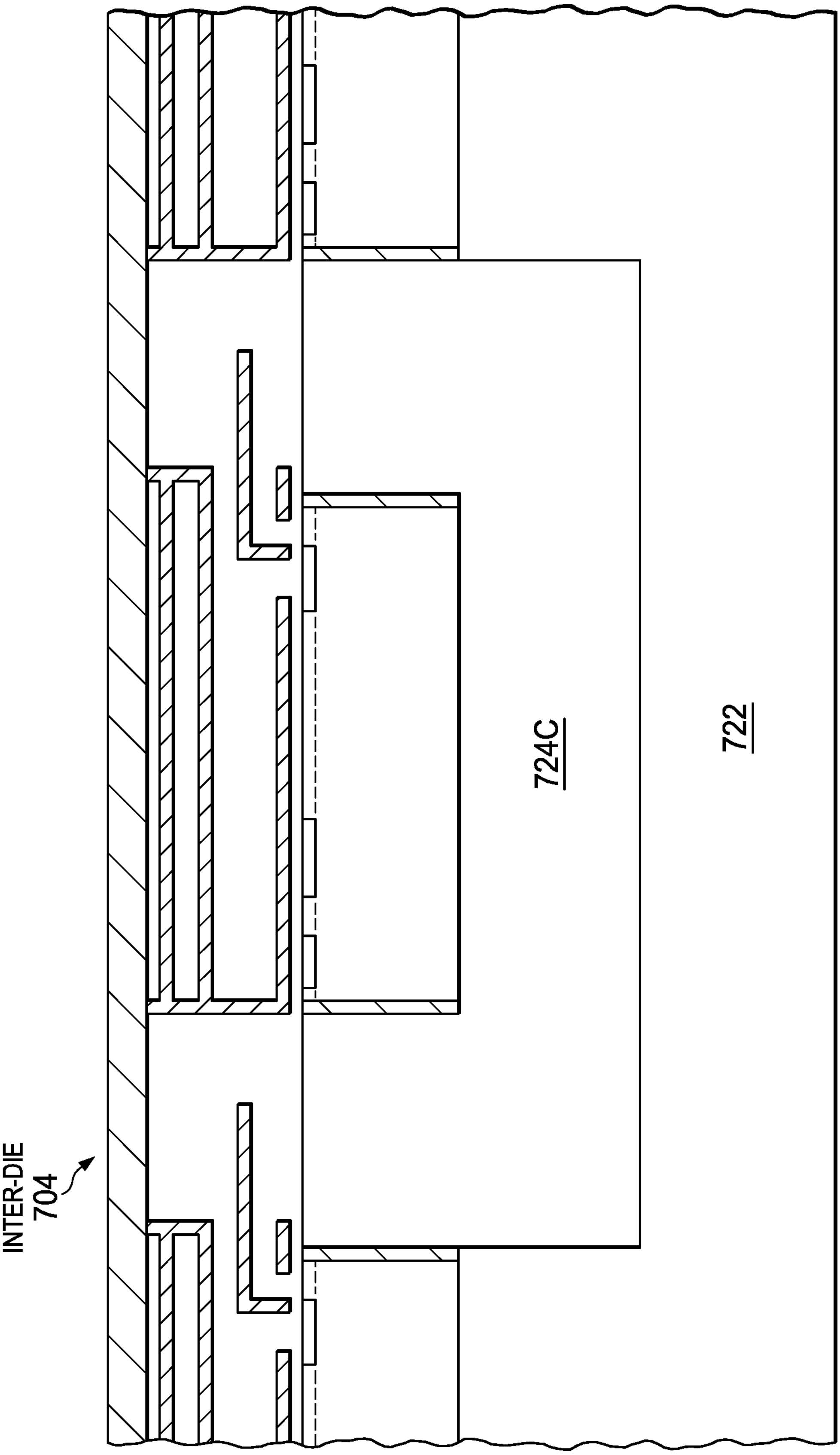


FIG. 7B

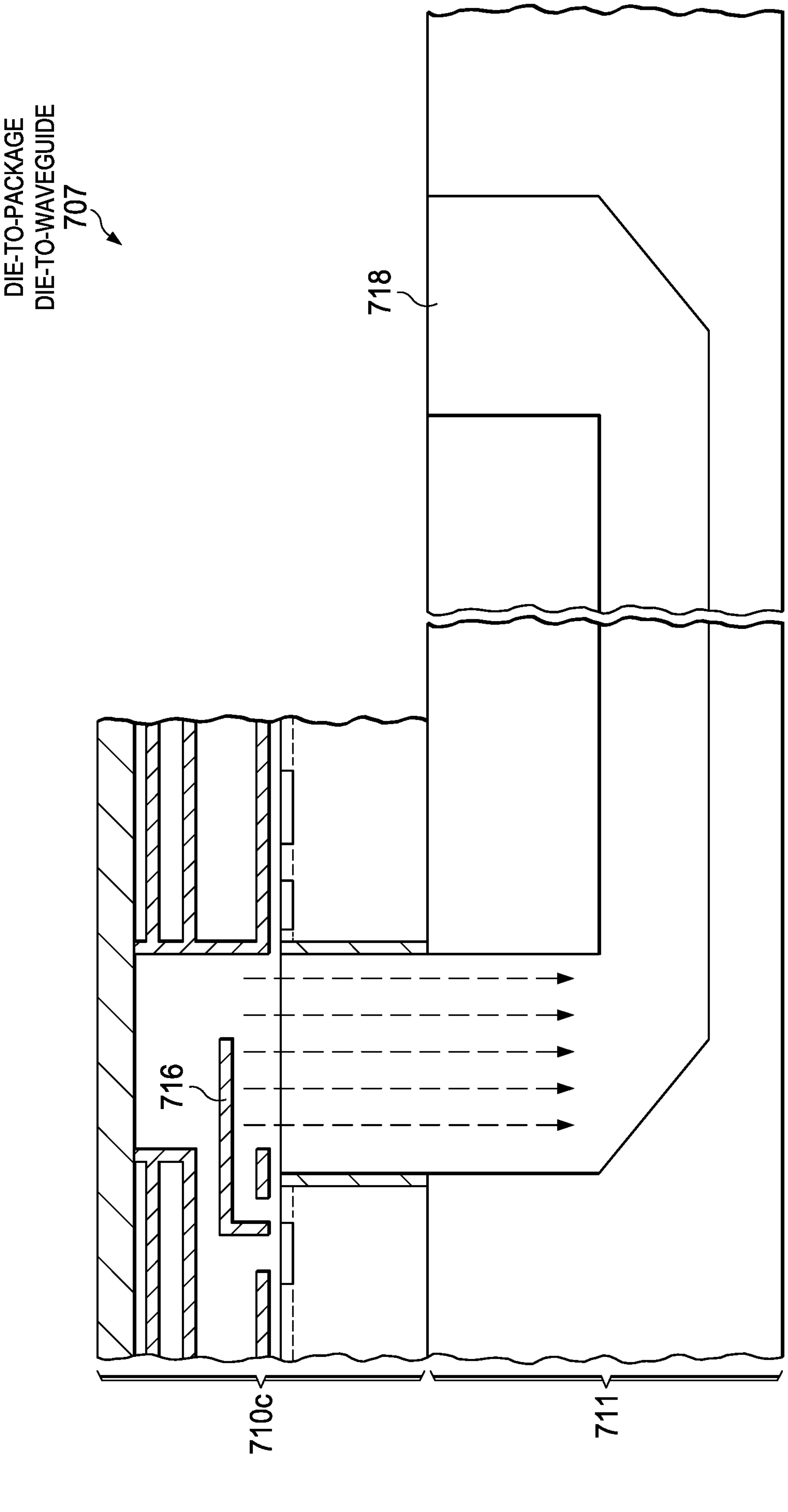


FIG. 7D

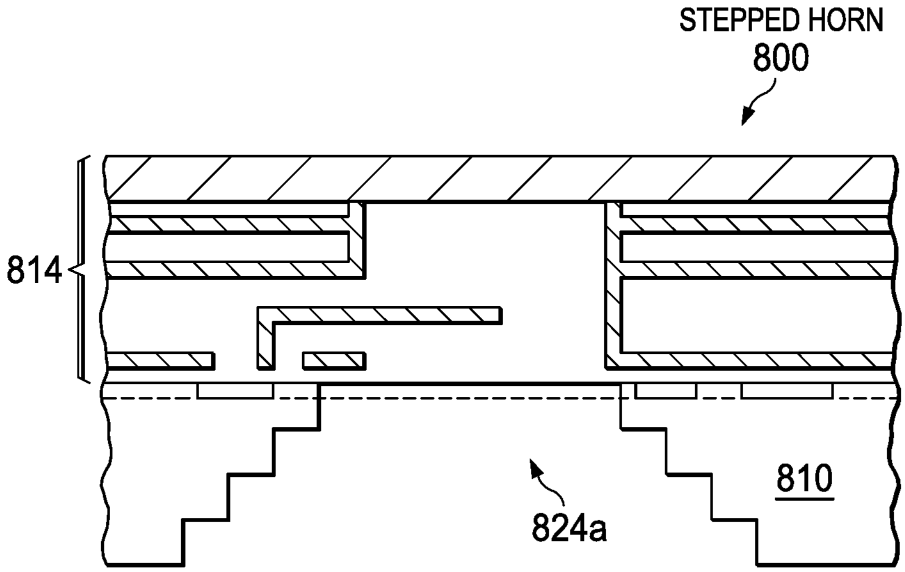


FIG. 8A

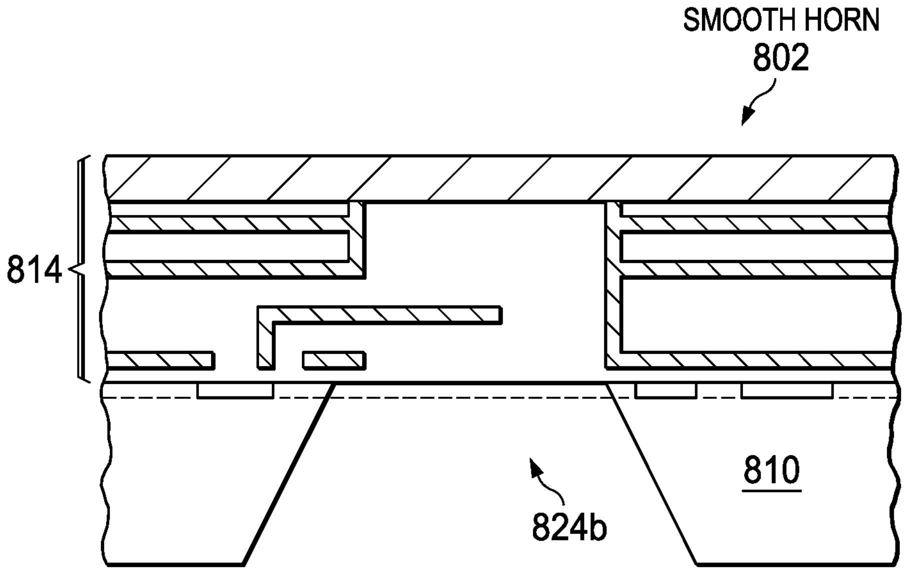


FIG. 8B

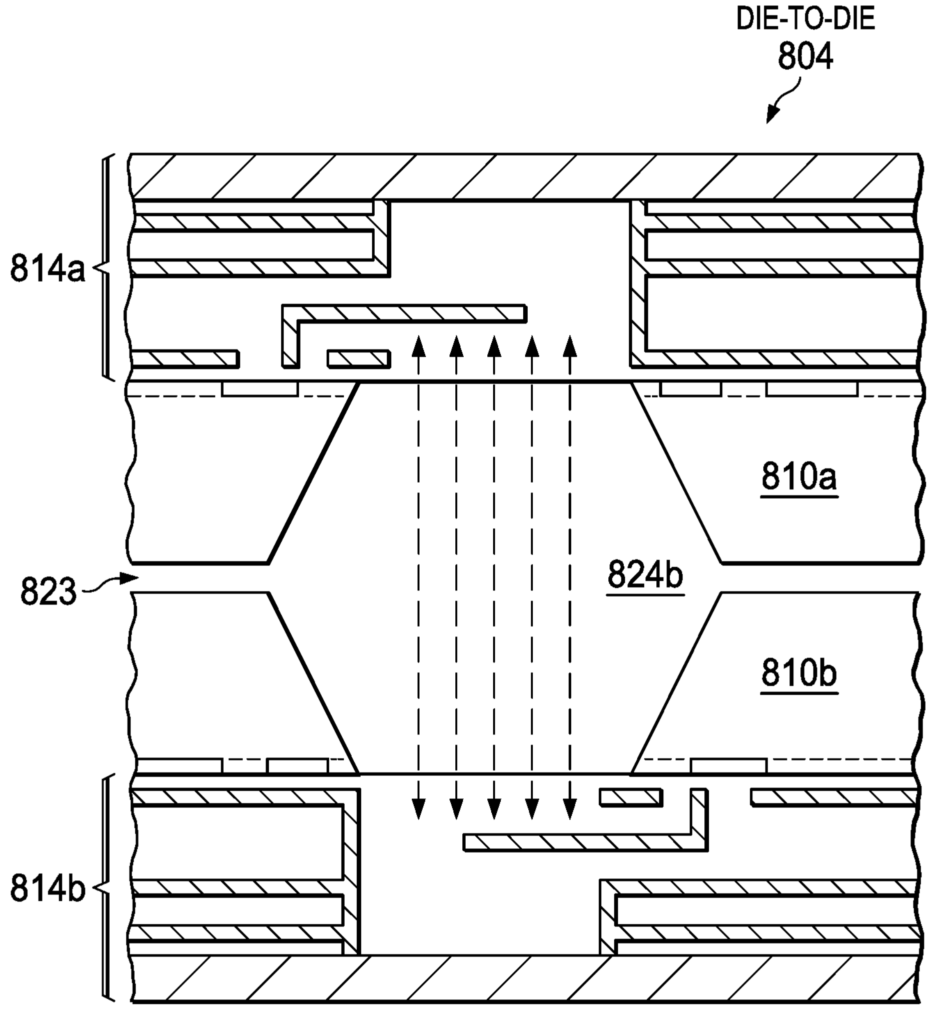


FIG. 8C