(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 October 2014 (30.10.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/172835 A1

(51) International Patent Classification:
H01L 21/768 (2006.01) *H01L 23/52* (2006.01)

(21) International Application Number:
PCT/CN2013/074524

(22) International Filing Date:
22 April 2013 (22.04.2013)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **ACM RESEARCH (SHANGHAI) INC** [—/CN]; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-tech Park, Shanghai 201203 (CN).

(72) Inventors: **WANG, Hui**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-tech Park, Shanghai 201203 (CN). **CHEN, Fuping**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-tech Park, Shanghai 201203 (CN). **ZHANG, Xiaoyan**; Bld. 4, No. 1690 Cailun Road, Zhangjiang High-tech Park, Shanghai 201203 (CN).

(74) Agent: **SHANGHAI PATENT & TRADEMARK LAW OFFICE, LLC**; 435 Guiping Road, Shanghai 200233 (CN).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: METHOD AND APPARATUS FOR THROUGH-SILICON VIAS REVEAL

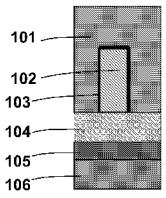

FIG 1a

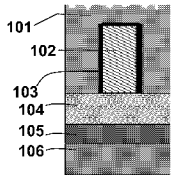

FIG 1b

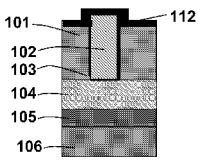

FIG 1e

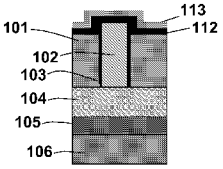

FIG 1f

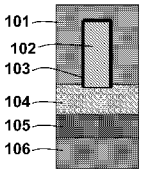

FIG 1c

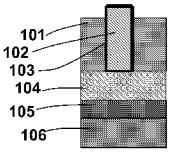

FIG 1d

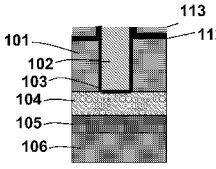

FIG 1g

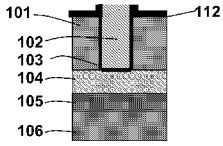

FIG 1h

(57) **Abstract**: A method and an apparatus for TSVs reveal are provided. The method includes the following steps: providing a Si substrate (101) having a plurality of TSVs (102) formed inside the Si substrate (101); rotating the Si substrate (101) and spraying a first etchant onto th backside of the Si substrate (101) to etch the backside of the Si substrate (101), and stopping etching before the TSVs (102) being exposed to the backside of the Si substrate (101); and rotating the Si substrate (101) and spraying a second etchant onto the backside o the Si substrate (101) to etch the backside of the Si substrate (101) until the TSVs (102) being exposed to the backside of the Si substrate (101), wherein reversing the rotation direction of the Si substrate (101) at fixed intervals during spraying the second etchant onto th backside of the Si substrate (101).

WO 2014/172835 A1

METHOD AND APPARATUS FOR THROUGH-SILICON VIAS REVEAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to a method and an apparatus for through-silicon vias (TSVs) reveal, and more particularly, relates to a method and an apparatus for silicon etching for exposing the TSVs.

2. The Related Art

[0002] Continuous scaling of VLSI can be reducing gate delays but rapidly increasing interconnection delays. As the technology node shrink, performance improvement of advanced VLSI has begun to saturate, and the heavier interconnection loading increases the power consumption in high-performance chips. Smaller wire cross-sections, smaller wire pitch and longer lines to traverse larger chips increase RC delays. Therefore, traditional 2D (Two-dimension) device scaling is increasingly difficult and fast approaching fundamental limits of physics.

[0003] In recent years, 3D IC (Three-dimensional integrated circuit) physical design attracts more and more attention. 3D IC technology has become the most promising solution to overcome the conventional 2D device scaling limitation. In electronics, a 3D IC is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit. The benefits of 3D IC stacking technology may include such as increased density, shorter interconnection length, less interconnection delay, increased bandwidth, reduced power consumption, lower cost and heterogeneous integration possibility. Wafer processing can be simplified within one layer or strata of stacked silicon for a specific function such as processor or memory function instead of adding process steps for heterogeneous function in a 2D structure. The key difference between the 3D IC and

the 2D IC is through-silicon vias (TSVs), which connect the device layers in a 3D IC. Several TSV approaches called Via First, Via Middle and Via Last, have been developed to fabricate 3D IC products. Via First is a process that vias are created early in the device manufacturing process. This TSV technology, called pre-process vias or Vias First, has to be completely compatible with subsequent standard CMOS process. Moreover, this technology is also available for other packaging applications such as MEMS packaging or memory stacking. Via Middle is a process that vias are created after Si FEOL (Front End of Line) transistor formation processing, and before BEOL (Back End of Line) metallization processing. Via Last is a process that vias are created after the BEOL processing. Generally, Via First and Via Middle processes need stringent CD control with small via diameters (5-20μm). The common used AR (Aspect Ratio) is usually from 3:1 to 10:1. Via Last process is relatively loose in CD control with bigger via diameters (20-50μm). The common used AR is usually from 3:1 to 15:1.

[0004] A conventional 3D TSVs fabrication process includes two major steps.

[0005] Step 1 is forming TSVs in a wafer, which includes etching a plurality of through holes in the wafer, CVD (chemical vapor deposition) dielectric oxide liner on the sidewall and bottom wall of the through holes, PVD (physical vapor deposition) barrier layer and seed layer on the sidewall and bottom wall of the through holes, and filling conductive material in the through holes. The conductive material could be copper, tungsten, poly Si or doped Si. The filling method could be ECD (electrochemical deposition), CVD and LPCVD.

[0006] Step 2 is thinning the wafer and revealing the TSVs. This step is a key technology to complete the 3D TSVs fabrication, which further includes steps as follows:

[0007] a) Bonding the frontside of the wafer to a temporary thin wafer carrier;

[0008] b) Thinning the backside of the wafer by grinding to approx 5-14μm below the TSVs, wherein the key for TSV technology is the control of the Si TTV (total thickness variation) and Si surface quality after grinding;

[0009] c) Cleaning the wafer in a single-wafer cleaning tool for a high number of particles and grinding-mark defects are generated both on the backside (particle adhesion) and the frontside (grinding marks) of the wafer while grinding;

[0010] d) CMP (chemical mechanical polishing) the backside of the wafer until center conductor of the TSVs is exposed from the backside of the wafer. After the backside of the wafer undergoes mechanical grinding, a thin and damaged Si layer is present. CMP performs dual function of removing the damaged Si layer and exposing the center conductor of the TSVs, which is a traditional TSVs reveal method. There are often some inborn failures after CMP reveal: device reliability issues due to contaminating the Si layer with the conductive material (like Cu, W) during CMP processing, scratching, dishing and erosion due to relative high Cu polish rate with relative low TOX polish rate.

SUMMARY

[0011] In order to solve the problems emerged during CMP reveal processing, a new method and apparatus for TSVs reveal is developed.

[0012] In an embodiment, the method of the present invention for TSVs reveal includes steps of: providing a Si substrate having a plurality of TSVs formed inside the Si substrate; rotating the Si substrate and spraying a first etchant onto the backside of the Si substrate to etch the backside of the Si substrate, and stopping etching before the TSVs being exposed to the backside of the Si substrate; and rotating the Si substrate and spraying a second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs being exposed to the backside of the Si

substrate, wherein reversing the rotation direction of the Si substrate at fixed intervals during spraying the second etchant onto the backside of the Si substrate.

[0013] In an embodiment, the apparatus of the present invention for TSVs reveal includes a rotatable chuck assembly and at least one nozzle. The chuck assembly is capable of reversing the rotation direction at fixed intervals. The chuck assembly holds and positions a Si substrate having a plurality of TSVs formed inside the Si substrate. The at least one nozzle is disposed above the chuck assembly. The at least one nozzle sprays a first etchant onto the backside of the Si substrate to etch the backside of the Si substrate, and stops spraying before the TSVs are exposed to the backside of the Si substrate. The at least one nozzle sprays a second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs are exposed to the backside of the Si substrate.

[0014] As described above, the present invention utilizes two wet etching steps to reveal the TSVs. Comparing to the CMP reveal method, there are great advantages by using the two wet etching steps: with high etching selectivity for Si and SiO_2; completely preventing Cu from contaminating the Si substrate; obviously decreasing the cost of ownership; avoiding the inborn CMP defects such as scratching, dishing and erosion. Moreover, during the second wet etching step, reversing the rotation direction of the Si substrate at fixed intervals can remove the Si residues leaving in the etching shadows.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The present invention provides a method and an apparatus for TSVs reveal. Other objects and features will become apparent from the following detailed description taken in connection with the accompanying drawings. However, the drawings are provided for purpose of illustration only, and are not intended as a definition of the limits of the invention.

[0016] FIGS. 1a-1h are cross sectional views showing an exemplary process for TSVs reveal according to the present invention;

[0017] FIG. 2 shows a general method for a Si substrate wet etching;

[0018] FIG. 3 shows an improved method for a Si substrate wet etching according to the present invention;

[0019] FIGS. 4a-4b are top views of the Si substrate during the wet etching process;

[0020] FIGS. 5a-5b are edge wet etching comparison views by using the general method and the improved method;

[0021] FIG. 6 is a top view showing an exemplary apparatus for TSVs reveal of the present invention;

[0022] FIG. 7 is a cross sectional view taken along line A-A' shown in FIG. 6;

[0023] FIG. 8 is an enlarged view of B portion shown in FIG. 7;

[0024] FIG. 9 shows another exemplary apparatus for TSVs reveal; and

[0025] FIG. 10 shows another exemplary apparatus for TSVs reveal.

DETAILED DESCRIPTION OF EMBODIMENTS

[0026] The present invention mainly utilizes two-steps wet etching to achieve TSVs reveal. There are generally two types of wet silicon etchants in used: a first etchant with low selectivity for Si and SiO_2 and a second etchant with high selectivity for Si and SiO_2. There are some differences between the first etchant and the second etchant. In general, the first etchant etches the substrate faster than the second etchant but the second etchant offers a more precise and defined profile on the substrate. The first etchant has the same etch rate in all directions, and the etch rate does not greatly depend upon the orientation of the mask. For the second etchant, etch rate depends upon the orientation to crystalline planes, and certain crystal plane is etch attacked

much more rapidly than others. This high etch rate selectivity can be used in the TSVs reveal process. The etch rate is orientation dependent in the crystal. For the case of silicon, <100> and <110> crystal planes are etched much faster than the <111> crystal plane. For example, a solution of KOH, water and alcohol can etch the <100>, <110>, and <111> crystal planes at a relative rate of 40:30:1.

[0027] The first etchant is a strong acid substance such as HN (HF/HNO_3) based solution which has low etching selectivity for Si and SiO_2. The etch rate depends on the ratio of the solution. For example, a solution with low HF and high HNO_3 will result in higher etch rate that is dependent on diffusion limitation. The surface of the substrate is rough while at high etch rate; and at very low etch rate, the surface of the substrate is highly flat and polished. The reaction mechanism is HNO_3 oxidizes Si, and HF removes SiO_2. The chemical equations are as follow:

[0028] $Si+4HNO_3 \rightarrow SiO_2+2H_2O+4NO_2$

[0029] $SiO_2+6HF \rightarrow H_2SiF_6+2H_2O$

[0030] For a $21HNO_3$(70%) mixed with 4HF(49%) 25℃ HN solution, the etch rate for Si is about 13.8μm/min, and the etch rate for SiO_2 is about 8.39μm/min. An accurate control of the etch rate requires a temperature control within ± 0.5°C.

[0031] The second etchant is a strong alkaline substance (pH>12) such as KOH (KOH Based) aqueous solution, TMAH (Tetramethyl Ammonium Hydroxide Based) solution or EDP (Ethylenediamine Pyrocatechol Based) solution. The reaction mechanism is as follow:

[0032] $Si+4OH^- \rightarrow Si(OH)_4+4e^-$

[0033] Since the bonding energy of Si atoms is different for each crystal plane, and KOH/TMAH Si etching is not diffusion but etch rate is limited, Si etching is highly anisotropic. For example, the doping concentration of the Si to be etched also strongly impacts the etching. Specifically, during etching, if the boron doping concentration exceeds $10^{19}cm^{-3}$, boron doped Si forms borosilicate glass on the

surface of the substrate can act as etch stop. Take another example, while the <100> and <110> crystal planes are being etched, the <111> crystal plane is almost not attacked by the second etchant. As a result, for a 44% 85℃ KOH solution, the etch rate ratio of <100> to<110> to <111> is 300:600:1, and the etch rate for <100> crystal plane is about 1.4μm/min, the etch rate for SiO_2 is about 14A/min, the etch rate for Si_3N_4 is less than 1A/min. For a 25% 80℃ TMAH solution, the etch rate ratio of <100> to<110> to <111> is 37:68:1, and the etch rate for <100> crystal plane is about 0.3-1μm/min, the etch rate for SiO_2 is about 2A/min, the etch rate for Si_3N_4 is less than 1A/min. For a 115℃ EDP solution, the etch rate ratio of <100> to<110> to <111> is 20:10:1, and the etch rate for <100> crystal plane is about 1.25μm/min, the etch rate for SiO_2 is about 2A/min, the etch rate for Si_3N_4 is less than 1A/min. For such high etch selectivity characteristic, the SiO_2 or Si_xN_y can be used as a hard mask in KOH based solution, but Si_xN_y is better, and both SiO_2 and Si_xN_y can be used as a hard mask in TMAH and EDP based solutions.

[0034] As described above, a method for TSVs reveal of the present invention will be introduced in detail hereinafter.

[0035] Referring to FIG. 1a, firstly, provide a Si substrate 101 having a plurality of TSVs 102 which are already formed inside the Si substrate 101. The TSVs 102 are filled with Cu encapsulated into a dielectric isolation oxide liner 103 for preventing Cu diffusion during subsequent processing. After the TSVs 102 are formed, a standard full BEOL metallization processing follows, and devices 104 are formed in the Si substrate 101. The subsequent processing step is thinning the backside of the Si substrate 101. In order to guarantee the required mechanical stability and rigidity of the thin Si substrate 101, temporary bonding is a general method, as shown in FIG. 1a, the frontside of the Si substrate 101 is placed facedown and mounted onto a carrier wafer 106 through a glue layer 105. The carrier wafer 106 can be silicon wafer or glass wafer.

[0036] Referring to FIG. 1b, secondly, thin the backside of the Si substrate 101 and stop thinning before the dielectric isolation oxide liner 103 is exposed. A general method for thinning the backside of the Si substrate 101 is grinding. In this processing step, in order to avoid damaging the dielectric isolation oxide liner 103 and Cu filled in the TSVs 102, the Si substrate 101 backside grinding will go to a distance that just close to but not touch the dielectric isolation oxide liner 103, so the TSVs 102 are not exposed. As shown in FIG. 1b, after the backside of the Si substrate 101 undergoes the mechanical grinding, a rough and damaged surface of the backside of the Si substrate 101 is present.

[0037] Referring to FIG. 1c, thirdly, etch the backside of the Si substrate 101 by using a first etchant and stop etching before the dielectric isolation oxide liner 103 is exposed. This is the first wet etching step and a fast bulk Si is etched. The first etchant is a strong acid substance such as HN (HF/HNO_3) based solution. This step removes the Si on the bottom of the TSVs 102, however not exposing the TSVs 102 to the backside of the Si substrate 101 yet, that because the first etchant can also etch the dielectric isolation oxide liner 103. As shown in FIG. 1c, after this processing step, a smooth and cleaning backside of the Si substrate 101 can be obtained.

[0038] Referring to FIG. 1d, fourthly, etch the backside of the Si substrate 101 by using a second etchant until the TSVs 102 are exposed to the backside of the Si substrate 101. The TSVs 102 are revealed. This is the second wet etching step which is a fine and precise etching reaction for Si recessing. The second etchant is a strong alkaline substance such as TMAH-, KOH- or EDP- solution. The second etchant has high selectivity for Si and SiO_2, so the second etchant can be used to reveal the TSVs 102 without damaging the dielectric isolation oxide liner 103. As shown in FIG. 1d, with this two-steps process, the TSVs 102 encapsulated in the Si substrate 101 are revealed and micro-bumps are formed.

[0039] During the two wet etching steps, the first etchant and the second etchant are applied on the backside of the Si substrate 101. For avoiding the first and

second etchants etching the frontside of the Si substrate 101, the carrier wafer 106 can be protected by a protecting liquid like DIW or a protecting gas like N_2.

[0040] Compared to the traditional CMP TSVs reveal process, there are great advantages by using the two wet etching steps: with high etching selectivity for Si and SiO_2; completely preventing Cu from contaminating the Si substrate 101; obviously decreasing the cost of ownership; avoiding the inborn CMP defects such as scratching, dishing and erosion. However, there are also great challenges with this method. The first challenge is how to control the Si TTV (Total Thickness Variation) during the wet etching steps. The second challenge is how to confirm there is no Si residue leaving on the TSVs 102 which have been exposing outside.

[0041] Referring to FIG. 2, a general method for a Si substrate wet etching is shown. The method includes: clockwise rotating the Si substrate 101 during the wet etching process; and spraying the etchant 111 (the first etchant or the second etchant) onto the backside of the Si substrate 101 by using a nozzle 110. The nozzle 110 can scan or swing horizontally from the center of the backside of the Si substrate 101 to the outer edge of the backside of the Si substrate 101. However, there are two great major challenges with this traditional wet etching process.

[0042] The first challenge is, although the nozzle 110 can move across the whole backside of the Si substrate 101, due to the variation of linear velocity between the center and the outer edge of the backside of the Si substrate 101, liquid layer thickness, liquid temperature, etc., the center of the backside of the Si substrate 101 often shows higher Si etch rate, while the outer edge of the backside of the Si substrate 101 often shows lower Si etch rate. As a result, an uniform Si etch rate is hard to be achieved, and it is very difficult to control the TTV (Total Thickness Variation) of the whole Si substrate 101.

[0043] The second challenge is there is often Si residue leaving onto the TSVs 102 which have been exposing outside. In the general wet etching process, the Si substrate 101 only rotates in one direction (clockwise or counterclockwise). Taking a

clockwise rotation for example, the etchant 111 flowing on the backside of the Si substrate 101 often spreads out from the center to the outer edge of the backside of the Si substrate 101, so the etch rate along the etchant flowing direction would be higher than that against the etchant flowing direction. In the center region, both sides of the TSVs 102 are located in a upstream area. In the right half region of the backside of the Si substrate 101, the left side of the TSVs 102 is located in a downstream area, and the right side of the TSVs 102 is located in a upstream area. While in the left half region of the backside of the Si substrate 101, the right side of the TSVs 102 is located in a downstream area, and the left side of the TSVs 102 is located in a upstream area. As shown in FIG. 2, it defines the sides of the TSVs 102 that are located in the downstream area as fast etching region, which is represented by the number 108. It also defines the sides of the TSVs 102 that are located in the upstream area as low etching region or etching shadow, which is represented by the number 109. There would be easy to leave Si residues at the etching shadows 109 with a traditional wet etching method. Besides, when the nozzle 110 moves on the outer edge of the backside of the Si substrate 101 for etching the Si residues at the etching shadows 109, if the chuck rotation speed is not high enough at that time, the etchant 111 sprayed on the backside of the Si substrate 101 has not enough time to achieve a synchronous speed with the Si substrate 101 so that the etchant 111 would fly out directly and the etching shadows 109 at the outer edge of the backside of the Si substrate 101 cannot be etched uniformly. Moreover, the Si substrate 101 are generally positioned on a chuck assembly by a plurality of pins. If the etchant 111 flies out, the etchant 111 may strike the pins, which results in splashing, as shown in FIG. 5a. The scattered etchant 111 contaminates the processing chamber.

[0044] In order to overcome these challenges, an improved method is put forward in this invention.

[0045] With reference to FIG. 3, the method includes spraying the etchant 111 (the first etchant or the second etchant) onto the backside of the Si substrate 101 by using a nozzle 110. The nozzle 110 can scan or swing horizontally from the center of

the backside of the Si substrate 101 to the outer edge of the backside of the Si substrate 101, and the horizontal move speed and acceleration of the nozzle 110 can be adjustable. For example, the nozzle 110 moves at a high speed above the center region of the backside of the Si substrate 101 and at a low speed above the edge region of the backside of the Si substrate 101. Furthermore, it is allowable to set a nozzle resting position during the wet etching process. Moreover, the nozzle 110 can also move vertically to be close to or far away from the backside of the Si substrate 101. With these new functions, the etch rate at each point can be well controlled, and a uniform Si etch rate can be achieved in various regions of the backside of the Si substrate 101.

[0046] Referring to FIG. 3 again, the method further includes changing spraying angle of the nozzle 110 during the wet etching process. For example, when the nozzle 110 is located above the center of the backside of the Si substrate 101, the spraying angle can be vertical with the backside of the Si substrate 101. When the nozzle 110 is located above the right half region of the backside of the Si substrate 101, the nozzle 110 can be an acute angle with the backside of the Si substrate 101, and the spraying angle range is from 0~90° . When the nozzle 110 is located above the left half region of the backside of the Si substrate 101, the nozzle 110 can be an obtuse angle with the backside of the Si substrate 101, the spraying angle range is from 90~180° . With this function, the Si residues leaving in the etching shadows 109 can be removed.

[0047] Please refer to FIGS. 4a-4b showing another method. The method includes the steps of reversing the rotating direction of the Si substrate 101 during the second etchant wet etching process, in which clockwise rotation mode and counterclockwise rotation mode are used alternatively. Referring to FIG. 4a, at the beginning of the wet etching process, when the etchant 111 flowing on the backside of the Si substrate 101, rotating the Si substrate 101 at a clockwise (or counterclockwise) rotation direction, due to centrifugal force and inertia effect, liquid droplet will fly off

the outer edge of the backside of the Si substrate 101 along tangent track at an anti-clockwise direction. As mentioned above, the number 108 represents the sides of the TSVs 102 that are located in a downstream area defined as fast etching region; and the number 109 represents the sides of the TSVs 102 that are located in an upstream area defined as etching shadow. It is very easy to leave Si residues in the etching shadows 109.

[0048] Referring to FIG. 4b, after an adjustable time interval, counter rotating the Si substrate 101, the etchant 111 flow direction on the backside of the Si substrate 101 is changed from anti-clockwise to clockwise. And the etching shadows 109 region shifts as the rotation direction of the Si substrate 101 reversed. This countercurrent etching method is benefit for removing the Si residues leaving in the etching shadows 109. Furthermore, for removing the Si residues leaving in the etching shadows 109 located at the outer edge of the backside of the Si substrate 101, the method further includes moving the nozzle 110 above the outer edge of the backside of the Si substrate 101 and then rotating the Si substrate 101 at a speed which is higher than the rotation speed of the Si substrate 101 when the nozzle 110 is above the center region of the backside of the Si substrate 101, so that the etchant 111 has enough time to achieve a synchronous speed with the Si substrate 101, as shown in FIG. 5b. Therefore the Si residues leaving in the etching shadows 109 located at the outer edge of the backside of the Si substrate 101 can be removed and no splashing happens. The rotation speed of the Si substrate 101 can be ranged from 800rpm to 2000rpm when the nozzle 110 is above the outer edge of the backside of the Si substrate 101.

[0049] With reference to FIGS. 1e-1h, after the TSVs 102 are revealed by the above methods, for connecting with another chip, the Cu encapsulated into the dielectric isolation oxide liner 103 needs to be exposed to outside. Therefore, the method for TSVs 102 reveal further includes: depositing SiO_2/Si_3N_4 112 on the backside of the Si substrate 101; coating PR 113 on the SiO_2/Si_3N_4 112; taking an etchback to remove the PR 113, SiO_2/Si_3N_4 112 and dielectric isolation oxide liner

103 on the bottom of the TSVs 102 and the Cu is exposed to outside; at last, removing the rest PR 113 from the backside of the Si substrate 101.

[0050] Referring to FIG. 6 and FIG. 7, an apparatus for TSVs reveal of the present invention is illustrated. The apparatus 200 includes a rotatable chuck assembly 201 connected with a rotary spindle (not shown). The chuck assembly 201 is optimally circular for supporting and positioning a Si substrate 203. The Si substrate 203 has a plurality of TSVs which are already formed inside the Si substrate 203 and the backside of the Si substrate 203 is thinned by grinding. The frontside of the Si substrate 203 is temporarily bonded onto a carrier wafer 202 through a glue layer. The rotation direction of the chuck assembly 201 can be clockwise and counter clockwise alternately. The chuck assembly 201 further defines a plurality of through holes 207 passing therethrough. The through holes 207 can be vertical or can form an angle with respect to the bottom surface of the chuck assembly 201. The chuck assembly 201 further includes a plurality of, e.g., six locating pins 206. These locating pins 206 are uniformly disposed at the outer edge of the top surface of the chuck assembly 201. The purpose of the locating pins 206 is for holding and positioning the Si substrate 203. A protecting ring 204a is disposed on the outer edge of the top surface of the chuck assembly 201 and surrounds the Si substrate 203. The protecting ring 204a can be detachable. According to different requirements, the protecting ring 204a can be dismounted from the chuck assembly 201 or mounted on the chuck assembly 201. In one embodiment, the protecting ring 204a defines a plurality of, e.g., six openings (not shown) for assembing the locating pins 206. In another embodiment, the protecting ring 204a is divided into e.g., six sections and each section is settled between every two adjacent locating pins 206. The locating pins 206 and the protecting ring 204a can be made of plastic which can keep the shape and be chemical compatible such as PVDF (Poly Vinylidene Fluoride), PP (Polypropylene), PTFE (Polytetrafluoroetylene), PEEK (Polyetheretherketone).

[0051] There is at least one nozzle 205 above the chuck assembly 201 for spraying the etchant 111 onto the backside of the Si substrate 203. The etchant 111

can be: a first etchant with low selectivity for Si and SiO_2, such as HN (HF/HNO_3) based solution for bulk Si etching, a second etchant with high selectivity for Si and SiO_2, such as TMAH-, KOH- or EDP- based solution for fine and precise Si recessing, DIW for rinsing the backside of the Si substrate 203, IPA for drying the backside of the Si substrate 203, hot or room temperature N_2 for drying the backside of the Si substrate 203, etc. The nozzle 205 can scan or swing horizontally from the center to outer edge of the backside of the Si substrate 203. The horizontal move speed and acceleration of the nozzle 205 can be adjustable, and it is allowable to set a nozzle resting position during wet etching process. Moreover, the nozzle 205 can move vertically to be close to or far away from the backside of the Si substrate 203, and can also change its spraying angle during the wet etching process.

[0052] For preventing the etchant 111 from etching the carrier wafer 202 and further etching the frontside of the Si substrate 203, a protecting gas 208 such as N_2 is supplied onto the surface of the carrier wafer 202 through the through holes 207, and the protecting ring 204a is used for shaping the airflow of the protecting gas 208 to further protect the carrier wafer 202 from chemical etching. If the protecting gas 208 is chosen for protecting the carrier wafer 202 from chemical etching, the chuck assembly 201 is preferable a Bernoulli chuck.

[0053] Please refer to FIG. 8 to FIG. 10. FIG. 8 shows the protecting ring 204a is jointed on the chuck assembly 201 and the inner wall of the protecting ring 204a is a vertical plane. The airflow of the protecting gas 208 is guided to curl upwards along the inner wall of the protecting ring 204a after the protecting gas 208 goes through the through holes 207, and then the protecting gas 208 spreads out from the edge of the carrier wafer 202. By this means, a gas cushion is formed and restricted in a shaped region for protecting the carrier wafer 202 from chemical etching.

[0054] FIG. 9 shows another exemplary apparatus. Comparing to the apparatus 200, the difference is the protecting ring. In this apparatus, a protecting ring 204b is jointed on the chuck assembly 201 and the inner wall of the protecting ring 204b is an

irregular plane. The airflow of the protecting gas 208 is guided to curl upwards along the inner wall of the protecting ring 204b after the protecting gas 208 goes through the through holes 207, and then the protecting gas 208 spreads out from the edge of the carrier wafer 202. By this means, a gas cushion is formed and restricted in a shaped region for protecting the carrier wafer 202 from chemical etching.

[0055] FIG. 10 shows another exemplary apparatus. Comparing to the apparatus 200, the difference is the protecting ring. In this apparatus, a protecting ring 204c is separated from the chuck assembly 201 so that a gap is formed between the protecting ring 204c and the chuck assembly 201. The protecting ring 204c can be supported by a plurality of pillars (not shown) which are connected with the chuck assembly 201. By this means, the airflow of the protecting gas 208 is divided into two parts. One part is guided to curl upwards along the inner wall of the protecting ring 204c after the protecting gas 208 goes through the through holes 207, and then spreads out from the edge of the carrier wafer 202. The other part flows out of the chuck assembly 201 from the gap between the protecting ring 204c and the chuck assembly 201. By this means, a gas cushion is formed and restricted in a shaped region for protecting the carrier wafer 202 from chemical etching.

[0056] Besides the protecting gas 208, a protecting liquid like DIW also can be used to protect the carrier wafer 202 from chemical etching. If choosing the protecting liquid, the protecting ring 204a/204b/204c needs to be removed from the apparatus and the chuck assembly 201 can be a general chuck. The protecting liquid is supplied onto the surface of the carrier wafer 202 through the through holes 207 to protect the carrier wafer 202 from chemical etching.

[0057] As described above, according to an exemplary apparatus, a method for TSVs reveal may comprise:

[0058] Step 1: Measure the Si substrate 203 thickness before process, and the thickness from the dielectric isolation oxide liner to the surface of the backside of the Si substrate 203 is known. The silicon etch rate for the first etchant and the second

etchant can be further obtained by empirical values from volume test. Therefore, the process time can be calculated. It shall be particularly pointed out that the Si substrate 203 has finished the TSVs formation and been processing the standard full BEOL metallization.

[0059] Step 2: Place the Si substrate 203 face down on the chuck assembly 201.

[0060] Step 3: Rotate the chuck assembly 201 at a speed range from 10 to 1500rpm.

[0061] Step 4: Supply DIW from the nozzle 205 onto the backside of the Si substrate 203 for pre wetting the backside of the Si substrate 203, and meanwhile, supply the protecting liquid onto the carrier wafer 202 from the through holes 207 for preventing the liquid supplied onto the backside of the Si substrate 203 from flowing onto the carrier wafer 202.

[0062] Step 5: Stop supplying DIW onto the backside of the Si substrate 203.

[0063] Step 6: Supply a first etchant such as HN (HF/HNO_3) based solution from the nozzle 205 onto the backside of the Si substrate 203, with a flowrate from 0.5LPM to 5LPM, preferably from 0.8LPM to 2LPM. The ratio of HNO_3 and HF can range from 1:1 to 20: 1. The temperature of the solution can range from 20℃ to 45℃.The process time is determined by etch rate. During step 6, the nozzle 205 moves both in a horizontal direction from the center to outer edge of the backside of the Si substrate 203 and in a vertical direction close to or far away from the backside of the Si substrate 203. For the horizontal direction motion, the nozzle 205 moves at a high speed above the center region of the backside of the Si substrate 203 and at a low speed above the edge region of the backside of the Si substrate 203. For the vertical direction motion, the moving distance between the nozzle 205 and the backside of the Si substrate 203 is between 0.5cm to 10cm. Several nozzle resting positions are set across the backside of the Si substrate 203. This step is used for removing the Si on the bottom of the TSVs, but not exposing the TSVs to outside, that because the first etchant can also etch the dielectric isolation oxide liner. Preferably, after etching by

using the first etchant, dry the Si substrate 203 and then measure the thickness of the Si substrate 203 for obtaining the next step processing time.

[0064] Step 7: Supply a second etchant such as TMAH based solution from the nozzle 205 onto the backside of the Si substrate 203, with a flowrate from 0.3LPM to 3LPM, preferably from 0.5LPM to 2LPM. The concentration of TMAH can range from 2% to 25%. The temperature of the solution can range from 25℃ to 90℃. The process time is determined by etch rate. During this step, reverse the rotating direction of the Si substrate 203 at fixed intervals, and the interval time can be set from 5s to 60s.

[0065] During step 7, the nozzle 205 moves both in a horizontal direction from the center to outer edge of the backside of the Si substrate 203 and in a vertical direction close to or far away from the backside of the Si substrate 203. For the horizontal direction motion, the nozzle 205 moves at a high speed above the center region of the backside of the Si substrate 203 and at a low speed above the edge region of the backside of the Si substrate 203. For the vertical direction motion, the moving distance between the nozzle 205 and the backside of the Si substrate 203 is between 0.5cm to 10cm. Several nozzle resting positions are set across the backside of the Si substrate 203. During the wet etching process, the nozzle 205 spraying angle changes. When the nozzle 205 is located above the center region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be vertical with the backside of the Si substrate 203. When the nozzle 205 is located above the right half region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be an acute angle with the backside of the Si substrate 203, and the angle range is from 0~90 °. When the nozzle 205 is located above the left half region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be an obtuse angle with, the backside of the Si substrate 203, and the angle range is from 90~180°. When the nozzle 205 moves above the outer edge of the backside of the Si substrate 203, the chuck assembly 201 rotates at a speed which is higher than the rotation speed of the Si

substrate 203 when the nozzle 205 is above the center region of the backside of the Si substrate 203, so that the etchant has enough time to achieve a synchronous speed with the Si substrate 203. Therefore the Si residues leaving in the etching shadows located at the outer edge of the backside of the Si substrate 203 can be removed and no splashing happens. The rotation speed of the chuck assembly 201 can be as high as 2000rpm when the nozzle 205 is above the outer edge of the backside of the Si substrate 203.

[0066] Step 8: Supply DIW from the nozzle 205 onto the backside of the Si substrate 203 for post rinsing the backside of the Si substrate 203. The process time can range from 10 to 60s.

[0067] Step 9: Stop supplying DIW onto the backside of the Si substrate 203, and stop supplying the protecting liquid onto the carrier wafer 202.

[0068] Step 10: Rotate the chuck assembly 201 at a predefined high speed that ranges from 1000 to 3000rpm.

[0069] Step 11: Supply a gas or a vapor for drying the Si substrate 203 with a flowrate from 1slm to 10slm, preferably from 4slm to 6slm. The process time can range from 10 to 60s.

[0070] Step 12: Measure the thickness of the Si substrate 203 for making sure that the etch rate is uniform within a Si substrate 203 and between Si substrates 203.

[0071] According to another exemplary apparatus of the present invention, a method for TSVs reveal may comprise:

[0072] Step 1: Measure the Si substrate 203 thickness before process, and the thickness from the dielectric isolation oxide liner to the surface of the backside of the Si substrate 203 is known. The silicon etch rate for the first etchant and the second etchant can be further obtained by empirical values from volume test. Therefore, the process time can be calculated. It shall be particularly pointed out that the Si substrate

203 has finished the TSVs formation and been processing the standard full BEOL metallization.

[0073] Step 2: Place the Si substrate 203 face down on the chuck assembly 201.

[0074] Step 3: Supply the protecting gas 208 onto the carrier wafer 202 through the through holes 207. A gas cushion is then formed for preventing the liquid supplied onto the backside of the Si substrate 203 from flowing onto the carrier wafer 202.

[0075] Step 4: Rotate the chuck assembly 201 at a speed range from 10 to 1500rpm.

[0076] Step 5: Supply DIW from the nozzle 205 onto the backside of the Si substrate 203 for pre wetting the backside of the Si substrate 203. The process time can range from 1 to 20s.

[0077] Step 6: Supply a first etchant such as HN (HF/HNO_3) based solution from the nozzle 205 onto the backside of the Si substrate 203, with a flowrate from 0.5LPM to 5LPM, preferably from 0.8LPM to 2LPM. The ratio of HNO_3 and HF can range from 1:1 to 20: 1. The temperature of the solution can range from 20℃ to 45℃. The process time is determined by etch rate. During step 6, the nozzle 205 moves both in a horizontal direction from the center to outer edge of the backside of the Si substrate 203 and in a vertical direction close to or far away from the backside of the Si substrate 203. For the horizontal direction motion, the nozzle 205 moves at a high speed above the center region of the backside of the Si substrate 203 and at a low speed above the edge region of the backside of the Si substrate 203. For the vertical direction motion, the moving distance between the nozzle 205 and the backside of the Si substrate 203 is between 0.5cm to 10cm. Several nozzle resting positions are set across the backside of the Si substrate 203. This step is used for removing the Si on the bottom of the TSVs, but not exposing the TSVs to outside, that because the first etchant can also etch the dielectric isolation oxide liner. Preferably, after etching by

using the first etchant, dry the Si substrate 203 and then measure the thickness of the Si substrate 203 for obtaining the next step processing time.

[0078] Step 7: Supply a second etchant such as TMAH based solution from the nozzle 205 onto the backside of the Si substrate 203, with a flowrate from 0.3LPM to 3LPM, preferably from 0.5LPM to 2LPM. The concentration of TMAH can range from 2% to 25%. The temperature of the solution can range from 25℃ to 90℃. The process time is determined by etch rate. During this step, reverse the rotating direction of the Si substrate 203 at fixed intervals, and the interval time can be set from 5s to 60s.

[0079] During step 7, the nozzle 205 moves both in a horizontal direction from the center to outer edge of the backside of the Si substrate 203 and in a vertical direction close to or far away from the backside of the Si substrate 203. For the horizontal direction motion, the nozzle 205 moves at a high speed above the center region of the backside of the Si substrate 203 and at a low speed above the edge region of the backside of the Si substrate 203. For the vertical direction motion, the moving distance between the nozzle 205 and the backside of the Si substrate 203 is between 0.5cm to 10cm. During the wet etching process, the nozzle 205 spraying angle changes. When the nozzle 205 is located above the center region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be vertical with the backside of the Si substrate 203. When the nozzle 205 is located above the right half region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be an acute angle with the backside of the Si substrate 203, and the angle range is from 0~90° . When the nozzle 205 is located above the left half region of the backside of the Si substrate 203, the spraying angle of the nozzle 205 can be an obtuse angle with, the backside of the Si substrate 203, and the angle range is from 90~180° . When the nozzle 205 moves above the outer edge of the backside of the Si substrate 203, the chuck assembly 201 rotates at a speed which is higher than the rotation speed of the Si substrate 203 when the nozzle 205 is above the center region of the backside

of the Si substrate 203, so that the etchant has enough time to achieve a synchronous speed with the Si substrate 203. Therefore the Si residues leaving in the etching shadows located at the outer edge of the backside of the Si substrate 203 can be removed and no splashing happens. The rotation speed of the chuck assembly 201 when the nozzle 205 is above the outer edge of the backside of the Si substrate 203 can be as high as 2000rpm.

[0080] Step 8: Supply DIW from the nozzle 205 onto the backside of the Si substrate 203 for post rinsing the backside of the Si substrate 203. The process time can range from 10 to 60s.

[0081] Step 9: Stop supplying DIW onto the backside of the Si substrate 203.

[0082] Step 10: Rotate the chuck assembly 201 at a predefined high speed that ranges from 1000 to 3000rpm.

[0083] Step 11: Supply a gas or a vapor for drying the Si substrate 203 with a flow rate from 1slm to 10slm, preferably from 4slm to 6slm. The process time can range from 10 to 60s.

[0084] Step 12: Stop supplying the protecting gas 208 onto the carrier wafer 202.

[0085] Step 13: Measure the thickness of the Si substrate 203 for making sure that the etch rate is uniform within a Si substrate 203 and between Si substrates 203.

[0086] Although the present invention has been described with respect to certain embodiments, examples, and applications, it will be apparent to those skilled in the art that various modifications and changes may be made without departing from the invention.

What is claimed is:

1. A method for TSVs reveal, comprising:

providing a Si substrate having a plurality of TSVs formed inside the Si substrate;

rotating the Si substrate and spraying a first etchant onto the backside of the Si substrate to etch the backside of the Si substrate, and stopping etching before the TSVs being exposed to the backside of the Si substrate; and

rotating the Si substrate and spraying a second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs being exposed to the backside of the Si substrate, and reversing the rotation direction of the Si substrate at fixed intervals during spraying the second etchant onto the backside of the Si substrate.

2. The method of claim 1, wherein the first etchant is a strong acid substance having a low selectivity for Si and SiO_2.

3. The method of claim 2, wherein the strong acid substance is HN (HF/HNO_3) based solution.

4. The method of claim 1, wherein the second etchant is a strong alkaline substance having a high selectivity for Si and SiO_2.

5. The method of claim 4, wherein the strong alkaline substance is TMAH-, KOH- or EDP- based solution.

6. The method of claim 1, wherein reversing the rotation direction of the Si substrate at fixed intervals further comprises:

rotating the Si substrate along clockwise direction and counterclockwise direction alternatively at fixed intervals.

7. The method of claim 1, wherein the first etchant and the second etchant are respectively sprayed onto the backside of the Si substrate by a nozzle.

8. The method of claim 7, further comprising:

moving the nozzle horizontally from the center to outer edge of the backside of the Si substrate during the etching steps.

9. The method of claim 8, wherein the horizontal move speed of the nozzle at the center region of the backside of the Si substrate is higher than at the edge region of the backside of the Si substrate.

10. The method of claim 8, further comprising:

setting nozzle resting positions during the nozzle moving horizontally from the center to outer edge of the backside of the Si substrate.

11. The method of claim 7, further comprising:

moving the nozzle vertically to be close to or far away from the backside of the Si substrate.

12. The method of claim 11, wherein the moving distance between the nozzle and the backside of the Si substrate is between 0.5cm to 10cm.

13. The method of claim 7, further comprising:

changing spraying angle of the nozzle along with the nozzle being located at different region of the backside of the Si substrate during spraying the second etchant

onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs are exposed to the backside of the Si substrate.

14. The method of claim 7, wherein rotating the Si substrate and spraying a second etchant onto the backside of the Si substrate further comprises:

moving the nozzle above the outer edge of the backside of the Si substrate and rotating the Si substrate at a speed which is higher than the rotation speed of the Si substrate when the nozzle is above the center region of the backside of the Si substrate, so that the second etchant achieves a synchronous speed with the Si substrate.

15. The method of claim 1, further comprising:

supplying a protecting gas or protecting liquid onto the frontside of the Si substrate to protect the frontside of the Si substrate from etching during the etching steps.

16. The method of claim 1, further comprising:

supplying DIW onto the backside of the Si substrate for pre wetting the backside of the Si substrate before spraying the first etchant onto the backside of the Si substrate.

17. The method of claim 1, further comprising:

supplying DIW onto the backside of the Si substrate for post rinsing the backside of the Si substrate after spraying the second etchant onto the backside of the Si substrate.

18. The method of claim 17, further comprising:

rotating the Si substrate at a predefined high speed and supplying a gas or a vapor for drying the Si substrate after spraying DIW onto the backside of the Si substrate for post rinsing.

19. The method of claim 1, further comprising:

measuring steps which comprising measuring the Si substrate thickness before spraying the first etchant onto the backside of the Si substrate, after etching by using the first etchant, and after etching by using the second etchant.

20. An apparatus for TSVs reveal, comprising:

a rotatable chuck assembly capable of reversing the rotation direction at fixed intervals, the chuck assembly holding and positioning a Si substrate having a plurality of TSVs formed inside the Si substrate; and

at least one nozzle disposed above the chuck assembly, the at least one nozzle spraying a first etchant onto the backside of the Si substrate to etch the backside of the Si substrate, and stopping spraying before the TSVs are exposed to the backside of the Si substrate, the at least one nozzle spraying a second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs are exposed to the backside of the Si substrate.

21. The apparatus of claim 20, wherein the chuck assembly rotates clockwise and counterclockwise alternately at fixed intervals when the at least one nozzle sprays the second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs are exposed to the backside of the Si substrate.

22. The apparatus of claim 20, wherein the chuck assembly defines a plurality of through holes through where a protecting gas or protecting liquid is supplied onto the frontside of the Si substrate.

23. The apparatus of claim 20, wherein the at least one nozzle scans or swings horizontally from the center to outer edge of the backside of the Si substrate.

24. The apparatus of claim 23, wherein the horizontal move speed and acceleration of the nozzle is adjustable.

25. The apparatus of claim 23, further comprising nozzle resting positions being set during the nozzle scanning or swinging horizontally from the center to outer edge of the backside of the Si substrate.

26. The apparatus of claim 20, wherein the nozzle moves vertically to be close to or far away from the backside of the Si substrate.

27. The apparatus of claim 26, wherein the moving distance between the nozzle and the backside of the Si substrate is between 0.5cm to 10cm.

28. The apparatus of claim 20, wherein the spraying angle of the nozzle is changable along with the nozzle being located at different region of the backside of the Si substrate when the at least one nozzle sprays the second etchant onto the backside of the Si substrate to etch the backside of the Si substrate until the TSVs are exposed to the backside of the Si substrate.

29. The apparatus of claim 20, wherein the at least one nozzle moves above the outer edge of the backside of the Si substrate and the chuck assembly rotates at a speed which is higher than the rotation speed of the chuck assembly when the nozzle is above the center region of the backside of the Si substrate, so that the second etchant achieves a synchronous speed with the Si substrate.

30. The apparatus of claim 22, further comprising a protecting ring disposed on the chuck assembly for shaping the airflow of the protecting gas.

31. The apparatus of claim 30, wherein the protecting ring is detachable from the chuck assembly.

32. The apparatus of claim 30, wherein the inner wall of the protecting ring is a vertical plane or an irregular plane.

33. The apparatus of claim 30, wherein the protecting ring is jointed on the chuck assembly or separated from the chuck assembly to form a gap therebetween.

34. The apparatus of claim 20, further comprising a plurality of locating pins uniformly disposed at the chuck assembly for holding and positioning the Si substrate.

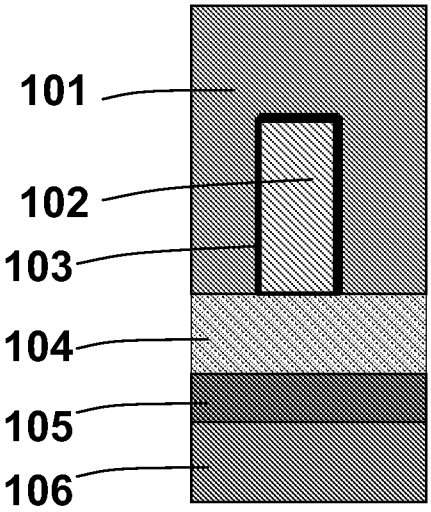

FIG 1a

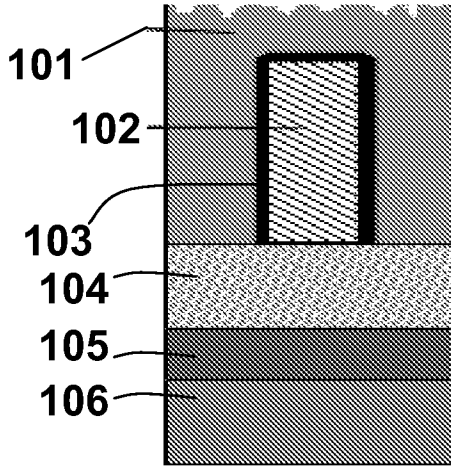

FIG 1b

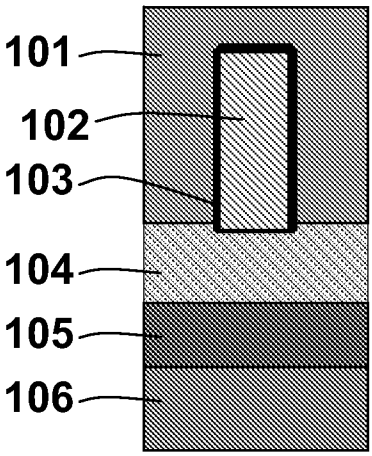

FIG 1c

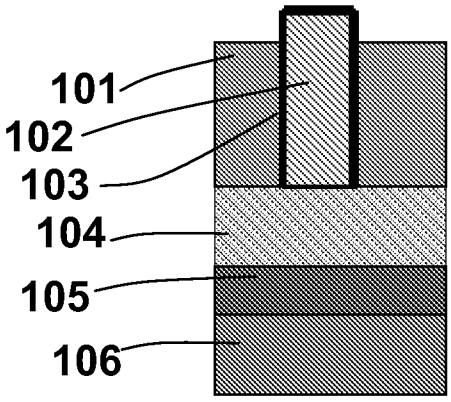

FIG 1d

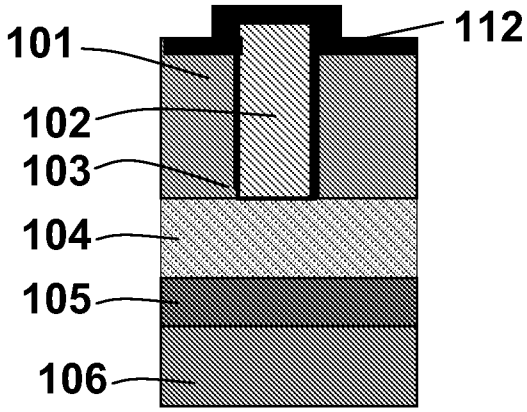

FIG 1e

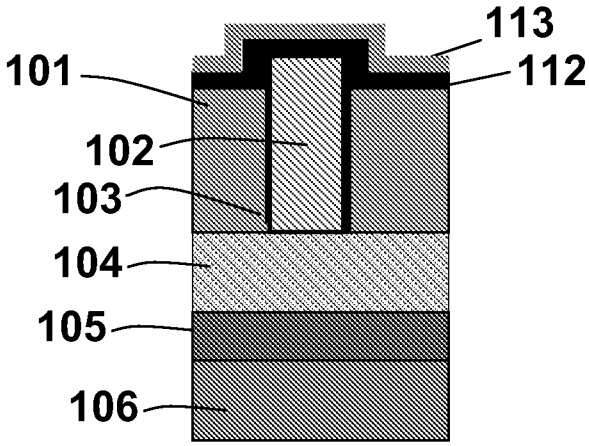

FIG 1f

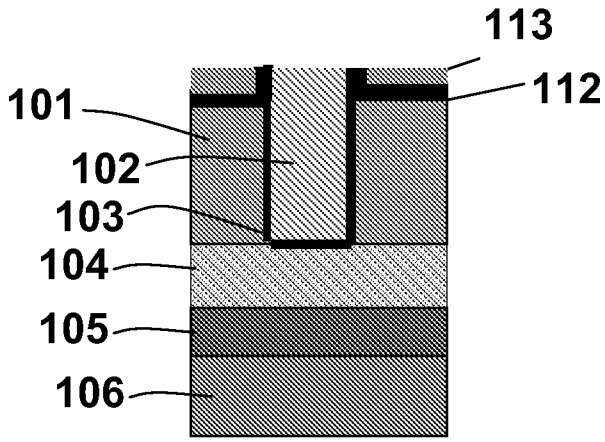

FIG 1g

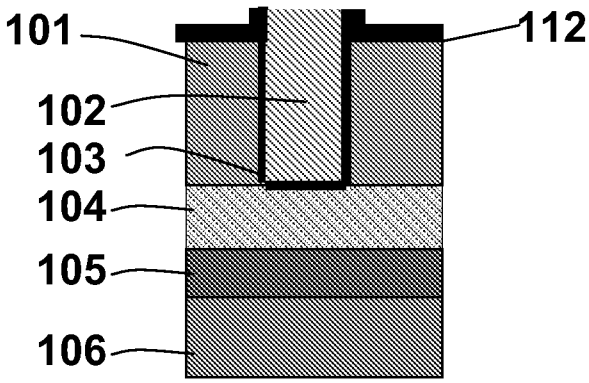

FIG 1h

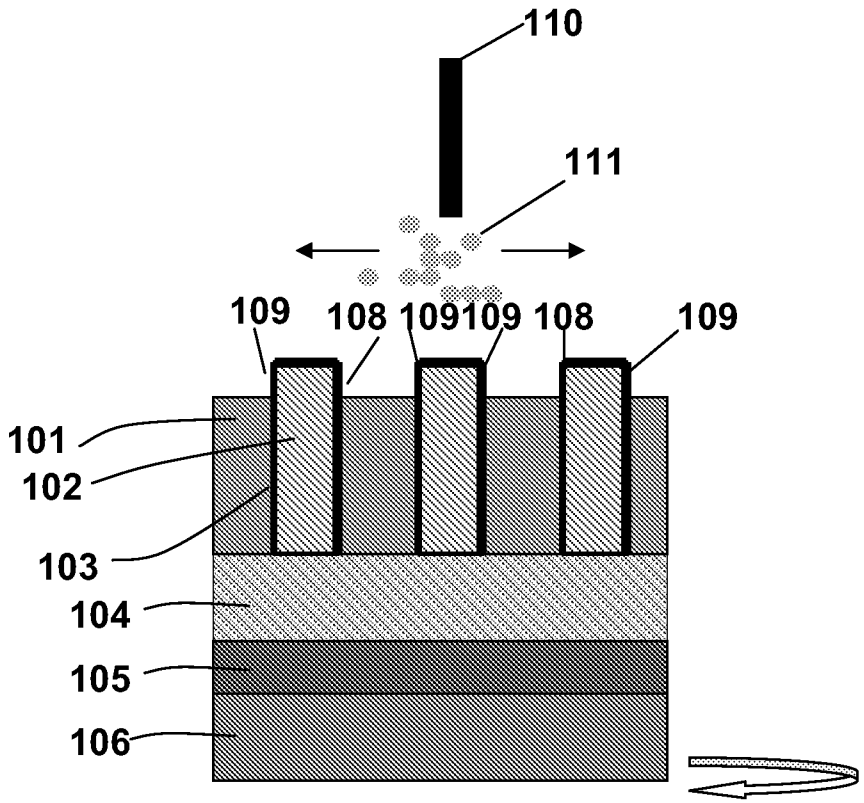

FIG 2

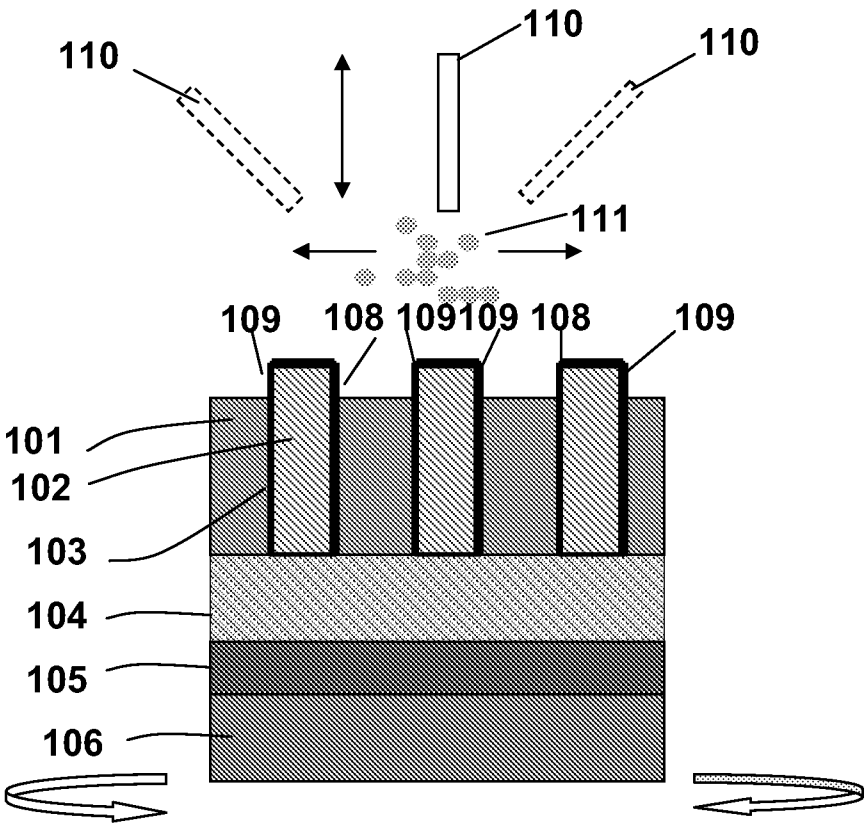

FIG 3

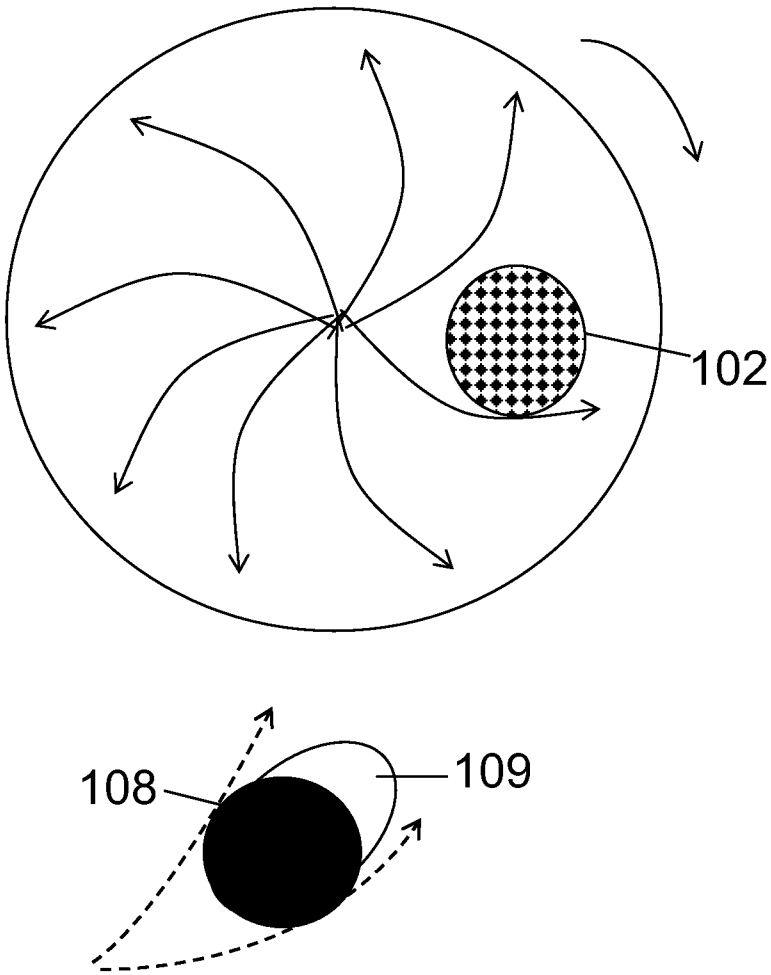

FIG 4a

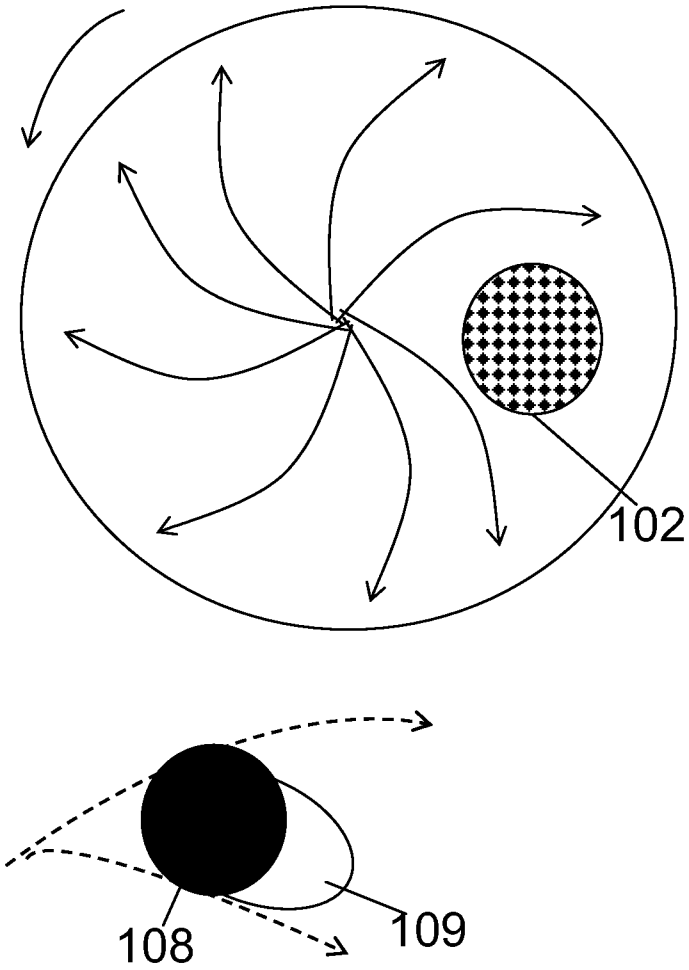

FIG 4b

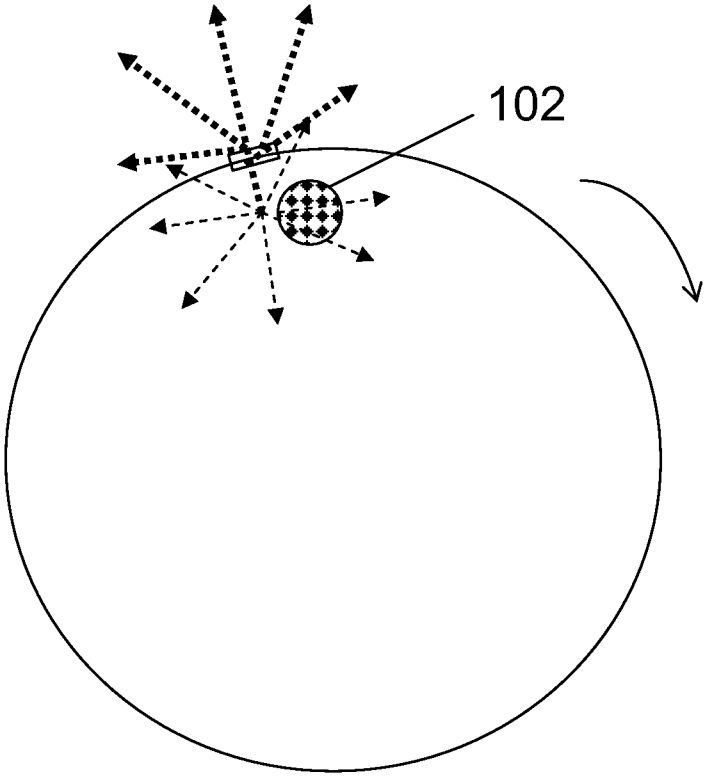

FIG 5a

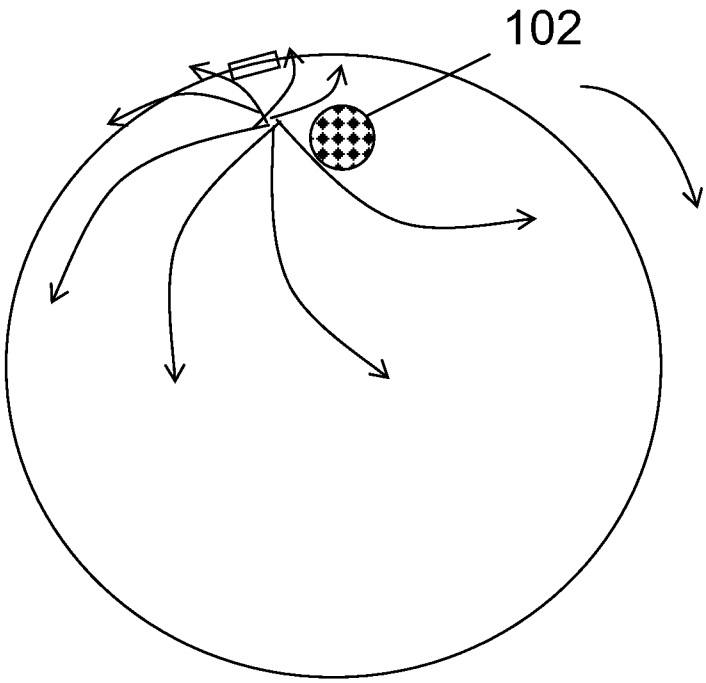

FIG 5b

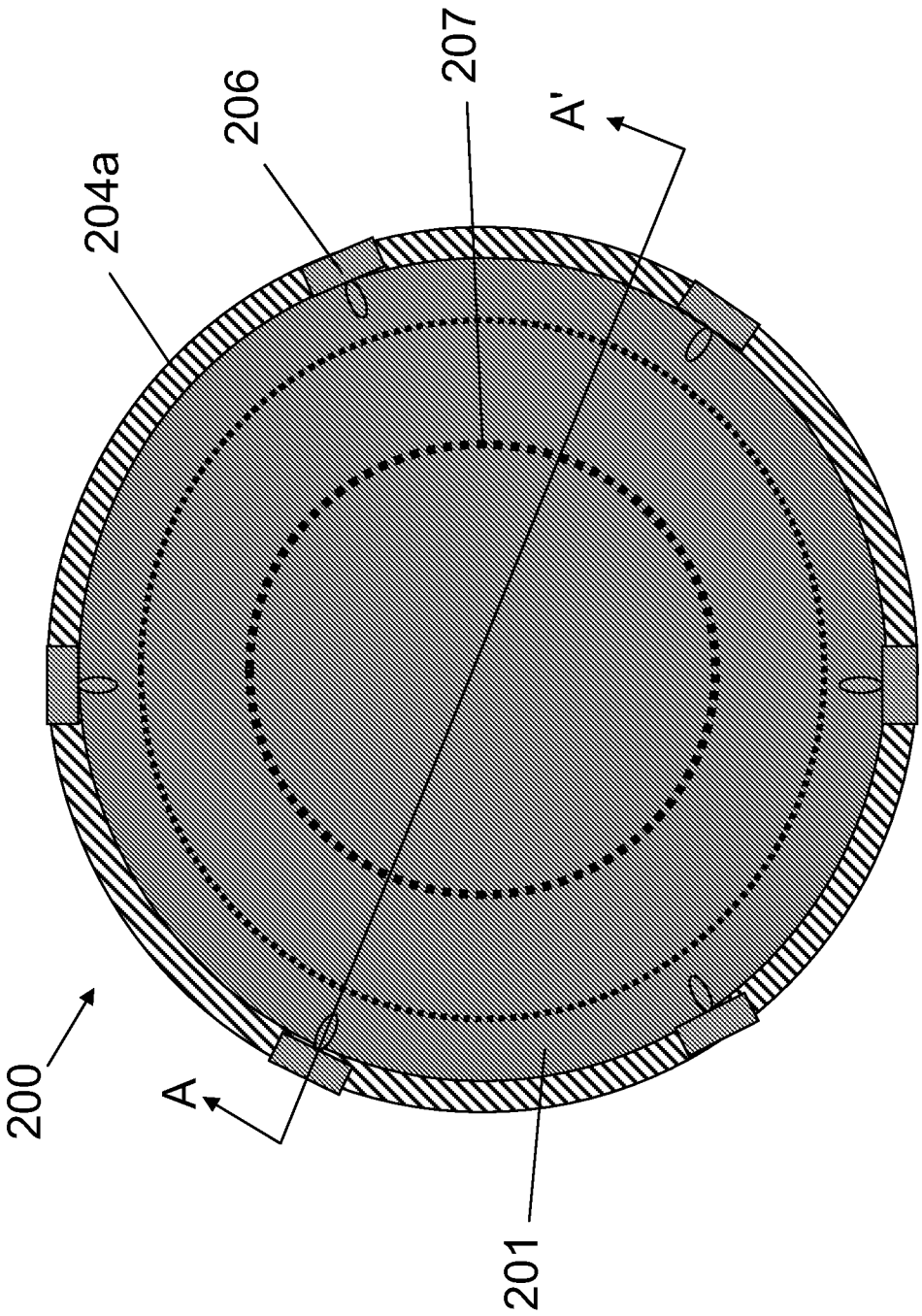

FIG 6

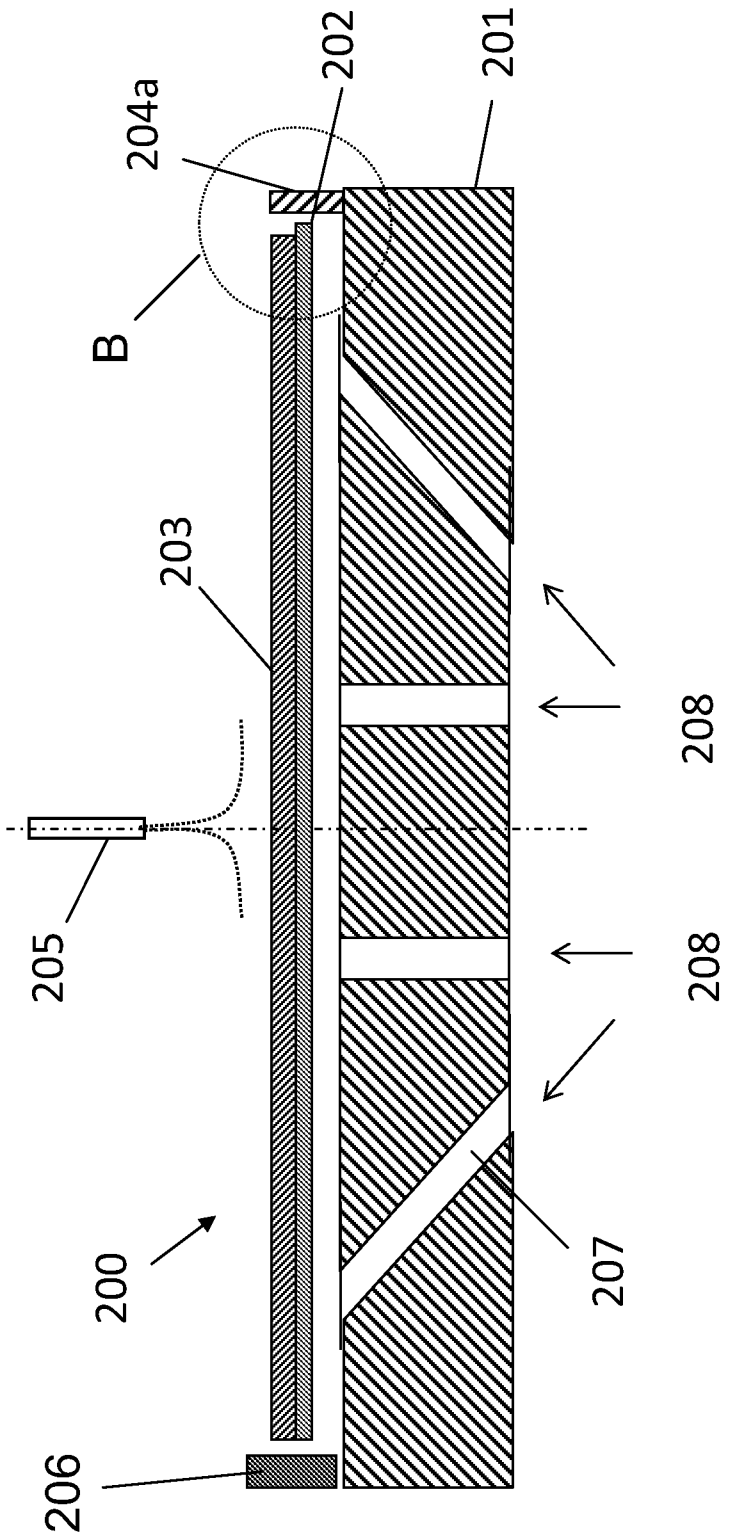

FIG 7

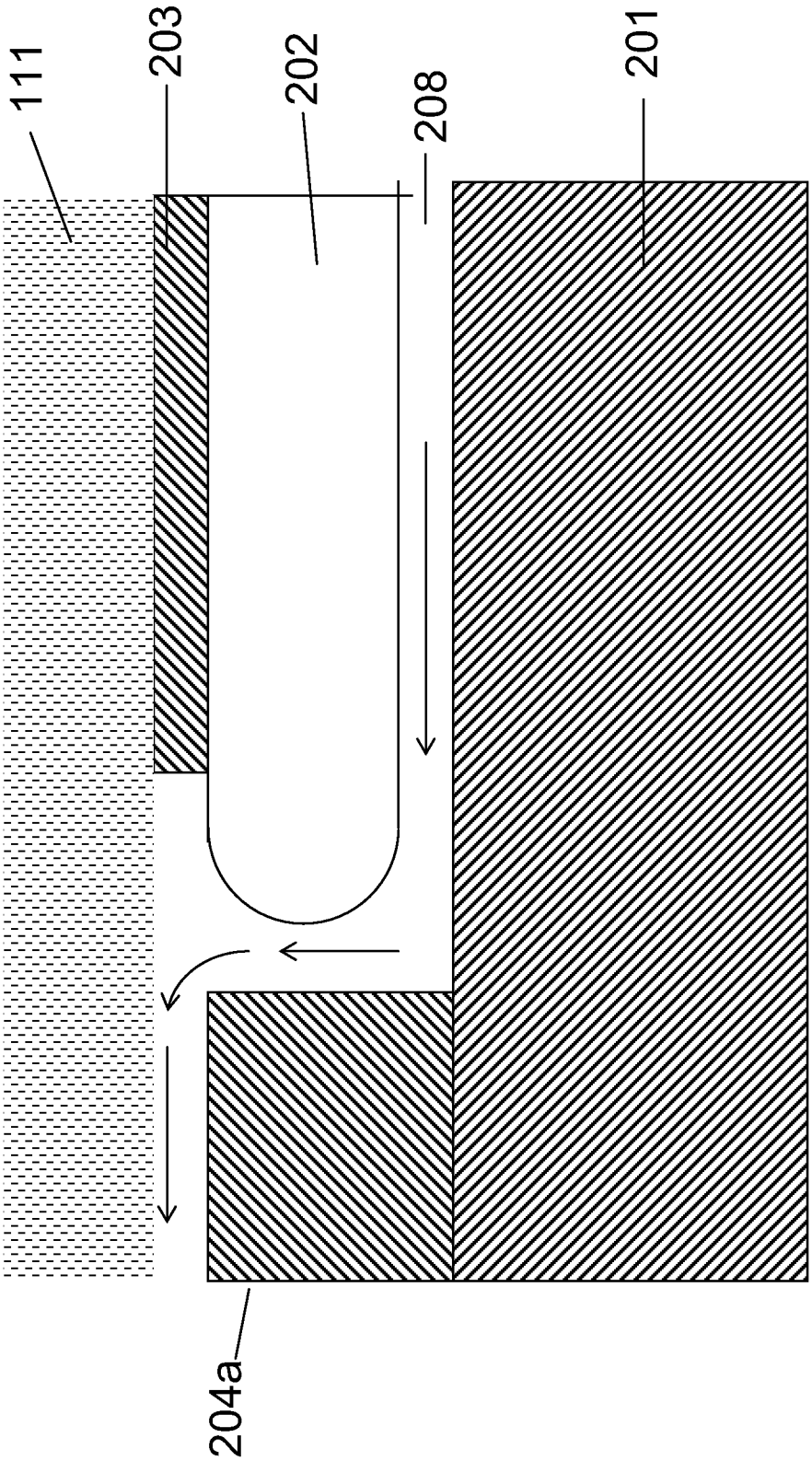

FIG 8

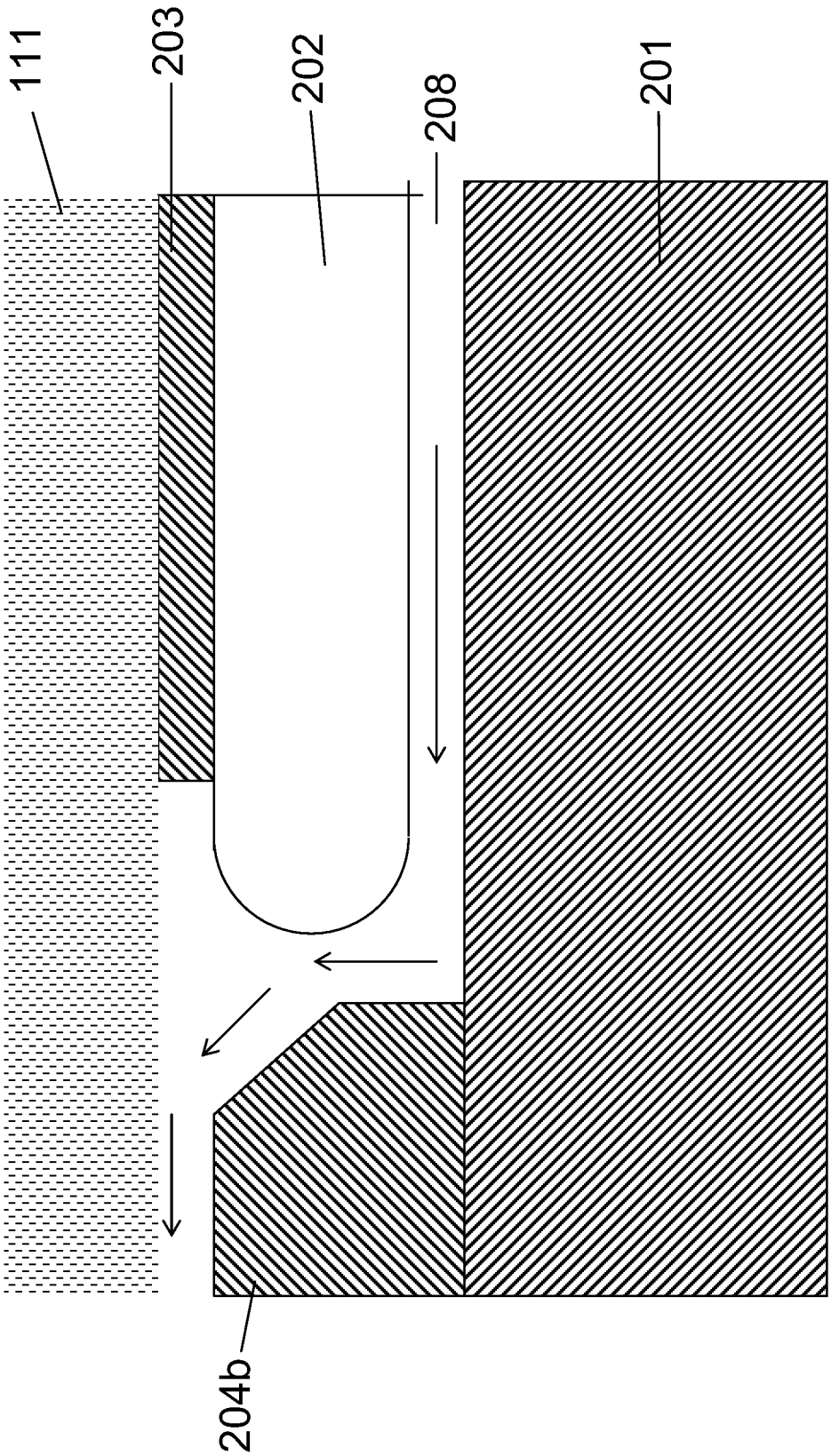

FIG 9

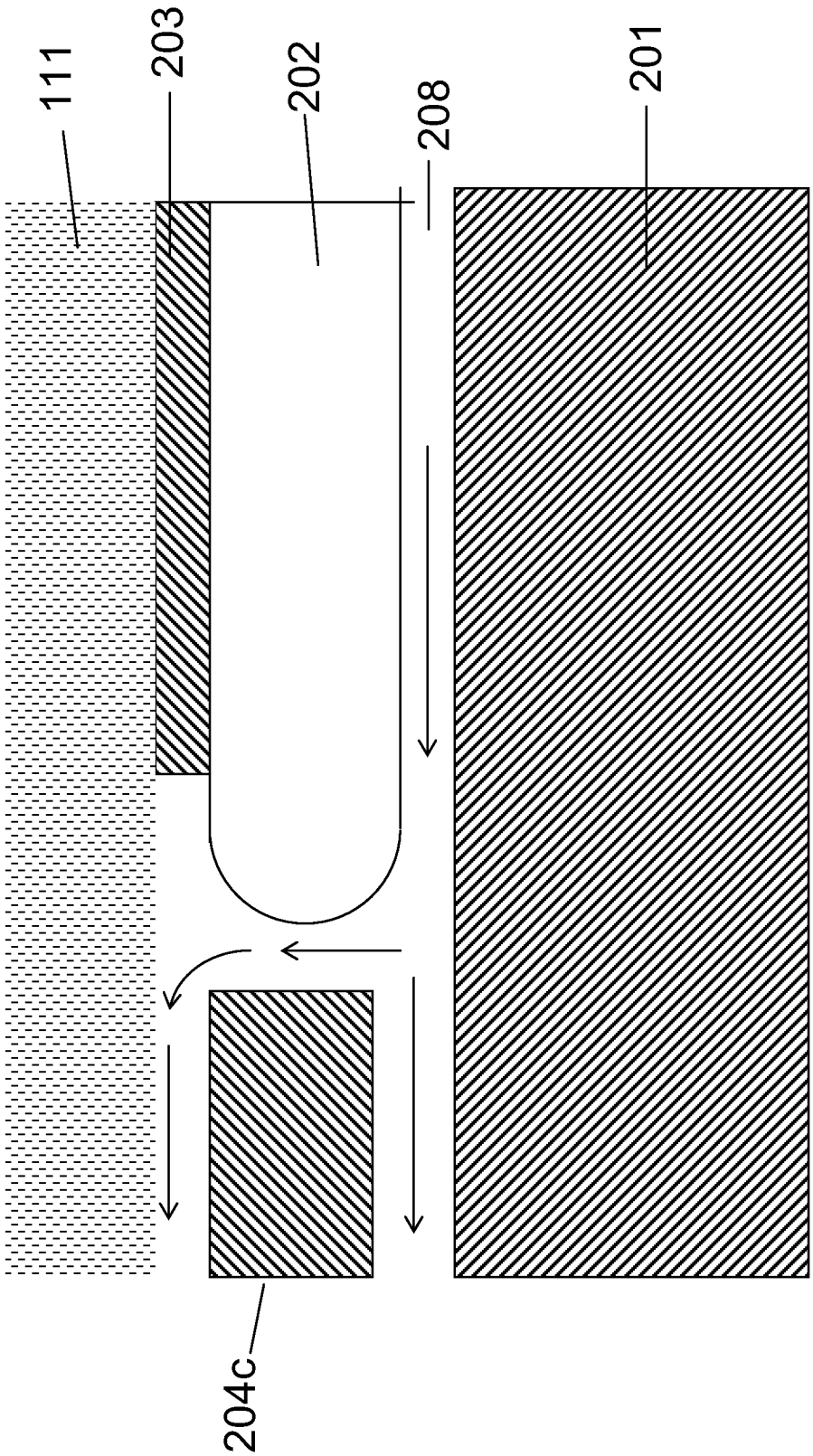

FIG 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/074524

A. CLASSIFICATION OF SUBJECT MATTER

See the extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 21/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC: TSV，通孔，蚀刻，腐蚀，背，减薄，露头，旋转，顺时针，逆时针，反转， through silicon via, wet etch, spray, clockwise, counter clockwise, rotate, reverse, thin

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/0178761 A1 (TAIWAN SEMICONDUCTOR MFG CO LTD, et al.) 15 July 2010 (15.07.2010) see paragraphs [0016]-[0063] of the description and figures 1a-2b	1-34
Y	US 2011/0309051 A1 (LG SILTRON INC, et al.) 22 December 2011 (22.12.2011) see paragraphs [0002]-[0068] of the description and figures 1-11	1-34
Y	US 2006/0261042 A1 (SOITEC SILICON ON INSULATOR TECHNOLOGIES, et al.) 23 November 2006 (23.11.2006) see paragraphs [0026]-[0050] and figures 1-3	8-14, 23-29

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 January 2014 (10.01.2014)	**13 Feb. 2014 (13.02.2014)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer LIU, Xiaohua Telephone No. (86-10)62412099

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/074524

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 102403270 A (NANTONG FUJITSU MICROELECTRONIC CO LTD) 04 April 2012 (04.04.2012) see the whole document	1-34
A	CN 102714153 A (LAM RES AG, et al.) 03 October 2012 (03.10.2012) see the whole document	1-34

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2013/074524

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US 2010/0178761 A1	15.07.2010	US 8501587 B2	06.08.2013
		CN 101794717 A	04.08.2010
		CN 101794717 B	23.05.2012
US 2011/0309051 A1	22.12.2011	JP 2012507881 A	29.03.2012
		WO 2010053280 A2	14.05.2010
		WO 2010053280 A3	05.08.2010
		EP 2357663 A2	17.08.2011
		KR 20100050403 A	13.05.2010
		CN 102246277 A	16.11.2011
		KR 20100050404 A	13.05.2010
		KR 1104016 B1	06.01.2012
		CN 103354213 A	16.10.2013
US 2006/0261042 A1	23.11.2006	WO 2007010149 A1	25.01.2007
		JP 2008541468 A	20.11.2008
		EP 1883954 A1	06.02.2008
		US 7396483 B2	08.07.2008
		FR 2886053 A1	24.11.2006
		EP 1883954 B1	02.11.2011
CN 102403270 A	04.04.2012	CN 102403270 B	19.09.2013
CN 102714153 A	03.10.2012	US 2011/0151675 A1	23.06.2011
		WO 2011073840 A3	01.12.2011
		KR 20120109509 A	08.10.2012
		WO 2011073840 A2	23.06.2011
		EP 2513954 A2	24.10.2012
		JP 2013514652 A	25.04.2013
		TW 201140667 A	16.11.2011
		US 8596623 B2	03.12.2013

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2013/074524

Continuation of A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768 (2006.01) i

H01L 23/52 (2006.01) i