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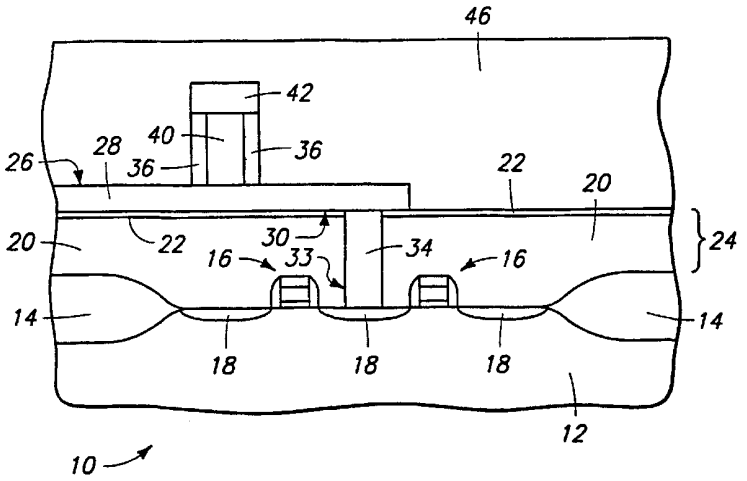
(54) Title: METHODS OF FORMING AN INTERLEVEL DIELECTRIC LAYER BETWEEN DIFFERENT LEVELS OF METAL LAYERS IN THE FABRICATION OF INTEGRATED CIRCUIT



(57) Abstract: The invention comprises methods of providing an interlevel dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry. In one implementation, a method of providing an interlevel dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry includes forming a conductive metal interconnect layer over a substrate. An insulating dielectric mass is provided about the conductive metal interconnect layer. The insulating dielectric mass has a first dielectric constant. At least a majority of the insulating dielectric mass is etched away from the substrate. After the etching, an interlevel dielectric layer is deposited to replace at least some of the etched insulating dielectric material. The interlevel dielectric layer has a second dielectric constant which is less than the first dielectric constant.

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DESCRIPTION

METHODS OF FORMING AN INTERLEVEL DIELECTRIC LAYER BETWEEN DIFFERENT LEVELS OF METAL LAYERS IN THE FABRICATION OF INTEGRATED CIRCUIT

Technical Field

This invention relates to methods of providing an interlevel dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry.

Background Art

In methods of forming integrated circuits, it is frequently desired to electrically isolate components of the integrated circuits from one another with an insulative material. For example, conductive layers can be electrically isolated from one another by separating them with an insulating material. Insulating material received between two different elevation conductive or component layers is typically referred to as an interlevel dielectric material. Also, devices which extend into a semiconductive substrate can be electrically isolated from one another by insulative materials formed within the substrate between the components, such as for example, trench isolation regions.

One typical insulative material for isolating components of integrated circuits is silicon dioxide, which has a dielectric constant of about 4. Yet in many applications, it is desired to utilize insulative materials having dielectric constants lower than that of silicon dioxide to reduce parasitic capacitance from occurring between conductive components separated by the insulative material. Parasitic capacitance reduction continues to have increasing importance in the semiconductor fabrication industry as device dimensions and component spacing continues to shrink. Closer spacing adversely effects parasitic capacitance.

One way of reducing the dielectric constant of certain inherently insulative materials is to provide some degree of carbon content therein. One example technique for doing so has recently been developed by Trikon Technology of Bristol, UK which they refer to as Flowfill™ Technology. Where more carbon incorporation is desired, methylsilane in a gaseous form and H2O2 in a liquid form are separately introduced into a chamber, such as a parallel plate reaction chamber. A reaction

between the methylsilane and H2O2 can be moderated by introduction of nitrogen into the reaction chamber. A wafer is provided within the chamber and ideally maintained at a suitable low temperature, such as 0° C, at a exemplary pressure of 1 Torr to achieve formation of a methylsilanol structure. Such structure/material condenses on the wafer surface. Although the reaction occurs in the gas phase, the deposited material is in the form of a viscus liquid which flows to fill small gaps on the wafer surface. In applications where deposition thickness increases, surface tension drives the deposited layer flat, thus forming a planarized layer over the substrate.

The liquid methylsilanol is converted to a silicon dioxide structure by a two-step process occurring in two separate chambers from that in which the silanol-type structure was deposited. First, planarization of the liquid film is promoted by increasing the temperature to above 100° C, while maintaining the pressure at about 1 Torr, to result in solidification and formation of a polymer layer. Thereafter, the temperature is raised to approximately 450°C, while maintaining a pressure of about 1 Torr, to form (CH3)ySiO(2-y). y/2 is the percentage of CH3 incorporated. The (CH3)ySiO(2-y) has a dielectric constant of less than or equal to about 3, and is accordingly less likely to be involved in parasitic capacitance than silicon dioxide and/or phosphorous doped silicon dioxide.

Other example low k dielectric layer materials include fluorine doped silicon dioxide, high carbon and hydrogen containing materials, and other organic films having less than 20% silicon.

A prior art problem associated with low k dielectric material usage is that many of these materials cannot withstand high temperature processing. Specifically, many melt or gassify at comparatively low temperatures at which the substrate is subjected after deposition of the low k materials. This can essentially destroy the circuitry being fabricated. It is further very difficult to quickly strip photoresist when processing over such low k dielectric layers, as the typical photoresist stripping processes undesirably cause some isotropic etching of the low k dielectric layers.

Disclosure of the Invention

The invention comprises methods of providing an interlevel dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry. In one implementation, a method of providing an interlevel

dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry includes forming a conductive metal interconnect layer over a substrate. An insulating dielectric mass is provided about the conductive metal interconnect layer. The insulating dielectric mass has a first dielectric constant. At least a majority of the insulating dielectric mass is etched away from the substrate. After the etching, an interlevel dielectric layer is deposited to replace at least some of the etched insulating dielectric material. The interlevel dielectric layer has a second dielectric constant which is less than the first dielectric constant.

Brief Description of the Drawings

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 2.

Fig. 4 is a view of an alternate embodiment semiconductor wafer fragment at a processing step subsequent to that depicted by Fig. 2.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that depicted by Fig. 3.

Fig. 6 is a diagrammatic sectional view of another alternate embodiment wafer fragment at a processing step in accordance with an aspect of the invention.

Fig. 7 is a view of the Fig. 6 wafer at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 6 wafer at a processing step subsequent to that depicted by Fig. 7.

Fig. 9 is a view of the Fig. 6 wafer fragment at a processing step subsequent to that depicted by Fig. 8.

Fig. 10 is a view of the Fig. 6 wafer at a processing step subsequent to that depicted by Fig. 9.

Best Modes for Carrying Out the Invention and Disclosure of Invention

A method of providing an interlevel dielectric layer intermediate different elevation conductive layers in the fabrication of integrated circuitry is initially described with reference to Figs. 1-5. Referring initially to Fig. 1, a semiconductor wafer fragment in process is indicated generally with reference numeral 10. Such comprises a bulk semiconductive substrate 12, preferably lightly p-doped monocrystalline silicon, having field oxide regions 14 formed therein. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

A pair of gate line constructions 16 are fabricated over substrate 12, and comprise a gate dielectric layer, a conductive polysilicon layer, a conductive silicide layer, and insulating sidewalls spacers and caps, which are not specifically designated. Source/drain diffusion regions 18 are fabricated within substrate 12. Such constitute exemplary circuit devices which are at least partially fabricated over a substrate. Any alternate electric devices or components are also, of course, contemplated.

An insulating layer 20 is formed over devices 16 and substrate 12. An example and preferred material is borophosphosilicate glass (BPSG). An exemplary thickness is from 5,000 Angstroms to 30,000 Angstroms. An insulating layer 22 is formed over insulating layer 20. Such is preferably provided to function as an etch stop material, as will be described subsequently. Example materials include undoped silicon dioxide deposited by decomposition of tetraethylorthosilicate (TEOS) and silicon nitride. An exemplary thickness for layer 22 is from 0 Angstroms to 2,000 Angstroms. Layer 20 and 22 comprise but one example insulating dielectric mass which is formed over at least partially fabricated circuit devices over a substrate. An opening 33 has been formed in insulating dielectric mass 24 between word line 16 to substrate diffusion region 18. Such has been filled with a conductive plugging material 34, for example conductively doped polysilicon or a metal, and planarized back to have an outermost surface substantially coincident with the outer surface of layer 22.

A first conductive interconnect layer 26 is formed over substrate 12. Preferred materials are elemental metals or metal alloys. Conductive interconnect layer 26 has been formed into the shape of at least one conductive interconnect line 28 having an outer top 29, an inner base 30 and sidewalls 31. Accordingly, first conductive interconnect layer 26 and line 28 are supported by second insulating dielectric mass 24.

An insulating dielectric mass 36 is provided about conductive metal interconnect layer 26. Accordingly in this example, insulating dielectric mass 36 is formed over another conductive metal interconnect layer, here in the form of layer 28. Further accordingly, insulating dielectric mass 36 is formed over top 29 and sidewalls 31 of line 28. Example and preferred materials for layer 36 are the same as layer 20, for example BPSG. Insulating dielectric mass 24 has some first dielectric constant, with the dielectric constant of BPSG being about 3.9. An exemplary deposition thickness for layer 36 is from 1,000 Angstroms to 15,000 Angstroms, with layer 36 being shown as having been planarized subsequent to deposition. An opening 38 has been formed through layer 36 and filled with conductive material 40 for making electric connection with conductive line 28. An exemplary conductive line 42 has been patterned thereatop and over insulating dielectric mass 36 for, in this example, providing conductive line interconnection between conductive line 42 and line 28. Accordingly, line 42 constitutes a second conductive interconnect layer and line which is supported at least partially by second insulating dielectric mass 36. Layers 42, 40, 26, and 34 are all preferably metallic. Most preferably at this point in the process, substantially all of the integrated circuitry to be fabricated relative to substrate 10 has been so fabricated. Further preferably, any subsequent processing relative to substrate 10 is preferably void of any photolithographic processing.

Referring to Fig. 3, at least a portion of insulating dielectric mass 36 is etched away from substrate 10. More preferably, the etching removes at least a majority (if not all) of insulating dielectric mass 36 from substrate 10. Fig. 3 depicts exemplary anisotropic etching, with a dry etching being an example. A specific example where layer 36 comprises BPSG is 12 sccm C4F8, 200 sccm Ar, 1300W source, 1400W bias, at 10 mTorr in a LAM 9100™ oxide etch chamber. Regardless and further preferably, the etching preferably comprises etching second insulating dielectric mass 36 inwardly to proximate line base 30. In the Fig. 3

depicted example, the etching has also been conducted substantially selectively relative to first conductive interconnect line 28 and second conductive interconnect line 42, and substantially selectively relative to etch stop layer 22 and accordingly relative to insulative dielectric mass 24. Further preferably, such etching has been conducted to expose first conductive interconnect line 28 and insulating dielectric mass 24.

Such etching in this example leaves insulating dielectric material 36 beneath conductive line 42 as shown. Exemplary alternate processing to that depicted by Fig. 3 is shown in Fig. 4. Here, essentially isotropic etching has been conducted and to a degree sufficient whereby no insulating dielectric material 36 has been left beneath conductive line 42, and such that the etching comprises etching essentially all of insulating dielectric mass 36 from substrate 10. Exemplary preferred processing to achieve the illustrated Fig. 4 construction includes wet etching, for example utilizing a chemistry of HF, NH4F:HF or a nonaqueous blend of glycol, phosphoric acid, HF and a carboxylic acid. The above recited specific chemistries will provide etch selectivity relative to aluminum lines and plugs, BPSG, and silicon nitride for layer 22. Removal of layer 36 results in lines 42 being supported by various conductive pillars 40 and/or remnant insulating layer 36.

Referred to Fig. 5, an interlevel dielectric layer 46 has been deposited to replace at least some of etched insulating dielectric material 36. Interlevel dielectric layer 46 has a second dielectric constant which is less than the first dielectric constant of layer 36. Example and preferred low k materials are those described above in the "Background" section, and include low k dielectric materials yet to be developed. In the preferred and Fig. 5 depicted example, the interlevel dielectric layer depositing preferably replaces all of insulating dielectric material 36 which was etched from the substrate as exemplified in the Figs. 4 and 5 embodiments. Such layer is preferably planarized back as shown.

The above described exemplary processing depicts conductive metal interconnect layer and line 42 as being formed or otherwise provided after formation of insulating dielectric mass 36, and by a subtractive etching of a deposited metal interconnect layer from which line 42 is formed. Figs. 6-10 depict alternate exemplary processing whereby the line forming comprises a damascene etching of an insulating dielectric mass into a desired line shape. Fig. 6 depicts a wafer fragment in process indicated generally by reference numeral 50. Such includes an

insulating layer 52 having an opening 54 formed therein. A conductive plugging material 56 is received within opening 54. An insulating dielectric layer 60 is formed over layer 52, and a preferred insulating etch stop layer 62 is formed thereover. An opening 64 has been etched through layers 62 and 60 to expose plugging material 56. Thereafter, insulating and etch stop layers 64 and 66, respectively, have been formed over layer 62. A desired line shape opening 68 has been patterned and formed through layers 66 and 64, and overlies the illustrated singular opening 64. Layers 60, 62, 64 and 66 constitute but one exemplary insulating dielectric mass 70.

Referring to Fig. 7, a conductive interconnect layer 72 is deposited to fill damascene line opening 68 and contact opening 64.

Referring to Fig. 8, layer 72 has been planarized back to provide a desired patterned and isolated conductive interconnect line 74.

Referring to Fig. 9, insulating dielectric mass 70 has been etched away from substrate 50. Isotropic or anisotropic etching could be conducted as described above, whereby some or none of insulating dielectric mass 70 remains over the substrate.

Referring to Fig. 10, an interlevel dielectric layer 76 has been deposited to replace at least some, and here all, of etched insulating dielectric material 70. Layer 76 has a lower overall k value than does insulative mass 70 which was removed.

CLAIMS

1. A method of providing an interlevel dielectric layer intermediate different elevation conductive metal layers in the fabrication of integrated circuitry, the method comprising:

forming a conductive metal interconnect layer over a substrate;

providing an insulating dielectric mass about the conductive metal interconnect layer, the insulating dielectric mass having a first dielectric constant;

etching at least a majority of the insulating dielectric mass away from the substrate; and

after the etching, depositing an interlevel dielectric layer to replace at least some of the etched insulating dielectric material, the interlevel dielectric layer having a second dielectric constant which is less than the first dielectric constant.

2. The method of claim 1 wherein the conductive metal interconnect layer is formed after providing the insulating dielectric mass.

3. The method of claim 1 comprising forming the conductive interconnect layer into a conductive line, the line forming comprising a subtractive etching of the metal interconnect layer.

4. The method of claim 1 comprising forming the conductive interconnect layer into a conductive line, the line forming comprising a damascene etching of the insulating dielectric mass into a desired line shape.

5. The method of claim 1 wherein the first dielectric constant is at least 3.9, and the second dielectric constant is less than 3.9.

6. The method of claim 1 wherein the depositing replaces all of the insulating material which was etched from the substrate.

7. The method of claim 1 wherein the etching comprises isotropic etching.

8. The method of claim 1 wherein the etching comprises anisotropic etching.

9. The method of claim 1 wherein the insulating dielectric mass is formed over another conductive metal interconnect layer, the etching comprising etching all the insulating dielectric mass from the substrate.

10. The method of claim 1 wherein the etching is conducted substantially selective relative to the conductive metal interconnect layer.

11. The method of claim 1 wherein the etching is conducted after substantially all of the integrated circuitry to be fabricated has been fabricated on the substrate.

12. The method of claim 1 being void of any photolithographic processing of the substrate after the etching.

13. A method of providing an interlevel dielectric layer intermediate different elevation conductive layers in the fabrication of integrated circuitry, the method comprising:

forming a first insulating dielectric mass over at least partially fabricated circuit devices over a substrate;

forming a first conductive interconnect layer supported by the first insulating dielectric mass;

forming a second insulating dielectric mass over the first conductive interconnect layer, the second insulating dielectric mass having a first dielectric constant;

forming a second conductive interconnect layer supported by the second insulating dielectric mass;

etching at least a portion of the second insulating dielectric mass away from the substrate; and

after the etching, depositing an interlevel dielectric layer to replace at least some of the etched second insulating dielectric material, the interlevel dielectric layer having a second dielectric constant which is less than the first dielectric constant.

14. The method of claim 13 wherein the portion etched is a majority of the second insulating dielectric mass.

15. The method of claim 13 comprising providing the first conductive interconnect layer in the shape of at least one conductive interconnect line, wherein the first conductive interconnect line has an inner base, sidewalls and an outer top, the second insulating dielectric mass being formed over the top and the sidewalls, the etching comprising etching the second insulating dielectric mass inwardly to proximate the base.

16. The method of claim 13 wherein the etching comprises isotropic etching.

17. The method of claim 13 wherein the etching comprises anisotropic etching.

18. The method of claim 13 wherein the etching etches all of the second insulating dielectric mass from the substrate.

19. The method of claim 13 wherein the etching exposes the first conductive interconnect layer.

20. The method of claim 13 comprising providing the second conductive interconnect layer into the shape of at least one conductive line, the etching leaving second insulating dielectric material beneath the conductive line.

21. The method of claim 13 comprising providing the second conductive interconnect layer into the shape of at least one conductive line, the etching not leaving second insulating dielectric material beneath the conductive line.

22. The method of claim 13 wherein the first and second conductive interconnect layers are metallic.

23. The method of claim 13 wherein the etching is conducted after substantially all of the integrated circuitry to be fabricated has been fabricated on the substrate.

24. The method of claim 13 being void of any photolithographic processing of the substrate after the etching.

25. A method of providing an interlevel dielectric layer intermediate different elevation conductive layers in the fabrication of integrated circuitry, the method comprising:

forming a first insulating dielectric mass over at least partially fabricated circuit devices over a substrate;

forming a first conductive interconnect line supported by the first insulating dielectric mass;

forming a second insulating dielectric mass over the first conductive interconnect line, the second insulating dielectric mass having a first dielectric constant;

forming a second conductive interconnect line supported by the second insulating dielectric mass;

etching a majority of the second insulating dielectric mass away from the substrate substantially selectively relative to the first and second conductive interconnect lines and substantially selectively relative to the first insulative dielectric mass, the etching exposing the first conductive interconnect line and the first insulating dielectric mass; and

after the etching, depositing an interlevel dielectric layer to replace at least some of the etched second insulating dielectric material, the interlevel dielectric layer having a second dielectric constant which is less than the first dielectric constant.

26. The method of claim 25 wherein the etching leaves second insulating dielectric material beneath the second conductive interconnect line.

27. The method of claim 25 wherein the etching does not leave second insulating dielectric material beneath the second conductive interconnect line.

28. The method of claim 25 wherein the etching comprises isotropic etching.

29. The method of claim 25 wherein the etching comprises anisotropic etching.

30. The method of claim 25 wherein the etching etches all of the second insulating dielectric mass from the substrate.

31. The method of claim 25 wherein the etching is conducted after substantially all of the integrated circuitry to be fabricated has been fabricated on the substrate.

32. The method of claim 25 being void of any photolithographic processing of the substrate after the etching.

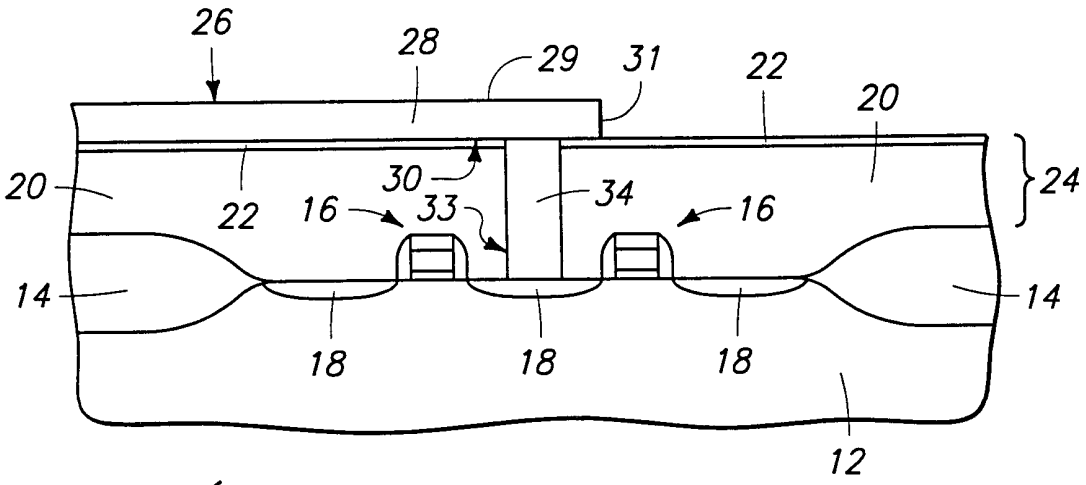
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Fig. 1

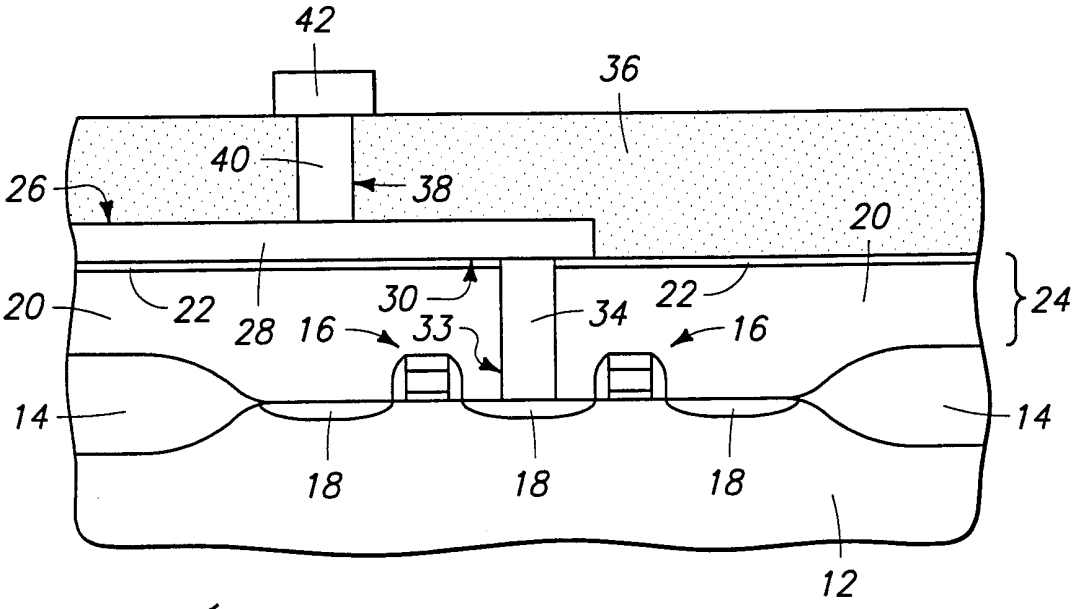
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Fig. 2

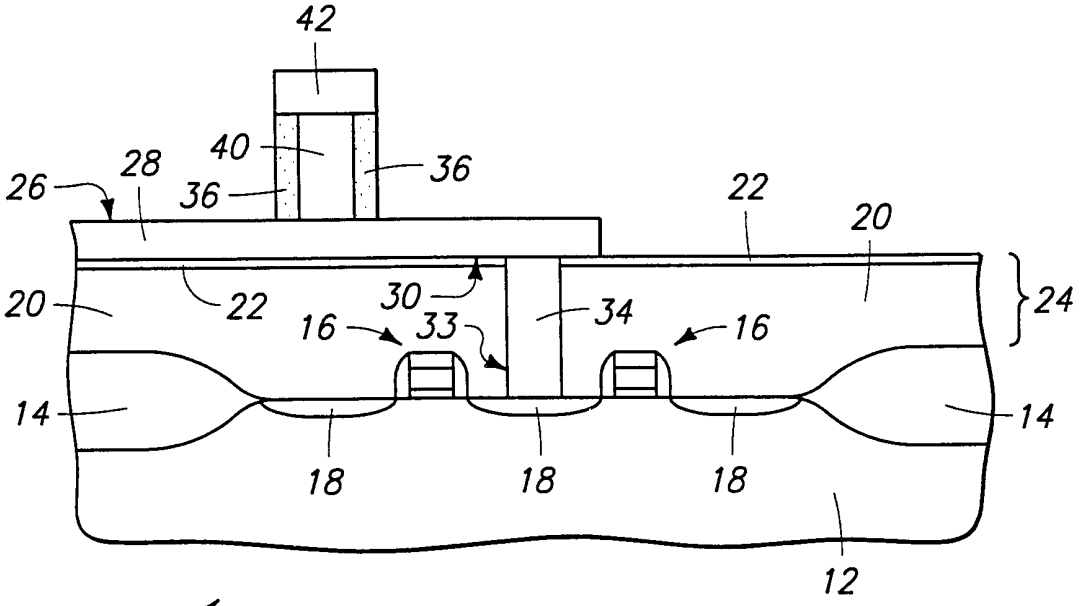
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Fig. 3

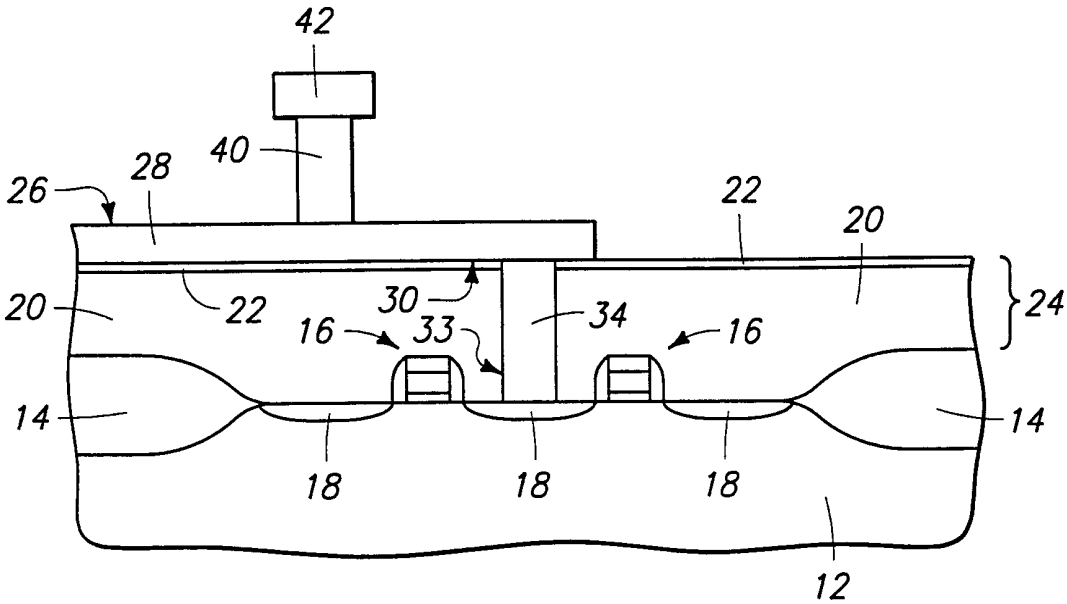
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Fig. 4

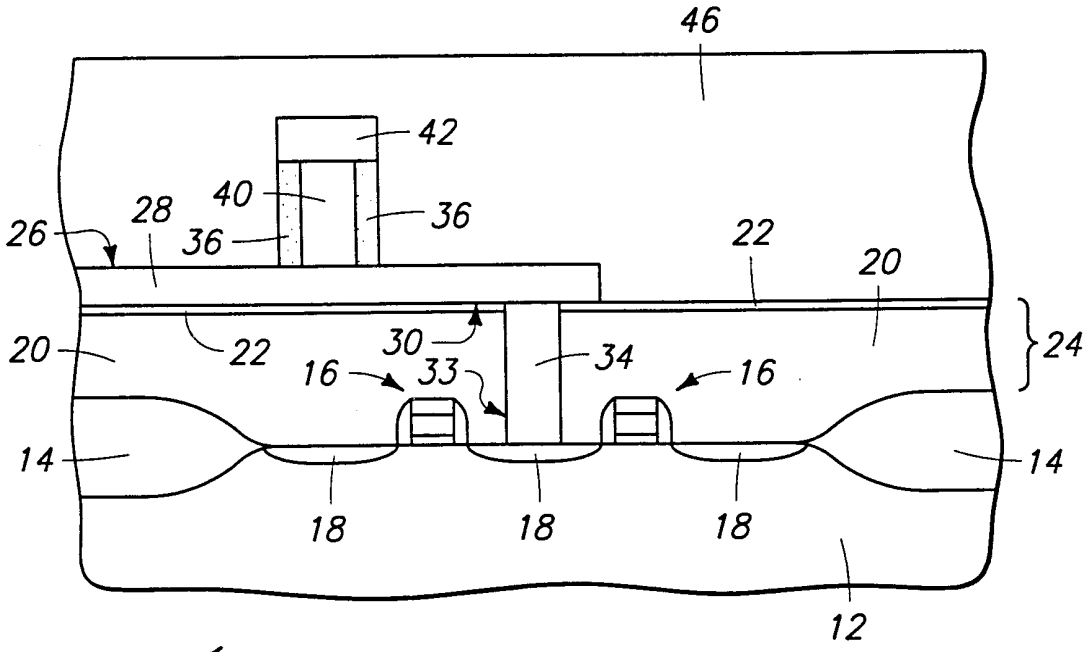
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Fig 5

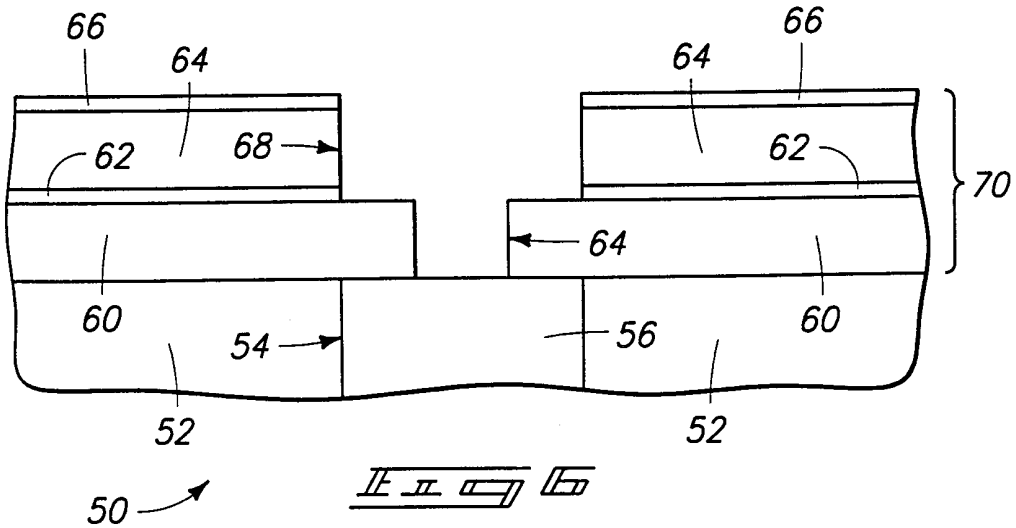
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Fig 6

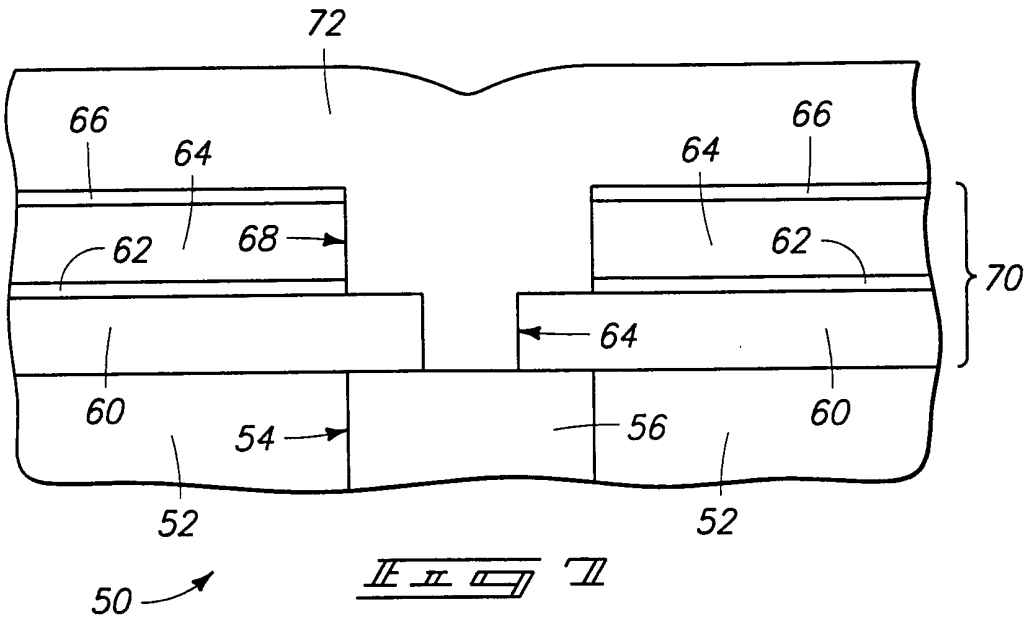
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Fig 1

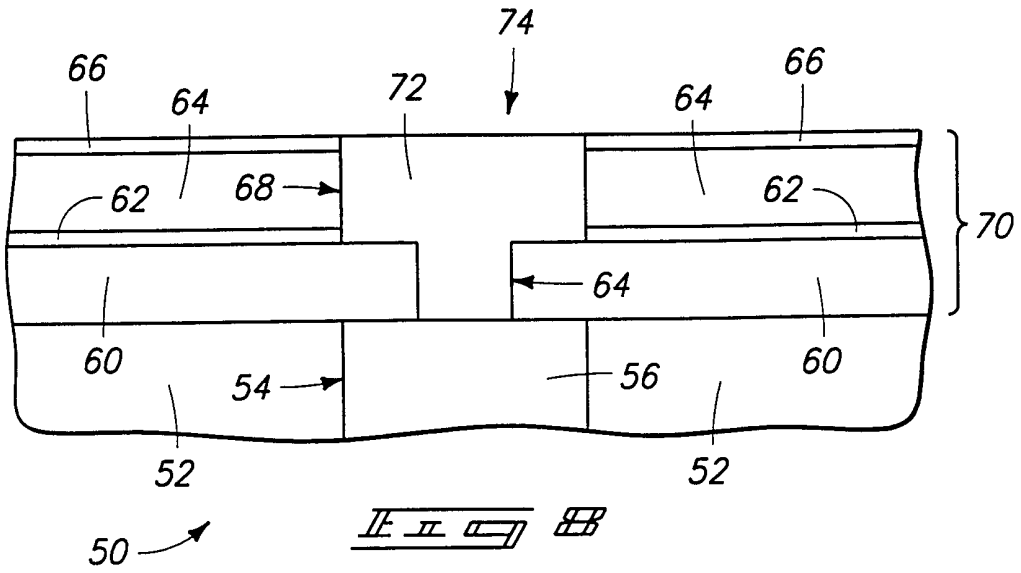
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Fig 2

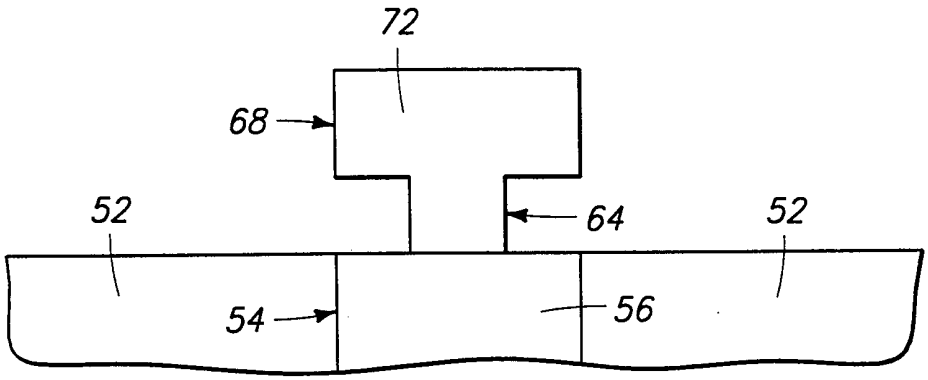

Fig 9

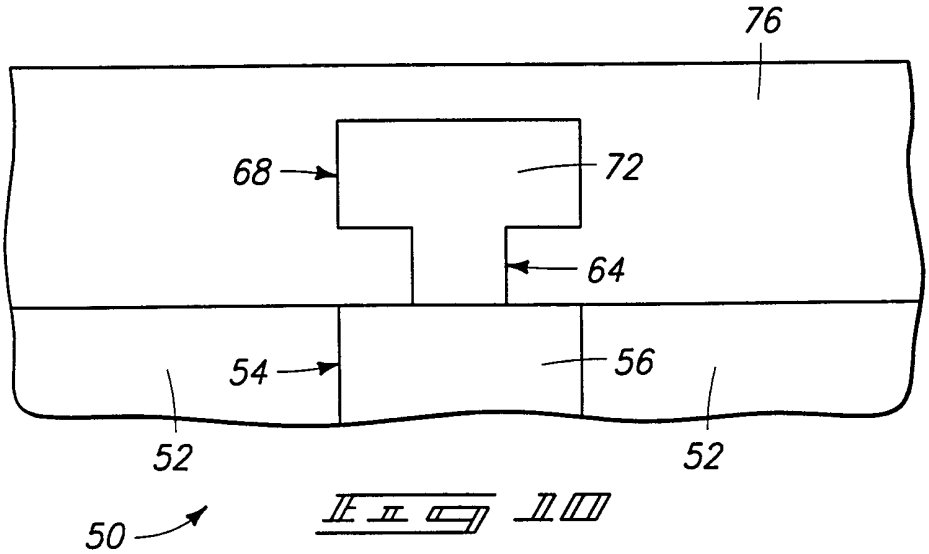

Fig 10

INTERNATIONAL SEARCH REPORT

Internat Application No
PCT/US 00/21111

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 923 125 A (STMICROELECTRONICS SA ;FRANCE TELECOM (FR)) 16 June 1999 (1999-06-16) column 4, line 35 -column 5, line 24 figures 3A-3G,4C-4J	1-32
X	US 5 149 615 A (CHAKRAVORTY KISHORE K ET AL) 22 September 1992 (1992-09-22) column 3, line 55 -column 4, line 36 figures 3-5	1-3,6-12
A	US 5 808 854 A (FIGURA THOMAS A ET AL) 15 September 1998 (1998-09-15) column 4, line 35 -column 5, line 15 figures 13-15	1-4,7-12

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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1 November 2000	10/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Giordani, S

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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