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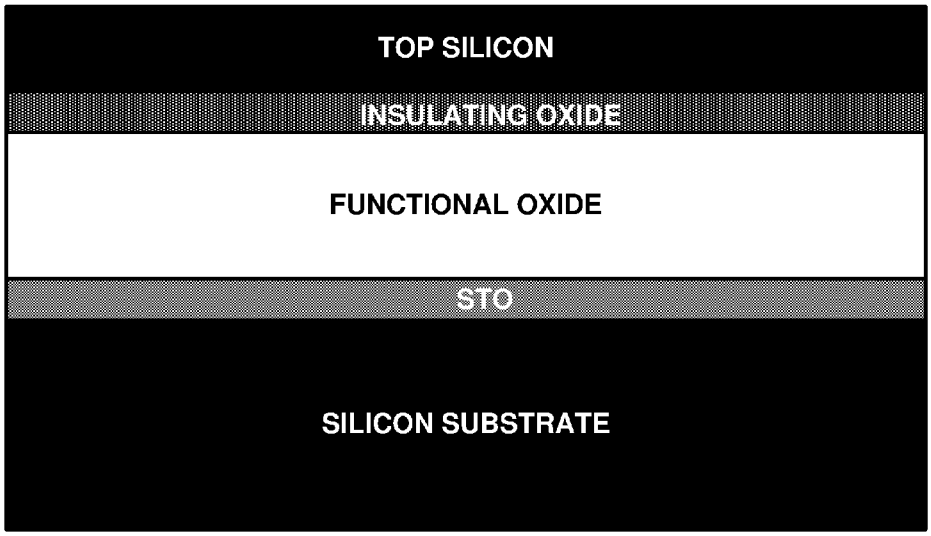

FIG. 1

(57) Abstract: Some embodiments of the present technology simplify the process of producing SOI wafers significantly compared to traditional methods. Furthermore, various embodiments provide a route for the integration of perovskite transition metal oxide thin films with different properties into SOI wafers. As such films display a wide array of novel electronic, magnetic, and optical phenomena, their integration into technologically-relevant SOI wafers will likely allow for the construction of a wide array of novel devices.

WO 2020/180940 A1

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SILICON-ON-OXIDE-ON-SILICON

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Application No. 62/813,283 filed March 4, 2019, which is incorporated herein by reference in its entirety for all purposes.

FEDERALLY FUNDED RESEARCH

[0002] The invention was made with government support under Grant no. FA9550-12-1-0494 awarded by the Air Force Office of Scientific Research. The government has certain rights in the invention.

TECHNICAL FIELD

[0003] Various embodiments of the present technology generally relate to semiconductor manufacturing. More specifically, some embodiments of the present technology relate to epitaxial integration of a device silicon layer on an insulating oxide (e.g., $LaAlO_3$), which is itself epitaxially integrated on a silicon (001) substrate.

BACKGROUND

[0004] Silicon-on-insulator (SOI) wafers are ubiquitous in the semiconductor industry, finding use in a wide variety of integrated circuits and devices. Traditional SOI platforms feature a thin device silicon layer attached on top of a buried oxide (BOX) SiO_2 layer. Fabrication of such SOI wafers relies on complicated, energy intensive processes, such as the separation by implantation of oxygen (SIMOX) or wafer bonding. Additionally, these processes are limited in their applicability to materials other than silicon, excluding the use of BOX materials other than SiO_2.

SUMMARY

[0005] Various embodiments of the present technology generally relate to semiconductor manufacturing. More specifically, some embodiments of the present technology relate to epitaxial integration of a device silicon layer on insulating $LaAlO_3$, which is itself epitaxially integrated on a silicon (001) substrate.

[0006] Various embodiments of the present technology provide an epitaxial integration of a device silicon layer on insulating $LaAlO_3$, which is itself epitaxially

integrated on a silicon (001) substrate by means of a thin $SrTiO_3$ buffer layer. Some embodiments provide for a novel SOI system prepared by direct thin film deposition techniques rather than complex implantation and wafer bonding processes. Additionally, some embodiments allow for the incorporation of BOX materials other than SiO_2 into the SOI wafer.

[0007] While multiple embodiments are disclosed, still other embodiments of the present invention will become apparent to those skilled in the art from the following detailed description, which shows and describes illustrative embodiments of the invention. As will be realized, the invention is capable of modifications in various aspects, all without departing from the scope of the present invention. Accordingly, the drawings and detailed description are to be regarded as illustrative in nature and not restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the present technology will be described and explained through the use of the accompanying drawings.

[0009] Fig. 1 illustrates a cross-sectional schematic of silicon-on-insulator-on-silicon (SOS) platform.

[0010] Fig. 2 illustrates a cross-sectional schematic showing the potential to realize multiple layers of functional oxides integrated with silicon within a single platform by repetition of the SOS structure.

[0011] Fig. 3 illustrates a 2x1 RHEED pattern of Si(001) covered by 1/2 ML Sr to form a template, viewed from the Si (110) azimuth.

[0012] Fig. 4A illustrates a 2x1 structure of the Si-STO interface with a 1/2 ML of Sr at the interface.

[0013] Fig. 4B is an enlarged HAADF image from the defect-free region of the BTO/STO/Ge heterostructure showing the Ge surface step (arrowed) between 2x and 1x periodicities.

[0014] Fig. 5 illustrates HRTEM micrograph of the $LaAlO_3$/Si interface (grown at 850ºC and annealed at 900ºC) along $LaAlO_3$ where the black arrow indicates a twin in the Si film and the white arrows indicate regions along the interface that show periodic contrast changes.

[0015] Fig. 6A is the RHEED pattern from ten unit cells of STO deposited on Si(001) surface, taken along the STO [110] direction.

[0016] Fig. 6B is the RHEED pattern from 50 unit cells of LAO deposited on STO(001) surface, taken along the LAO [110] direction.

[0017] Fig. 7 is RHEED pattern of Si deposited at 875 °C on the surface of a fifty-unit cell LAO film where the large red circles indicate the positions of RHEED spots from the primary crystalline lattice of the Si islands, while the small blue circles indicate the observation of a minor, secondary phase.

[0018] Fig. 8 is survey XPS spectrum of SOS sample showing predominantly Si 2*s* and 2*p* core levels, with only small O 1*s* and La 3*d* peaks visible in the spectrum.

[0019] Fig. 9A is a cross-sectional STEM image of a completed SOS sample taken in high-angle annular dark field (HAADF) imaging mode. In this imaging mode, the intensity of the atomic columns scales roughly as the square of the atomic number *Z*.

[0020] Fig. 9B is a high-resolution image of the LAO/Si interface taken in annular bright field (ABF) imaging mode.

[0021] Fig. 10 is a selected area electron diffraction patterns of the Si substrate (right panel) and deposited Si (left panel) with the cross-sectional STEM image indicating the areas of the sample from which the SAED patterns were collected is shown in the center panel.

[0022] Figs. 11A-11B illustrate a comparison between BTO-on-SiO_2 photonic devices fabricated via the SOS platform (11A) and the wafer-bonding approach (11B).

[0023] Fig. 12 is a flowchart illustrating a set of operations for manufacturing an SOS structure in accordance with some embodiments of the present technology.

[0024] The drawings have not necessarily been drawn to scale. Similarly, some components and/or operations may be separated into different blocks or combined into a single block for the purposes of discussion of some of the embodiments of the present technology. Moreover, while the technology is amenable to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and are described in detail below. The intention, however, is not to limit the technology to the particular embodiments described. On the contrary,

the technology is intended to cover all modifications, equivalents, and alternatives falling within the scope of the technology as defined by the appended claims.

DETAILED DESCRIPTION

[0025] Systems and methods are described for epitaxial integration of a device silicon layer on insulating $LaAlO_3$ (LAO), which is itself epitaxially integrated on a silicon (001) substrate by means of an oxide buffer layer. Some embodiments provide a route to integrate crystalline silicon, including that which is grown epitaxially, on an insulating oxide (e.g., LAO) with a silicon (001) substrate. Some embodiments can produce samples with the following layer stack: silicon (001) substrate/thin film $SrTiO_3$ (STO; buffer layer)/thin film functional oxide (e.g., $BaTiO_3$; buried oxide)/thin film LAO (oxygen scavenging barrier; insulating oxide)/epitaxial top silicon (Fig. 1). Such a materials system is likely to find use in a wide variety of microelectronic and optoelectronic circuits and devices, including in next-generation metal-oxide-semiconductor field effect transistors (MOSFETs) and integrated photonics. This also opens the possibility of going beyond planar devices and allowing for vertical or 3D integration (Fig. 2), vastly increasing device density.

[0026] The layer stack presented in various embodiments of the present technology has not previously been prepared. In standard silicon-on-insulator (SOI) wafers, a so-called “device layer” of silicon is attached to an insulating amorphous SiO_2 layer, which is itself grown on a separate silicon wafer. In the final structure, the SiO_2 is referred to as the buried oxide, or BOX layer. SOI wafers are typically prepared via the separation by implantation of oxygen (SIMOX) process or using wafer bonding techniques. In contrast, various embodiments of the present technology allow for the direct epitaxial deposition of a device silicon layer on the insulating oxide LAO, which can itself be epitaxially deposited on a silicon (001) substrate via a thin STO seed layer. A wide variety of functional oxides can be epitaxially deposited atop the STO seed layer. The resulting layer stack is a novel form of SOI wafer, where the STO serves as a seed layer facilitating the epitaxial growth of oxides on a silicon substrate, the functional oxide or oxides serve as the BOX layer, and the LAO serves as an oxygen scavenging barrier between the deposited device silicon and the underlying functional oxide(s). Accordingly, various embodiments allow for SOI wafers to be

prepared via direct deposition techniques rather than with the more energy intensive ion implantation and wafer bonding processes used in traditional SOI manufacturing.

[0027] Moreover, various embodiments greatly simplify the process of producing SOI wafers by relying on straight-forward thin film deposition methods rather than complicated and energy intensive processes such as SIMOX or wafer bonding. Furthermore, some embodiments open the possibility of integrating a wide array of perovskite transition metal oxide thin films into novel SOI wafers. As perovskite transition metal oxides display a remarkable array of correlated electronic, magnetic and optical phenomena, the integration of such oxide thin films into SOI wafers, especially as a 3D stack, opens the door to the creation and demonstration of a plethora of novel devices (e.g., microelectronic and photonic devices).

[0028] Some embodiments rely upon a simple integration process for the fabrication of SOI wafers as compared to the complex processes currently used. Furthermore, due to the epitaxial compatibility of many perovskite transition metal oxides with one another, our layer stack allows for the integration of a wide variety of oxide materials with a wide variety of electronic, magnetic, and optical properties into SOI wafers, as opposed to current SOI wafers which exclusively use amorphous SiO_2 for the BOX layer.

[0029] The formation of a smooth surface in the device silicon layer as-deposited is challenging due to the energetics of the LAO/silicon interface. This challenge can be overcome through a variety of methods. One method is through the inclusion of a suitable wetting layer or surfactant at the LAO/silicon interface. Another method is by employing a two-step growth process of the device silicon layer, in which an initial layer is deposited at high temperature for nucleation, followed by additional deposition at lower temperature. Such a deposition method results in the progressive smoothening of the device silicon surface. Finally, post-deposition methods can also be used to smoothen the device silicon layer surface, such as chemical-mechanical planarization.

[0030] Various embodiments of the present technology open the door for a multitude of new use cases that have not yet been considered. The epitaxial integration of a device silicon layer in close proximity to highly-correlated perovskite transition metal oxide thin films should allow for the construction of a wide range of

novel devices relying on the electronic, magnetic and optical properties of transition metal oxide thin films. Potential examples include uses in silicon photonics platforms, non-volatile ferroelectric field-effect transistors, superconducting devices, and sensor technology.

[0031] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of embodiments of the present technology. It will be apparent, however, to one skilled in the art that embodiments of the present technology may be practiced without some of these specific details.

[0032] The phrases "in some embodiments," "according to some embodiments," "in the embodiments shown," "in other embodiments," and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one implementation of the present technology and may be included in more than one implementation. In addition, such phrases do not necessarily refer to the same embodiments or different embodiments.

Deposition of STO on Si according to the Motorola process.

[0033] To deposit STO on silicon (001) various embodiments of the present technology use a variant of the MBE process developed over a decade ago at Motorola. For example, epi-grade prime silicon (001) wafers can be cleaned ultrasonically with acetone, isopropanol, and de-ionized water. The samples can then be exposed to ultraviolet (UV)-ozone for a period of time (e.g., 15 min) to remove residual carbon contamination. After cleaning, the samples can be introduced into the MBE growth chamber and outgassed (e.g., at 675 °C for 15 min) prior to growth. The native SiO_2 layer is desorbed using a variation of the Sr-assisted de-oxidation process also developed by Motorola, allowing the SiO_2 desorption to occur at a reduced temperature.

[0034] After removal of the native oxide as confirmed by a 2×1 RHEED pattern, the substrate temperature is reduced to 575 °C. During the cooling, the RHEED pattern changes to 3×2 indicating sub-monolayer Sr coverage. Additional Sr can then be deposited until the 2×1 pattern is recovered, which corresponds to a clean Si surface covered with 0.5 monolayer (ML) of Sr (Fig. 3). This is followed by STO growth via co-deposition of Sr and Ti at 200 °C in an oxygen environment of 8×10^{-8} Torr. After

the growth of 1.5 unit cells of STO, the oxygen partial pressure can be quickly increased from 8×10^{-8} Torr to 7×10^{-7} Torr as an additional 2.5 unit cells are deposited. The 4-unit cell film is then annealed at 525 °C without oxygen for 5 min to fully crystallize the thin STO layer. Additional unit cells of STO are deposited at 550 °C in an oxygen atmosphere of 4×10^{-7} Torr.

Si cleaning and de-ox, according to Motorola process.

[0035] Sr can volatilize the native oxide on silicon (001) thus leading to its desorption. In addition, the Sr template protects Si from oxidation at moderate temperatures and oxygen pressures. A density functional theory model of the oxidation of the Si surface passivated by ½ ML of Sr reveals that the surface is protected for up to five adsorbed O atoms (5/6 coverage) (see, e.g., Fredrickson *et al.*, *Journal of Applied Physics* **120**, 065301 (2016) which is hereby incorporated by reference for all purposes). This is in contrast to the bare Si surface, where the first two O atoms are adsorbed at a bridging site in the Si dimer and then in its associated back-bond. With Sr present, the O atom first decorates the dimers until two O atoms are on the same dimer, and then the next O atom oxidizes the dimer bond. Crucially, the next O atom does not lead to an O back-bond, and so vertical formation of SiO_2 does not occur. This is in good agreement with experimental observation that the Sr passivation layer inhibits the formation of SiO_2.

[0036] In accordance with various embodiments, on the ¼ ML Sr surface, Sr preferentially protects one dimer, with O attracted to this dimer. The subsequent adsorption of additional O atoms onto an unprotected dimer causes the Sr to migrate to the new dimer and protect it instead. This explains the ability of the ¼ ML Sr to protect the Si surface from oxidation. Thus, either ½ ML or ¼ ML of Sr protects the Si surface by preferential O adsorption on the Sr-protected dimer's decorating and bridging sites, which do not lead to back-bond adsorption and SiO_2 formation.

The atomic structure of the Si/STO interface is well established.

[0037] Though there are still some open questions about the integration of STO on silicon (001), such as the accommodation of silicon surface step edges across the interface, the overall atomic structure of the interface is reasonably well understood for perovskites integrated on silicon and germanium. This understanding comes primarily from two sources, ab-initio calculations and Z-contrast scanning tunneling

electron microscopy (STEM). The dimer structure of the (2x1)-reconstructed semiconductor surface is mostly intact when half a monolayer of alkaline earth such as Sr is added, with a Zintl SrM_2 (M=Si or Ge) template formed as clearly seen in Figs. 4A-4B. In particular, Fig. 4A illustrates a 2x1 structure of the Si-STO interface with a 1/2 ML of Sr at the interface. Fig. 4B is an enlarged HAADF image from the defect-free region of the BTO/STO/Ge heterostructure showing the Ge surface step (arrow 210) between 2x and 1x periodicities.

LAO/STO deposition

[0038] The LAO/STO materials system has been heavily-studied owing to the discovery of an emergent two-dimensional electron gas at the interface of these two insulating oxides. As such, fabrication of LAO/STO heterostructures has been demonstrated with many deposition techniques including molecular beam epitaxy, pulsed laser deposition and rf magnetron sputtering. The two oxides are reasonably well lattice matched, with the main control issue being oxide stoichiometry, as quantified by the La/Al or Sr/Ti ratio. Despite significant structural distortions present at the LAO/STO interfaces, a recent report has even demonstrated the high-quality fabrication of arbitrarily thick LAO/STO superlattices grown by MBE. Therefore, with the growth of LAO/STO heterostructures firmly established in the literature, the integration of such heterostructures with silicon (001) is now discussed.

LAO/STO/Si deposition

[0039] Attempts at growing LAO directly on Si using high temperature deposition methods results in rapid interface reactions yielding amorphous films. Performing the deposition at low temperature prevents the interfacial reaction but produces an amorphous LAO film. Because LAO grows well on STO and STO can be grown epitaxially directly on Si, the growth of LAO on STO/Si has been studied by several groups. However, these still produce a silicate layer between the thin STO layer and the Si substrate after the LAO deposition because of the higher temperature needed to crystallize LAO film. A process for growing LAO on STO/Si consisting of only 2.5 unit cells of STO with clean interfaces is described in J. W. Reiner, et al., J. Appl. Phys. 105, 124501 (2009) which is hereby incorporated by reference in its entirety for all purposes.

[0040] Two unit cells of amorphous LAO are deposited at 400°C at a pressure of ~10^{-8} mbar and then heated to 700 °C under the same oxygen environment to crystallize the LAO seed layer. The oxygen pressure is then increased to ~10^{-7} mbar and La and Al are co-deposited with the pressure slowly ramped to ~10^{-6} mbar over the course of 5 minutes. LAO films up to 120 nm thick have been grown with clean interfaces using this process.

Oxygen Scavenging (Posadas)

[0041] The surface reactivity of the STO surface, which is a widely used substrate for the growth of other functional oxide thin films has been explored in A. Posadas, et al., "Scavenging of oxygen from SrTiO3 during oxide thin film deposition and the formation of interfacial 2DEGs," J. Appl. Phys. 121, 105302 (2017) which is hereby incorporated by reference in its entirety for all purposes. Various embodiments use the idea that the reactivity of the substrate with the deposited film material, particularly with regard to redox reactions, is very important. By depositing a variety of metals (Ti, Al, Nb, Pt, Eu, and Sr) and measuring the in situ core level spectra of both the metal and STO, three distinct types of behavior in thin metal films on STO (100) were demonstrated depending on the oxide formation energy and work function of the deposited metal. In many cases, there will be an interfacial layer of oxygen-deficient STO formed at the interface with the deposited metal-oxide film. This ability of STO to easily part with oxygen, combined with the large oxygen affinity of the silicon surface, clearly makes STO an unsuitable substrate for the direct deposition of silicon. It is the kinetics of scavenging, not thermodynamics that control the process of interface formation between STO and a deposited metal such as silicon.

[0042] Thus, the understanding of the oxygen scavenging process from STO suggests a general strategy of depositing silicon on crystalline oxides. The oxide materials on which crystalline silicon can be deposited must have a large affinity for oxygen, which comes with the additional benefit of being wide band gap materials. One example of such a material is the perovskite LAO. LAO has a pseudo-cubic structure and, with the usual 45º rotation, is a decent lattice match for silicon epitaxy. Indeed, such growth has been attempted with a certain level of success.

Epitaxial deposition of Si on LAO (001)

[0043] Previously, silicon was grown on LAO single crystals (see, e.g., D. O. Klenov, et al., "The Interface between Single Crystalline (001) LaAlO3 and (001) Silicon," Jap. J. of Appl. Phys. 44, L 617 (2005) which is hereby incorporated herein in its entirety for all purposes). Substrates were commercial (001) LAO single crystals with their backsides coated with 2000 Å of Ti to ensure uniform heating in the ultra-high vacuum environment of the MBE system. Samples were boiled for 15 min in de-ionized water and blown dry with N_2 prior to introduction into the ultra-high vacuum environment. The base pressure of the MBE system (DCA Instruments, Inc.) was less than 1.2 x 10^{-8} Torr with both the electron-beam-heated silicon source and the substrate hot. The substrate was heated in vacuum to temperatures between 800 and 950 ºC for deposition and exposed to a silicon flux for 20 min, resulting in ~170 nm thick films.

[0044] In situ RHEED showed a three-dimensional island (Volmer–Weber) growth mode. After growth, the films were cooled in vacuum. Selected samples were annealed in N_2 for 20 s at 900, 950 and 1025 ºC. Fig. 5 shows a high-resolution TEM (HRTEM) image. Clearly, the authors encountered the problem of wetting, as indicated by the observation of three-dimensional island formation mentioned in the text.

Si on LAO on STO on Si (001)

[0045] Various embodiments allow for sample fabrication by performing the Sr-assisted Si de-oxidation process described above. Successful de-oxidation can be confirmed by the observation of the 2x1 reconstructed silicon (001) surface in RHEED. Then, an STO template (e.g., a five unit cell STO template) can be deposited according to the Motorola process described above. After recrystallization of the STO template, an additional five unit cells of STO are deposited at 600 °C in an oxygen partial pressure of 5 x 10^{-7} Torr, resulting in ten unit cells of crystalline STO on silicon (001). When the STO growth has been completed, the substrate temperature can be increased to 750 °C and the oxygen partial pressure is ramped at the same time to 1 x 10^{-6} Torr for the LAO deposition. Fifty-unit cells of LAO are deposited atop the STO (001) surface. Crystallinity of the deposited STO and LAO layers is confirmed *in situ* using RHEED (Figs. 6A-6B).

[0046] Si deposition atop the fifty-unit cell LAO film proceeds according to a two-step process. First, the sample temperature is increased to 875 °C in ultra-high vacuum (pressure ~ 1 x 10^{-8} Torr) and Si is deposited on the LAO surface using e-beam evaporation. When enough Si has been deposited such that the LAO film is completely buried beneath the Si film, the Si deposition is temporarily halted as the substrate temperature is reduced to 600 °C. The Si deposition is resumed when the sample temperature reaches 600 °C. All subsequent Si deposition occurs at 600 °C. A similar process, entailing an initial high-temperature deposition followed by a subsequent low-temperature deposition, has been demonstrated for the epitaxial deposition of Ge on the insulating oxide $SrHfO_3$ (see e.g., Seo et al., Microelectronic Eng. 84, 2328 (2007) which is hereby incorporated herein by reference in its entirety for all purposes).

[0047] Characterization of the deposited Si surface is accomplished via *in situ* RHEED (Fig. 7). The formation of three-dimensional Si islands on the surface of the deposited LAO film can be observed. The majority phase of the Si islands appears to be commensurate with the underlying LAO lattice, as indicated by the spacing between the primary RHEED spots (circles 710 in Fig. 7). However, a secondary phase is also observed, leading to the formation of weaker spots around the primary spots in the RHEED pattern (circles 720 in Fig. 7).

[0048] After Si deposition, the resulting samples can be characterized with *in situ* XPS. Notably, only a very small O 1*s* core level peak was observed (Fig. 8), demonstrating minimal surface oxidation of the deposited Si. This is important, as it indicates the deposited Si does not scavenge oxygen from the underlying LAO film. The observed small O 1*s* core level peak in the XPS spectrum is likely due to the slight oxidation of the deposited Si surface as a result of the small residual background oxygen and water vapor pressure in the MBE and XPS systems.

[0049] After removal from the ultra-high vacuum environment, the SOS samples were characterized with scanning transmission electron microscopy (STEM). The cross-section of the layer stack indicates the excellent crystalline quality of the STO and LAO films. This can be clearly seen from the images taken in high-angle annular dark field (HAADF) mode (Fig. 9A). In this imaging mode, the intensity of the atomic columns scales roughly as the square of the atomic number *Z*. Thus, the LAO columns are the brightest (due to the large atomic mass of La), followed by the STO columns.

The Si substrate and the deposited Si are both dim when viewed in this imaging mode owing to silicon's relatively small atomic mass.

[0050] When imaged using annular bright field (ABF) mode, the deposited Si layer can be much more clearly resolved (Fig. 9B). From the image in Fig. 9B, evidence of the 3 x 1 interface reconstruction between LAO and Si can be seen. Furthermore, the image indicates the deposited Si is largely single crystalline, although some stacking faults can be observed along the right-hand side of the image. In order to more directly compare the crystalline nature of the deposited Si with that of the underlying Si substrate, selected area electron diffraction (SAED) has been carried out on the prepared STEM sample.

[0051] A comparison between the electron diffraction pattern obtained from the Si substrate and that obtained from the deposited Si (Fig. 10) shows that the two Si layers have predominantly the same crystalline symmetry. However, while the Si substrate displays a single, uniform symmetry in the diffraction analysis, additional spots are observed between major spots in the diffraction pattern of the deposited Si film. These small spots indicate the presence of defects in the deposited Si, such as stacking faults. This observation is consistent with the surface electron diffraction (RHEED) pattern presented in Fig. 7. Despite the presence of a small amount of crystalline defects in the deposited Si, the SAED analysis suggests the experimental results have succeeded in our attempts to integrate silicon (001) on Si-integrated transition metal oxide thin films, resulting in the formation of a silicon-on-oxide-on-silicon (SOS) layer stack.

Insulating oxide layer

[0052] Pertaining to the insulating oxide layer inserted in between the "$SrTiO_3$ buffer layer" and the "top silicon layer", the insulating oxide layer is not limited to $LaAlO_3$ used to demonstrate the claim. The insulating oxide layer can be any oxide that can be deposited epitaxially on STO that will not allow Si to scavenge oxygen from it and cause the formation of an amorphous SiO_2 interlayer. This means that the formation energy for the oxide should be greater than the formation energy for SiO_2 per oxygen atom. Additionally, this oxide should have a phase (stable or meta-stable) that can be reasonably lattice-matched (<5% mismatch) to Si and STO. For binary oxides, these include ZrO_2, HfO_2, CeO_2, PrO_2, BeO, MgO, γ-Al_2O_3, Y_2O_3, Sc_2O_3, and

RE_2O_3 (where RE is a medium to small rare earth element = Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu). Several ternary oxides will also satisfy the requirements, including: perovskite hafnates/zirconates ($SrZrO_3$, $SrHfO_3$, $CaZrO_3$, $CaHfO_3$, $EuZrO_3$), rare earth scandates ($YScO_3$, $REScO_3$ <RE= rare earth element>), large rare earth aluminates ($PrAlO_3$, $NdAlO_3$, $CeAlO_3$), and aluminum spinels ($MgAl_2O_4$, $BeAl_2O_4$).

Technologies and applications

[0053] The novel silicon-on-insulator-on-silicon (SOS) platform used in various embodiments can be used in many potential technological applications, depending in large part on the choice of functional oxide layer. Oxides are progressively finding use in a wide variety of applications, including magnetic sensing, silicon photonics, electronics, and photovoltaics, to name a few. Many of these oxides feature crystalline lattices compatible with that of STO, allowing for their integration into the SOS platform.

[0054] One notable area in which functional oxides are currently gaining increased interest is in the field of silicon photonics. In particular, the ferroelectric oxide $BaTiO_3$ (BTO) has garnered significant attention due to its large linear electro-optic response (the so-called Pockels effect). Current state-of-the-art BTO photonic devices employ a wafer-bonding technique, in which BTO is first epitaxially grown on silicon via an STO buffer layer and then bonded to a thermally oxidized silicon wafer via an Al_2O_3 bonding layer. This procedure results in crystalline BTO on amorphous SiO_2 and offers superior electrical and optical isolation when compared to BTO photonic devices grown directly on traditional SOI. By utilizing various embodiments of the SOS platform, the fabrication of such photonic devices can be simplified significantly.

[0055] The fabrication concept of hybrid BTO-silicon waveguides using the SOS platform bypasses the difficult and costly wafer-bonding process previously used for the fabrication of such devices by instead relying only on direct epitaxial integration techniques throughout. Critically, devices fabricated using the SOS platform can be distinguished from wafer-bonded devices by the absence of a bonding layer in the final device stack and by the orientation of the STO buffer layer with respect to the silicon waveguide (Figs. 11A-11B). Additionally, the inclusion of an insulating oxide layer between the silicon waveguide and the functional oxide is not necessary in devices

fabricated via the wafer-bonding process and is therefore unlikely to be present in wafer-bonded devices. Note the relative orientation of the STO buffer layer in the two devices, the absence of a bonding layer in the SOS-based device (Fig. 11A) and the absence of an insulating oxide layer in the wafer-bonded device (Fig. 11B).

[0056] The potential to epitaxially integrate an additional STO layer on the top silicon also opens the door for three-dimensional integration of various oxide/silicon devices into a single platform (Fig. 2). Through this procedure, made possible by the SOS platform, complicated oxide/silicon circuitry can be engineered featuring multiple layers of sensors, waveguides, detectors, and many other device types. The potential applications of such technology are numerous owing to the vast array of magnetic, electrical and optical phenomena present in transition metal oxide thin films and heterostructures.

[0057] Fig. 12 is a flowchart illustrating a set of operations 1200 for manufacturing an SOS structure in accordance with some embodiments of the present technology. As illustrated in Fig. 12, a silicon substrate can be provided (1210). Then, a buffer layer can be created (1220) by epitaxially growing a seed layer (e.g., a perovskite alloy, strontium titanate (SrTiO3), calcium titanate (CaTiO3), etc.) on the silicon substrate. An insulating oxide (e.g., LAO) can be created (1230) on top of the buffer layer. The insulating oxide may be lattice matched with the buffer layer and does not react with the silicon substrate. A top silicon layer of arbitrary thickness can be applied (1240) (e.g., via direct epitaxial deposition) on the insulating oxide. Alternating depositions of functional oxides and crystalline silicon can be applied in some embodiments (e.g., to create a three-dimensional silicon-oxide-silicon integrated photonic circuit).

[0058] In some embodiments, the top silicon layer can be applied on the insulating oxide by using a two-step growth process with an initial Si layer deposited at a first temperature that is higher than a second temperature used during deposition of a second layer. In addition, some embodiments include smoothing a surface of the top silicon layer using chemical-mechanical planarization. Some embodiments may choose the surface composition of LAO to control wetting.

[0059] Various embodiments may use different methods of growing LAO. For example, to avoid SiO_2 formation below STO, some embodiments grow amorphous

LAO (e.g., 1 nm) at low temperature and oxygen pressure, anneal to crystallize then continue normal LAO deposition, or one can start growing immediately while temperature and oxygen pressure are increasing to the LAO growth conditions. Some embodiments may use co-deposition of La/Al. Still yet, some embodiments can use alternating layers of LaO and AlO_2 to control surface termination.

Conclusion

[0060] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." As used herein, the terms "connected," "coupled," or any variant thereof means any connection or coupling, either direct or indirect, between two or more elements; the coupling or connection between the elements can be physical, logical, or a combination thereof. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or," in reference to a list of two or more items, covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0061] The above Detailed Description of examples of the technology is not intended to be exhaustive or to limit the technology to the precise form disclosed above. While specific examples for the technology are described above for illustrative purposes, various equivalent modifications are possible within the scope of the technology, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative implementations may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified to provide alternative or subcombinations. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed or implemented in parallel, or may be performed at different

times. Further any specific numbers noted herein are only examples: alternative implementations may employ differing values or ranges.

[0062] The teachings of the technology provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various examples described above can be combined to provide further implementations of the technology. Some alternative implementations of the technology may include not only additional elements to those implementations noted above, but also may include fewer elements.

[0063] These and other changes can be made to the technology in light of the above Detailed Description. While the above description describes certain examples of the technology, and describes the best mode contemplated, no matter how detailed the above appears in text, the technology can be practiced in many ways. Details of the system may vary considerably in its specific implementation, while still being encompassed by the technology disclosed herein. As noted above, particular terminology used when describing certain features or aspects of the technology should not be taken to imply that the terminology is being redefined herein to be restricted to any specific characteristics, features, or aspects of the technology with which that terminology is associated. In general, the terms used in the following claims should not be construed to limit the technology to the specific examples disclosed in the specification, unless the above Detailed Description section explicitly defines such terms. Accordingly, the actual scope of the technology encompasses not only the disclosed examples, but also all equivalent ways of practicing or implementing the technology under the claims.

[0064] To reduce the number of claims, certain aspects of the technology are presented below in certain claim forms, but the applicant contemplates the various aspects of the technology in any number of claim forms. For example, while only one aspect of the technology is recited as a computer-readable medium claim, other aspects may likewise be embodied as a computer-readable medium claim, or in other forms, such as being embodied in a means-plus-function claim. Any claims intended to be treated under 35 U.S.C. § 112(f) will begin with the words "means for", but use of the term "for" in any other context is not intended to invoke treatment under 35 U.S.C. § 112(f). Accordingly, the applicant reserves the right to pursue additional

claims after filing this application to pursue such additional claim forms, in either this application or in a continuing application.

CLAIMS

What is claimed is

1. A silicon-on-insulator-on-silicon platform comprising:

a silicon substrate;

a buffer layer of strontium titanate ($SrTiO_3$) or calcium titanate ($CaTiO_3$) formed on the silicon substrate;

a functional oxide layer;

a scavenging barrier insulating oxide layer formed on top of the functional oxide layer; and

a device silicon layer grown via direct epitaxial deposition on that scavenging barrier insulating oxide layer,

wherein the scavenging barrier insulating oxide layer is sufficiently lattice matched to silicon and the underlying functional oxide such as to allow for nucleation and subsequent single crystal growth of both the scavenging barrier oxide layer and the device silicon layer; and

wherein the scavenging barrier insulating oxide layer and functional oxide do not react with either the buffer layer or the device silicon.

2. The silicon-on-insulator-on-silicon platform of claim 1, further comprising alternating depositions of functional oxides and crystalline silicon.

3. The silicon-on-insulator-on-silicon platform of claim 2, wherein the alternating depositions of the functional oxides and crystalline silicon create a three-dimensional silicon-oxide-silicon integrated circuit.

4. The silicon-on-insulator-on-silicon platform of claim 3, wherein the integrated circuit includes an integrated photonic circuit, an integrated electronic circuit, an integrated optoelectronic circuit, or an integrated magneto-optic circuit.

5. The silicon-on-insulator-on-silicon platform of claim 2, wherein at least one of the functional oxides is ferroelectric or ferromagnetic.

6. The silicon-on-insulator-on-silicon platform of claim 5, wherein the functional oxides include $BaTiO_3$ or $La_x Sr_{1-x}MnO_3$.

7. The silicon-on-insulator-on-silicon platform of claim 1, wherein the scavenging barrier insulating oxide layer oxide layer includes $LaAlO_3$ (LAO).

8. The silicon-on-insulator-on-silicon platform of claim 1, wherein the silicon substrate is a bulk silicon wafer or a silicon layer on a silicon-on-insulator wafer.

9. A method for producing silicon-on-insulator-on-silicon platforms via direct deposition techniques, the method comprising:

creating a buffer layer by epitaxially growing a seed layer of strontium titanate ($SrTiO_3$) or calcium titanate ($CaTiO_3$) on a silicon substrate;

creating an insulating scavenging barrier oxide on top of the buffer layer,

wherein the insulating oxide is lattice matched with the buffer layer and does not react with the silicon substrate or the buffer layer; and

applying, via direct epitaxial deposition, a top silicon layer of arbitrary thickness on the insulating oxide.

10. The method of claim 9, wherein applying the top silicon layer on the insulating oxide is achieved using a two-step growth process with an initial Si layer deposited at a first temperature that is higher than a second temperature used during deposition of a second layer.

11. The method of claim 9, further comprising smoothing a surface of the top silicon layer using chemical-mechanical planarization.

12. The method of claim 9, further comprising applying alternating depositions of functional oxides and crystalline silicon.

13. The method of claim 12, wherein the alternating depositions of the functional oxides and crystalline silicon create a three-dimensional silicon-oxide-silicon integrated circuit.

14. The method of claim 13, wherein the three-dimensional silicon-oxide-silicon integrated circuit includes an integrated photonic circuit, an integrated electronic circuit, an integrated optoelectronic circuit, or an integrated magneto-optic circuit.

15. The method of claim 9, wherein the insulating oxide includes $LaAlO_3$.

16. The method of claim 9, wherein creating the insulating scavenging barrier oxide on top of the buffer layer includes growing an epitaxial layer of the insulating oxide on top of the buffer layer.

17. The method of claim 9, wherein the insulating oxide includes LAO and the method further comprises:

growing an amorphous 1 nm LAO at a first temperature and oxygen pressure;

annealing to crystallize; and

continuing normal LAO deposition.

18. The method of claim 9, wherein the insulating oxide includes LAO and the insulating oxide is grown while temperature and oxygen pressure are increasing to LAO growth conditions.

19. The method of claim 9, further comprising use of a co-deposition of La/Al or alternating layers of LaO and AlO2 to control surface termination.

20. The method of claim 9, wherein the insulating oxide includes LAO and the method further comprises selecting a surface composition of LAO to control wetting.

21. The method of claim 9, wherein the silicon substrate is a bulk silicon wafer or a silicon layer from a silicon-on-insulator wafer.

22. A method for integrating crystalline silicon atop functional oxides via an epitaxial, insulating oxide buffer layer, the method comprising:

creating a buffer layer by epitaxially growing a seed layer of strontium titanate ($SrTiO_3$) or calcium titanate ($CaTiO_3$) on a silicon substrate;

creating a functional oxide on the buffer layer;

creating an insulating scavenging barrier oxide on top of the functional oxide,

wherein the insulating oxide is lattice matched with the functional oxide layer and does not react with the functional oxide; and

applying, via direct epitaxial deposition, a top silicon layer of arbitrary thickness on the insulating oxide.

23. The method of claim 22, wherein the insulating oxide buffer layer include γ-alumina or $LaAlO_3$.

24. The method of claim 22, wherein the function oxide includes $BaTiO_3$ or $LaSrMnO_3$.

25. The method of claim 22, wherein the silicon substrate is a bulk silicon wafer or a silicon layer on a silicon-on-insulator wafer.

26. The method of claim 22, wherein at least one of the functional oxide is ferroelectric, ferromagnetic, elastooptic, magnetoelastic, or piezoelectric.

27. The method of claim 22, wherein the functional oxide includes $BaTiO_3$, $La_x Sr_{1-x}MnO_3$, or $SrMnO_3$.

28. A method comprising:

directly depositing crystalline silicon atop functional oxides without oxygen scavenging; and

processing the crystalline silicon to create an oxidation and amorphization of the crystalline silicon.

29. A silicon-on-insulator-on-silicon platform comprising crystalline silicon directly deposited atop functional oxides without oxygen scavenging, subsequent oxidation and amorphization of deposited silicon, or wafer bonding.

30. The silicon-on-insulator-on-silicon platform comprising of claim 29, wherein at least one of the functional oxides are ferroelectric, ferromagnetic, elastooptic, magnetoelastic, or piezoelectric.

31. The silicon-on-insulator-on-silicon platform comprising of claim 29, wherein the functional oxides include $BaTiO_3$, or $LaMnO_3$,

32. A silicon-on-insulator-on-silicon platform comprising:

a silicon substrate;

a buffer layer that includes an epitaxial oxide buffer layer formed on the silicon substrate;

an insulating oxide layer formed on top of the buffer layer,

wherein the insulating oxide layer is a scavenging barrier layer to prevent oxygen scavenging from the buffer layer; and

a device silicon layer grown via direct epitaxial deposition on the insulating oxide layer,

wherein the insulating oxide layer is sufficiently lattice matched with the device silicon layer and does not react with the device silicon.

33. The silicon-on-insulator-on-silicon platform of claim 32, wherein the epitaxial oxide buffer layer includes strontium titanate ($SrTiO_3$) or calcium titanate ($CaTiO_3$).

34. The silicon-on-insulator-on-silicon platform of claim 32, wherein the silicon substrate is a bulk silicon wafer or a silicon layer on a silicon-on-insulator wafer.

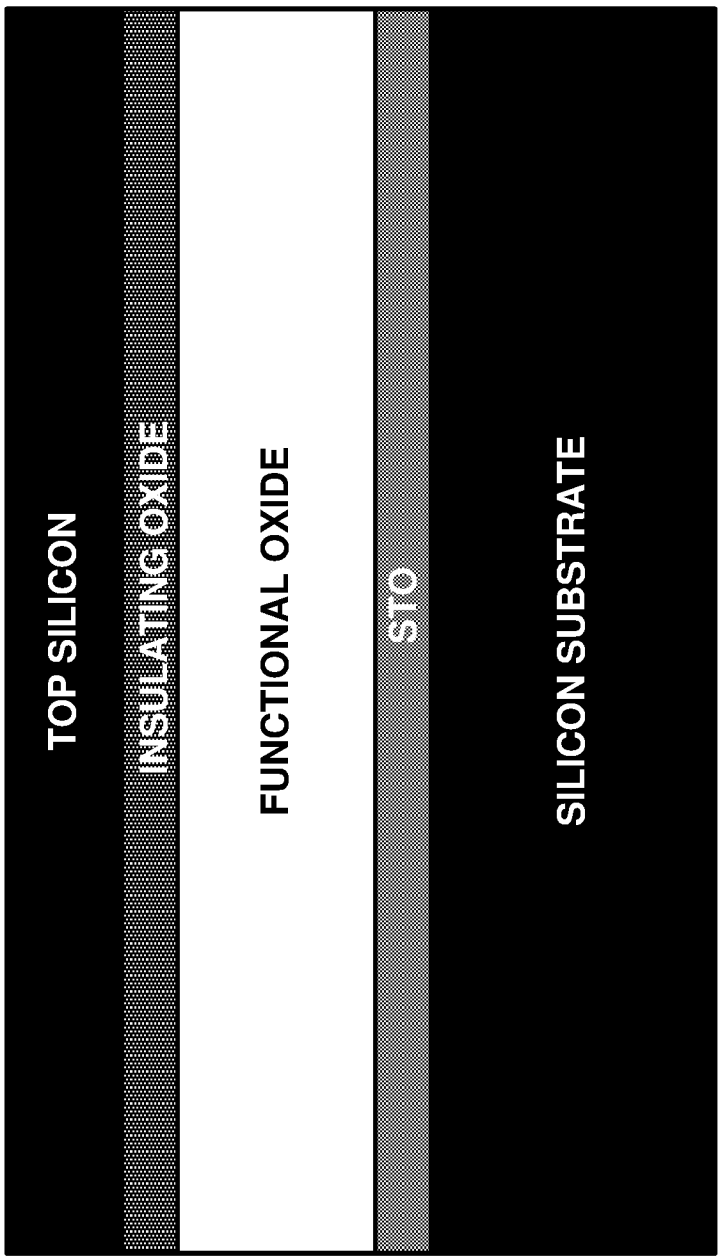
TOP SILICON
INSULATING OXIDE
FUNCTIONAL OXIDE
STO
SILICON SUBSTRATE

FIG. 1

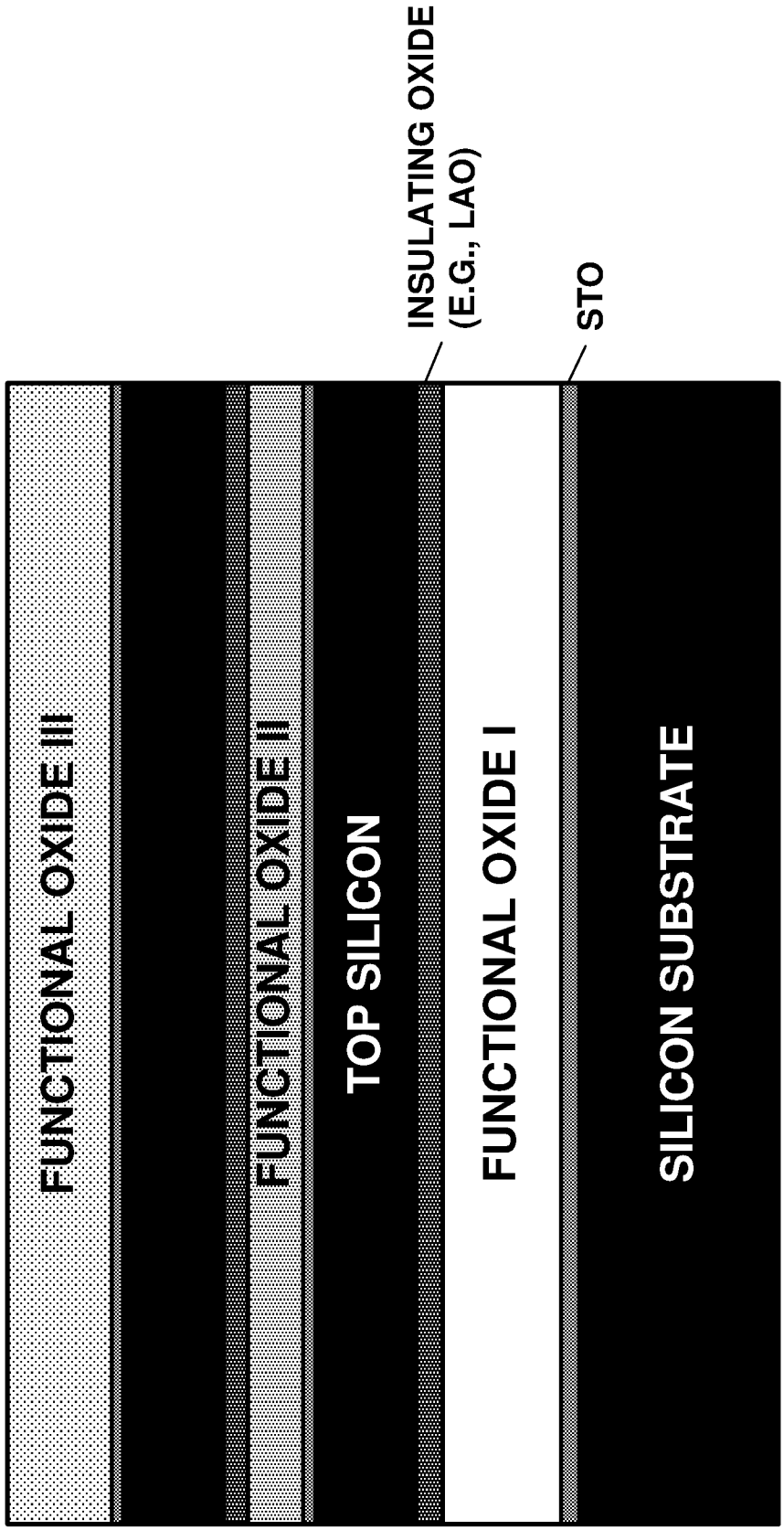
FUNCTIONAL OXIDE III
FUNCTIONAL OXIDE II
TOP SILICON
INSULATING OXIDE
(E.G., LAO)
STO
FUNCTIONAL OXIDE I
SILICON SUBSTRATE

FIG. 2

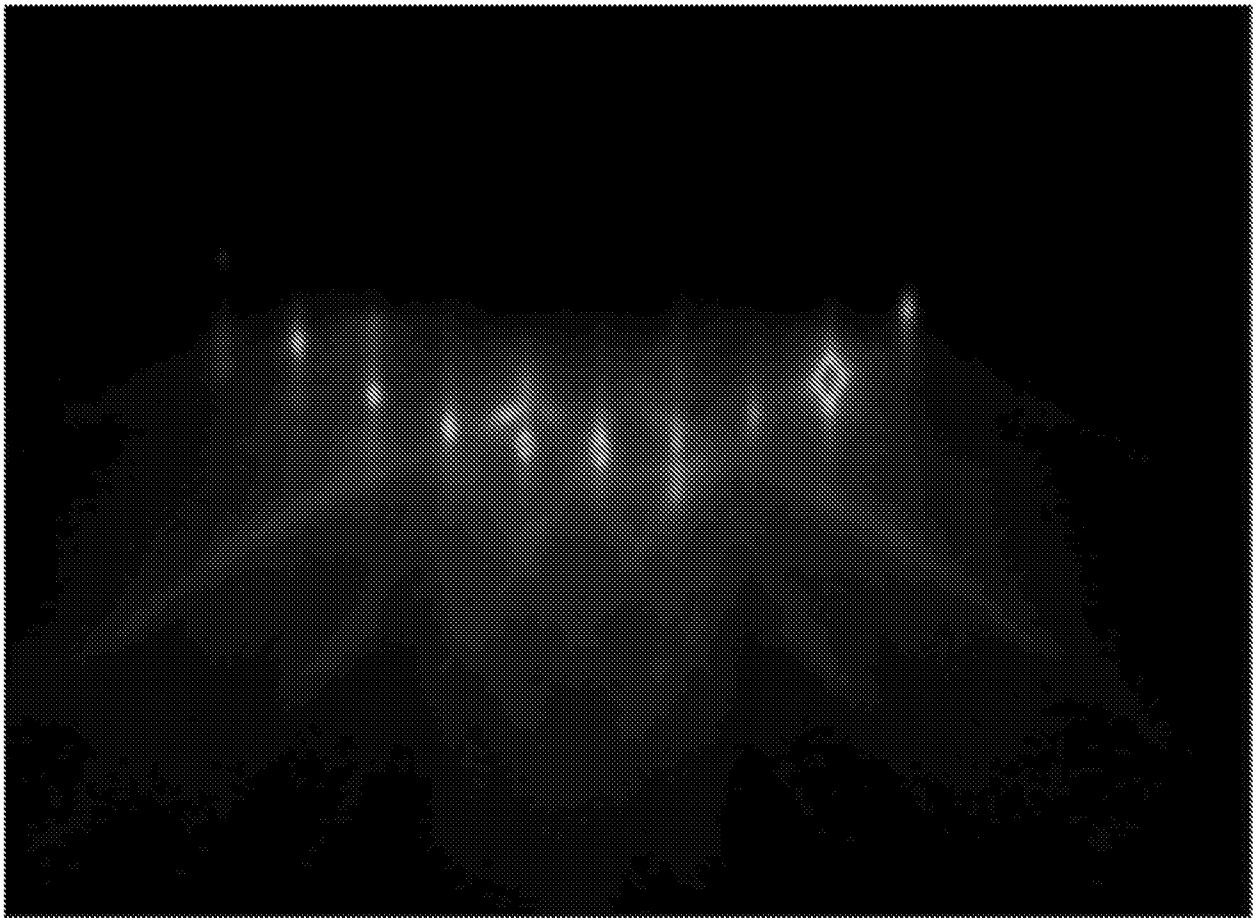

FIG. 3

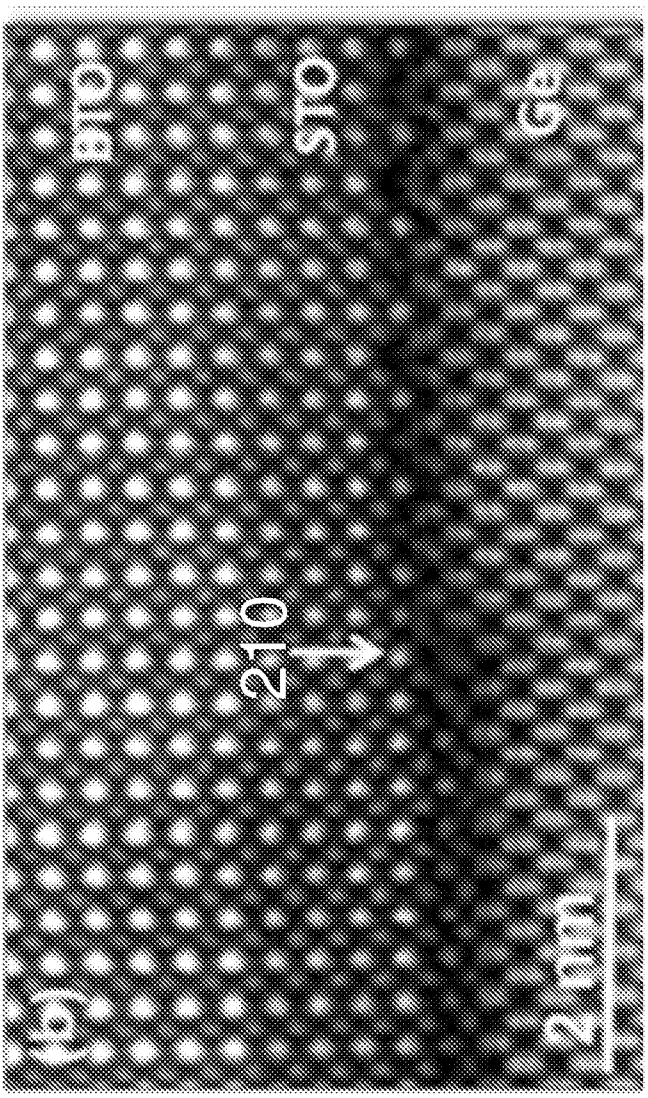

FIG. 4B

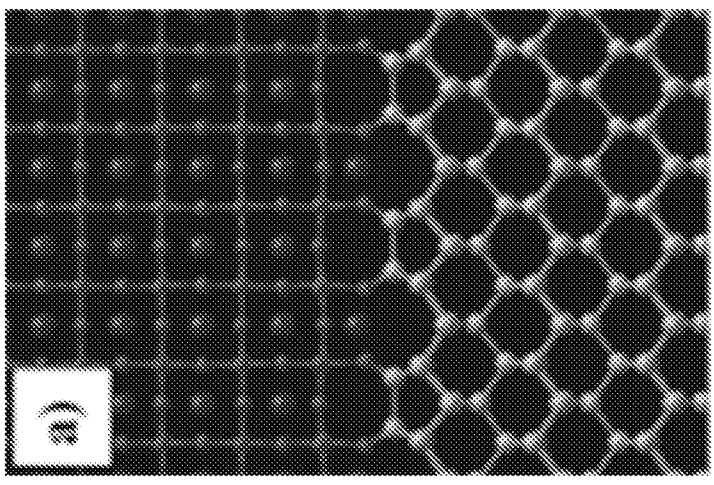

FIG. 4A

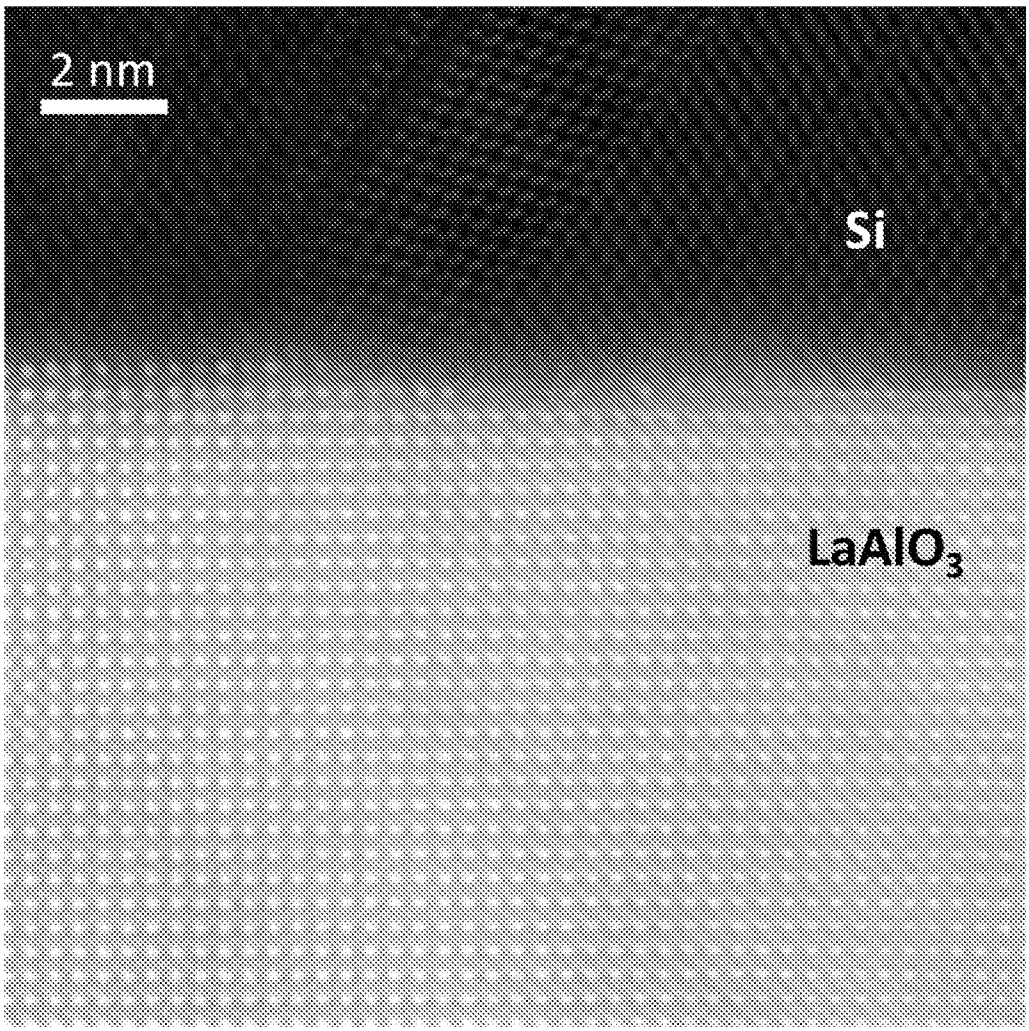

FIG. 5

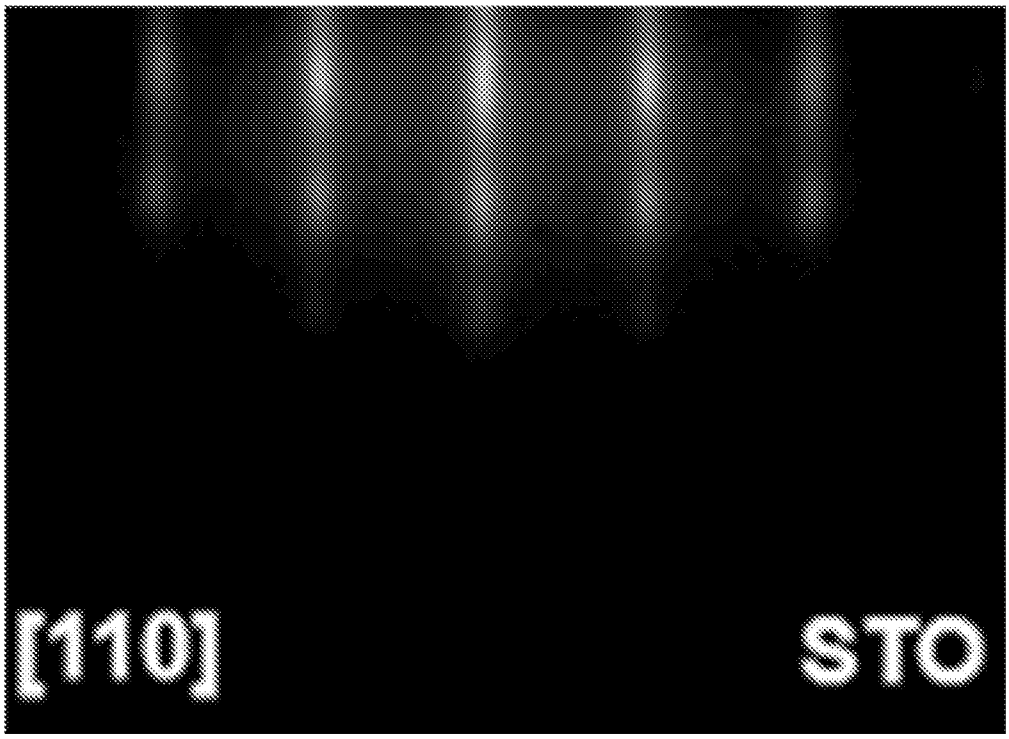

FIG. 6A

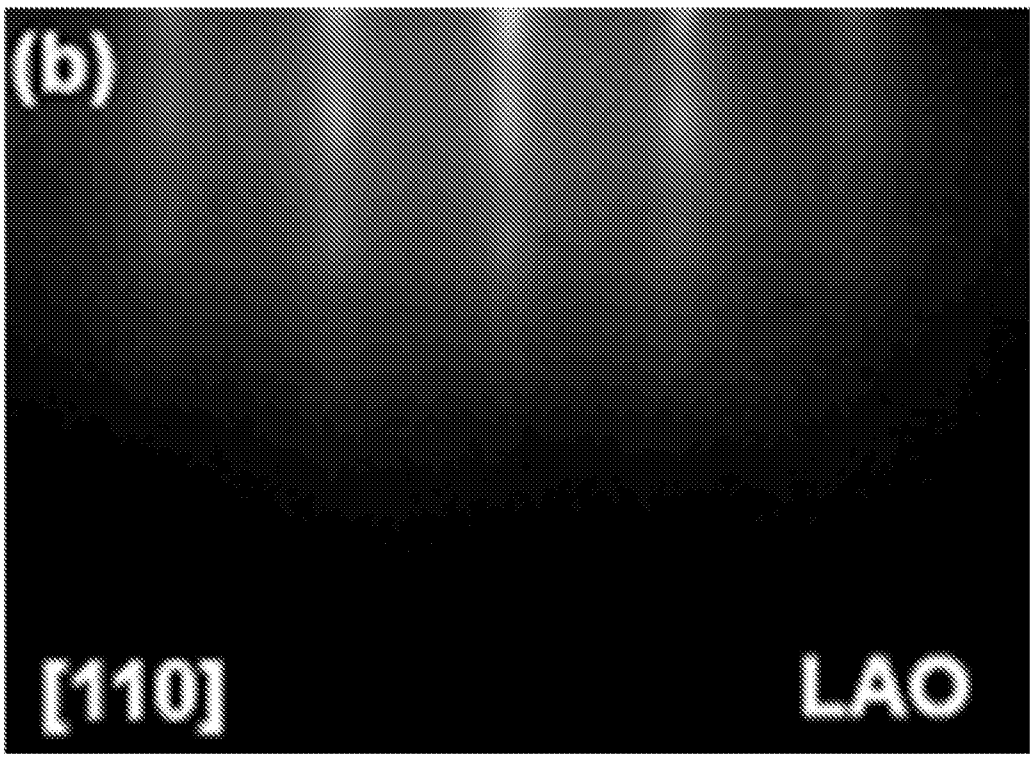

FIG. 6B

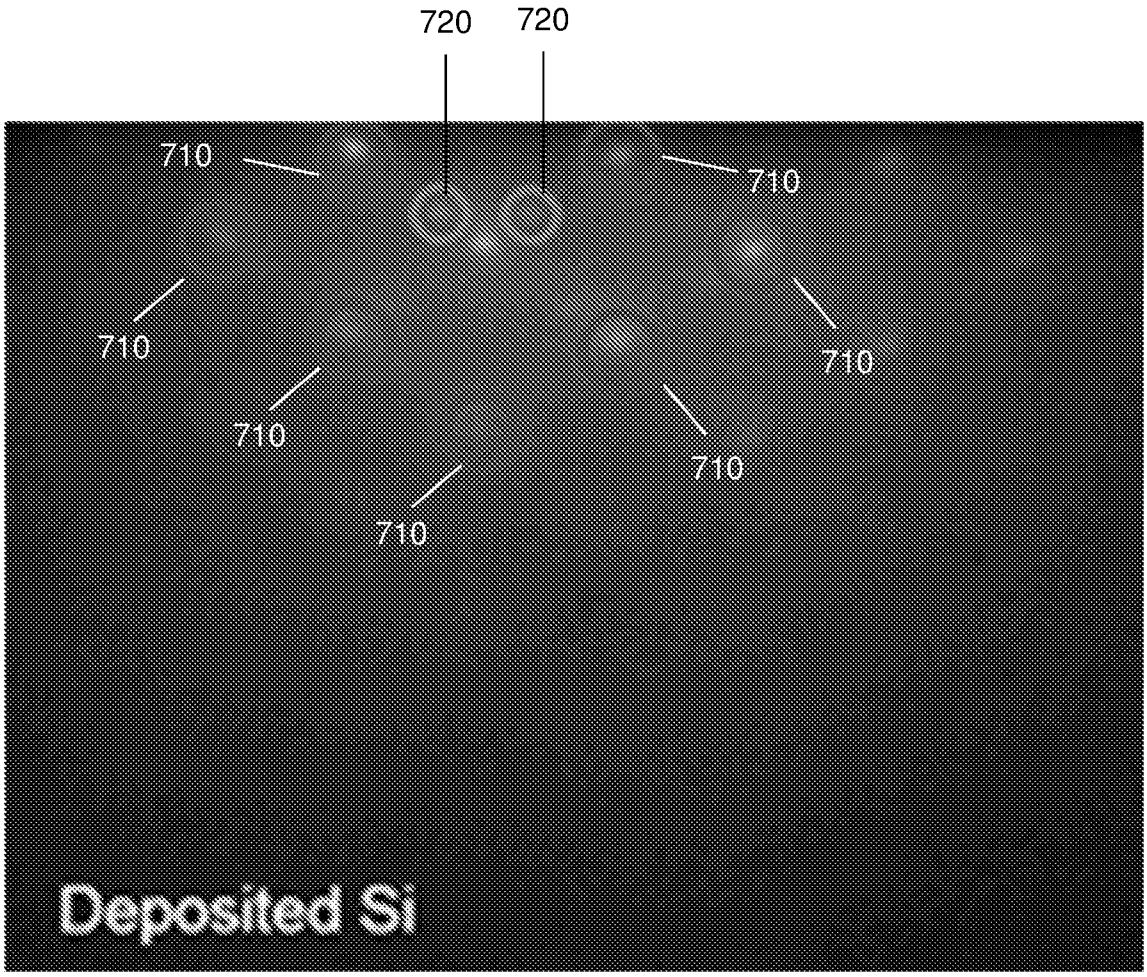

FIG. 7

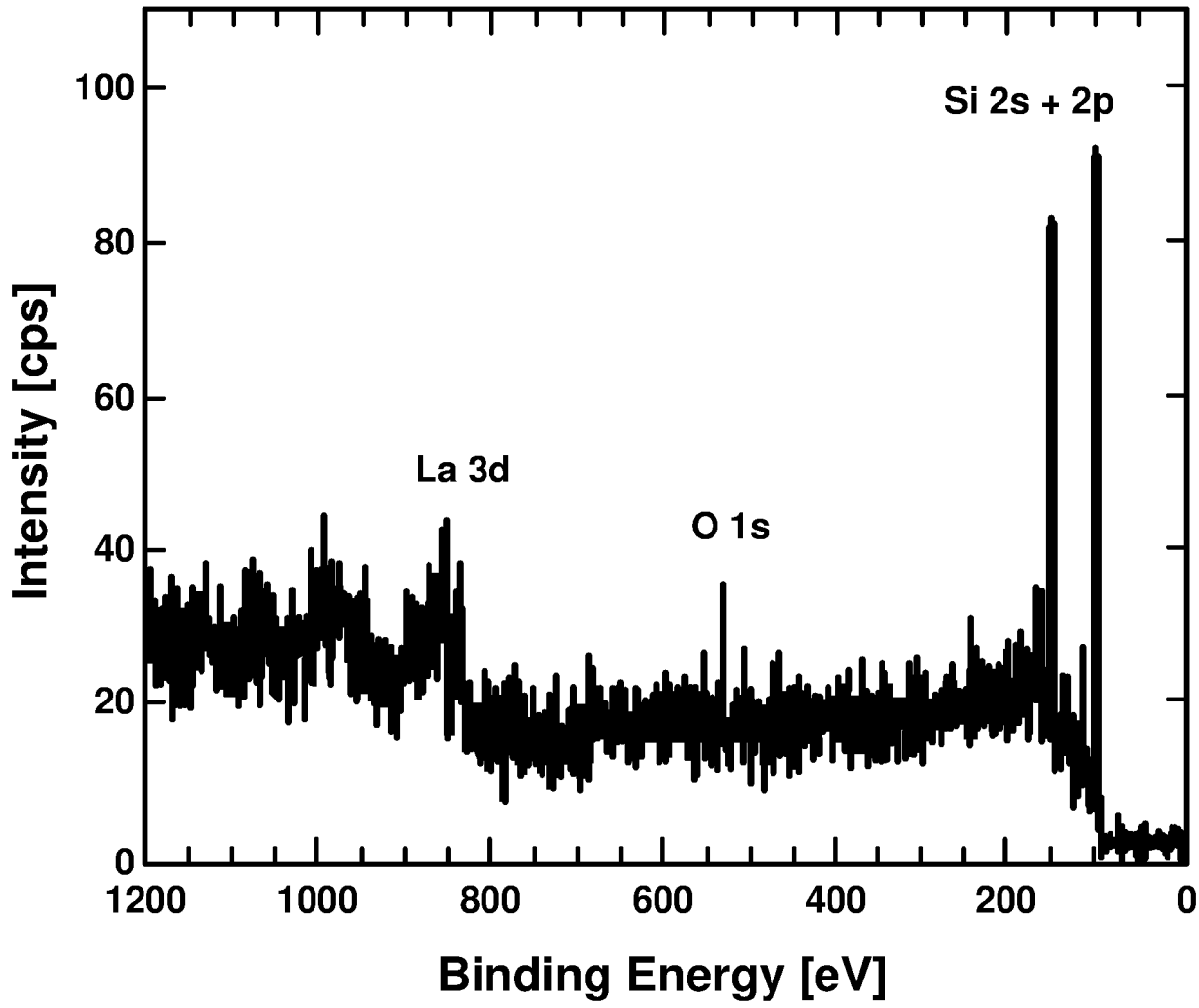
Intensity [cps]
100
80
60
40
20
0
1200
1000
800
600
400
200
0
Binding Energy [eV]
Si 2s + 2p
La 3d
O 1s

FIG. 8

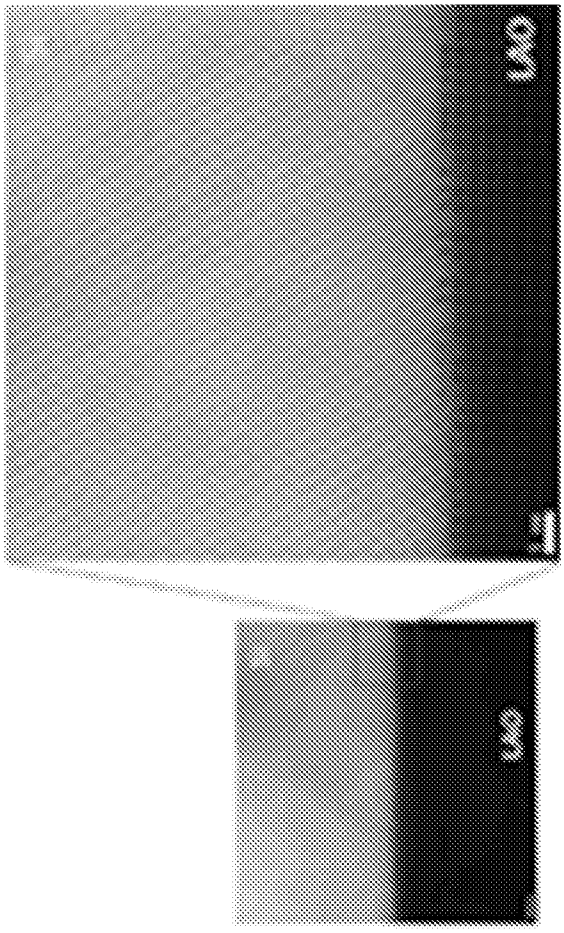

FIG. 9B

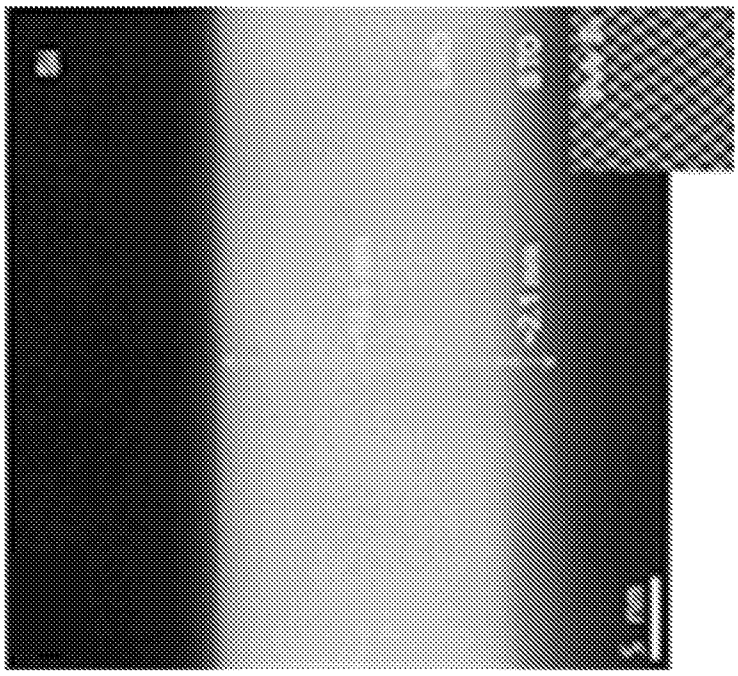

FIG. 9A

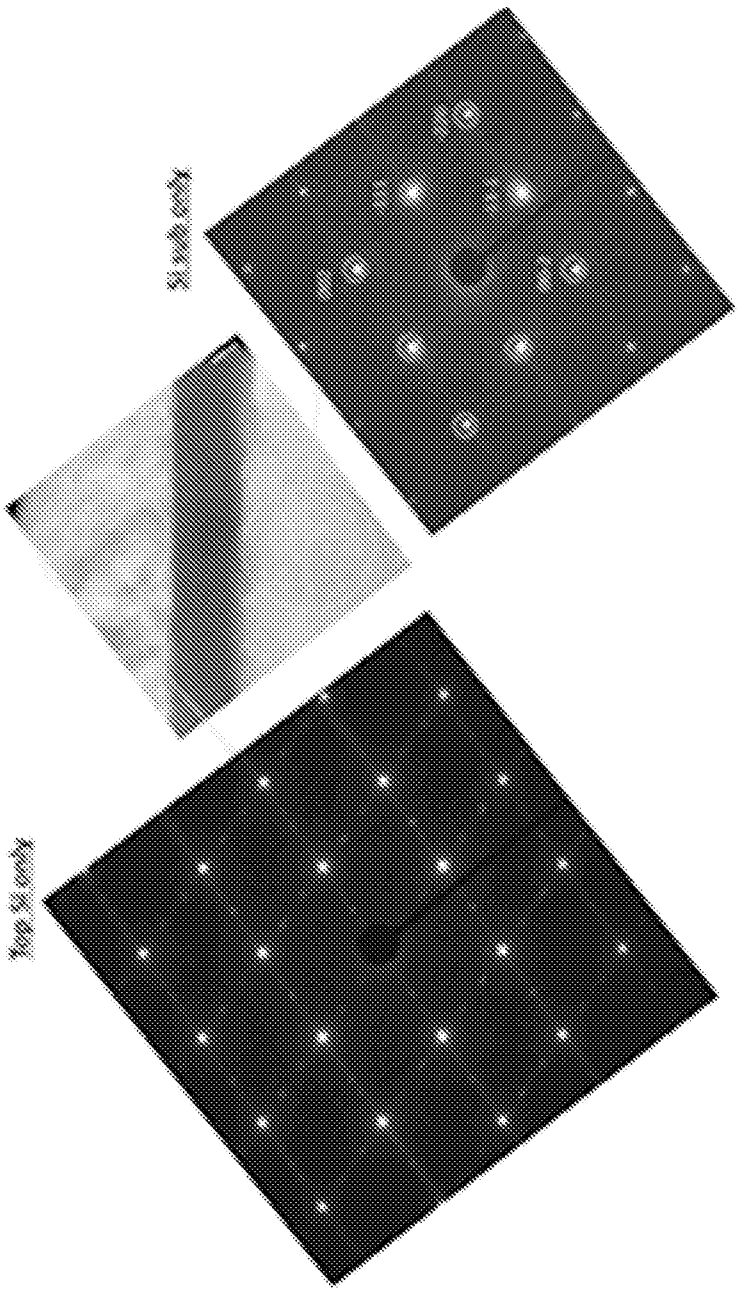

FIG. 10

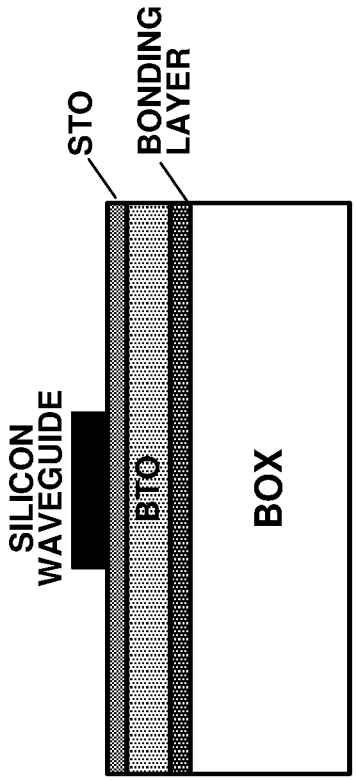

FIG. 11B

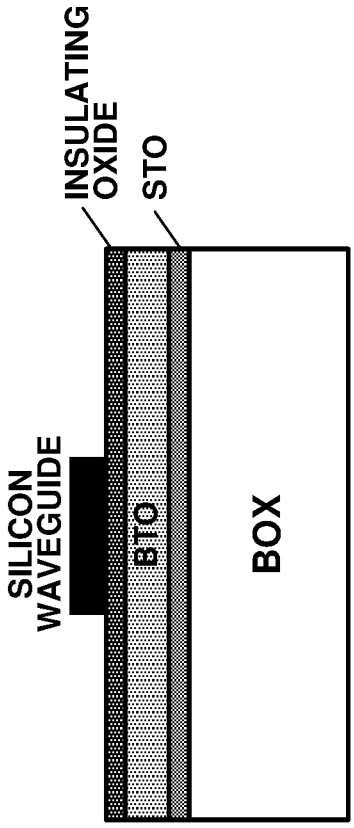

FIG. 11A

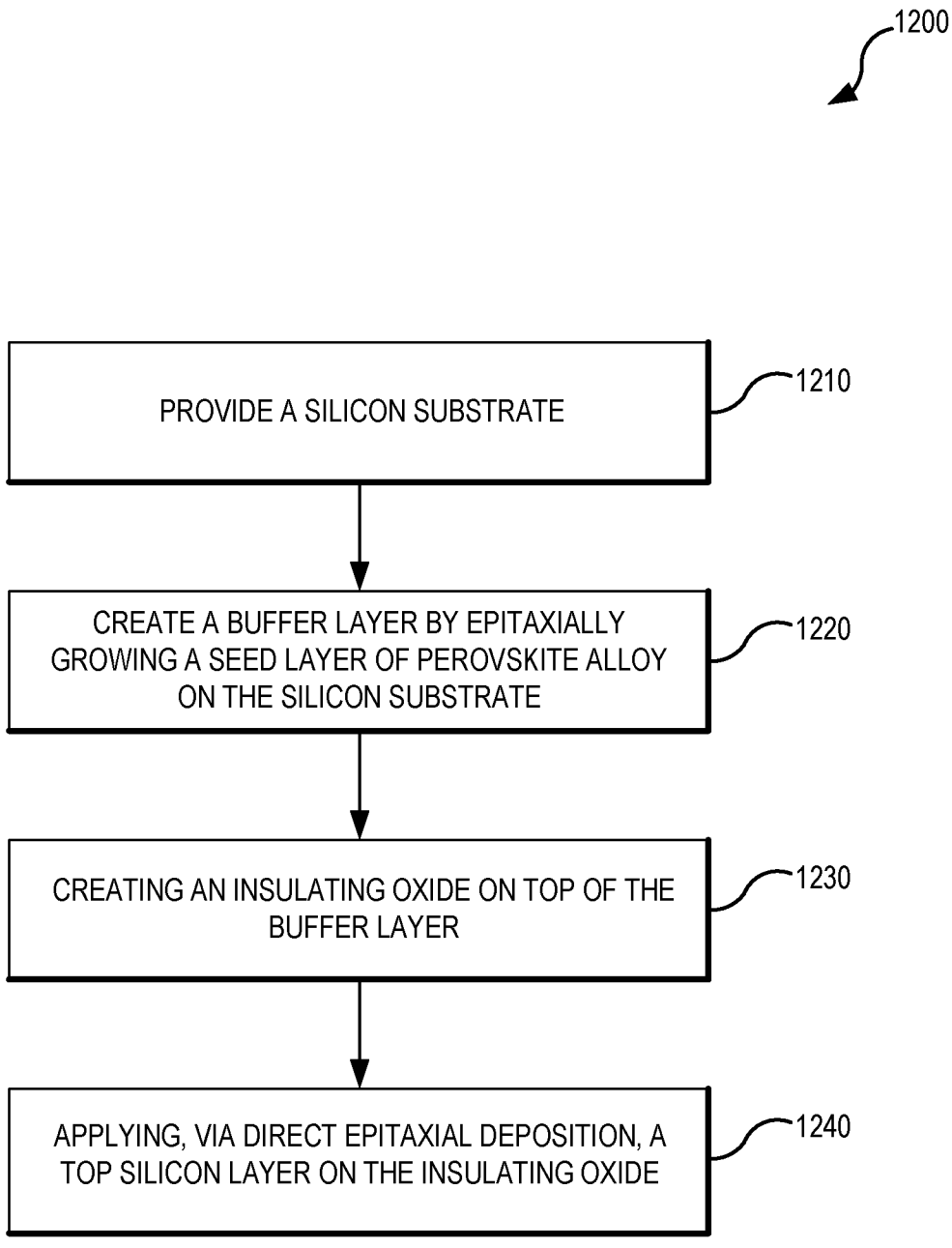
1200
PROVIDE A SILICON SUBSTRATE
1210
CREATE A BUFFER LAYER BY EPITAXIALLY GROWING A SEED LAYER OF PEROVSKITE ALLOY ON THE SILICON SUBSTRATE
1220
CREATING AN INSULATING OXIDE ON TOP OF THE BUFFER LAYER
1230
APPLYING, VIA DIRECT EPITAXIAL DEPOSITION, A TOP SILICON LAYER ON THE INSULATING OXIDE
1240

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/20910

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01L 27/088; H01L 29/423; H01L 29/66 (2020.01)

CPC - H01L 21/76834; H01L 21/76897; H01L 27/088; H01L 27/1207

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014/0346587 A1 (International Business Machines Corporation) 27 November 2014 (27.11.2014) para [0004], [0016], [0017], [0026].	1-8, 32-34
A	US 2017/0141750 A1 (IQE, PLC) 18 May 2017 (18.05.2017) para [0042], [0061]	1-8, 32-34
A	US 2005/0035345 A1 (Lin et al.) 17 February 2005 (17.02.2005) entire document	1-8, 32-34
A	US 2009/0011575 A1 (Shinomura et al.) 08 Janurary 2009 (08.01.2009) entire document	1-8, 32-34

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 May 2020	01 JUL 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/20910

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
(see supplemental box)

1. ☐ As all *required additional search fees were timely paid by the applicant, this international search report covers all searchable* claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-8, 32-34

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US 20/20910

Continuation of Box III

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I: Claims 1-8, 32-34 is directed towards a silicon-on-insulator-on-silicon platform comprising: a silicon substrate; a buffer layer of strontium titanate (SrTiO3) or calcium titanate (CaTiO3) formed on the silicon substrate; a functional oxide layer; a scavenging barrier insulating oxide layer formed on top of the functional oxide layer; and a device silicon layer grown via direct epitaxial deposition on that scavenging barrier insulating oxide layer, wherein the scavenging barrier insulating oxide layer is sufficiently lattice matched to silicon and the underlying functional oxide such as to allow for nucleation and subsequent single crystal growth of both the scavenging barrier oxide layer and the device silicon layer; and wherein the scavenging barrier insulating oxide layer and functional oxide do not react with either the buffer layer or the device silicon.

Group II: Claims 9-27 is directed towards a method for producing silicon-on-insulator-on-silicon platforms via direct deposition techniques, the method comprising: creating a buffer layer by epitaxially growing a seed layer of strontium titanate (SrTiO3) or calcium titanate (CaTiO3) on a silicon substrate; creating an insulating scavenging barrier oxide on top of the buffer layer, wherein the insulating oxide is lattice matched with the buffer layer and does not react with the silicon substrate or the buffer layer; and applying, via direct epitaxial deposition, a top silicon layer of arbitrary thickness on the insulating oxide.

Group III: Claims 28-31 is directed towards a method comprising: directly depositing crystalline silicon atop functional oxides without oxygen scavenging; and processing the crystalline silicon to create an oxidation and amorphization of the crystalline silicon.

The inventions listed as Groups I-III do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:

Group I requires a silicon-on-insulator-on-silicon platform comprising: a silicon substrate; a buffer layer of strontium titanate (SrTiO3) or calcium titanate (CaTiO3) formed on the silicon substrate; a functional oxide layer; a scavenging barrier insulating oxide layer formed on top of the functional oxide layer; and a device silicon layer grown via direct epitaxial deposition on that scavenging barrier insulating oxide layer, wherein the scavenging barrier insulating oxide layer is sufficiently lattice matched to silicon and the underlying functional oxide such as to allow for nucleation and subsequent single crystal growth of both the scavenging barrier oxide layer and the device silicon layer; and wherein the scavenging barrier insulating oxide layer and functional oxide do not react with either the buffer layer or the device silicon, not required by groups II and III

Group II requires a method for producing silicon-on-insulator-on-silicon platforms via direct deposition techniques, the method comprising: creating a buffer layer by epitaxially growing a seed layer of strontium titanate (SrTiO3) or calcium titanate (CaTiO3) on a silicon substrate; creating an insulating scavenging barrier oxide on top of the buffer layer, wherein the insulating oxide is lattice matched with the buffer layer and does not react with the silicon substrate or the buffer layer; and applying, via direct epitaxial deposition, a top silicon layer of arbitrary thickness on the insulating oxide, not required by groups I or III.

Group III requires a method comprising: directly depositing crystalline silicon atop functional oxides without oxygen scavenging; and processing the crystalline silicon to create an oxidation and amorphization of the crystalline silicon, not required by groups I-II.

Shared Technical Features:

Groups I and III share the common feature of a silicon-on-insulator-on-silicon platform comprising: a silicon substrate and a buffer layer of strontium titanate (SrTiQ3) or calcium titanate (CaTiQ3) formed on the silicon substrate. However, these shared technical features do not represent a contribution over prior art, because the shared technical feature is anticipated by US 2014/0346587 A1 to International Business Machines Corporation (hereinafter 'International'). International discloses a silicon-on-insulator-on-silicon platform (para [0016] "It should be further realized that while the embodiments...will be described in the context of ETSOI (ETSOI stands for 'extremely thin silicon on insulator') comprising: a silicon substrate (para [0004] " crystalline semiconductor substrate"; it is understood the semiconductor is silicon as its based on a silicon-on-insulator substrate) and a buffer layer of strontium titanate (SrTiQ3) or calcium titanate (CaTiQ3) formed on the silicon substrate (para [0004] " depositing a layer of crystalline dielectric material onto a surface of the crystalline semiconductor substrate"; para [0026] "The crystalline dielectric layer...may include...strontium titanate").

As the shared technical features were known in the art at the time of the invention, they cannot be considered special technical features that would otherwise unify the groups. Therefore, Groups I-III lack unity under PCT Rule 13.