

(57) Abstract: A Schottky rectifier is provided. The Schottky rectifier comprises: (a) a semiconductor region having first and second opposing faces, with the semiconductor region comprising a cathode region of first conductivity type adjacent the first face and a drift region having a lower net doping concentration than that of the cathode region; (b) one or more trenches extending from the second face into the semiconductor region and defining one or more mesas within the semiconductor region; (c) an insulating region adjacent the semiconductor region in lower portions of the trench; (d) and an anode electrode that is (i) adjacent to and forms a Schottky rectifying contact with the semiconductor at the second face, (ii) adjacent to and forms a Schottky rectifying contact with the semiconductor region within upper portions of the trench and (iii) adjacent to the insulating region within the lower portions of the trench.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TRENCH SCHOTTKY RECTIFIER

FIELD OF THE INVENTION

This invention relates to rectifiers and more particularly to Schottky barrier rectifying devices, and methods of forming these devices.

BACKGROUND OF THE INVENTION

Rectifiers exhibit relatively low resistance to current flow in a forward direction and a high resistance to current flow in a reverse direction. Schottky barrier rectifiers are a type of rectifier that have found use as output rectifiers in switching-mode power supplies and in other high-speed power switching applications, such as motor drives. These devices are capable of carrying large forward currents and supporting large reverse blocking voltages.

U.S. Patent No. 5,365,102 to Mehrotra et al. and entitled "Schottky Barrier Rectifier with MOS Trench", the entire disclosure of which is hereby incorporated by reference, discloses Schottky barrier rectifiers which have a higher breakdown voltage than is theoretically attainable with an ideal abrupt parallel-plane P-N junction. A cross-sectional representation of one embodiment of the described rectifiers is illustrated in FIG. 1. In this figure, rectifier 10 includes a semiconductor substrate 12 of first conductivity type, typically N-type conductivity, having a first face 12a and a second opposing face 12b. The substrate 12 comprises a relatively highly doped cathode region 12c (shown as N⁺) adjacent the first face 12a. A drift region 12d of first conductivity type (shown as N) extends from the cathode region 12c to the second face 12b. Accordingly, the doping concentration

of the cathode region 12c is greater than that of the drift region 12d. A mesa 14 having a cross-sectional width " W_m ", defined by opposing sides 14a and 14b, is formed in the drift region 12d. The mesa can be of stripe, rectangular, cylindrical or other similar geometry. Insulating regions 16a and 16b (described as SiO_2) are also provided on the mesa sides. The rectifier also includes an anode electrode 18 on the insulating regions 16a, 16b. The anode electrode 18 forms a Schottky rectifying contact with the mesa 14 at second face 12b. The height of the Schottky barrier formed at the anode electrode/mesa interface is dependent on the type of electrode metal and semiconductor (e.g., Si, Ge, GaAs, and SiC) used and is also dependent on the doping concentration in the mesa 14. Finally, a cathode electrode 20 is provided adjacent the cathode region 12c at the first face 12a. The cathode electrode 20 ohmically contacts cathode region 12c.

According to U.S. Patent No. 5,612,567, desirable effects are achieved with the device of FIG. 1, due to the occurrence of charge coupling between the majority charge carriers in the mesa-shaped portion of the drift region 14 and the portion of the metal anode 18 opposite the insulated sidewalls 16a, 16b of the trenches. Specifically, the electric field at center of the metal-semiconductor contact (Schottky contact) is reduced significantly relative to an ideal plane-parallel rectifier. The reduction in electric field at the center of the Schottky contact causes a significant decrease in the reverse-biased leakage current through a reduction in Schottky barrier height lowering. Reverse-biased leakage current is the current in the rectifier during a reverse-biased (blocking) mode of operation. Moreover, the peak in the electric field profile shifts away from the metal-semiconductor contact and into the drift region. As the peak of the electric field moves away from the Schottky contact, the mesa is able to support more voltage, and thus provides higher breakdown voltages (reverse blocking voltages) than those of an ideal parallel-plane rectifier.

As the voltages of modern power supplies continue to decrease in response to need for reduced power consumption and increased energy efficiency, it becomes advantageous to decrease the forward-biased voltage drop across a power rectifier. The need for reduced power consumption also generally makes it advantageous to

minimize reverse-biased leakage current. Hence, to minimize power consumption, both the forward-biased voltage drop and reverse-biased leakage current should be minimized.

Unfortunately, although the trench Schottky rectifier of U.S. Patent No. 5,365,102 results in high reverse-biased breakdown voltage (blocking voltages) and lower reverse-biased leakage current, this design is nevertheless disadvantageous for many energy-efficient applications, because it results in an undesirably high forward-biased voltage drop across the rectifier.

U.S. Patent No. 5,612,567 to Bagila and entitled "Schottky Barrier Rectifiers and Methods of Forming the Same," the entire disclosure of which is hereby incorporated by reference, discloses that low forward-biased voltage drop, low reverse-biased leakage current and high breakdown voltage can be simultaneously achieved by modifying the trench Schottky rectifier of U.S. Patent No. 5,365,102. Specifically, the mesa-shaped portion of the drift region is provided with a non-uniform doping concentration, which is said to provide low forward-biased voltage drop, along with high blocking voltage capability and low reverse-biased leakage current. The drift region is preferably non-uniformly doped so that the doping concentration increases monotonically in a direction away from the Schottky rectifying junction formed between the anode electrode and the drift region. This non-uniform doping is preferably achieved by performing computer-controlled in-situ doping, during epitaxial growth of the drift region upon a more highly doped cathode region. The doping profile and concentrations are preferably selected so that when the rectifier is reverse biased at the onset of breakdown, the electric field profile in the drift region is substantially uniform and/or negatively sloped to have a monotonically decreasing profile in a direction from the Schottky rectifying junction to the cathode region.

Unfortunately, the need for a graded doping profile introduces substantial complexity, and hence expense, into the manufacturing process. Accordingly, there remains a need within the art to provide a Schottky barrier rectifier device that can be easily manufactured, while simultaneously providing low forward-biased voltage drop, low reverse-biased leakage current and high breakdown voltage.

SUMMARY OF THE INVENTION

The above and other needs are met by the present invention. In particular, a Schottky rectifier is provided which comprises: (a) a semiconductor region having first and second opposing faces, with the semiconductor region comprising a cathode region of first conductivity type adjacent the first face and a drift region of the first conductivity type adjacent the second face, and with the drift region having a lower net doping concentration than that of the cathode region; (b) one or more trenches extending from the second face into the semiconductor region and defining one or more mesas within the semiconductor region; (c) an insulating region adjacent the semiconductor region in lower portions of the trench; (d) and an anode electrode that is (i) adjacent to and forms a Schottky rectifying contact with the semiconductor region at the second face, (ii) adjacent to and forms a Schottky rectifying contact with the semiconductor region within upper portions of the trench and (iii) adjacent to the insulating region within the lower portions of the trench.

Preferably, the semiconductor is silicon, the first conductivity type is n-type conductivity, and a cathode electrode is provided on the first face.

The lower portions of the trenches preferably correspond to approximately 25 to 40% of the depth of the trenches. In some embodiments, the trench extends into the cathode region, with the insulated lower portions of the trench preferably extending between the cathode region and the drift region.

The insulating region preferably comprises silicon dioxide, which can be either deposited or thermally grown.

In some embodiments, a polysilicon region is disposed on the insulating region and forms part of the anode electrode.

The present invention also provides a method of forming a trench Schottky rectifier. The method comprises: (a) forming a semiconductor region having first and second opposing faces, with the semiconductor region comprising a cathode region of first conductivity type adjacent the first face and a drift region of the first conductivity type adjacent the second face, and with the drift region having a lower

net doping concentration than that of the cathode region; (b) forming one or more trenches extending from the second face into the semiconductor region, with the trenches defining one or more mesas within the semiconductor region; (c) forming an insulating region adjacent the semiconductor region in lower portions of the trench; (d) and forming an anode electrode that is (i) adjacent to and forms a Schottky rectifying contact with the semiconductor region at the second face, (ii) adjacent to and forms a Schottky rectifying contact with the semiconductor region within upper portions of the trench and (iii) adjacent to the insulating region within the lower portions of the trench.

The step of forming the semiconductor region preferably comprises providing a semiconductor substrate that corresponds to the cathode region, and growing an epitaxial semiconductor layer that corresponds to the drift region on the substrate.

The step of forming the trenches preferably comprises the steps of forming a patterned masking layer over the second face of the semiconductor region and etching the trenches through the masking layer.

The step of forming the insulating region can comprise providing an oxide layer over the second face and in the trenches, and subsequently etching portions of the oxide layer. In some embodiments, a photoresist pattern is provided on the oxide layer (which can be thermally grown), and portions of the oxide layer not covered by the photoresist etched, whereupon the photoresist is removed. In other embodiments, a polysilicon layer is provided on the oxide layer (which can be thermally grown), and the polysilicon layer is etched such that portions of the oxide layer over the second face and over the upper portions of the trenches are exposed, and these exposed portions are subsequently removed by etching.

The step of forming the insulating region can also comprise depositing an oxide layer. For example, a tetraethylorthosilicate layer can be deposited on the second face and within the trenches. The tetraethylorthosilicate layer can then be etched until it is removed from the second surface and the upper portions of the trenches. Subsequently, the tetraethylorthosilicate can be converted into a high-density silicon dioxide layer.

One advantage of the present invention is that a novel Schottky barrier rectifier is provided having low forward-biased voltage drop, low reverse-biased leakage current and high breakdown voltage.

Another advantage is that such a Schottky barrier rectifier can be made using simple, and thus economical, manufacturing techniques.

Still other embodiments and advantages will become readily apparent to those skilled in the art upon review of the Detailed Description, Examples and Claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional representation of a trench MOS barrier Schottky rectifier according to the prior art.

FIG. 2 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 3 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 4 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 5 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 6 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 7 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 8 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIG. 9 is a cross-sectional representation of a trench Schottky rectifier according to an embodiment of the present invention.

FIGS 10A-10D are cross sectional views illustrating a method of forming the trench Schottky rectifier of FIG. 2, according to an embodiment of the invention.

FIGS 11A-11D are cross sectional views illustrating a method of forming the trench Schottky rectifier of FIG. 3, according to an embodiment of the invention.

FIGS 12A-12C are cross sectional views illustrating a method of forming the trench Schottky rectifier of FIG. 6, according to an embodiment of the invention.

DETAILED DESCRIPTION OF CERTAIN PREFERRED EMBODIMENTS OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

Referring now to FIG. 2, a cross-sectional illustration of a Schottky barrier rectifier according to the present invention is shown. The rectifier 10 includes a semiconductor region 12 of first conductivity type, typically N-type conductivity, having a first face 12a and second opposing faces 12b. The substrate semiconductor region 12 preferably comprises a relatively highly doped cathode region 12c (shown as N⁺) adjacent first face 12a. As illustrated, the cathode region 12c is doped to a first conductivity type dopant concentration of about $5 \times 10^{19}/\text{cm}^3$. A drift region 12d of first conductivity type (shown as N) preferably extends from the cathode region 12c to second faces 12b. As illustrated, the drift region 12d is doped to a first conductivity type dopant concentration of about $3.3 \times 10^{16}/\text{cm}^3$ for a 30 Volt device. Drift region 12d and cathode region 12c form a non-rectifying N⁺/N junction.

Mesas 14 having cross-sectional width "W_m" are formed in the drift region 12d. Mesas are defined by opposing trenches. Insulating regions 16 (in this case, shown as thermally grown oxide layers) are formed within the trenches and are adjacent the semiconductor region 12 along lower portions 14b of the semiconductor/trench interfaces. Insulating regions 16 typically have a thickness

on the order of about 700 to 2000 Angstroms. W_m is typically on the order of 1 micron. Trench depth "d" is typically on the order of 3 microns.

Mesas 14 extend in a third dimension (not shown) and can be of stripe, rectangular, cylindrical or other similar geometry. Hence, as will be understood by those skilled in the art, mesas 14 can be formed in the semiconductor region 12 using numerous trench configurations.

For example, mesa 14 can be formed between pairs of adjacent linear trenches that extend in a third dimension. As another example, an annular-shaped trench can form mesa 14. For both of these examples, when viewed in transverse cross section, the trenches will appear as shown in FIG. 2.

Anode electrode 18 is found immediately adjacent to the drain region 12d along faces 12b and along upper portions 14a of the semiconductor/trench interfaces. Anode electrode 18 is also found immediately adjacent to the insulating regions 16. Anode electrode 18 forms a Schottky barrier rectifying junction where it contacts the semiconductor drain region 12d, i.e., along upper portions 14a and second faces 12b.

Finally, a cathode electrode (not shown) is provided adjacent the cathode region 12c at the first face 12a. The cathode electrode preferably ohmically contacts the cathode region 12c.

Such a rectifier provides low forward-biased voltage drop, low reverse-biased leakage current and high breakdown voltage. Without wishing to be held to any particular theory of operation, it is believed that this design provides improved forward voltage drop by increasing the surface area of the Schottky rectifying contact between the anode electrode 18 and the drift region 12d by extending the contact area beyond second face 12b and into the upper portions 14a. At the same time, the insulating region 16 adjacent lower portions 14b, causes charge coupling to occur between the anode electrode 18 and mesa 14, favorably affecting the voltage profiles within the mesa structure and providing high reverse bias breakdown voltages and low leakage currents. It is well within the skill of those in the art to optimize the amount of trench depth d associated with upper portions 14a and the amount of trench depth d associated with lower portions 14b. Typically, a

trench depth of about 3 microns is used, of which about 2 microns is in contact with the anode electrode.

Another embodiment of the present invention is provided in FIG. 3. This embodiment is similar to that of FIG. 2, except that a polysilicon conductive region 19 is provided over the insulating region 16 in the trenches between mesas 14.

Other embodiments of the present invention are shown in FIGS. 4 and 5. These embodiments are similar to those of FIGS. 2 and 3, respectively, except that the trenches extend beyond drift regions 12d and into cathode region 12c.

Still other embodiments of the present invention are illustrated in FIGS. 6 and 7. These embodiments are similar to those of FIGS 2 and 4, respectively, except that the insulating regions 16 in these figures comprise deposited oxide layers, rather than thermally grown layers.

Other embodiments of the present invention are shown in Figures 8 and 9. In Figure 8, the Schottky rectifying characteristics of the contact between the anode electrode and the drift region 12d are improved by using a multi-layer anode electrode, which comprises a titanium layer 18a, a titanium-tungsten layer 18b and a tungsten layer 18c. In this specific example, the titanium-tungsten layer 18b comprises 50% titanium and 50% tungsten. Further improvements in forward biased voltage drop are made by forming N⁺ regions 12e within the device (see Figure 9). In this specific example, the doping concentration of the N⁺ regions is $1 \times 10^{19}/\text{cm}^3$. FIGS. 10A-10D illustrate an embodiment of the present invention for providing the trench Schottky rectifier 10 shown in FIG. 2.

Referring now to these figures, an N-doped epitaxial layer (corresponding to drift region 12d) is grown on a conventionally N⁺ doped substrate (corresponding to cathode region 12c). Epitaxial layer 12d is typically about 7 microns thick. Next, a photoresist masking process is used to form mask portions (not shown), which define the location of trenches 21. Trenches 21 are preferably dry etched through openings between mask portions by reactive ion etching, typically to a depth of about 3 microns. Mask portions are removed and an oxide layer 16 is formed over the surface of the entire structure by thermal oxidation. Thicknesses in the vicinity of about 700 to 2000 Angstroms are typical for thermal oxide layer 16.

Subsequently, the surface is covered with photoresist, which is partially stripped, for example, by reactive ion etching, until only photoresist portions 23 at the bottoms of trenches 21 remain, covering only a portion of oxide layer 16 as shown in FIG. 10A.

Next, oxide layer 16 is etched, for example, by wet etch, to provide oxide regions 16 as shown in FIG. 10B. In this way, surfaces 12b and upper portions 14a are exposed, while lower portions 14b remain covered with oxide.

Photoresist 23 is then completely removed, for example, by reactive ion etching, to provide the structure of FIG. 10C.

Finally, anode electrode 18 is provided to complete the structure of FIG. 10D. For example, the anode electrode can be obtained by providing (a) a Ti:W layer, followed by (b) a Pt:Si layer, followed by (c) an Al layer. As another example, the anode electrode can be obtained by providing (a) a Ti:N layer, followed by (b) a Pt:Si layer, followed by (c) an Al layer.

Yet another example of the anode electrode 18 structure is found in Figure 8 (see discussion above). In this example, the anode electrode is obtained by providing (a) Ti layer, followed by (b) a Ti:W layer, followed by (c) a W layer.

In the event that a structure like that of Figure 9 is to be fabricated, the above steps can be followed except that, after growing the epitaxial layer 12d, an N⁺ layer 12e is formed in the upper portion of epitaxial layer 12d, for example, by ion implantation and diffusion.

FIGS 11A-D illustrate an embodiment of the invention for forming the trench Schottky rectifier of FIG. 3. The steps for FIG. 11A are the same as for FIG. 10A up to the point after which the oxide layer 16 is thermally grown. Then, the device is covered (and the trenches are filled) with polysilicon layer 19, i.e., polycrystalline silicon, using techniques known in the art, such as CVD, to provide the structure shown in Fig. 11A. Polysilicon layer 19 is typically doped N-type to reduce its resistivity. N-type doping can be carried out, for example, during CVD with phosphorous chloride or by implantation with arsenic or phosphorous.

Polysilicon layer 19 is then isotropically etched, for example, by reactive ion etching, to expose the portions of oxide layer 16 over surfaces 12b and upper

portions 14a as shown in FIG 11B. Oxide layer 16 over lower portions 14b remains covered with polysilicon 19.

The exposed oxide layer is then preferentially etched, for example, by wet etch, leaving only portions of oxide layer 16 that are protected by polysilicon region 19, in this case, those portions of oxide layer 16 that are adjacent lower portions 14b as shown in FIG. 11C. Finally, anode electrode 18 is provided as discussed above to provide the structure of FIG 11D.

FIGS. 12A-C illustrate a further embodiment of the invention. The steps associated with FIG. 12A are the same as in FIG. 10A up to the point of trench formation. At this point, as seen in FIG 12A, a TEOS (tetraethylorthosilicate or $\text{Si}(\text{OC}_2\text{H}_5)_4$) layer 25 is deposited, for example, by LPCVD at temperatures between 650 and 800 °C, to provide the structure of FIG. 12A. After a dry isotropic etch back, for example, using a parallel-electrode (planar) type dry etcher, the structure of FIG. 12B is achieved. At this point, lower portions 14b are covered with TEOS layer 25, while upper portions 14a are not. The TEOS layer is subsequently densified to provide a high-density silicon dioxide layer 16. An anode electrode 18 is provided as discussed above, resulting in the structure of FIG 12C.

The present invention thus provides a trench Schottky rectifier and methods of making the same. The rectifier has an anode electrode in Schottky rectifying contact with the semiconductor drain region along upper portions of the semiconductor/trench interfaces, while the drain region is separated from the rectifier anode along lower portions of the semiconductor/trench interfaces by an insulating region. The rectifier provides low forward-biased voltage drop, low reverse-biased leakage current and high breakdown voltage. Although the present invention has been described with respect to several exemplary embodiments, there are many other variations of the above-described embodiments that will be apparent to those skilled in the art. It is understood that these variations are within the teaching of the present invention, which is to be limited only by the claims appended hereto.

CLAIMS

1. A Schottky rectifier, comprising:

a semiconductor region having first and second opposing faces, said semiconductor region comprising a cathode region of first conductivity type adjacent the first face and a drift region of said first conductivity type adjacent the second face, said drift region having a lower net doping concentration than that of said cathode region;

one or more trenches extending from said second face into said semiconductor region and defining one or more mesas within said semiconductor region;

an insulating region adjacent said semiconductor region in lower portions of said trench ;

and an anode electrode that is (a) adjacent to and forms a Schottky rectifying contact with said semiconductor region at said second face, (b) adjacent to and forms a Schottky rectifying contact with said semiconductor region in upper portions of said trench and (3) adjacent to said insulating region in said lower portions of said trench.

2. The Schottky rectifier of claim 1, wherein said semiconductor is silicon.

3. The Schottky rectifier of claim 1, wherein said first conductivity type is n-type conductivity.

4. The Schottky rectifier of claim 1, wherein said trench extends into said cathode region.

5. The Schottky rectifier of claim 4, wherein said lower portions of said trench extend between said cathode region and said drift region.

6. The Schottky rectifier of claim 1, wherein said insulating region comprises silicon dioxide.

7. The Schottky rectifier of claim 6, wherein said silicon dioxide is deposited silicon dioxide.
8. The Schottky rectifier of claim 6, wherein said silicon dioxide is thermally grown from said semiconductor region.
9. The Schottky rectifier of claim 1, wherein a polysilicon region is disposed on said insulating region and forms part of said anode electrode.
10. A method of forming a trench Schottky rectifier, comprising:
 - forming a semiconductor region having first and second opposing faces, said semiconductor region comprising a cathode region of first conductivity type adjacent the first face and a drift region of said first conductivity type adjacent the second face, said drift region having a lower net doping concentration than that of said cathode region;
 - forming one or more trenches extending from said second face into said semiconductor region, said trenches defining one or more mesas within said semiconductor region;
 - forming an insulating region adjacent said semiconductor region in lower portions of said trench; and
 - forming an anode electrode that is (a) adjacent to and forms a Schottky rectifying contact with said semiconductor region at said second face, (b) adjacent to and forms a Schottky rectifying contact with said semiconductor region in upper portions of said trench and (3) adjacent to said insulating region in said lower portions of said trench.
11. The method of claim 10, further comprising providing a cathode electrode on said first face of said semiconductor region.
12. The method of claim 10, wherein said step of forming said semiconductor region comprises providing a semiconductor substrate, said semiconductor substrate

corresponding to said cathode region; and growing an epitaxial semiconductor layer on said substrate, said epitaxial layer corresponding to said drift region.

13. The method of claim 10, wherein said step of forming said trenches comprises the steps of forming a patterned masking layer over the second face of the semiconductor region and etching said trenches through said masking layer.

14. The method of claim 10, wherein said trenches are formed such that they extend into said cathode region.

15. The method of claim 14, wherein said insulating region is formed such that it extends from said cathode region to said drift region.

16. The method of claim 10, wherein said step of forming said insulating region comprises providing an oxide layer over said second face and in said trenches; and etching portions of said oxide layer.

17. The method of claim 16, further comprising providing a photoresist pattern on the oxide layer, etching portions of the oxide layer not covered by said photoresist, and removing said photoresist.

18. The method of claim 17, wherein said oxide layer is thermally grown.

19. The method of claim 16, further comprising the steps of providing a polysilicon layer on said oxide layer, etching said polysilicon layer such that portions of said oxide layer over said second face and over said upper portions of said trenches are exposed; and etching said oxide layer such that said portions of said oxide layer over said second face and over said upper portions of said trenches are removed.

20. The method of claim 19, wherein said oxide layer is thermally grown.

21. The method of claim 10, wherein said step of forming said insulating region comprises depositing an oxide layer.
22. The method of claim 21, further comprising the steps of depositing a tetraethylorthosilicate layer on said second face and within said trenches; etching said tetraethylorthosilicate layer until it is removed from said second surface and said upper portions of said trenches; and converting said tetraethylorthosilicate into a high density silicon dioxide layer.
23. The Schottky rectifier of claim 1, wherein said lower portions of said trenches correspond to approximately 25 to 40% of the depth of said trenches.
24. The Schottky rectifier of claim 1, further comprising a cathode electrode provided on the first face.
25. The method of claim 10, wherein said lower portions of said trenches correspond to approximately 25 to 40% of the depth of said trenches.

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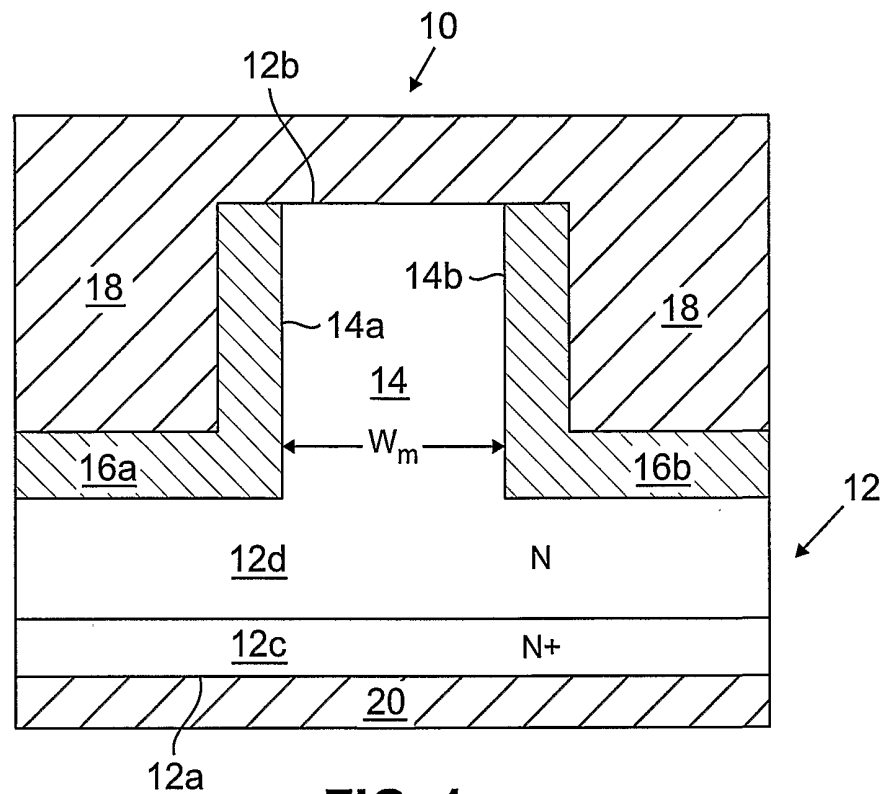


FIG. 1
(PRIOR ART)

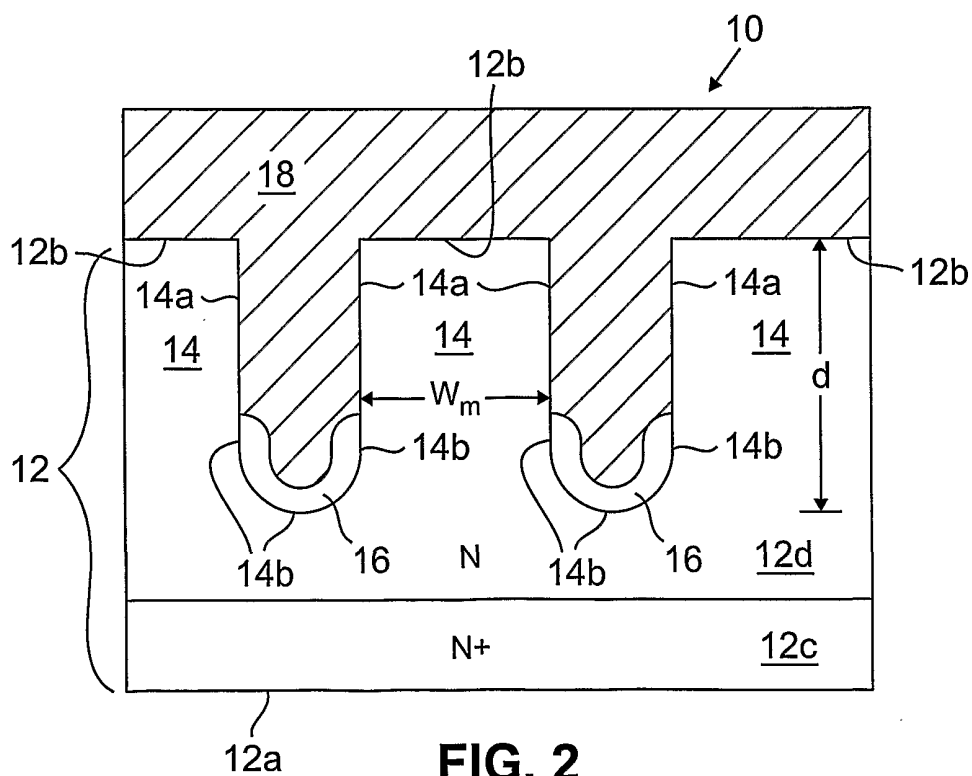


FIG. 2

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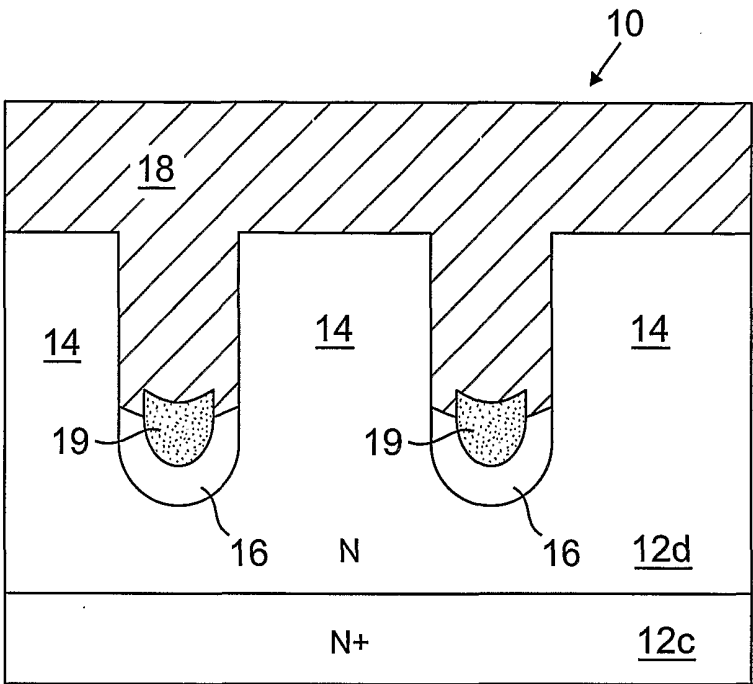


FIG. 3

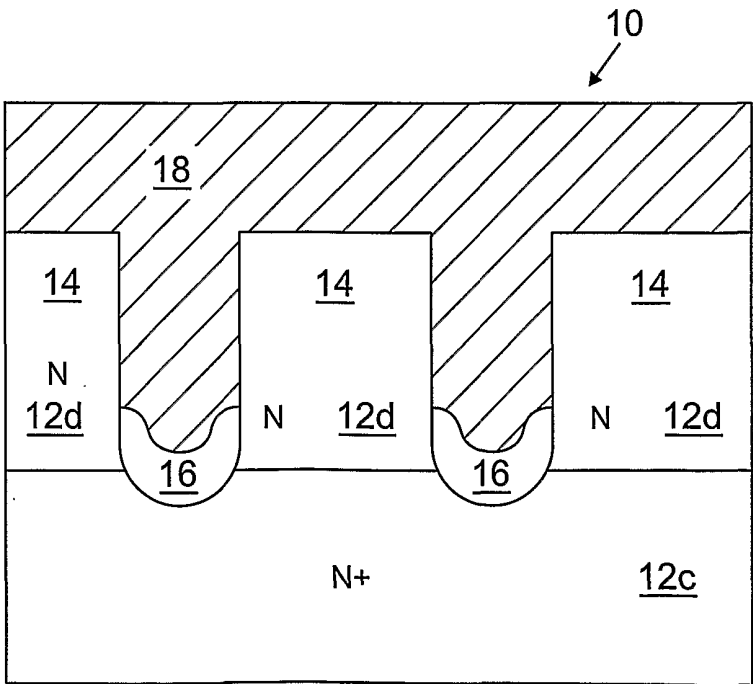


FIG. 4

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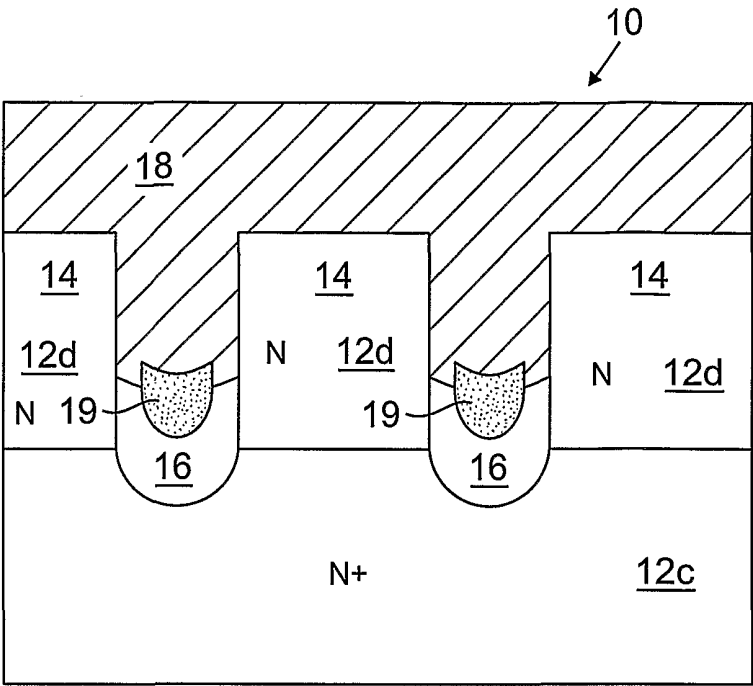


FIG. 5

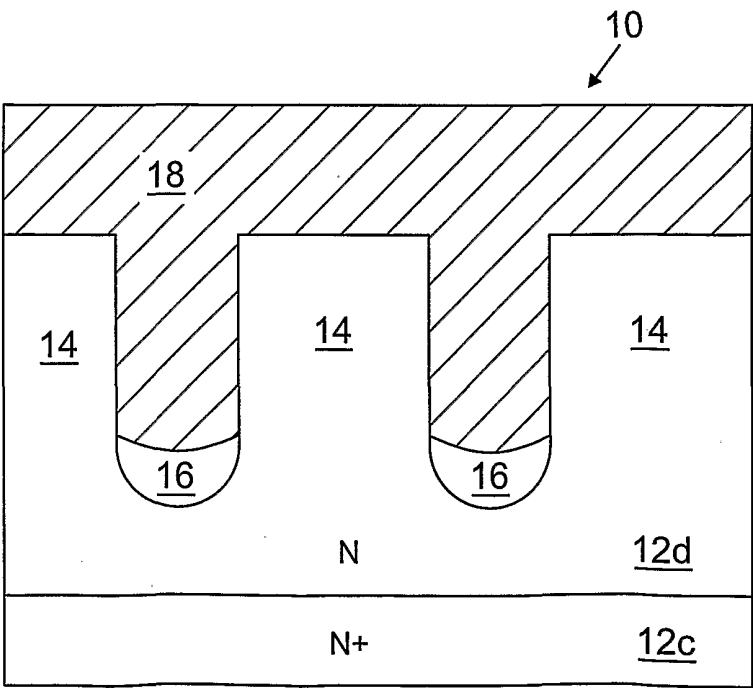


FIG. 6

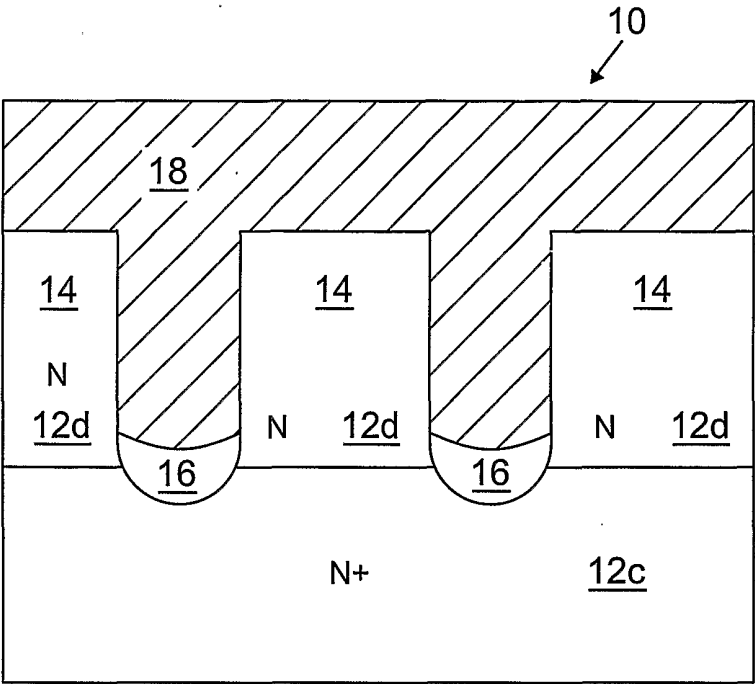


FIG. 7

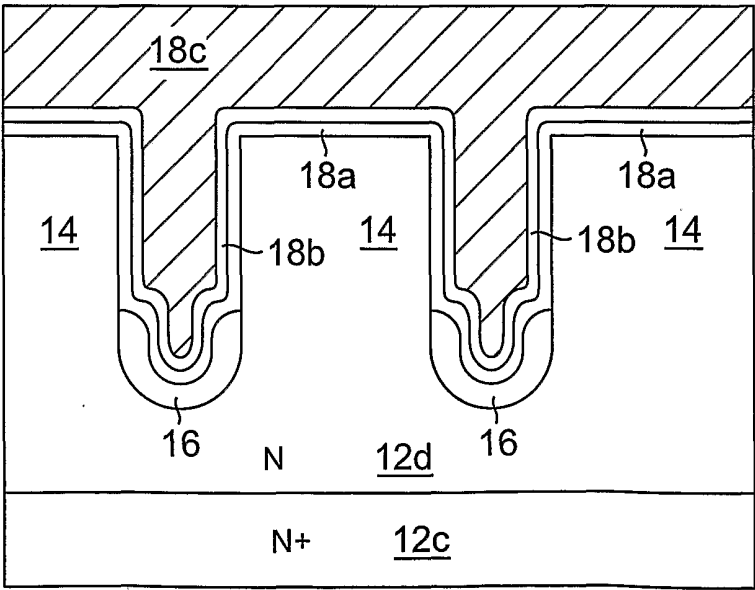


FIG. 8

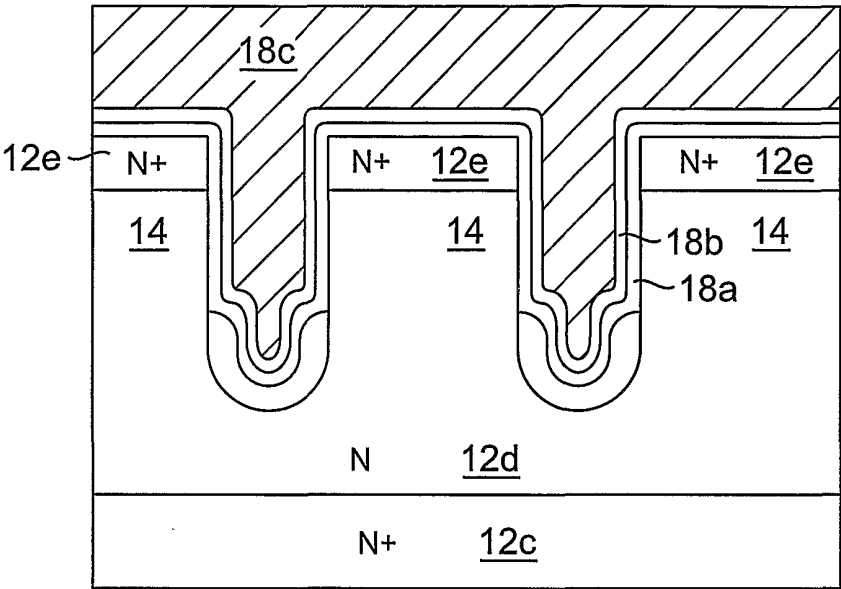


FIG. 9

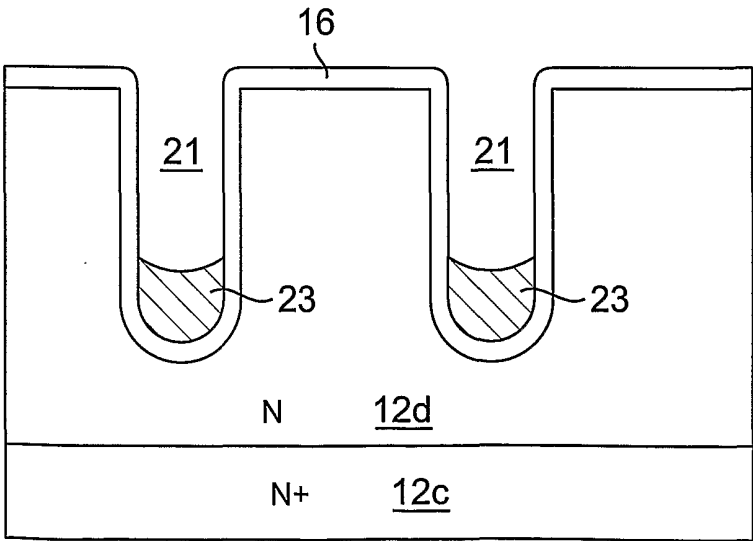


FIG. 10A

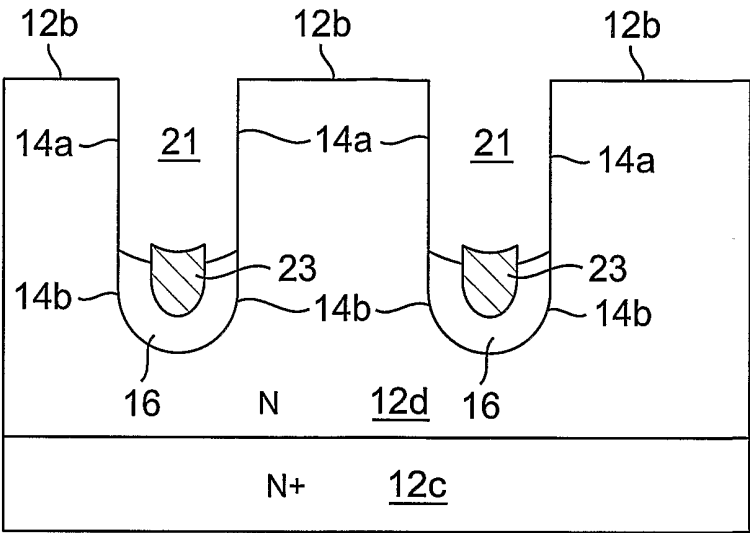


FIG. 10B

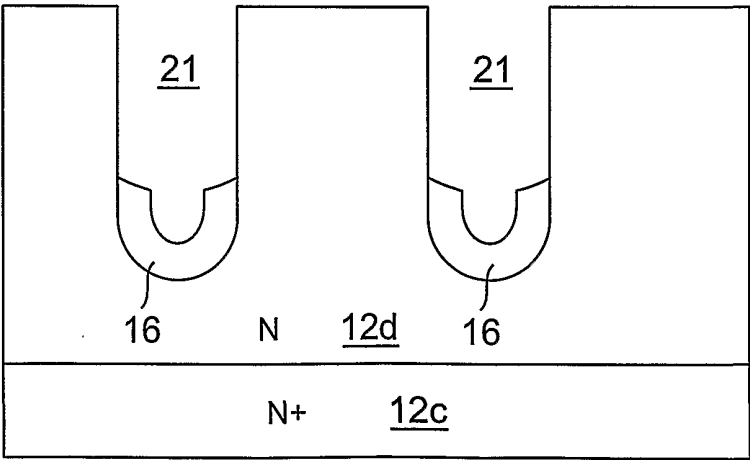


FIG. 10C

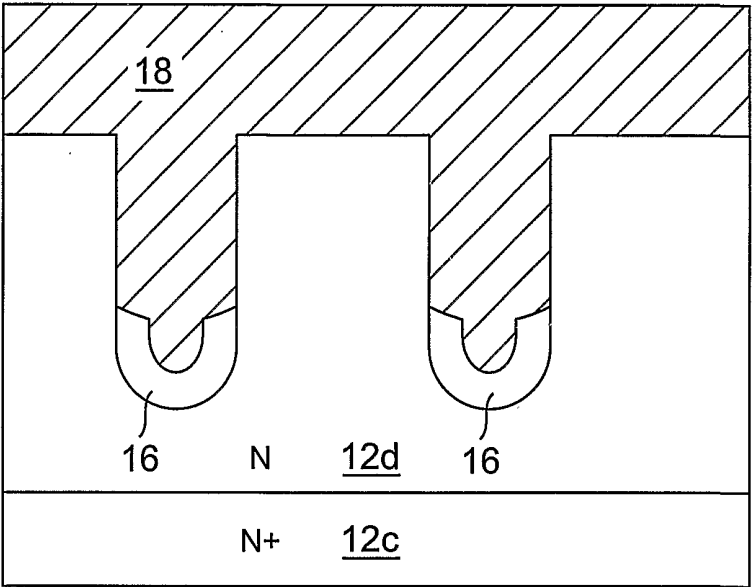


FIG. 10D

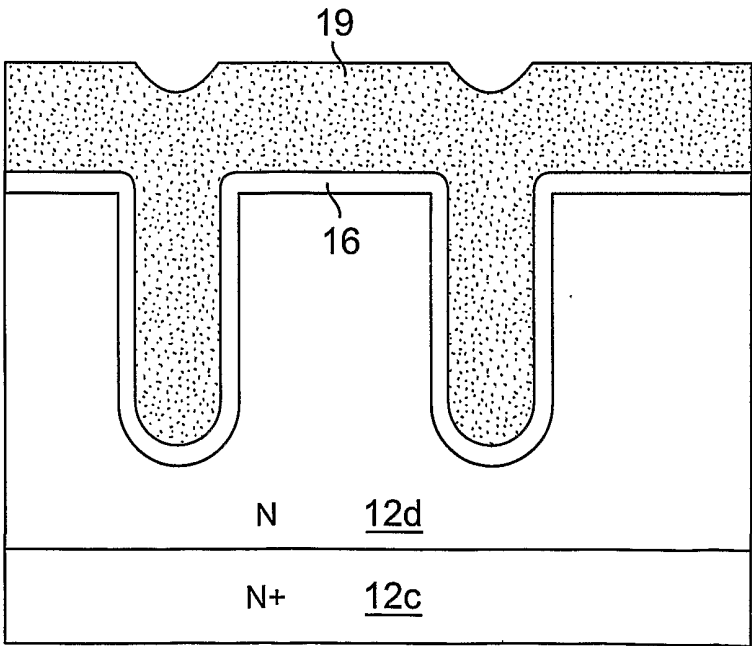


FIG. 11A

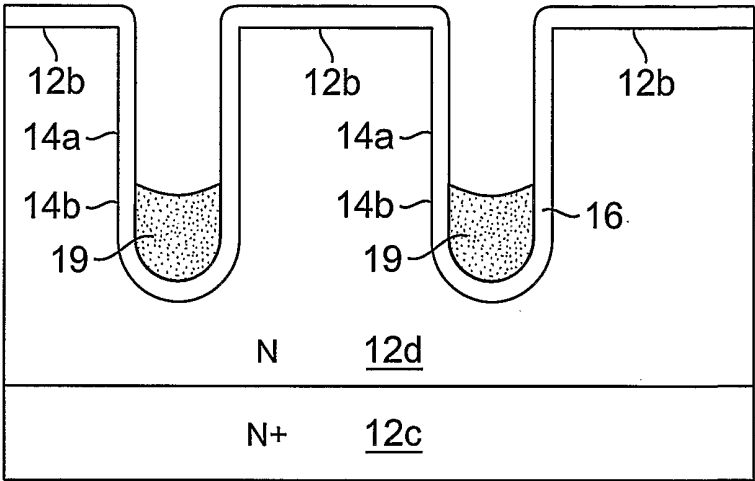


FIG. 11B

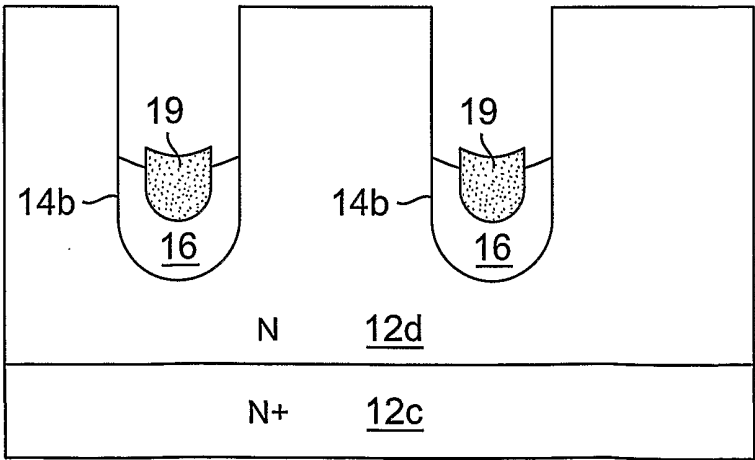


FIG. 11C

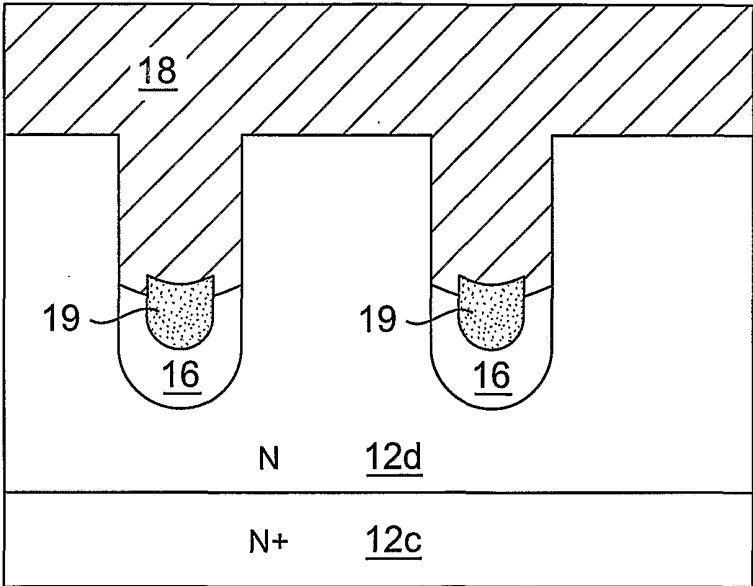


FIG. 11D

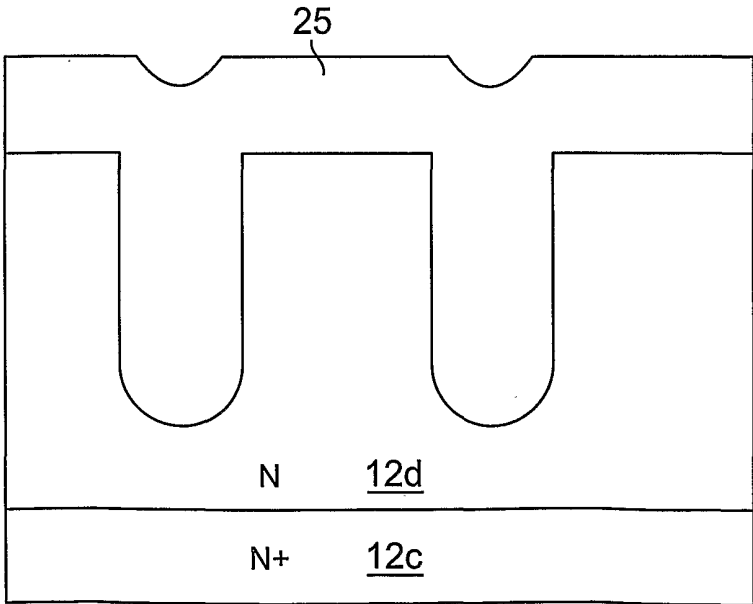


FIG. 12A

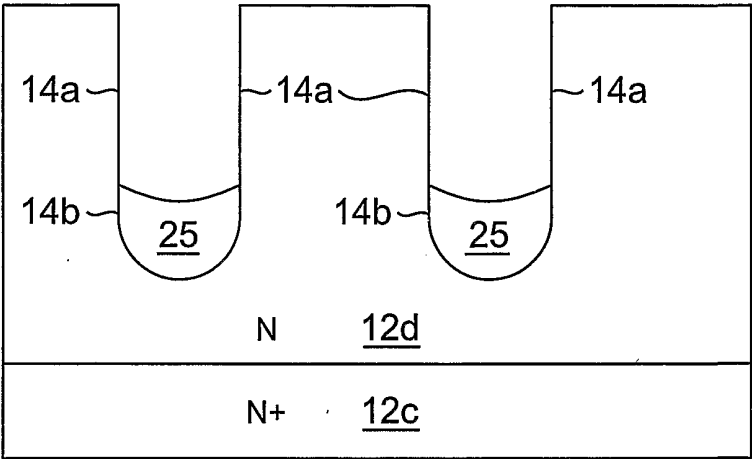


FIG. 12B

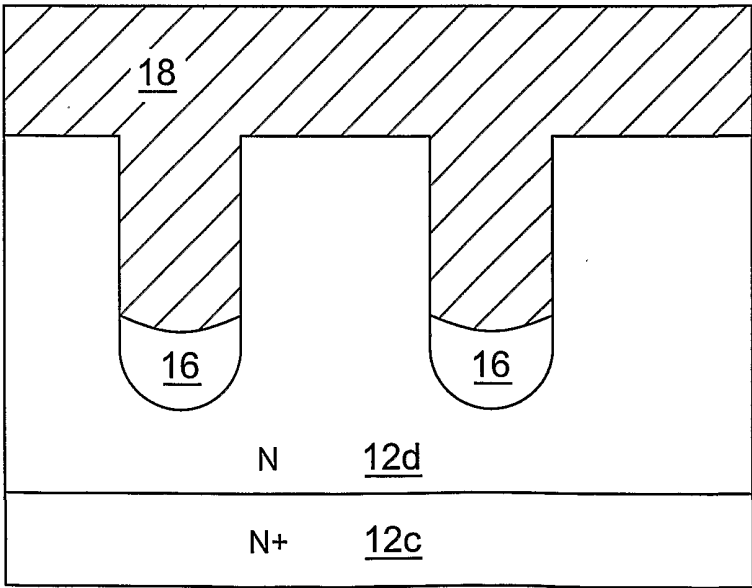


FIG. 12C