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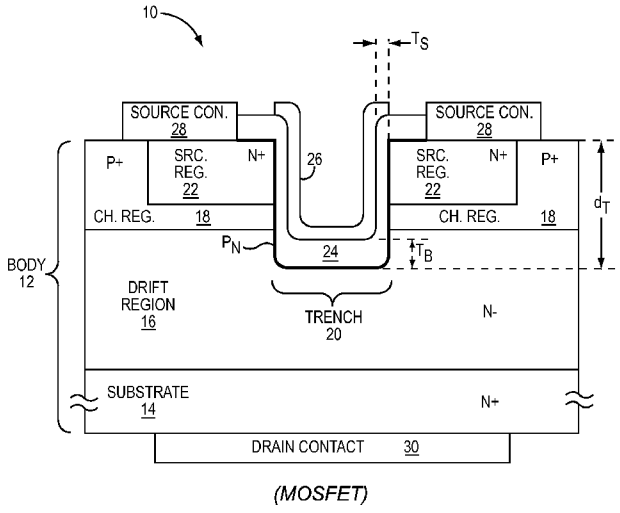
(54) Title: ENHANCED GATE DIELECTRIC FOR A FIELD EFFECT DEVICE WITH A TRENCHED GATE



(MOSFET)

FIG. 1

(57) Abstract: The present disclosure relates to a silicon carbide (SiC) field effect device that has a gate assembly formed in a trench. The gate assembly includes a gate dielectric that is an dielectric layer, which is deposited along the inside surface of the trench and a gate dielectric formed over the gate dielectric. The trench extends into the body of the device from a top surface and has a bottom and side walls that extend from the top surface of the body to the bottom of the trench. The thickness of the dielectric layer on the bottom of the trench is approximately equal to or greater than the thickness of the dielectric layer on the side walls of the trench.

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ENHANCED GATE DIELECTRIC FOR A FIELD EFFECT DEVICE WITH A TRENCHED GATE

Government Support

[0001] This invention was made with government funds under contract number W911NF-10-2-0038 awarded by the U.S. Army. The U.S. Government has rights in this invention.

Field of the Disclosure

[0002] The present disclosure relates to enhanced gate dielectrics for field effect devices.

Background

[0003] Semiconductor devices, especially those designed to block high voltages and conduct large currents in high power applications, are subjected to powerful electrical forces and electromagnetic fields at the molecular level. Further, these devices may be subjected to high temperatures during fabrication and operation. These forces, fields, and temperatures can damage the molecular structure of the various layers and regions within the device, as well as the interface between these various layers or regions. Such damage leads to device failures as well as degraded performance over time. For field effect devices employing a metallized gate that is separated from the body of the device by adielectric layer, the dielectric layer and the interface between the dielectric layer and the body are particularly vulnerable. As such, there is a need for a gate dielectric for a field effect device that is less vulnerable to the forces and fields that are generated in high voltage and current applications as well as the potentially damaging temperatures associated with fabrication and operation.

Summary

[0004] The present disclosure relates to a silicon carbide (SiC) field effect device that has a gate assembly formed in a trench. The gate assembly includes a gate dielectric that is a dielectric layer, which is deposited along the inside

surface of the trench, and a gate dielectric formed over the gate dielectric. The trench extends into the body of the device from a top surface, has a bottom, and has side walls that extend from the top surface of the body to the bottom of the trench. The thickness of the dielectric layer on the bottom of the trench is approximately equal to or greater than the thickness of the dielectric layer on the side walls of the trench. The thickness of the dielectric layer on the bottom surface may exceed that of the side walls by 25%, 50%, 100% or more. The side walls may be substantially orthogonal to the top surface or may form an angle of less than 90° with the top surface, such that the trench is generally V-shaped.

[0005] In one embodiment, a nitrogen passivation is provided at the interface between the dielectric layer and the trench due to the dielectric layer being annealed with nitric oxide (NO). The nitrogen passivation provides an excellent interface between the dielectric layer and the trench. The dielectric layer may be silicon dioxide (SiO_2), aluminum oxide (AlO_2), magnesium oxide (MgO), or the like. Alternatively, the dielectric layer may be formed from multiple layers of dielectric oxides, nitrides, or both as well as mixed alloys of similar dielectrics.

[0006] An exemplary process for forming the field effect device includes providing a field effect device precursor that includes a body and forming the trench into the top surface of the body using an etching or mechanical cutting process. Next, the dielectric layer for the gate dielectric is deposited, as opposed to thermally grown, using a deposition process, such as a chemical vapor deposition (CVD) or an evaporative process. The dielectric layer may be annealed in an oxidant, such as oxygen (O_2), nitrous oxide (N_2O), water, or the like. This annealing step is optional, but may be used to improve the insulating properties of the gate dielectric. The dielectric layer is then annealed in nitric oxide (NO) to increase the density of the dielectric layer, enhance the interface between the dielectric layer and the trench, or both. Annealing with nitric oxide (NO) allows nitrogen (N) to build up at the interface between the dielectric layer and the trench, and thus, provide the nitrogen passivation at the interface.

[0007] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following

detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0008] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0009] Figure 1 illustrates a MOSFET that has a gate structure formed according to a first embodiment of the present disclosure.

[0010] Figure 2 illustrates a MOSFET that has a gate structure formed according to a second embodiment of the present disclosure.

[0011] Figure 3 illustrates a MOSFET that has a gate structure formed according to a third embodiment of the present disclosure.

[0012] Figure 4 illustrates one process for forming the gate structure of the embodiments provided in Figures 1 through 3.

[0013] Figure 5 illustrates an IGBT that has a gate structure formed according to a first embodiment of the present disclosure.

[0014] Figure 6 illustrates an IGBT that has a gate structure formed according to a second embodiment of the present disclosure.

[0015] Figure 7 illustrates an IGBT that has a gate structure formed according to a third embodiment of the present disclosure.

Detailed Description

[0016] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0017] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0018] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0019] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0020] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used

herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0021] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0022] With reference to Figure 1, a first embodiment of a field effect device 10 is illustrated. The field effect device is a silicon carbide (SiC) metal oxide field effect transistor (MOSFET) that has a body 12, which includes a substrate 14, a drift region 16 over the substrate 14, and a channel region 18 over the drift region 16. A trench 20 extends into the body 12 from a top surface of the body 12. As illustrated, the trench 20 may extend through the channel region 18 and into the drift region 16 to a depth d_T. As such, the trench 20 divides the channel region 18. Source regions 22 are effectively formed in the channel regions 18 on either side of the trench 20.

[0023] The substrate 14 may be an N-doped, single crystal, SiC substrate 14. The substrate 14 may have various crystalline polytypes, such as 2H, 4H, 6H, 3C and the like. In other embodiments, the substrate 14 may also be formed from other material systems, such as gallium nitride (GaN), gallium arsenide (GaAs), silicon (Si), germanium (Ge), SiGe, and the like. The substrate may be heavily doped with an N-type dopant at concentrations of between about $1x10^{17}$ cm^{-3} and $1x10^{19}$ cm^{-3} and have a thickness of between about 100 microns and 600 microns; however, the doping concentrations and thicknesses of the substrate 14

and the other layers may vary based on the desired parameters of the field effect device 10.

[0024] A SiC drift region 16 may be grown over the substrate 14 and doped *in situ*, wherein the drift region 16 is lightly doped as it is grown with an N-type doping material. Notably, one or more buffer layers (not shown) may be formed on the substrate 14 prior to forming the drift region 16. The buffer layer(s) may be used as a nucleation layer and be relatively heavily doped with an N-type doping material.

[0025] The drift region 16 may be relatively uniformly doped throughout or may employ graded doping throughout all or a portion thereof. For a uniformly doped drift region 16, the doping concentration may be between about $1x10^{14}$ cm^{-3} and $1x10^{16}$ cm^{-3} in one embodiment. With graded doping, the doping concentration is highest at the bottom of the drift region 16 near the substrate 14 and lowest at the top of the drift region 16. The doping concentration generally decreases in a stepwise or continuous fashion from a point at or near the bottom to a point at or near the top of the drift region 16. In one embodiment employing graded doping, the lower portion of the drift region16 may be doped at a concentration of about $1x10^{14}$ cm^{-3} and the upper portion of the drift region 16 may be doped at a concentration of about $1x10^{16}$ cm^{-3}. The drift region 16 may be between four and ten microns thick in select embodiments depending on the desired parameters of the field effect device 10.

[0026] A SiC channel region 18 may be grown over the drift region 16 and doped *in situ*, wherein the channel region 18 is heavily doped as it is grown with a P-type doping material at concentrations between about $1x10^{17}$ cm^{-3} and $5x10^{18}$ cm^{-3}. The channel region 18 at its thickest point may be between about 1 microns and 5 microns. Prior to the trench 20 being formed, the source regions 22 are effectively created as a single source well in the channel region 18 and heavily doped with an N-type doping material.

[0027] The trench 20 is etched from the top surface of the body 12 through the central portion of the source well and the channel region 18 and into the drift region 16. As a result, a channel region 18 and a source region 22 are provided

on each side of the trench 20. Both side walls of the trench 20 are formed from portions of the source region 22, the channel regions 18, and the drift region 16. The bottom of the trench 20 resides in the drift region 16 and extends between the lower ends of the side walls of the trench 20. In the embodiment of Figure 1, the side walls of the trench 20 are substantially orthogonal to the top surface of the body 12, and the bottom of the trench 20 is substantially parallel to the top surface of the body 12. In one embodiment, the corners between the bottom and the side walls of the trench 20 are rounded to reduce electric field concentrations, which would be higher with sharper corners.

[0028] The gate assembly for the field effect device 10 is formed in the trench 20 and includes a uniquely formed dielectric layer 24 and a gate contact 26. The dielectric layer 24 is formed substantially continuously along the side walls and bottom of the trench 20. The gate contact 26 is formed on the dielectric layer 24. The dielectric layer 24 may be an oxide, such as silicon dioxide (SiO_2), aluminum oxide (AlO_2), magnesium oxide (MgO). Alternatively, the dielectric layer 24 may be formed from multiple layers of dielectric oxides, nitrides, or both as well as mixed alloys of similar dielectrics. For the following example, the dielectric layer 24 is an oxide. The gate contact 26 is generally relatively thick and formed from a highly doped semiconductor such as Si or Ge, or a metal, such as aluminum (Al), gold (Au), Silver (Ag), and the like.

[0029] Unlike other SiC-based field effect devices with a gate assembly formed in a trench, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is approximately equal to or greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. For example, the thickness of the dielectric layer 24 on the bottom surface may exceed that of the side walls by 25% or more, 50% or more, or even 100% or more. As illustrated, the bottom of the trench 20 is approximately 100%, or two times, greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20.

[0030] In conventional SiC field effect devices, the dielectric layer is grown using a thermal growth process. With a thermal growth process where the trench

is etched into the Si-face (0001) SiC, the growth rate of the oxide on the bottom (Si-face (0001)) of the trench is around three times slower than that on the side walls, which may reside in the a-face {11-20} and m-face {10-10} family of planes. As a result, the thickness of the dielectric layer on the side walls is much thicker than the dielectric layer on the bottom of the trench. The thicker dielectric layer on the side walls leads to higher electric fields along the portion of the dielectric layer that is formed on the bottom of the trench than along the portions of the dielectric layer that are formed on the side walls of the trench. The higher electric fields along the portion of the dielectric layer along the bottom of the trench leads to device failure, and thus, reduces the long-term reliability of the field effect device.

[0031] To improve reliability, the present disclosure provides for the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 to be approximately equal to or greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. As illustrated in the embodiment of Figure 1, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is substantially greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. A unique process for forming the dielectric layer 24 in this manner is provided further below.

[0032] With continued reference to Figure 1, the MOSFET embodiment of the field effect device 10 includes source contacts 28 on the respective source regions 22 and one or more drain contacts 30 on the bottom surface of the substrate 14. Like the gate contact 26, the source and drain contacts 28, 30 may be formed from aluminum (Al), gold (Au), Silver (Ag), and the like.

[0033] In the embodiment of Figure 1, the width of the trench 20 and the thicknesses of the dielectric layer 24 and the metal for the gate contact 26 on the side walls is such that the gate contact 26 is U-shaped. As such, an open trench is formed by the gate contact 26. Other materials may fill the open trench during subsequent processing steps.

[0034] Figure 2 provides an alternative embodiment wherein the metal for the gate contact 26 completely, or at least substantially, fills any trench left over after

the dielectric layer 24 has been deposited on the bottom and side walls of the trench 20. Figure 2 also illustrates an embodiment wherein the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is approximately equal to the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20.

[0035] With reference to Figure 3, an embodiment is illustrated wherein the side walls of the trench 20 form an angle α of less than 90° with the top surface, such that the trench is generally V-shaped. As such, the side walls of the trench 20 do not need to be orthogonal to the top surface of the body 12. In the illustrated embodiment, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is approximately 100%, or two times, greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. For example, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 may be between 80 and 100 nanometers (nm) while the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20 may be between 40 and 50 nm.

[0036] While keeping within the confines of the bottom thickness T_B being substantially equal to or greater than the side thickness T_S, the bottom thickness T_B may range between 20 and 200 nm or more, and the side thickness T_S may range between 10 and 50 nm, 5 and 100 nm, and 25 and 75 nm, depending on the desired performance parameters. These measurements are solely for purposes of illustration and are not intended to limit the scope of this disclosure or the claims that follow.

[0037] With reference to the flow diagram of Figure 4, an exemplary process is provided for forming the dielectric layer 24 such that the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is approximately equal to or greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. The process is performed on a field effect device precursor that includes the body 12 without the trench 20 being etched. Initially, the trench 20 is formed into the top surface of the body 12 wherein the top surface corresponds to the Si-face (0001) SiC (step 100). The trench 20 may be formed using

standard etching processes, or perhaps a mechanical cutting process. The trench 20 will pass through the source regions 22 and the channel regions 18 into the drift region 16.

[0038] Once the trench 20 is formed, the dielectric layer is deposited using a deposition process until the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 and the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20 reach desired levels (step 102). By using a deposition process, such as a CVD or evaporative process, as opposed to a thermal growth process, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 and the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20 are more readily controlled. Unlike a thermal growth process, a deposition process allows the dielectric layer 24 to form such that the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 is approximately equal to or greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. If a thermal growth process were used to form the dielectric layer 24 in the trench 20 of a SiC-based body 12, the bottom thickness T_B of the dielectric layer 24 on the bottom of the trench 20 would undesirably end up much less than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 20. Depending on the embodiment, the dielectric layer 24 may be silicon dioxide (SiO_2), aluminum oxide (AlO_2), magnesium oxide (MgO); or it may be formed from multiple layers of dielectric oxides or nitrides, from mixed alloys of similar dielectrics, or the like. A silicon dioxide (SiO_2) dielectric layer 24 is an effective match with SiC-based applications.

[0039] After the dielectric layer 24 is deposited, the dielectric layer may be annealed in an oxidant, such as oxygen (O_2), nitrous oxide (N_2O), water, or the like (step 104). The annealing may take place at a relatively high temperature, such as between 1100 and 1300 Celsius (C) and last for 0.1 to 10 hours. This annealing step is optional in this exemplary process, but may be used to improve the insulating properties of the dielectric layer 24.

[0040] Next, the dielectric layer 24 is annealed in nitric oxide (NO) (step 106). This step of annealing in nitric oxide (NO) has been found to increase the density

of the dielectric layer 24 and enhance the molecular interface between the dielectric layer 24 and the trench 20. Annealing with nitric oxide (NO) allows nitrogen (N) to build up at the interface between the dielectric layer 24 and the trench 20, and thus, provides nitrogen passivation PN (see Figures 1-3, 5, and 6) at the interface. The annealing may take place at a relatively high temperature, such as between 1100 and 1300 Celsius (C) and last for 0.5 to 5 hours.

[0041] Finally, the gate contact 26 may be formed over the annealed dielectric layer 24 (step 108). The gate contact 26 may be formed in conjunction with forming the source contacts 28.

[0042] With reference to Figure 5, a second embodiment of a field effect device 10′ is illustrated. The field effect device 10′ is a SiC insulated gate bipolar transistor (IGBT), which has a body 32 that is configured similarly to the MOSFET described above. The gate assembly is formed in the same manner as that described above. The body 32 of the IGBT includes a substrate 34, a drift region 36 over the substrate 34, and a channel region 38 over the drift region 36. A trench 40 extends into the body 32 from a top surface of the body 32. As described above, the trench 40 may extend through the channel region 38 and into the drift region 36 to a depth d_T. As such, the trench 40 divides the channel region 38. Emitter regions 42 are effectively formed in the channel regions 38 on either side of the trench 40.

[0043] In contrast with the MOSFET, the substrate 34 may be a P-doped, single crystal, SiC substrate 34. The substrate 34 may be heavily doped with a P-type dopant at concentrations of between about $1x10^{16}$ cm^{-3} and $1x10^{19}$ cm^{-3} and have a thickness of between about 2 microns and 500 microns; however, the doping concentrations and thicknesses of the substrate 34 and the other layers may vary based on the desired parameters of the IGBT variant of the field effect device 10′.

[0044] A SiC drift region 36 may be grown over the substrate 34 and doped *in situ*, wherein the drift region 36 is lightly doped as it is grown with an N-type doping material. Notably, one or more buffer layers (not shown) may be formed on the substrate 34 prior to forming the drift region 36. The buffer layer(s) may

be used as a nucleation layer and be relatively heavily doped with an N-type doping material.

[0045] The drift region 36 may be relatively uniformly doped throughout or may employ graded doping throughout all or a portion thereof. For a uniformly doped drift region 36, the doping concentration may be between about $1x10^{14}$ cm^{-3} and $1x10^{16}$ cm^{-3} in one embodiment. With graded doping, the doping concentration is highest at the bottom of the drift region 36 near the substrate 34 and lowest at the top of the drift region 36. The doping concentration generally decreases in a stepwise or continuous fashion from a point at or near the bottom to a point at or near the top of the drift region 36.

[0046] A SiC channel region 38 may be grown over the drift region 36 and doped *in situ*, wherein the channel region 38 is heavily doped as it is grown with a P-type doping material at concentrations between about $1x10^{17}$ cm^{-3} and $5x10^{18}$ cm^{-3}. Prior to a trench 40 being formed, the emitter regions 42 are effectively created as a single emitter well in the channel region 38 and heavily doped with an N-type doping material.

[0047] The trench 40 is etched from the top surface of the body 32 through the central portion of the emitter well and the channel region 38 and into the drift region 36. As a result, a channel region 38 and an emitter region 42 are provided on each side of the trench 40. Both side walls of the trench 40 are formed from portions of the emitter region 42, the channel regions 38, and the drift region 36. One or more collector contacts 50 are provided on the bottom surface of the substrate 34.

[0048] The bottom of the trench 40 resides in the drift region 36 and extends between the lower ends of the side walls of the trench 40. In the embodiment of Figure 5, the side walls of the trench 40 are substantially orthogonal to the top surface of the body 32, and the bottom of the trench 40 is substantially parallel to the top surface of the body 32. As noted above, the corners between the bottom and the side walls of the trench 40 are rounded to reduce electric field concentrations, which would be higher with sharper corners.

[0049] As with the MOSFET embodiment, the gate assembly for the IGBT is formed in the trench 40 and includes a uniquely formed dielectric layer 44 and a gate contact 46. The dielectric layer 44 is formed substantially continuously along the side walls and bottom of the trench 40. The gate contact 46 is formed on the dielectric layer 44. As noted above, the bottom thickness T_B of the dielectric layer 44 on the bottom of the trench 40 is approximately equal to or greater than the side thickness T_S of the dielectric layer 24 on the side walls of the trench 40.

[0050] Figure 6 provides an alternative embodiment wherein the metal for the gate contact 46 completely, or at least substantially, fills any trench left over after the dielectric layer 44 has been deposited on the bottom and side walls of the trench 40. Figure 6 also illustrates an embodiment wherein the bottom thickness T_B of the dielectric layer 44 on the bottom of the trench 40 is approximately equal to the side thickness T_S of the dielectric layer 44 on the side walls of the trench 40. As another variant that is illustrated in Figure 7, the trench 40 may be created such that the side walls of the trench 40 form an angle α of less than 90° with the top surface, such that the trench is generally V-shaped.

[0051] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A field effect device comprising:
   - a body having a top surface and a trench extending into the body from the top surface wherein the trench has a bottom and a plurality of side walls;
   - a deposited dielectric layer formed substantially along an inside surface of the trench such that a thickness of the deposited dielectric layer on the bottom of the trench is substantially equal to or greater than a thickness of the deposited dielectric layer on the plurality of side walls of the trench; and
   - a gate contact formed over the deposited dielectric layer wherein the deposited dielectric layer and the gate contact form a gate assembly for the field effect device and the body comprises silicon carbide.

2. The field effect device of claim 1 wherein the deposited dielectric layer is a nitric oxide annealed deposited dielectric layer.

3. The field effect device of claim 1 wherein a nitrogen passivation is provided at an interface between the deposited dielectric layer and the inside surface of the trench.

4. The field effect device of claim 1 wherein the deposited dielectric layer is silicon dioxide.

5. The field effect device of claim 1 wherein the deposited dielectric layer is silicon dioxide, the deposited dielectric layer is a nitric oxide annealed deposited dielectric layer, and a nitrogen passivation is provided at an interface between the deposited dielectric layer and the inside surface of the trench.

6. The field effect device of claim 5 wherein the thickness of the deposited dielectric layer on the bottom of the trench is substantially greater than the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

7. The field effect device of claim 1 wherein the body comprises a substrate, a drift region over the substrate, and channel regions on either side of the trench.

8. The field effect device of claim 7 wherein the trench extends into the drift region.

9. The field effect device of claim 8 wherein at least one of source or emitter contacts are provided over the top surface on either side of the trench and at least one of a drain or collector contact is provided over a bottom surface of the substrate.

10. The field effect device of claim 1 wherein the thickness of the deposited dielectric layer on the bottom of the trench is substantially equal to the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

11. The field effect device of claim 1 wherein the thickness of the deposited dielectric layer on the bottom of the trench is greater than the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

12. The field effect device of claim 1 wherein the thickness of the deposited dielectric layer on the bottom of the trench is at least 25% greater than the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

13. The field effect device of claim 1 wherein the thickness of the deposited dielectric layer on the bottom of the trench is at least 50% greater than the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

14. The field effect device of claim 1 wherein the thickness of the deposited dielectric layer on the bottom of the trench is at least 100% greater than the thickness of the deposited dielectric layer on the plurality of side walls of the trench.

15. The field effect device of claim 1 wherein the field effect device is a metal oxide semiconductor field effect device.

16. The field effect device of claim 1 wherein the field effect device is an insulated gate bipolar transistor.

17. The field effect device of claim 1 wherein the plurality of side walls are substantially perpendicular to the top surface.

18. The field effect device of claim 1 wherein the bottom is substantially parallel with the top surface.

19. The field effect device of claim 1 wherein the trench is generally V-shaped.

20. A method for fabricating a field effect device comprising:

- providing a body having a top surface;
- forming a trench extending into the body from the top surface wherein the trench has a bottom and a plurality of side walls;
- depositing an dielectric layer substantially along an inside surface of the trench;
- annealing the dielectric layer in nitric oxide; and

- forming a gate contact over the dielectric layer wherein the dielectric layer and the gate contact form a gate assembly for the field effect device and the body comprises silicon carbide.

21. The method of claim 20 wherein the dielectric layer is deposited such that a thickness of the dielectric layer on the bottom of the trench is substantially equal to or greater than a thickness of the dielectric layer on the plurality of side walls of the trench.

22. The method of claim 20 wherein the dielectric layer is deposited such that a thickness of the dielectric layer on the bottom of the trench is substantially greater than a thickness of the dielectric layer on the plurality of side walls of the trench.

23. The method of claim 20 wherein the dielectric layer is deposited such that a thickness of the dielectric layer on the bottom of the trench is substantially equal to a thickness of the dielectric layer on the plurality of side walls of the trench.

24. The method of claim 20 further comprising annealing the dielectric layer in an oxidant prior to annealing the dielectric layer in the nitric oxide.

25. The method of claim 20 wherein the annealing with the nitric oxide results in nitrogen passivation at an interface between the dielectric layer and the inside surface of the trench.

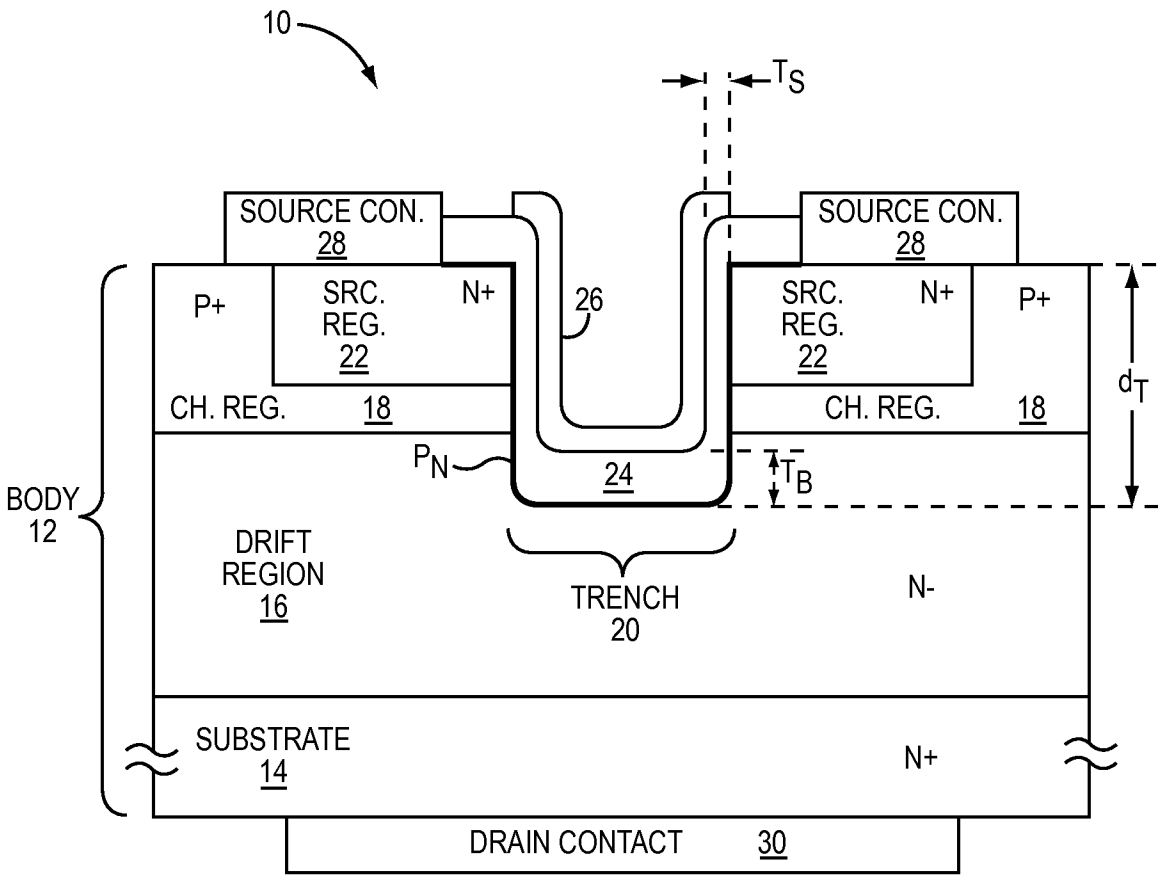
26. The method of claim 20 wherein the dielectric layer is silicon dioxide.

27. The method of claim 20 wherein the dielectric layer is silicon dioxide and nitrogen passivation is provided at an interface between the dielectric layer and the inside surface of the trench.

28. The method of claim 20 wherein the body comprises a substrate, a drift region over the substrate, and channel regions on either side of the trench.

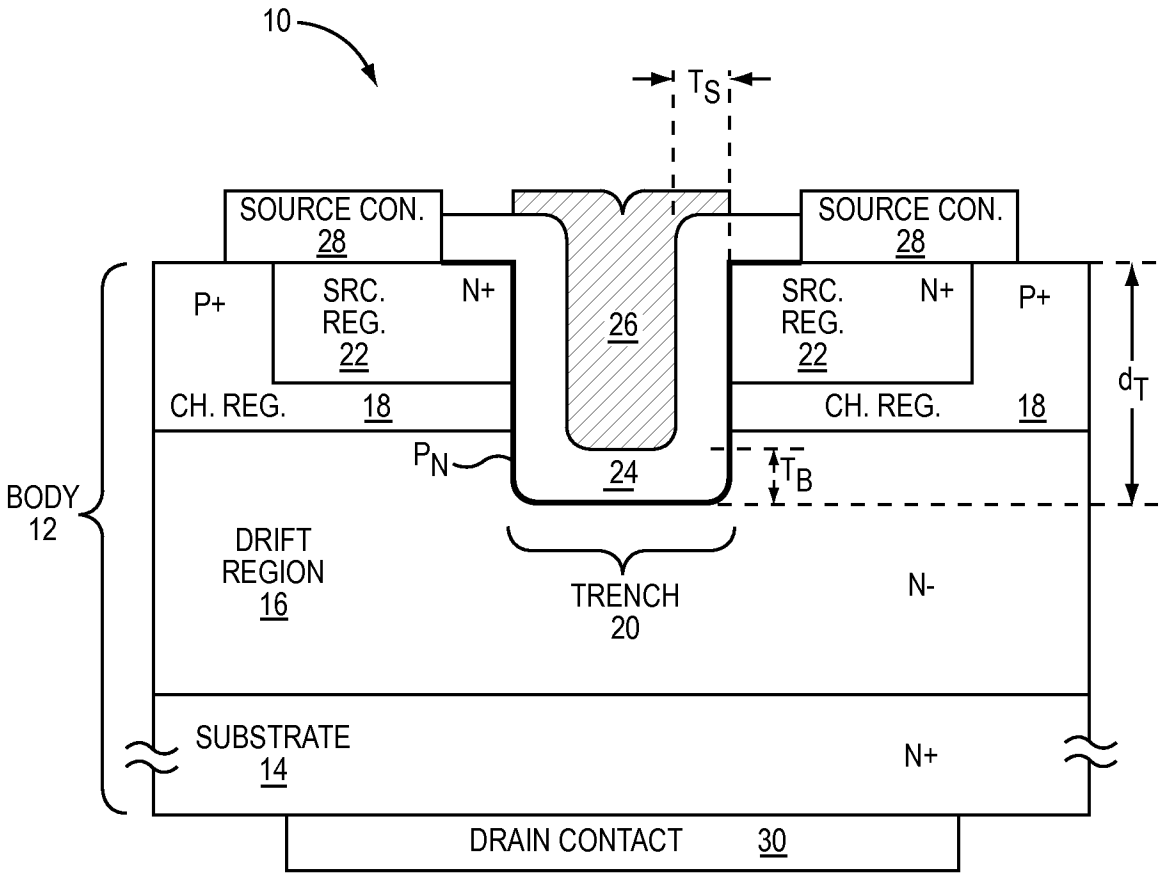
29. The method of claim 28 wherein the trench extends into the drift region.

30. The method of claim 29 wherein at least one of source or emitter contacts are provided over the top surface on either side of the trench and at least one of a drain or collector contact is provided over a bottom surface of the substrate.


10
T_S
SOURCE CON.
28
SOURCE CON.
28
P+
SRC.
REG.
22
N+
26
SRC.
REG.
22
N+
P+
d_T
CH. REG.
18
CH. REG.
18
P_N
24
T_B
BODY
12
DRIFT
REGION
16
TRENCH
20
N-
SUBSTRATE
14
N+
DRAIN CONTACT
30

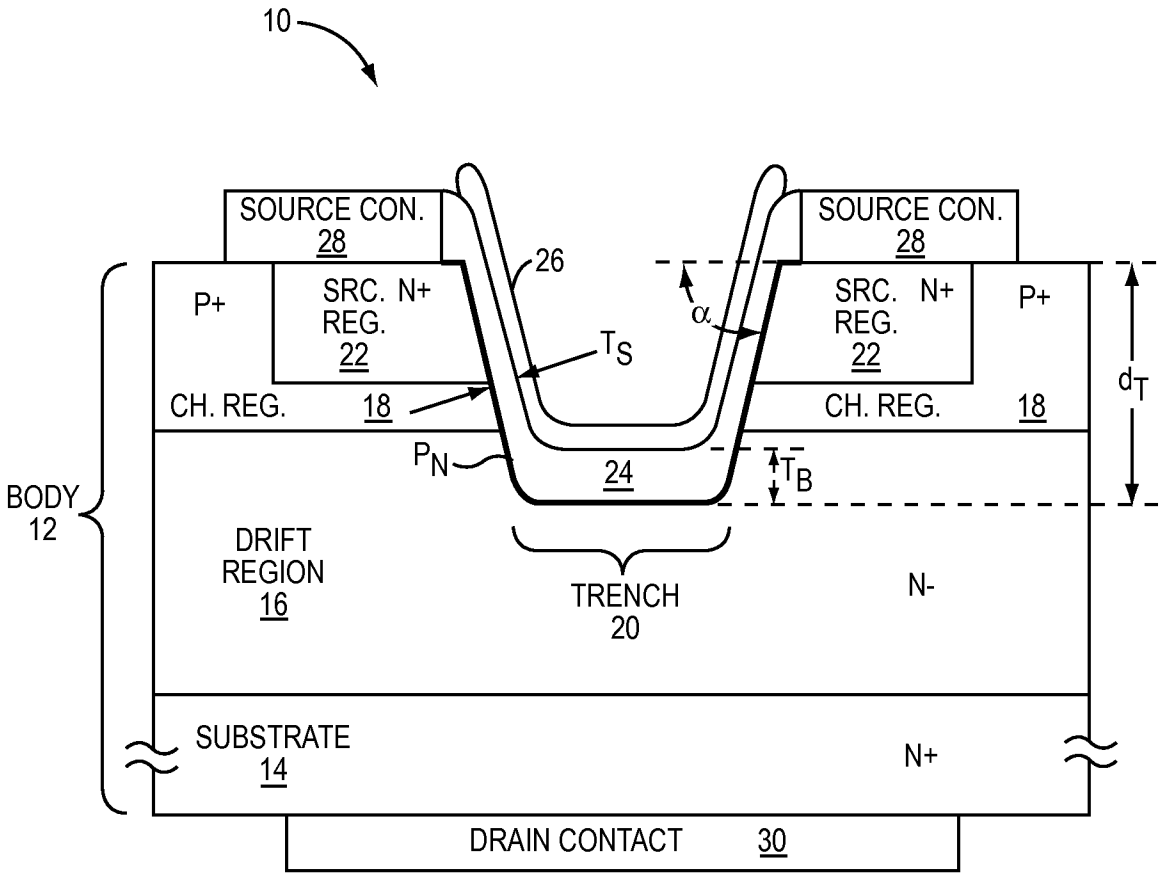
(MOSFET)

FIG. 1


10
T_S
SOURCE CON.
28
SOURCE CON.
28
P+
SRC.
REG.
22
N+
26
SRC.
REG.
22
N+
P+
d_T
CH. REG.
18
CH. REG.
18
P_N
24
T_B
BODY
12
DRIFT
REGION
16
TRENCH
20
N-
SUBSTRATE
14
N+
DRAIN CONTACT
30

(MOSFET)

FIG. 2


10
SOURCE CON.
28
SOURCE CON.
28
26
P+
SRC. N+
REG.
22
T_S
α
SRC. N+
REG.
22
P+
d_T
CH. REG.
18
CH. REG.
18
P_N
24
T_B
BODY
12
DRIFT
REGION
16
TRENCH
20
N-
SUBSTRATE
14
N+
DRAIN CONTACT
30

(MOSFET)

FIG. 3

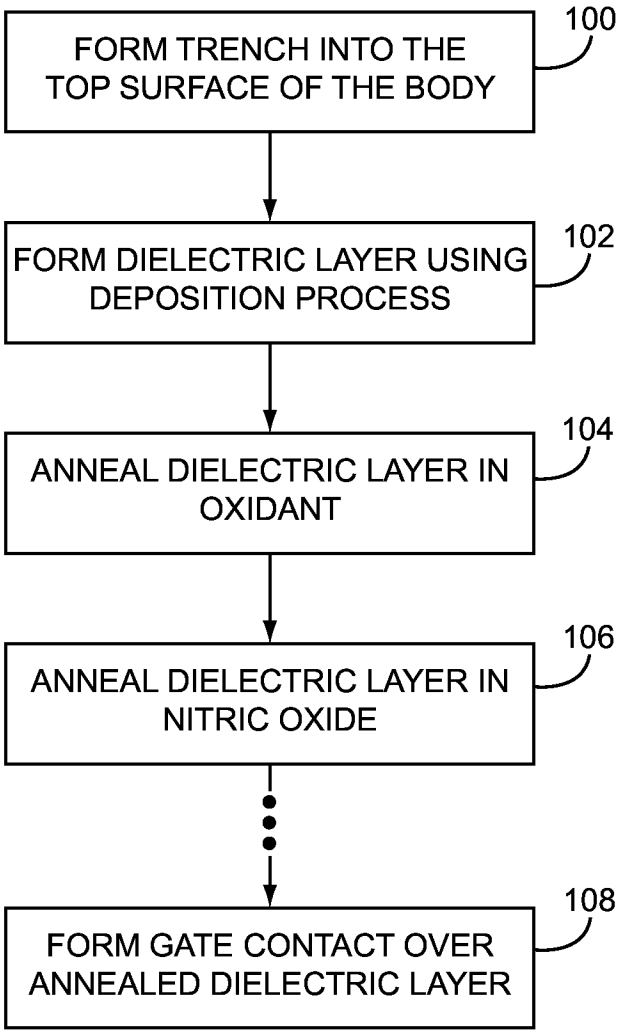
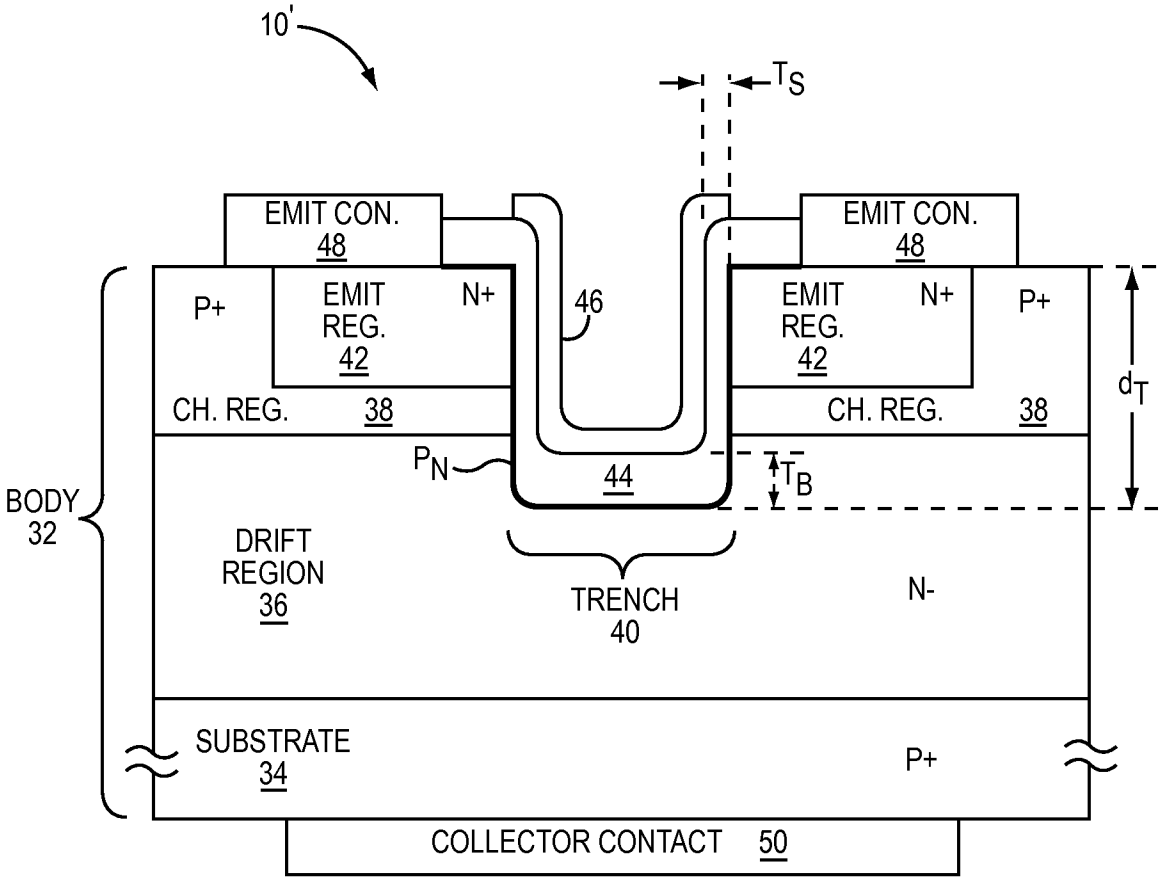
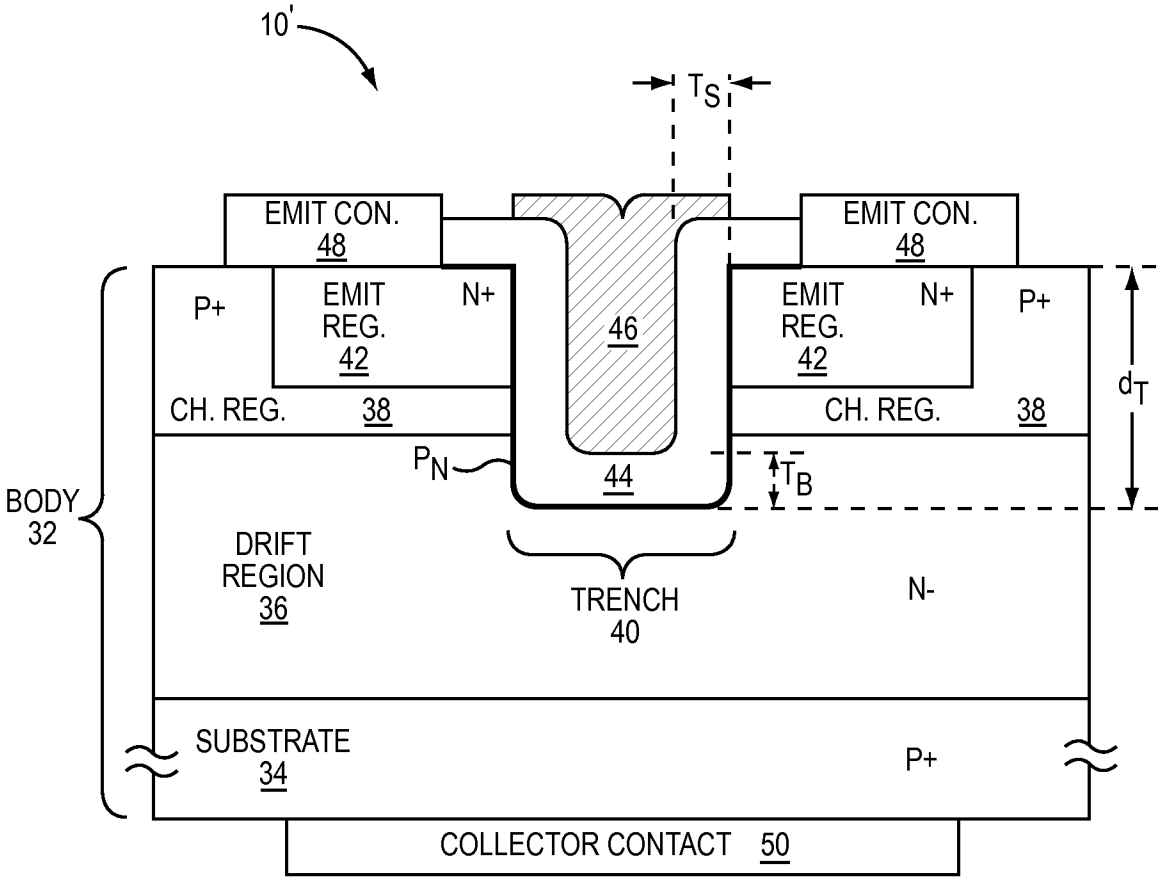

FORM TRENCH INTO THE TOP SURFACE OF THE BODY
100
FORM DIELECTRIC LAYER USING DEPOSITION PROCESS
102
ANNEAL DIELECTRIC LAYER IN OXIDANT
104
ANNEAL DIELECTRIC LAYER IN NITRIC OXIDE
106
FORM GATE CONTACT OVER ANNEALED DIELECTRIC LAYER
108

FIG. 4


10'
T_S
EMIT CON.
48
EMIT CON.
48
P+
EMIT
REG.
42
N+
46
EMIT
REG.
42
N+
P+
d_T
CH. REG.
38
CH. REG.
38
P_N
44
T_B
BODY
32
DRIFT
REGION
36
TRENCH
40
N-
SUBSTRATE
34
P+
COLLECTOR CONTACT
50

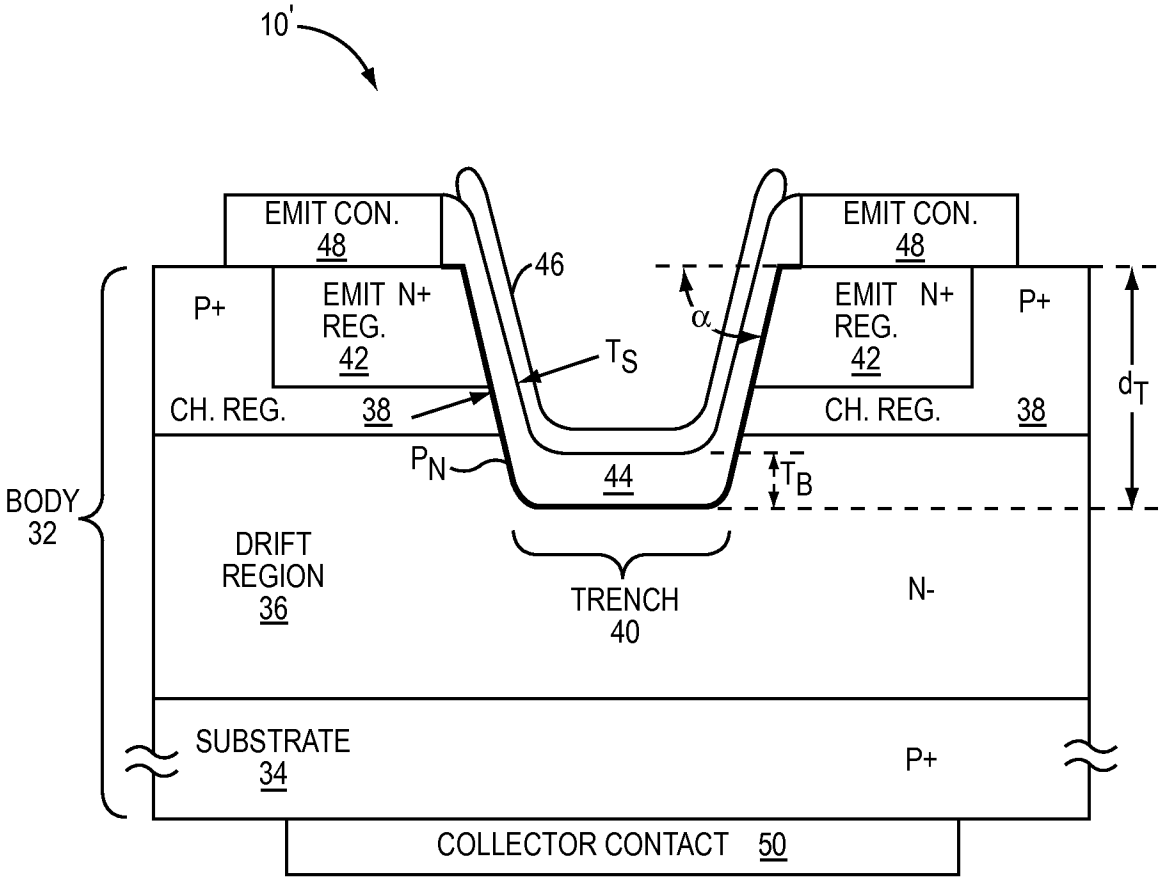
(IGBT)

FIG. 5


10'
T_S
EMIT CON.
48
EMIT CON.
48
P+
EMIT
REG.
42
N+
46
EMIT
REG.
42
N+
P+
d_T
CH. REG.
38
CH. REG.
38
P_N
44
T_B
BODY
32
DRIFT
REGION
36
TRENCH
40
N-
SUBSTRATE
34
P+
COLLECTOR CONTACT
50

(IGBT)

FIG. 6


10'
EMIT CON.
48
EMIT CON.
48
46
P+
EMIT N+
REG.
42
α
EMIT N+
REG.
42
P+
T_S
d_T
CH. REG.
38
CH. REG.
38
P_N
44
T_B
BODY
32
DRIFT
REGION
36
TRENCH
40
N-
SUBSTRATE
34
P+
COLLECTOR CONTACT 50

(IGBT)

FIG. 7