United States Patent [19]

Rockefeller, Jr.

[11] **3,731,152**

[45] **May 1, 1973**

[54] IMPEDANCE DISTANCE RELAY

[75] Inventor: **George D. Rockefeller, Jr.,** Morris Plains, N.J.

[73] Assignee: **Westinghouse Electric Corporation,** Pittsburgh, Pa.

[22] Filed: **May 25, 1972**

[21] Appl. No.: **256,668**

[52] **U.S. Cl.** .....**317/27 R,** 235/151.31, 317/36 D

[51] **Int. Cl.** **H02h 3/40**

[58] **Field of Search** .....317/27 R, 36 D; 235/151.31, 151.32, 182, 151.21; 328/127

[56] **References Cited**

UNITED STATES PATENTS

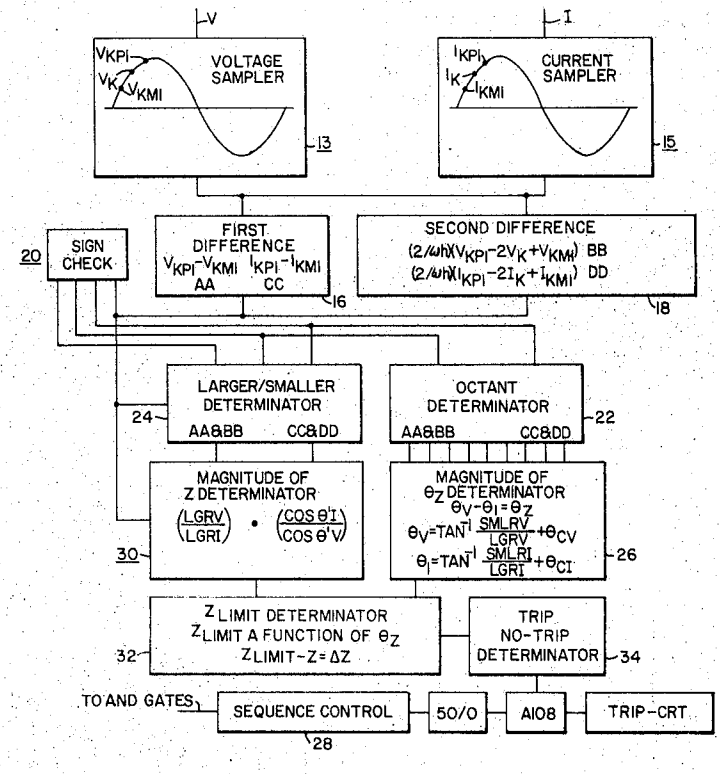
3,569,785	3/1971	Durbeck	235/151.31 X
3,654,516	4/1972	Traversi	317/27 R

Primary Examiner—James D. Trammell
Attorney—A. T. Stratton et al.

[57] **ABSTRACT**

An apparatus for determining the peak value of the sinusoidal component of an electrical quantity which may include a non-sinusoidal component by means of comparing the first and second differential magnitudes of the electrical quantity at any time interval of the period of the sinusoidal component whereby the value of any low rate of change component is attenuated, as for example the D.C. offset which is normally present during fault conditions. The apparatus also includes means to determine the phase angles between two sinusoidal components and when such two sinusoidal components represent current and voltage to determine the magnitude of the impedance of the network energized by said sinusoidal quantities.

37 Claims, 24 Drawing Figures



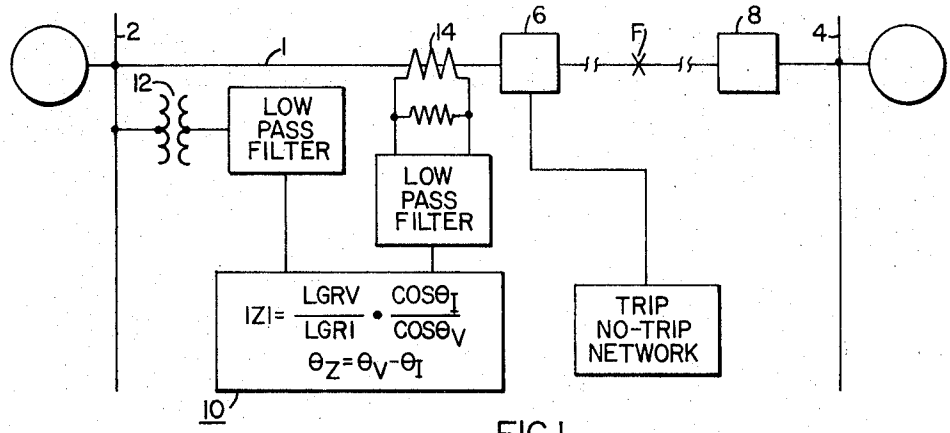

2
1
14
6
F
8
4
12
LOW PASS FILTER
LOW PASS FILTER
$|Z| = \frac{LGRV}{LGRI} \cdot \frac{\cos\theta_I}{\cos\theta_V}$
$\theta_Z = \theta_V - \theta_I$
TRIP NO-TRIP NETWORK
10

FIG.1

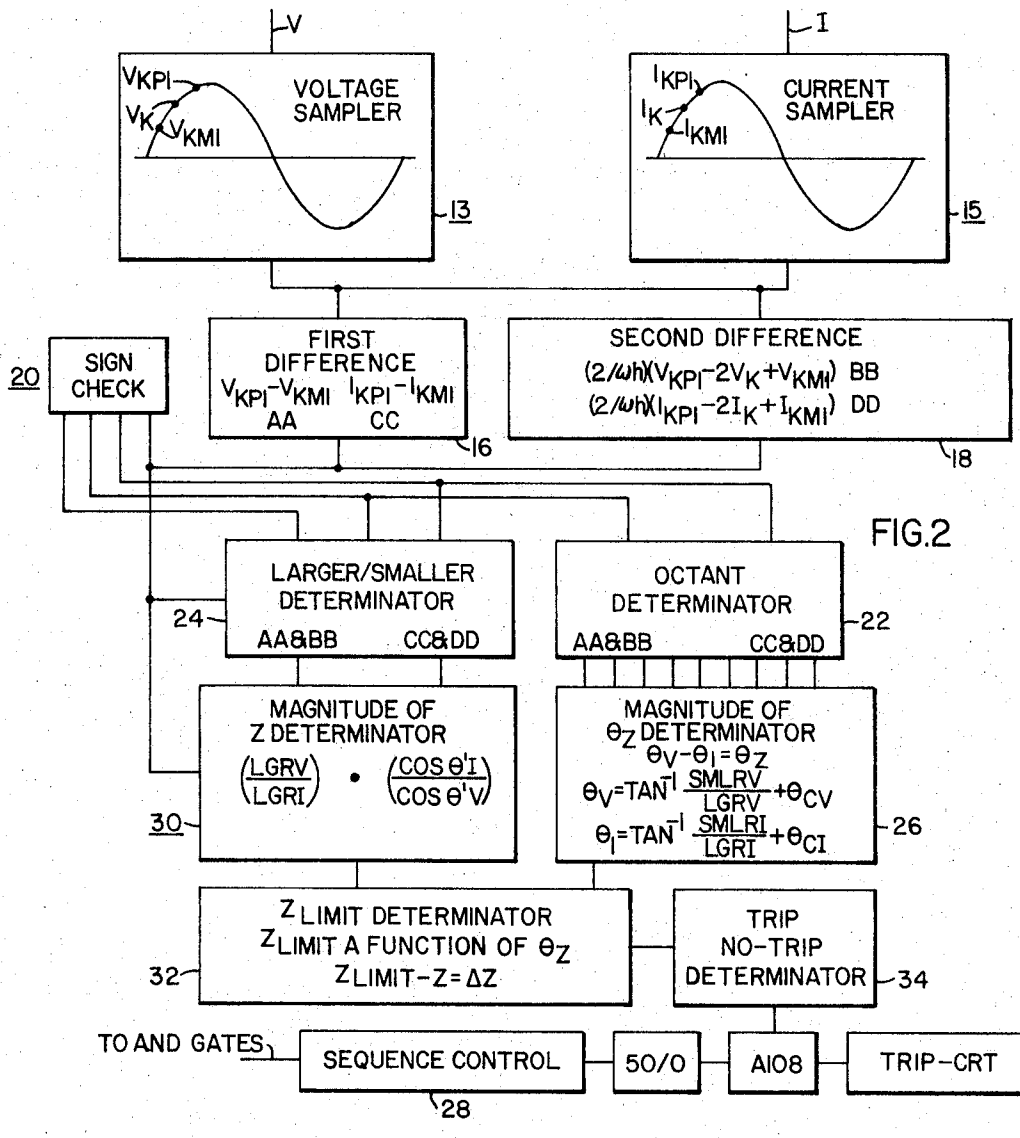
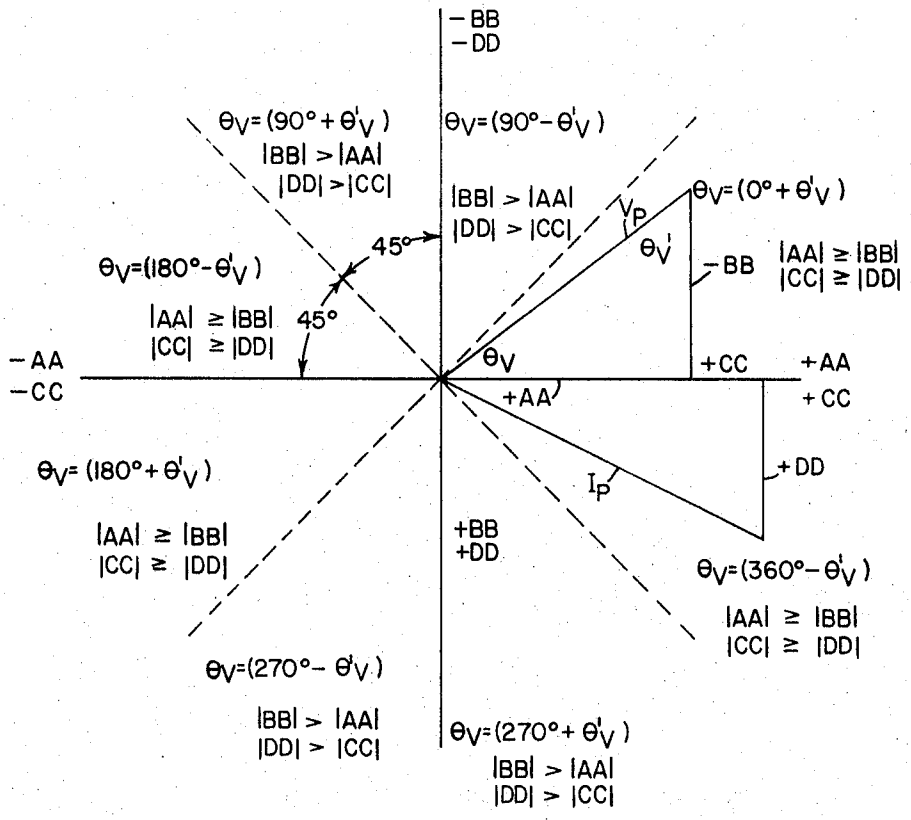

V
V_{KPI}
V_K
V_{KMI}
VOLTAGE SAMPLER
13
I
I_{KPI}
I_K
I_{KMI}
CURRENT SAMPLER
15
20
SIGN CHECK
FIRST DIFFERENCE
$V_{KPI}-V_{KMI}$ AA
$I_{KPI}-I_{KMI}$ CC
16
SECOND DIFFERENCE
$(2/\omega h)(V_{KPI}-2V_K+V_{KMI})$ BB
$(2/\omega h)(I_{KPI}-2I_K+I_{KMI})$ DD
18
LARGER/SMALLER DETERMINATOR
24
AA&BB CC&DD
OCTANT DETERMINATOR
22
AA&BB CC&DD
MAGNITUDE OF Z DETERMINATOR
$\left(\frac{LGRV}{LGRI}\right) \cdot \left(\frac{\cos\theta'_I}{\cos\theta'_V}\right)$
30
MAGNITUDE OF θ_Z DETERMINATOR
$\theta_V-\theta_I=\theta_Z$
$\theta_V=\tan^{-1}\frac{SMLRV}{LGRV}+\theta_{CV}$
$\theta_I=\tan^{-1}\frac{SMLRI}{LGRI}+\theta_{CI}$
26
Z LIMIT DETERMINATOR
Z_{LIMIT} A FUNCTION OF θ_Z
$Z_{LIMIT}-Z=\Delta Z$
32
TRIP NO-TRIP DETERMINATOR
34
TO AND GATES
SEQUENCE CONTROL
28
50/0
AIO8
TRIP-CRT

FIG.2

FIG.3


−BB
−DD
θV=(90°+θ'V)
|BB| > |AA|
|DD| > |CC|
θV=(90°−θ'V)
|BB| > |AA|
|DD| > |CC|
θV=(0°+θ'V)
VP
θV'
45°
θV=(180°−θ'V)
|AA| ≥ |BB|
|CC| ≥ |DD|
45°
−BB
|AA| ≥ |BB|
|CC| ≥ |DD|
−AA
−CC
θV
+CC
+AA
+CC
+AA
+DD
IP
θV=(180°+θ'V)
|AA| ≥ |BB|
|CC| ≥ |DD|
+BB
+DD
θV=(360°−θ'V)
|AA| ≥ |BB|
|CC| ≥ |DD|
θV=(270°−θ'V)
|BB| > |AA|
|DD| > |CC|
θV=(270°+θ'V)
|BB| > |AA|
|DD| > |CC|

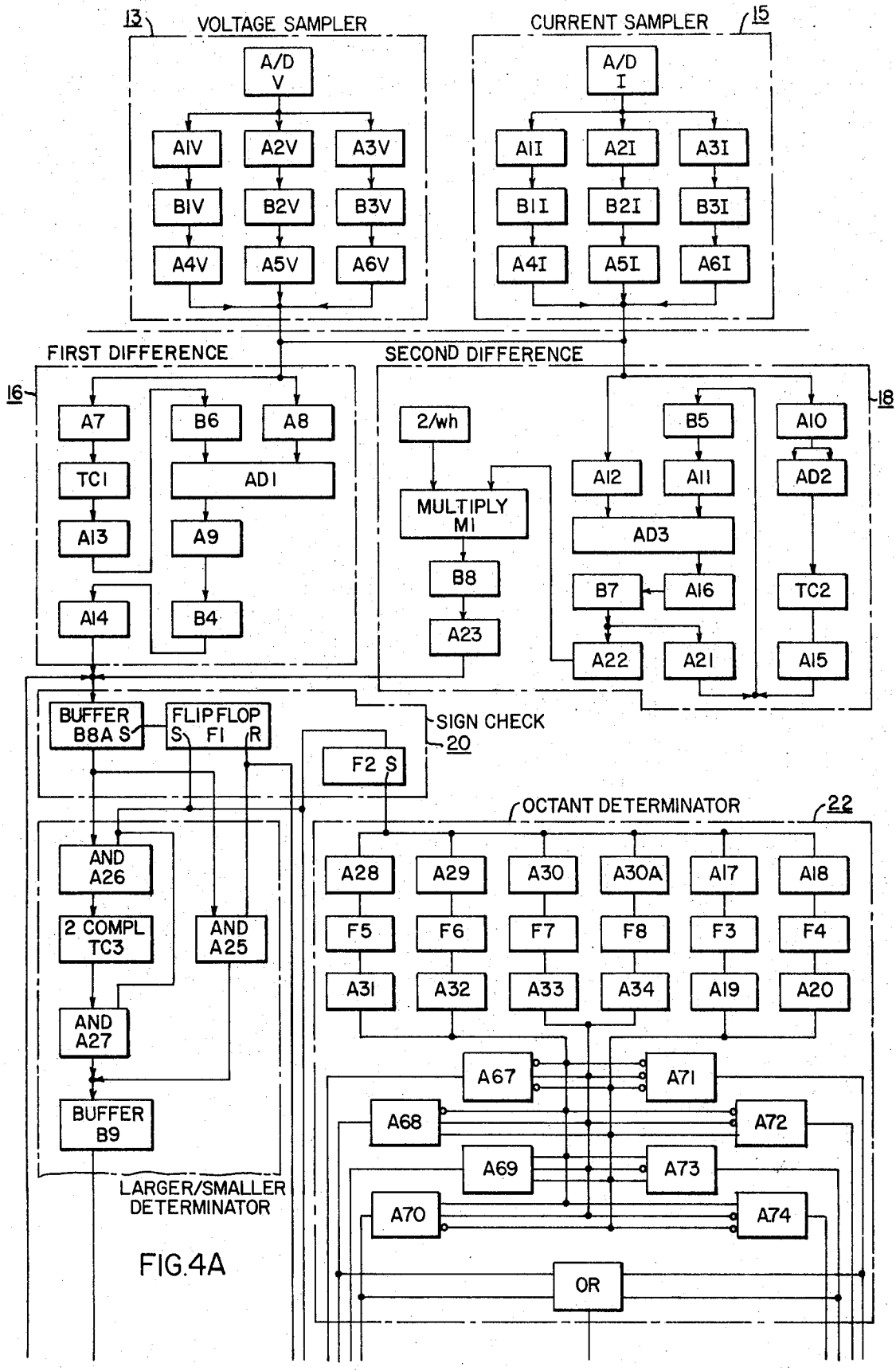

13
VOLTAGE SAMPLER
A/D V
AIV
A2V
A3V
BIV
B2V
B3V
A4V
A5V
A6V
15
CURRENT SAMPLER
A/D I
AII
A2I
A3I
BII
B2I
B3I
A4I
A5I
A6I
FIRST DIFFERENCE
16
A7
B6
A8
TC1
AD1
AI3
A9
AI4
B4
SECOND DIFFERENCE
18
2/wh
MULTIPLY MI
B8
A23
B5
AI0
AI2
AII
AD2
AD3
B7
AI6
TC2
A22
A21
AI5
BUFFER B8A S
FLIPFLOP S FI R
SIGN CHECK
20
F2 S
OCTANT DETERMINATOR
22
AND A26
2 COMPL TC3
AND A25
AND A27
BUFFER B9
LARGER/SMALLER DETERMINATOR
A28
A29
A30
A30A
AI7
AI8
F5
F6
F7
F8
F3
F4
A31
A32
A33
A34
AI9
A20
A67
A71
A68
A72
A69
A73
A70
A74
OR

FIG.4A

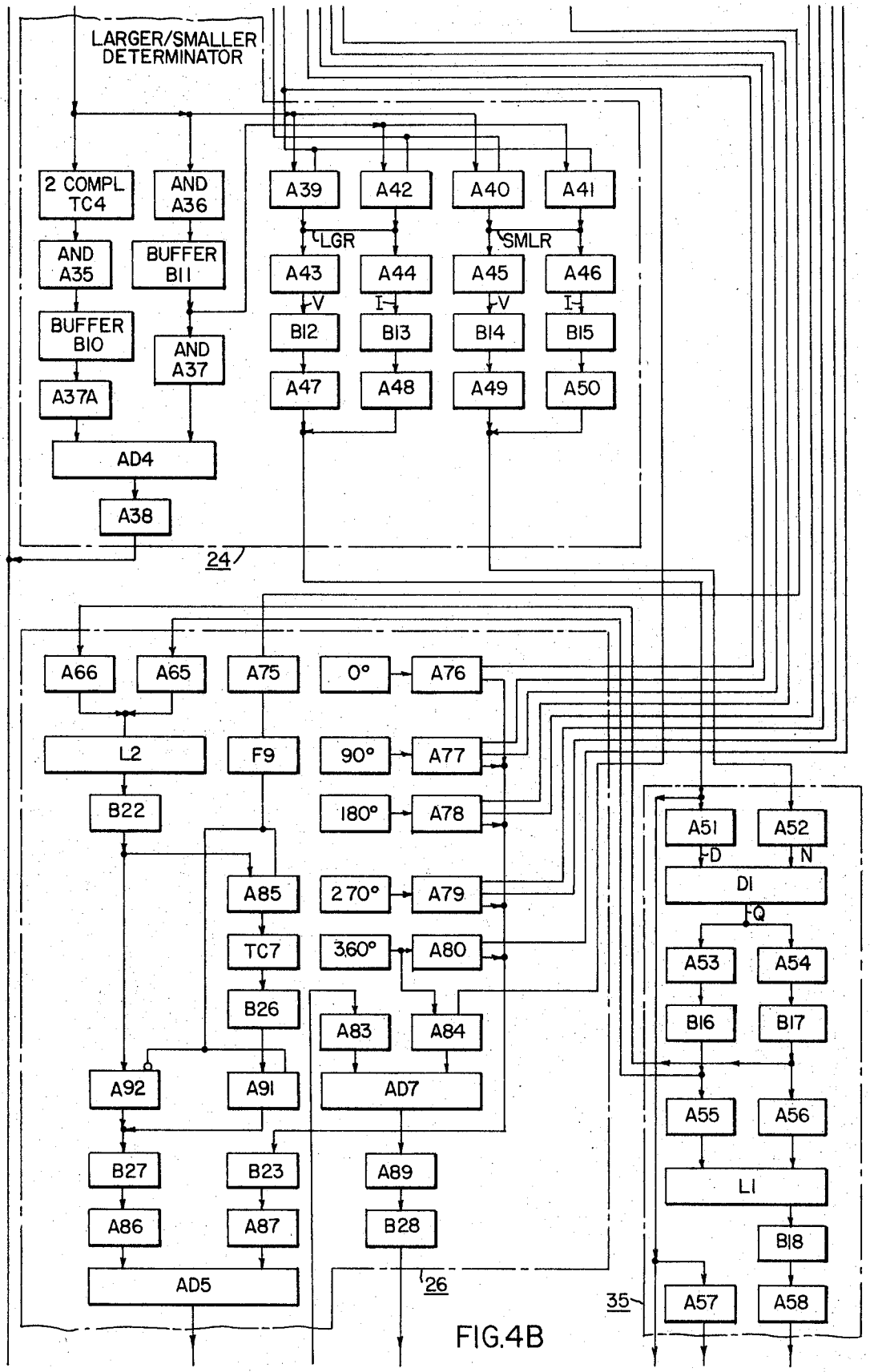

LARGER/SMALLER DETERMINATOR
2 COMPL TC4
AND A36
AND A35
BUFFER BII
BUFFER BIO
AND A37
A37A
AD4
A38
24
A39
A42
A40
A41
LGR
SMLR
A43
A44
A45
A46
V
I
V
I
BI2
BI3
BI4
BI5
A47
A48
A49
A50
A66
A65
A75
0°
A76
L2
F9
90°
A77
B22
180°
A78
A85
270°
A79
TC7
360°
A80
B26
A83
A84
A92
A91
AD7
B27
B23
A89
A86
A87
B28
AD5
26
A51
A52
D
N
DI
Q
A53
A54
BI6
BI7
A55
A56
LI
BI8
35
A57
A58

FIG.4B

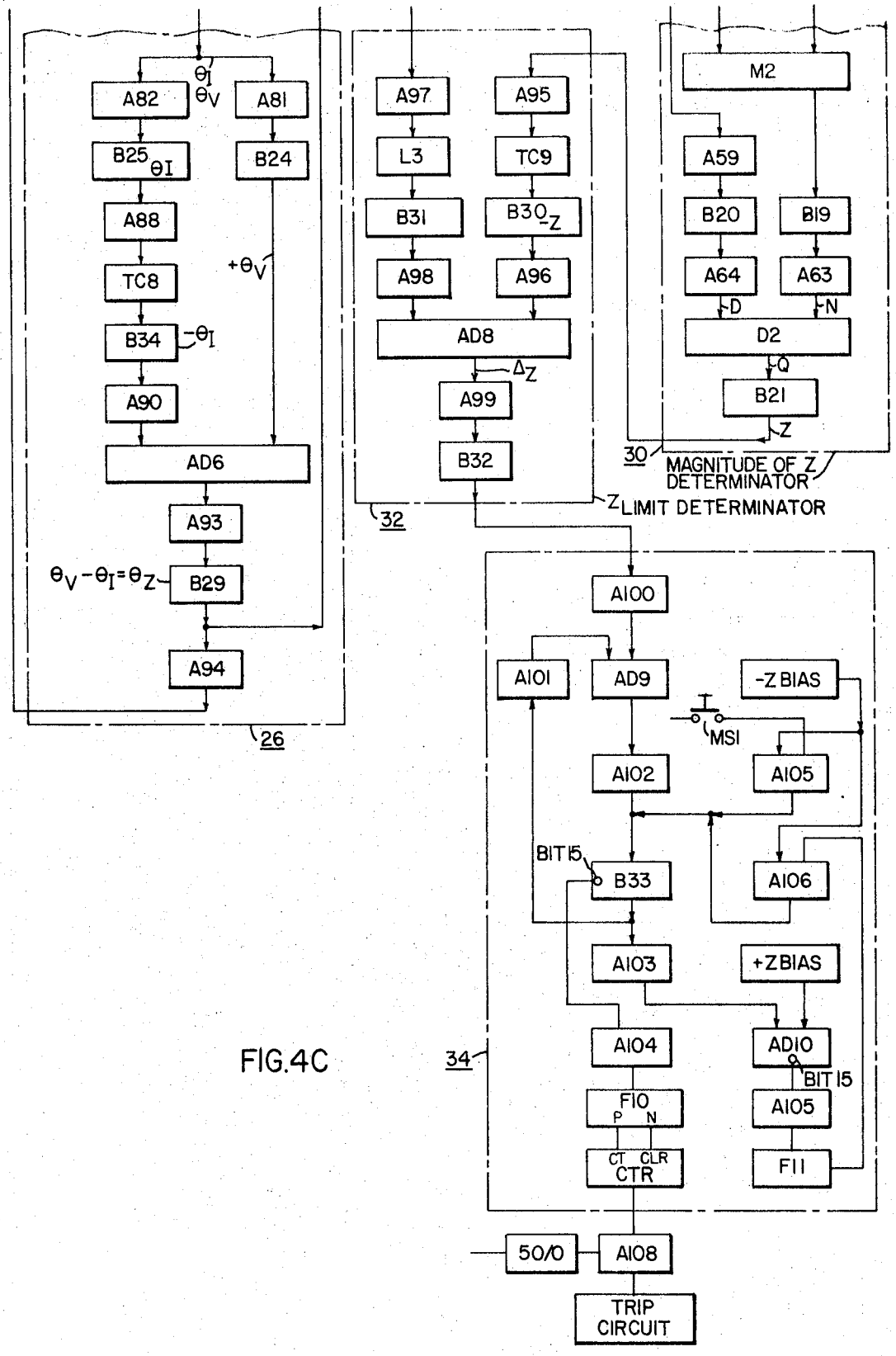

θI
θV
A82
A81
B25 θI
B24
A88
TC8
+θV
B34 -θI
A90
AD6
A93
θV-θI=θZ
B29
A94
26
A97
A95
L3
TC9
B31
B30 -Z
A98
A96
AD8
ΔZ
A99
B32
32
M2
A59
B20
B19
A64
A63
-D
-N
D2
-Q
B21
Z
30
MAGNITUDE OF Z DETERMINATOR
Z LIMIT DETERMINATOR
A100
A101
AD9
-Z BIAS
MSI
A102
A105
BIT 15
B33
A106
A103
+Z BIAS
A104
AD10
BIT 15
FIO
P N
A105
CT CLR
CTR
FII
34
50/0
A108
TRIP CIRCUIT

FIG.4C

TIME INT.	CONDUCTING AND GATES			TIME INT.	CONDUCTING AND GATES			TIME INT.	CONDUCTING AND GATES		
0	A3V	A3I	A5I	20	A1V	A1I	A6I	40	A2V	A2I	A4I
1			A4I	21			A5I	41			A6I
2			A6I	22			A4I	42			A5I
3				23				43			
4				24				44			
5				25				45			
6			A4I	26			A5I	46			A6I
7				27				47			
8				28				48			
9				29				49			
10				30				50			
11				31				51			
12			A5V	32			A6V	52			A4V
13			A4V	33			A5V	53			A6V
14			A6V	34			A4V	54			A5V
15				35				55			
16			A4V	36			A5V	56			A6V
17				37				57			
18				38				58			
19				39				59			

FIG. 5A

TIME INTERVALS			CONDUCTING AND GATES												
0	20	40	A10	A23	A30	A36									
1	21	41	A7	A13	A15	A25	A26	A27	A82	A86	A87	A91			
2	22	42	A8	A9	A11	A12	A16	A35	A88						
3	23	43	A17	A21	A37	A37A	A38								
4	24	44	A41	A42	A43	A45									
5	25	45	A39	A40	A43	A45									
6	26	46	A11	A12	A14	A16	A19	A29	A31	A33	A47	A49	A51	A52	A53
7	27	47	A22	A25	A26	A27	A55	A56	A65						
8	28	48	A47	A57	A58	A75	A85								
9	29	49	A30A	A36	A63	A64	A91								
10	30	50	A25	A26	A27	A81	A86	A87	A95						
11	31	51	A90	A93	A94										
12	32	52	A10	A35	A83	A84	A89								
13	33	53	A7	A13	A15	A18	A37	A37A	A38	A97					
14	34	54	A8	A9	A11	A12	A16	A41	A42	A44	A46	A96	A98	A99	
15	35	55	A21	A39	A40	A44	A46	A100	A101						
16	36	56	A11	A12	A16	A20	A32	A34	A48	A50	A51	A52	A54	A75	A102
17	37	57	A14	A28	A48	A59	A66	A103	A104	A105					
18	38	58	A22	A25	A26	A27	A106	A107							
19	39	59	A85	A92											

FIG. 5B

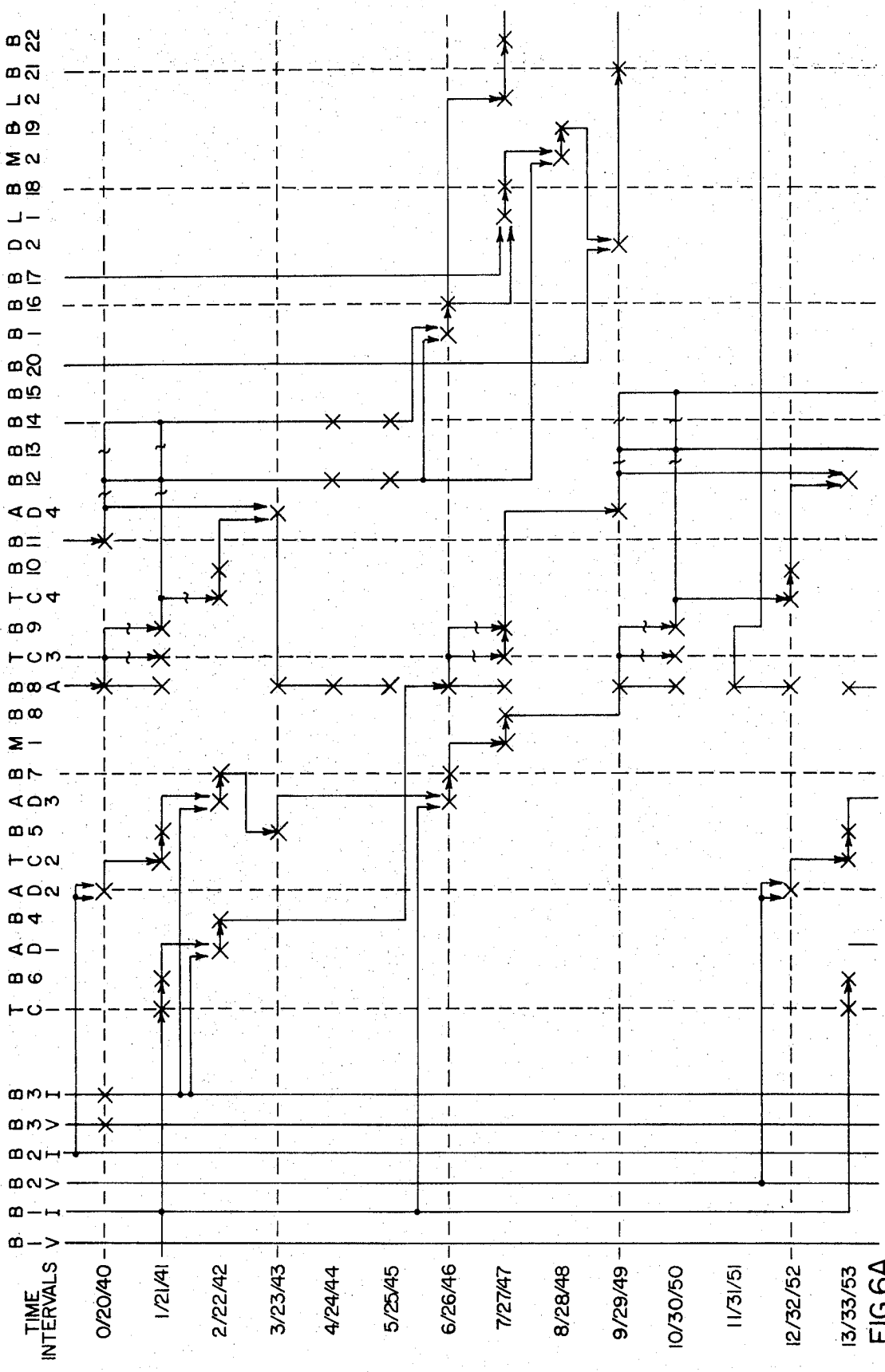

TIME INTERVALS
0/20/40
1/21/41
2/22/42
3/23/43
4/24/44
5/25/45
6/26/46
7/27/47
8/28/48
9/29/49
10/30/50
11/31/51
12/32/52
13/33/53

FIG.6A

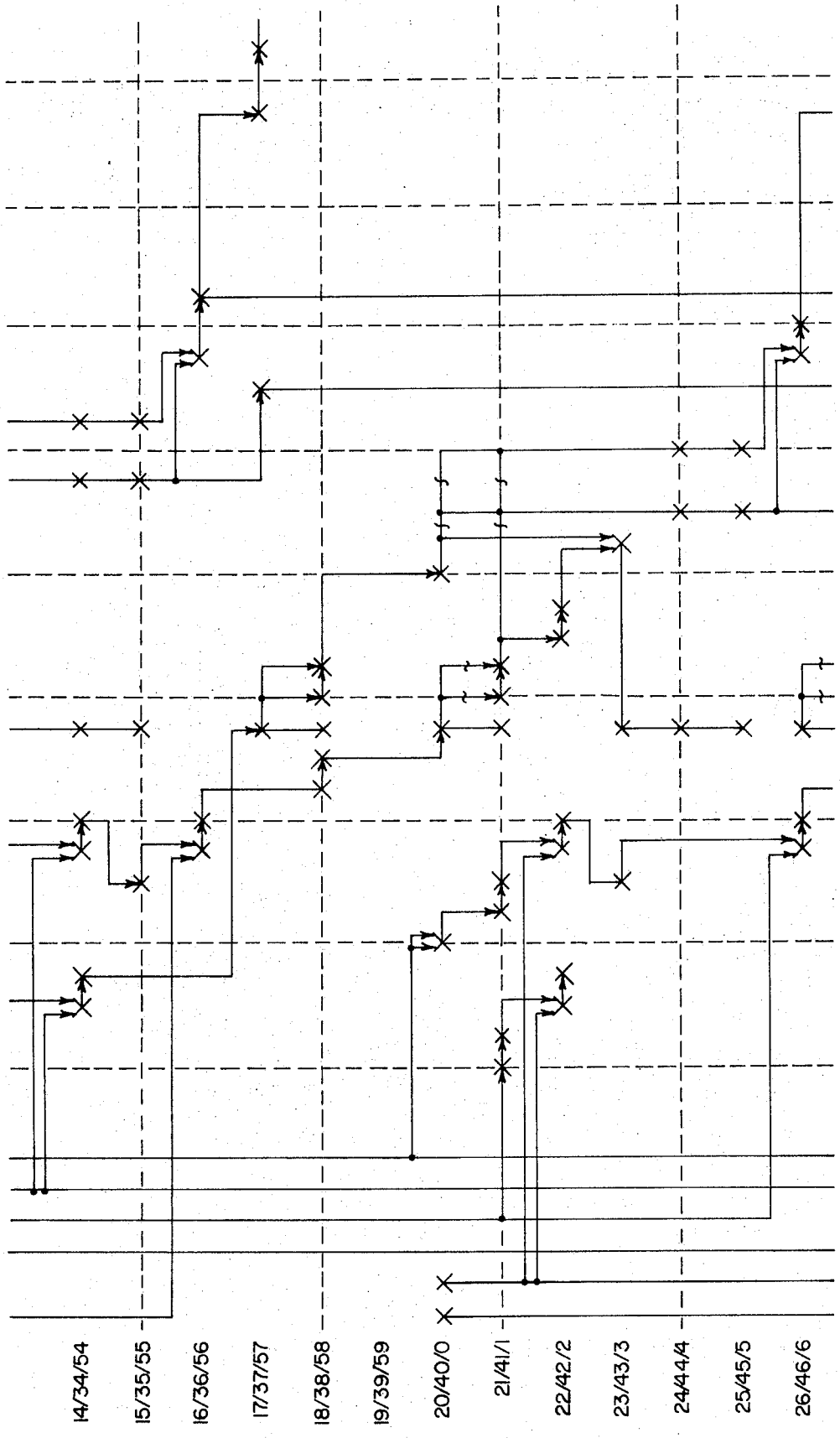

14/34/54
15/35/55
16/36/56
17/37/57
18/38/58
19/39/59
20/40/0
21/41/1
22/42/2
23/43/3
24/44/4
25/45/5
26/46/6

FIG.6B

FIG.6C

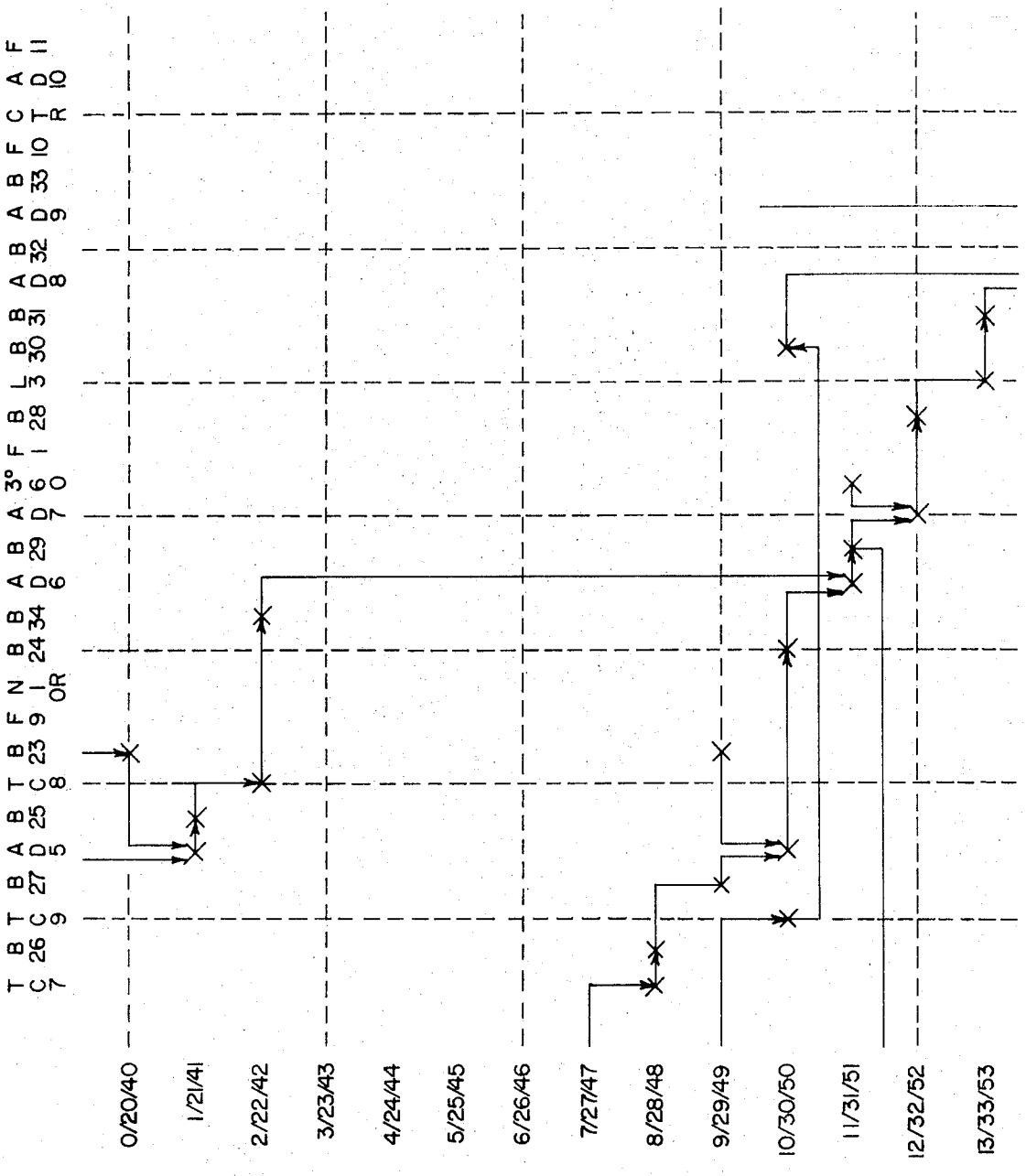
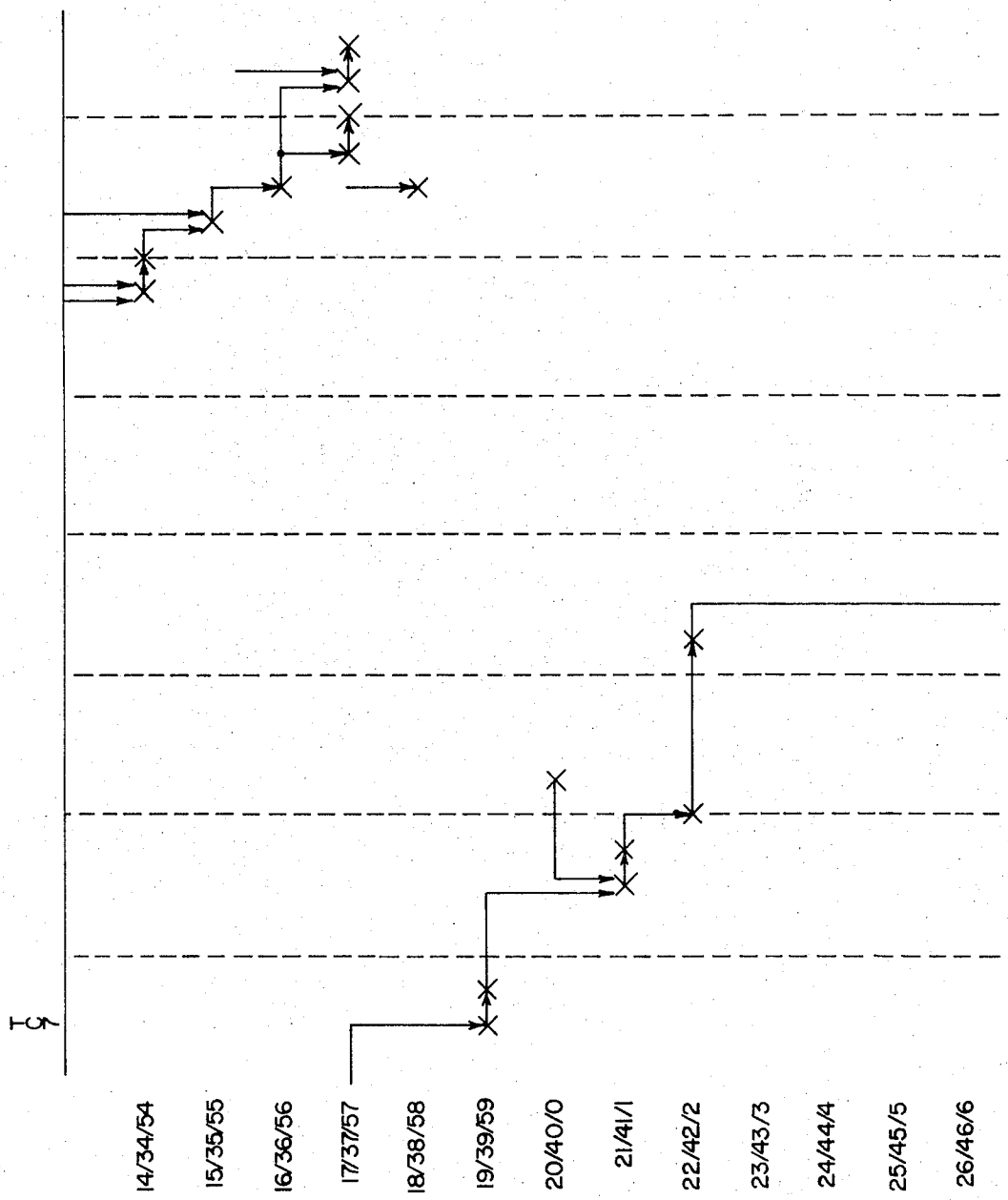

T B T B A B T B F N B B A B A 3° F B L B B A B A B F C A F
C 26 C 27 D 25 C 23 9 I 24 34 D 29 D 6 I 28 3 30 31 D 32 D 33 10 T R D 11
7 9 5 8 OR 6 7 0 9 10
0/20/40
1/21/41
2/22/42
3/23/43
4/24/44
5/25/45
6/26/46
7/27/47
8/28/48
9/29/49
10/30/50
11/31/51
12/32/52
13/33/53

FIG.6C	FIG.6D
FIG.6A	FIG.6B

FIG.6E

FIG.6D



	OCTANT OF ANGLE θ^1							
	1	2	3	4	5	6	7	8
F3 |BB| > |AA|	0	1	1	0	0	1	1	0
F4 |DD| > |CC|	0	1	1	0	0	1	1	0
F5 AA	0	0	1	1	1	1	0	0
F6 CC	0	0	1	1	1	1	0	0
F7 BB	1	1	1	1	0	0	0	0
F8 DD	1	1	1	1	0	0	0	0
OR (-θ)	0	1	0	1	0	1	0	1
A67	1	0	0	0	0	0	0	0
A68	0	1	0	0	0	0	0	0
A69	0	0	1	0	0	0	0	0
A70	0	0	0	1	0	0	0	0
A71	0	0	0	0	0	0	0	1
A72	0	0	0	0	0	0	1	0
A73	0	0	0	0	0	1	0	0
A74	0	0	0	0	1	0	0	0
A76	1	0	0	0	0	0	0	0
A77	0	1	1	0	0	0	0	0
A78	0	0	0	1	1	0	0	0
A79	0	0	0	0	0	1	1	0
A80	0	0	0	0	0	0	0	1

FIG. 7

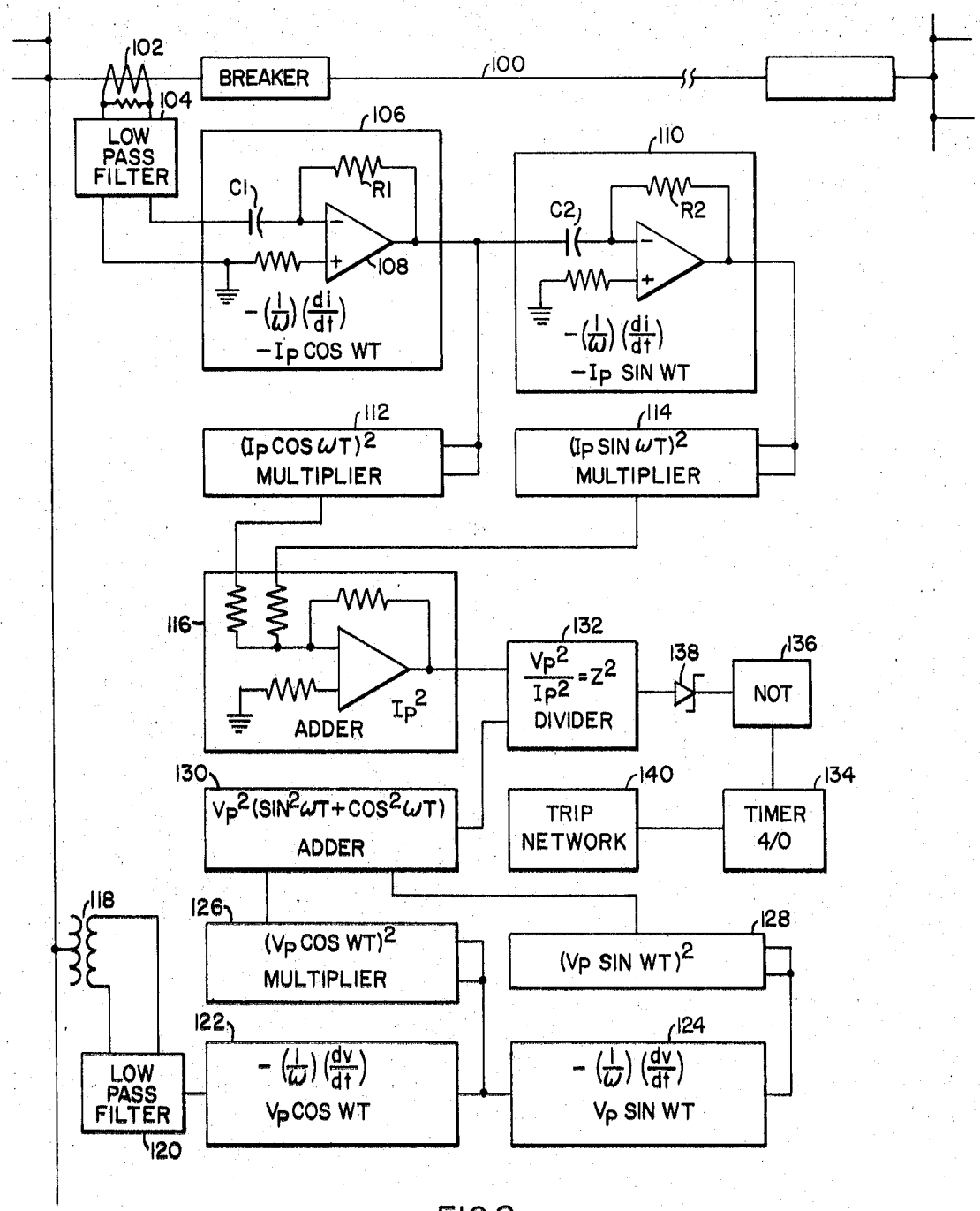

102
BREAKER
100
104
LOW PASS FILTER
106
C1
R1
108
$-\left(\frac{1}{\omega}\right)\left(\frac{di}{dt}\right)$
$-I_P \cos WT$
110
C2
R2
$-\left(\frac{1}{\omega}\right)\left(\frac{di}{dt}\right)$
$-I_P \sin WT$
112
$(I_P \cos \omega T)^2$ MULTIPLIER
114
$(I_P \sin \omega T)^2$ MULTIPLIER
116
ADDER
I_P^2
132
$\frac{V_P^2}{I_P^2} = Z^2$
DIVIDER
138
136
NOT
130
$V_P^2(\sin^2 \omega T + \cos^2 \omega T)$
ADDER
140
TRIP NETWORK
134
TIMER 4/0
118
126
$(V_P \cos WT)^2$ MULTIPLIER
128
$(V_P \sin WT)^2$
122
$-\left(\frac{1}{\omega}\right)\left(\frac{dv}{dt}\right)$
$V_P \cos WT$
124
$-\left(\frac{1}{\omega}\right)\left(\frac{dv}{dt}\right)$
$V_P \sin WT$
LOW PASS FILTER
120

FIG.8

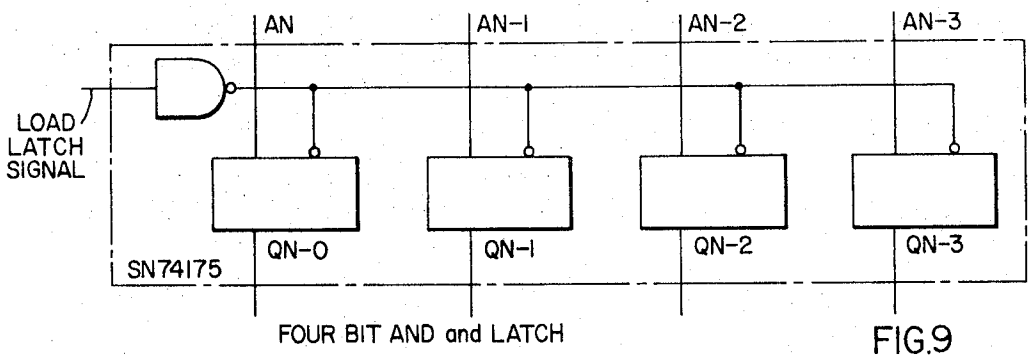


FIG.9

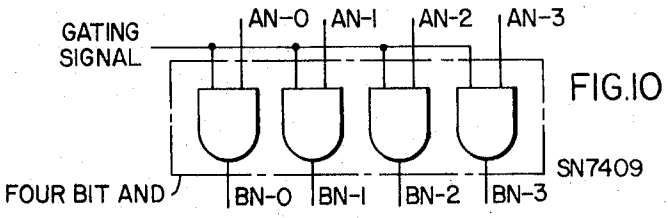


FIG.10

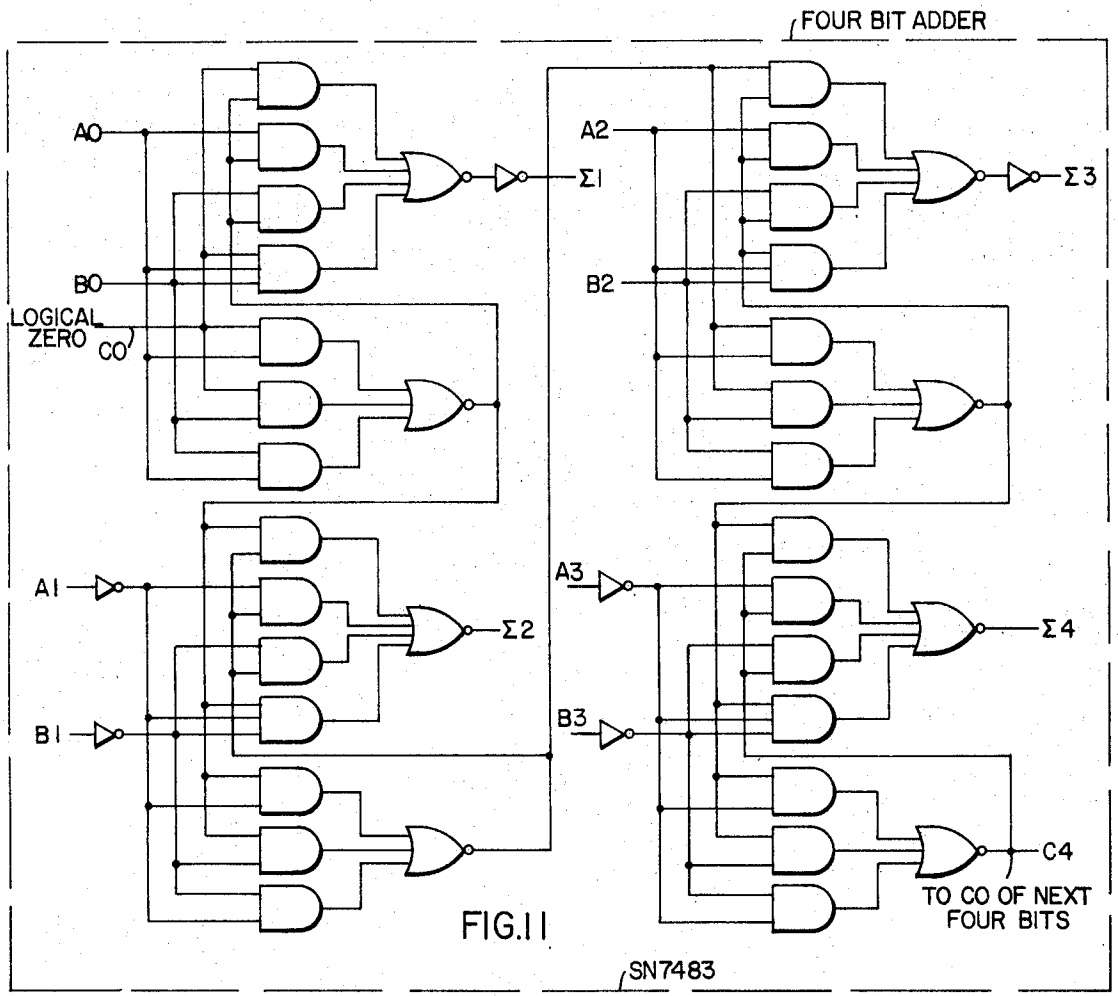


FIG.11

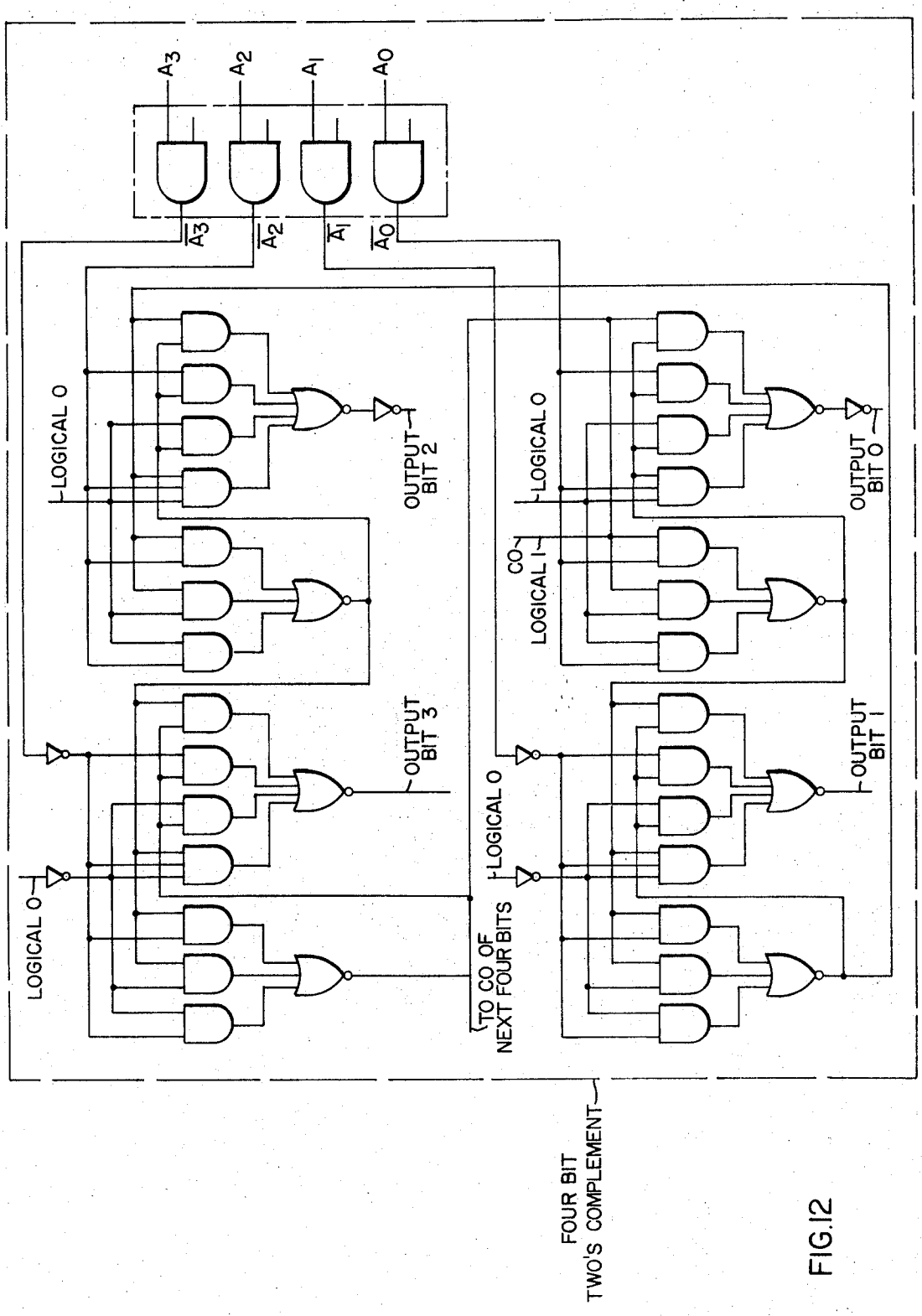

A3
A2
A1
A0
LOGICAL 0
OUTPUT BIT 2
OUTPUT BIT 3
LOGICAL 0
TO CO OF NEXT FOUR BITS
LOGICAL 0
CO
LOGICAL 1
OUTPUT BIT 0
OUTPUT BIT 1
FOUR BIT TWO'S COMPLEMENT

FIG.12

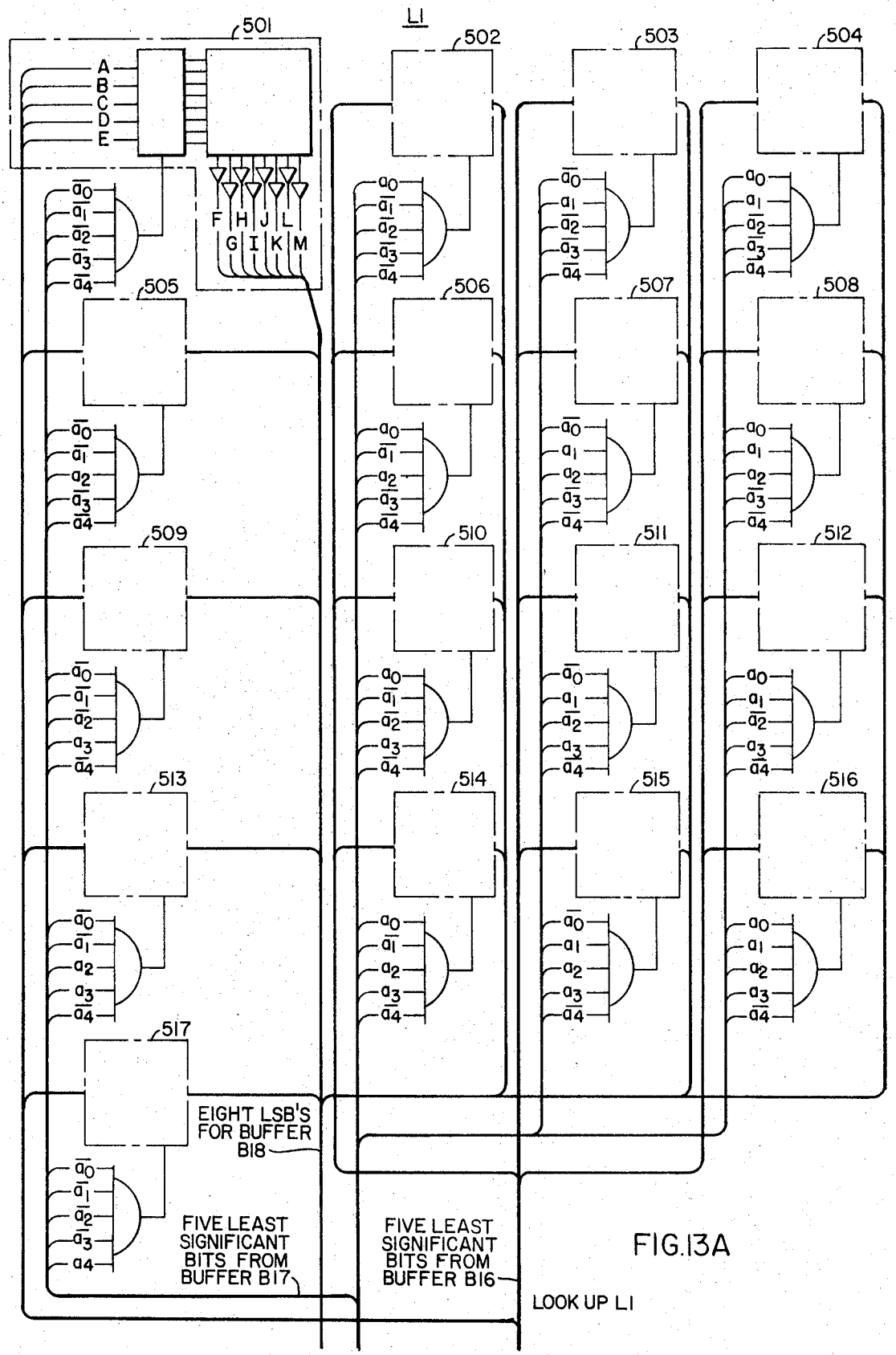

LI
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
A
B
C
D
E
F
G
H
I
J
K
L
M
EIGHT LSB'S FOR BUFFER B18
FIVE LEAST SIGNIFICANT BITS FROM BUFFER B17
FIVE LEAST SIGNIFICANT BITS FROM BUFFER B16
LOOK UP LI

FIG.13A

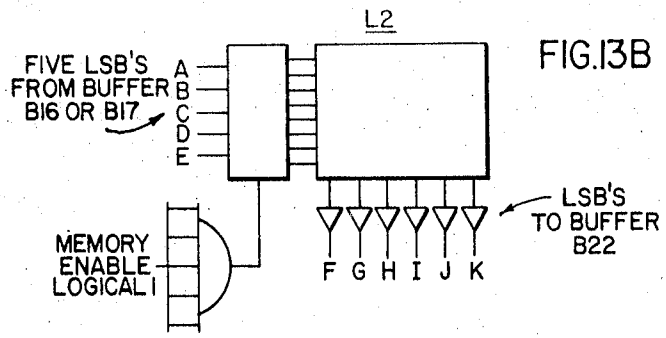
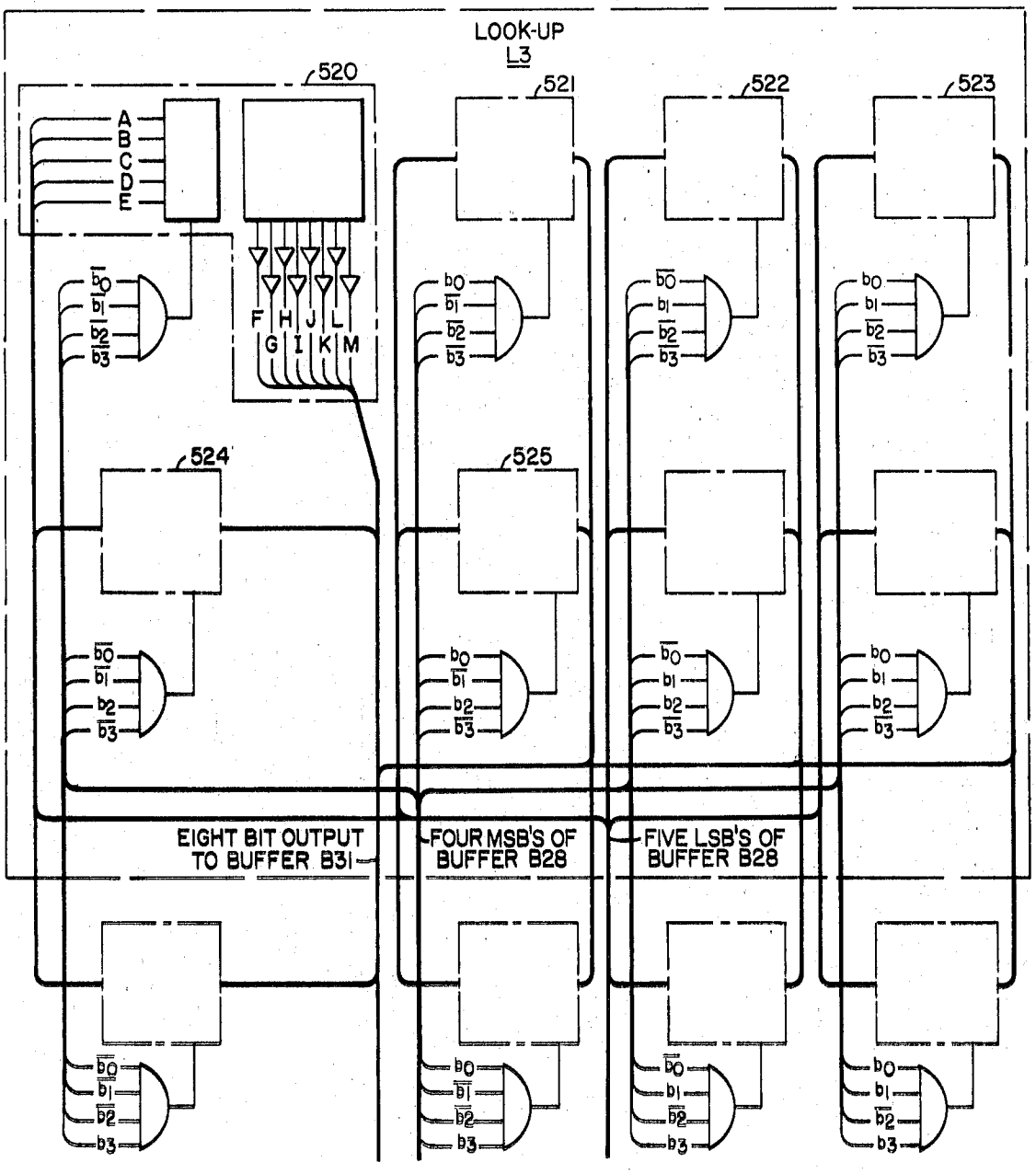


FIG.13B

FIG.13C



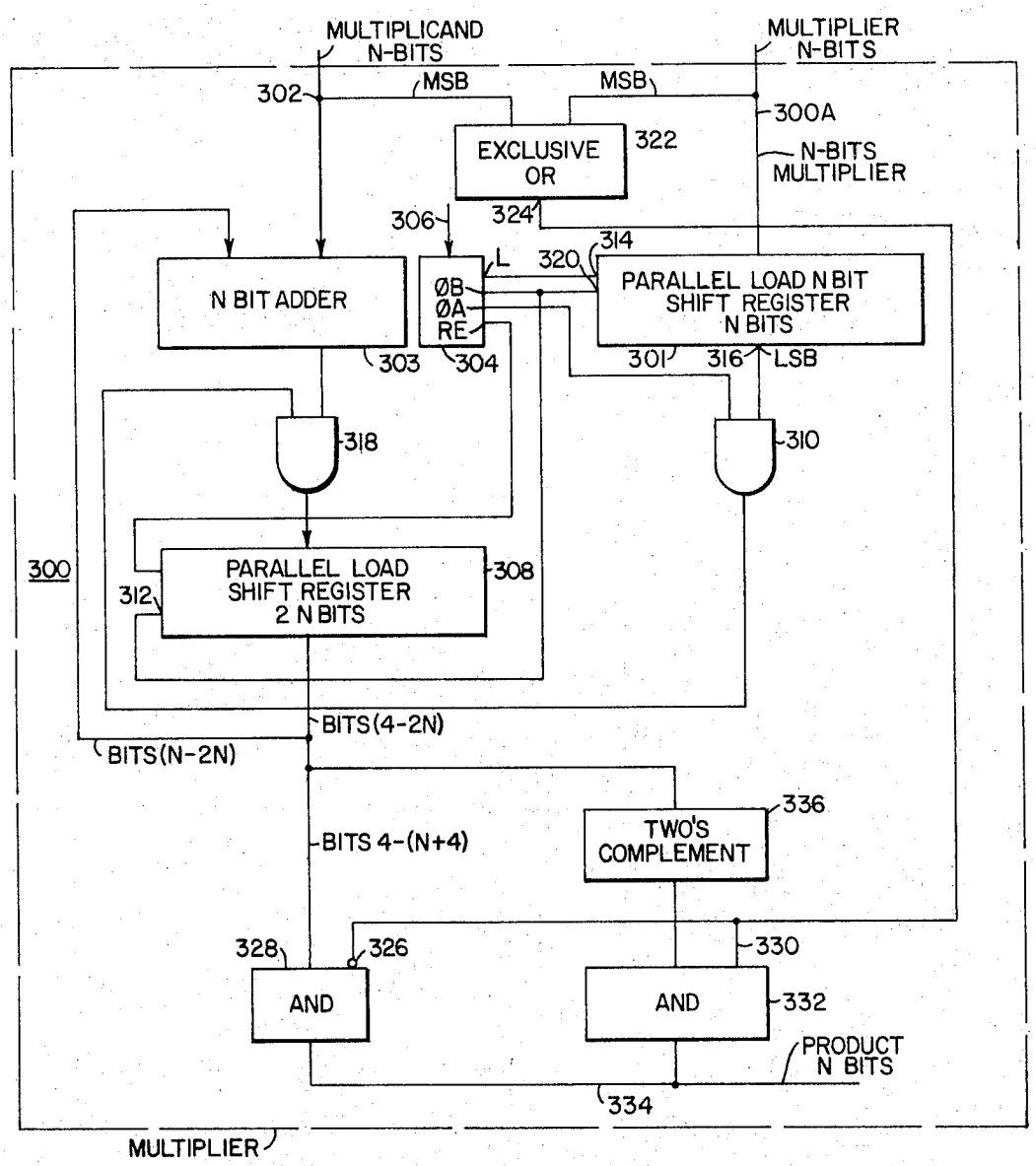

MULTIPLICAND N-BITS
MULTIPLIER N-BITS
302
MSB
MSB
300A
EXCLUSIVE OR
322
N-BITS MULTIPLIER
306
324
314
320
L
ØB
ØA
RE
N BIT ADDER
PARALLEL LOAD N BIT SHIFT REGISTER N BITS
303
304
301
316
LSB
318
310
300
PARALLEL LOAD SHIFT REGISTER 2 N BITS
312
308
BITS(4-2N)
BITS(N-2N)
BITS 4-(N+4)
TWO'S COMPLEMENT
336
328
326
330
AND
AND
332
PRODUCT N BITS
334
MULTIPLIER

FIG.14

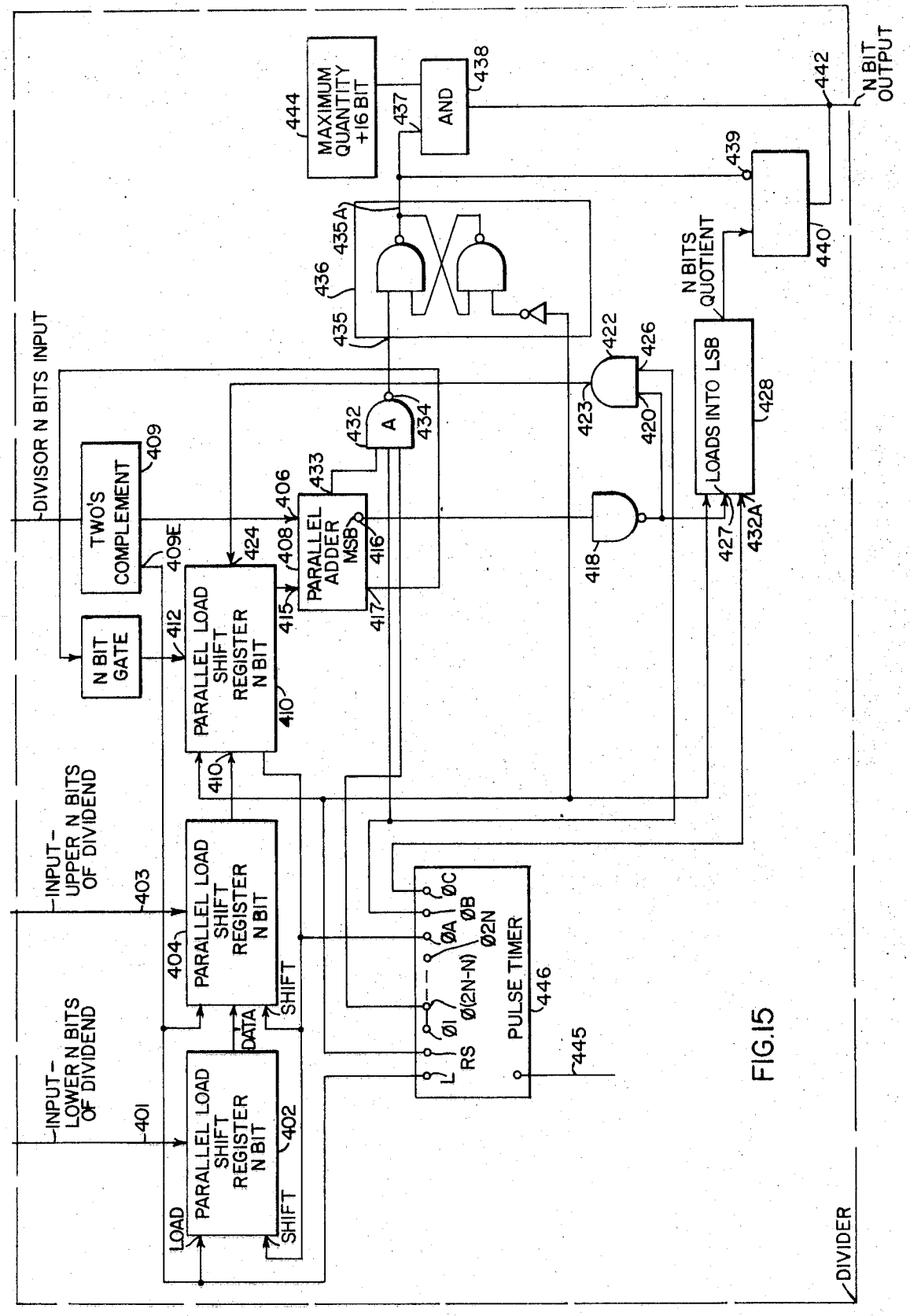

DIVISOR N BITS INPUT
TWO'S COMPLEMENT
409
N BIT GATE
409E
412
PARALLEL LOAD SHIFT REGISTER N BIT
410
424
408
415
PARALLEL ADDER MSB
406
433
416
417
432
A
434
INPUT - UPPER N BITS OF DIVIDEND
403
404
PARALLEL LOAD SHIFT REGISTER N BIT
SHIFT
DATA
INPUT - LOWER N BITS OF DIVIDEND
401
LOAD
PARALLEL LOAD SHIFT REGISTER N BIT
402
SHIFT
L
RS
Ø1
Ø(2N-N)
ØA
ØB
Ø2N
ØC
PULSE TIMER
446
445
MAXIMUM QUANTITY +16 BIT
444
437
AND
438
442
N BIT OUTPUT
439
440
435A
436
435
422
426
423
420
418
427
N BITS QUOTIENT
LOADS INTO LSB
428
432A
DIVIDER

FIG.15

IMPEDANCE DISTANCE RELAY

BRIEF SUMMARY OF THE INVENTION

The voltage and magnitude at which electric power is transmitted is constantly being increased. This increased power makes it desirable to interrupt any fault current in as short a time period as possible to maintain system stability and to minimize fault current damage and at the same time to maintain system security by preventing interruptions due to transient conditions which do not require such an interruption.

In accordance with this invention the peak magnitude of the sinusoidal quantity or quantities is determined by utilizing the first and second derivatives of the quantity. These derivatives are obtained by measuring the quantity of the sinusoidal component either continually or at frequent intervals. In the case of an analogue device, the sine and cosine quantities may be eliminated by squaring the cosine quantity of the first derivative and squaring the sine quantity of the second derivative of the sinusoidal quantity. The two quantities are thereafter added together and equated to unity in accordance with the trigonometric functions that the sum of the sine quantity squared and of the cosine quantity squared equals unity.

In the case of a digital sampling of the sinusoidal quantity, the first and second differences of the quantity which approximate the first and second differentials of the quantity are utilized. If desired, these difference quantities could be treated as set out above by squaring and equating to unity. I prefer, however, to utilize these difference quantities by dividing the second difference quantity by the first difference quantity and of thereafter using the values which have been established for trigonometric functions and which are readily available in table form. For example, by determining the angle from the tangent table portion and thereafter using the cosine quantity for that angle the peak magnitude of the quantity may be mathematically determined.

If the magnitudes of two sinusoidal quantities are substantially simultaneously sampled the angle between the two quantities is equal to the difference between the two angles as determined from the tables. If the sinusoidal quantities are current and voltage the magnitude of the impedance of that portion of the line through which the fault current flows may be determined by ratioing the peak magnitudes of the quantities.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of an impedance relay associated with a transmission line embodying the invention;

FIG. **2** is a more detailed block diagram showing the relay of FIG. **1** in somewhat greater detail;

FIG. **3** is a diagram helpful in understanding the octant determination of the angles;

FIGS. **4A**, **4B** and **4C** are block diagrams showing the relay of FIGS. **1** and **2** in still greater detail;

FIGS. **5A** and **5B** are tables setting forth the operating of the AND networks of FIG. **4**;

FIGS. **6A**, **6B**, **6C**, **6D** and **6E** are abbreviated flow charts showing the flow of information through the block diagram of FIG. **4**;

FIG. **7** is a chart illustrating the logical outputs of the octant determining units;

FIG. **8** is a schematic diagram of a modified form of relay embodying the invention;

FIG. **9** is a schematic illustration of an implementation of a Four Bit AND and Buffer;

FIG. **10** is a schematic illustration of an implementation of a Four Bit AND;

FIG. **11** is a schematic illustration of an implementation of a Four Bit adder;

FIG. **12** is a schematic illustration of an implementation of a Four Bit Two's Complement Logic;

FIGS. **13A**, **13B** and **13C** are schematic illustrations of an implementation of the three Look-Up tables;

FIG. **14** is a schematic illustration of an implementation of a multiplier; and

FIG. **15** is a schematic illustration of an implementation of a divider.

DETAILED DESCRIPTION

Referring to the drawings by characters of reference, the numeral **1** indicates generally a power transmission line connected to first and second busses **2** and **4** through power circuit breakers **6** and **8** respectively. Only the protective relay **10** associated with the breaker **6** is illustrated. The relay **10** is of the class of relays known as distance relays and more specifically the class in which the relay provides a control signal which is a measure of the impedance Z of the line from the bus **2** to the fault F. If the magnitude of the impedance Z at its angle θ_Z is above a predetermined value the breaker will not be tripped even if the line is faulted. If the magnitude of Z at its angle θ_Z is less than a predetermined value, the fault is considered as being within the reach of the relay **10** and the breaker **6** will be tripped to disconnect the line **1** from the energized bus **2**.

The relay **10** is energized with voltage and current signals from the potential and current transformers **12** and **14** and as will be discussed in greater detail below to determine the magnitude of Z from the magnitude of the first and second derivatives (first and second differences) of the sinusoidal current and voltage components and the angles thereof at the instant the sinusoidal components were measured. As illustrated in FIG. **1**, the magnitude of Z is determined by multiplying the ratio of the larger voltage derivative to the larger current derivative by the ratio of the cosine of the angle of the current with respect to the cosine of the angle of the voltage. When the magnitude of Z at the angle 74_Z is below a critical value for a critical number of consecutive measurements the relay **10** trips the breaker **6**.

The voltage samples, V_{KM1}; V_K; and V_{KP1} are derived from the transformer **12** by the voltage sampling network **13**. These samples are taken at equal intervals h which do not necessarily have any relationship to the frequency of the sinusoidal voltage component. The current samples I_{KM1}; I_K; and I_{KP1} are similarly taken by the current sampling network **15** by the transformer **14**. Preferably the corresponding current and voltage samples are simultaneously taken but since the value of h is small and the samples are sequentially taken, the error will be small. For example, h may be of the magnitude $1/2\omega$ of the sinusoidal component at the nominal line frequency.

The component magnitudes are taken in the order KM1 K; and KP1 and converted into the first and

second difference quantities by the networks **16** and **18**. As will be explained in greater detail below, these quantities are simplified into voltage quantities AA and BB and into current quantities CC and DD. The sign of each of these quantities AA through DD is sequentially checked in the sign check network **20** and sign signals are delivered to the octant determining network **22** for later use in determining the true angle θ_V and θ_I of the voltage and current sinusoidal wave components.

The quantities AA through DD are sequentially delivered to the larger-smaller determining networks **24** where the positive absolute value of AA is added to the negative absolute value of BB. If the sign of the sum is positive, $|AA| > |BB|$, $|AA| = LGRV$ and $|BB|$ $SMLRV$. If the sign of the sum is negative, $|AA| < |BB|$ $|AA| = SMLRV$ and $|BB| = LGRV$. The signs of these additions are checked in network **20** and supplied to network **22** which together with the individual signs of AA and BB enable the network **22** to determine the proper octant of the angle θ_V. The magnitude of the quantities CC and DD are similarly compared by adding $+|CC|$ and $-|DD|$ to determine the SMLRI and LGRI.

The angles θ_V and θ_I are determined by the angle magnitude determining network **26** which includes an arctan look-up table for determining the first octant angle θ'_I and thereafter θ'_V under control of the AND gate sequencing network **28**. The network **28** maintains the AND gates enabled throughout the time periods as set forth in FIGS. **5A** and **5B**. The octant determining network **22** determines the addition or subtraction of θ'_I and θ'_V from 90°; 180°; 270°; and 360° so that θ'_I and θ'_V are transformed into the absolute angles θ_I and θ_V as may be seen by reference to FIG. **3**. Angle θ_Z is determined by subtracting θ_I and θ_V. If the resulting angle is negative thereafter 360° is added thereto to make θ_Z a positive quantity.

The magnitude of Z is determined in the "magnitude of Z" network **30** which is supplied with the quantities $LGRV$ and $LGRI$ from the network **24** and with the arctan values of θ'_I and θ'_V from the angle determining network **26**. The arctan values are supplied to a two-part look-up table which is programmed to provide an output value equal to (128) (Cos θ'_I)/(Cos θ'_V). The output of this look-up table L1 is then progressively multiplied by $LGRV$ and divided by $LGRI$ to provide a quantity equal to 128Z.

The angle of 128Z is supplied to the Z_{LIMIT} look-up table L3 in the Z_{LIMIT} determination network **32** which provides an output equal to $128Z_{LIMIT}$. The value of 128Z is negated and added to the value of $128Z_{LIMIT}$. If the sum ΔZ is negative, Z is greater than Z_{LIMIT} and no fault exists within the reach of the relay **10**. If the sum ΔZ is positive, the value of Z is less than the value of Z_{LIMIT} and a fault exists within the reach of the relay.

The output ΔZ is supplied to the Trip-No-Trip determining network **34**. This network integrates successive positive values of ΔZ and when the result of its integration produces a positive output signal for two successive ΔZ inputs will supply a trip signal to the breaker **6**.

The sequence control or network **28** when initially energized energizes a timer 50/0 which after a 50 ms delay enables an AND network A**108** which as will be discussed below in connection with FIG. **4** prevents the energization of the trip circuit TRIP-CRT by any false operation prior to the loading of the buffers or latches in the voltage or current samplers **13** and **15**. As will be discussed more fully below, three samples of each over the desired time interval is necessary to provide a ΔZ of the proper magnitude. After the apparatus has made the original three sequential samples, determination of ΔZ is made for each new sample of current and voltage as will be seen from the flow chart of FIG. **6**.

The following is a mathematical explanation of the operation of relay **10**. Since the peak value of the voltage and of the current is determined in the same manner, the explanation will be directed toward the voltage determination. At any instant in the voltage wave the value of the voltage v may be expressed as follows:

$$v = V_X + V_P \sin \theta V$$

Where V_p is the peak value and θ_V is the angle (0° to 360°) at the particular instant and V_X is the value of any voltage present the value of which changes at a low rate or remains constant as, for example, a D.C. component. It will be appreciated that θ_V is a time factor and may be expressed as ωt where ω equals $2\pi f$ where f = frequency in Hertz and t is time in seconds.

$$dv/dt = \omega V_P \cos \omega t \cong (V_{KP1} - V_{KM1}/2h)$$

$$\frac{d^2v}{dt^2} = -\omega^2 V_P \sin \omega t \cong \frac{(V_{KP1} - V_K)/h - (V_K - V_{KM1})/h}{h}$$

$$-\omega^2 V_P \sin \omega t \cong (V_{KP1} - 2V_K + V_{KM1}/h^2)$$

$$\sin \omega t \cong -(V_{KP1} - 2V_K + V_{KM1})\,(1/h\omega^2 V_P)$$

$$\cos \omega t \cong (V_{KP1} - I_{KM1})\,(1/2h\omega V_P)$$

$$\tan \omega t = sin\ \omega\ t/\cos\ \omega\ t = -(V_{KP1} - 2V_K + V_{KM1})/(V_{KM} - V_{KM1}) \times 2/\omega h = \tan \theta_V$$

and

$$\tan \theta_V = -BB/AA$$

where

$AA = (V_{KP1} - V_{KM1})$ and

$BB = (V_{KM1} - 2V_K + V_{KM1})\,(2/\omega\, h)$

The function of the voltage angle θ_V in the first quadrant will be defined as angle θ'_V. The value of tan θ'_V in the first quadrant will vary from 0 to ∞. However, within the first octant (0° to 45°) the value of tan θ'_V will vary from 0 to 1.000 which values are easily manipulated. In the second octant (45° to 90° the values of tan (90° $-\theta'_V$) will vary from 1.000 to 0. As will be evident from FIG. **3**, θ_V in the first octant $= \theta'_V =$ tan $^{-1}$ $(-BB/+AA)$; in the second octant $\theta_V = 90° - \theta'_V =$ 90°−tan^{-1} $(+AA/-BB)$; in the third octant $\theta_V = 90° + \theta'_V$ $= 90° +$ tan^{-1} $(-AA/-BB)$; and so on until in the eighth octant $\theta_V = 360° - \theta'_V = 360° - \theta'_V = 360°$−tan^{-1} $(+BB/+AA)$.

Summarizing the foregoing, it is observed that in each octant θ'_V is equal to tan^{-1} $(SMLRV/LGRV)$ and the magnitude of angle θ'_V is always between 0° and 45°. In the first and second octants, the sign of BB is negative and the sign of AA is positive. In the third and fourth octants, the signs of AA and of BB are both negative; in the fifth and sixth octants, the sign of AA is

negative and the sign of *BB* is positive; and in the seventh and eighth octants, the signs of *AA* and *BB* are both positive. The first, fourth, fifth and eighth octants are distinguishable from the second, third, sixth and seventh octants by the fact that in the odd numbered octants the larger *LGRV* is *AA* and the smaller *SMLRV* is *BB*. In the even numbered octants the *LGRV* is *BB* and the *SMLRV* is *AA*. The quadrants are therefore determined by the signs of *AA* and *BB* and the different octants within the quadrants are determined by the relative absolute magnitudes of *AA* and *BB*. Having determined the octant, the absolute magnitude of θ_V is obtained by adding or subtracting θ'_V to 0°, 90°, 180°, 270°, and 360° as indicated in FIG. 3.

The value of Z is the quotient of voltage and current. As may be seen in FIG. 3,

$$V_P = LGRV/\text{Cos}\theta'_V$$

and

$$I_p = LGRI/\text{Cos}\theta'_V$$

therefore

$$Z = \frac{V_P}{I_P} = \frac{\frac{LGRV}{\text{Cos }\theta'_V}}{\frac{LGRI}{\text{Cos }\theta'_I}} = \frac{LGRV}{LGRI}\frac{\text{Cos }\theta'_I}{\text{Cos }\theta'_V}$$

The values of V_P and I_P could of course be calculated and the calculated magnitudes divided. However, to minimize calculating times the relay **10** determinations of Z is done by means of a two-part look-up table in which the input quantity initially supplied thereto is the value of the arctan of θ'_I or of θ'_V. The first part of the look-up table L1 determines the portion of the second part of the look-up table L1 from which the arctan value is obtained. The second part of the look-up table provides an output quantity which is 128 times the value of the quotient of the cosines of the angle θ'_I and of the θ'_V. The constant 128 is equal to 2^7 and insures that a number greater than 1 will define the ratio with sufficient accuracy. The "looked-up" quantity equal to the quantity (128) $\text{Cos}\theta'_I/\text{Cos}\theta'_V$ is thereafter multiplied by *LGRV* and thereafter divided by *LGRI*.

It is believed that the further description of the relay **10** may best be presented by a description of the operation thereof with particular reference to the more detailed block diagrams of FIG. **4**, to the time chart of FIG. **5** and to the flow chart of FIG. **6**. The charts of FIGS. **5** and **6** are somewhat simplified to eliminate some duplication since the same AND networks beginning with AND network A7 will be rendered conducting at each *x*, $(x + 20)$ and $(x + 40)$ interval as illustrated in FIG. **5B**. In accordance with my invention I utilize each measurement of each component as the value KP1, K and KM1 at *x*, $(x+20)$, and $(x+40)$ time interval repeating each 60 intervals (FIG. **5A**).

As is more clearly illustrated in FIG. **6** the relay **10** uses 34 time intervals to completely process one set of current and voltage data to its determination of ΔZ. During this time interval, however, a second set of data is being processed so that a ΔZ determination is made each **20** intervals as indicated by FIGS. **5** and **6**. The total time for the **20** intervals is equal to time h which may, for example, be 1.3263×10^{-3} seconds. This interval with a 60 Hz wave will make this quantity $2/\omega h = 4.000$.

A complete determination of ΔZ will be described starting at an initial time interval just prior to time 0 in which the quantities V_{KM1} and V_k are in buffers B1V and B2V, respectively, and the quantities I_{KM1} and I_K are in the buffer B1I and B2I, respectively. At time 0 the AND networks A3V and A3I as well as the A/D_I and A/D_V converters are rendered conducting. Conduction of the AND network A3V and of the A to D converter A/D_V supplies the value V_{KP1} to the buffer 3V. Conduction of the AND network A3I renders the A to D converter A/D_I effective to supply the value I_{KP1} to the buffer B3I. During this same time interval O the AND network A5I and A10 are rendered conducting and the quantity I_K is supplied from the buffer B2I to both of the two input terminals of adder AD2.

During the time interval **1**, the AND network A15 is rendered conducting and the quantity $2I_K$ supplied by the adder AD2 is inverted by the twos complement TC2 into $-2I_K$ and $-2I_K$ is supplied to the buffer B5. During this same time interval **1** the AND networks A4I and A7 are rendered conducting, whereby the quantity I_{KM1} is supplied from the buffer B1I through the twos complement TC1 and AND network A13 to the buffer B6 as $-I_{KM1}$.

At the time interval **2**, the AND networks A6I and A8 are rendered conducting to supply the quantity I_{KP1} to the adder AD1 to which the buffer B6 is supplying the quantity $-I_{KM1}$. These two quantities are added together and are transmitted through the AND network A9 to the buffer B4 as $(I_{KP1} - I_{KM1})$ and is designated as the quantity CC. During this same time interval **2**, the AND networks A6I and A12 are rendered conducting and the quantity I_{KP1} is supplied from buffer B31 to one input of the adder AD3. At the same time, the quantity $-2I_K$ is supplied through the now-conducting AND network All to the other input of the adder AD3. The output quantity $(I_{KP1} - 2I_K)$ is supplied to the buffer B7 through the AND network A16.

During the time interval **3** the AND network A21 is rendered conducting whereby the quantity $(I_{KP1} - 2I_K)$ is transferred from the buffer B7 to the buffer B5.

During the time interval **6**, the AND network A4I and A12 are rendered conducting whereby the quantity I_{KM1} is transmitted from the buffer B1I to one input terminal of the adder AD3, and the AND network All also conducts to transmit the quantity $(I_{KP1} - 2I_K)$ from the buffer B5 to the other terminal of the adder AD3. The adder AD3 adds these quantities and they pass through the AND network A16 into the buffer B7 as the quantity $(I_{KP1} - 2I_K + I_{KM1})$. Also during this time interval **6**, the conducting AND network A14 conducts the quantity CC from the buffer B4 into the sign checking buffer B8A. If this quantity CC is positive, the flip-flop F1 will be actuated by the logical 0 of the sign bit of the buffer 8A to supply a logical 0 output quantity of the flip-flop F2 and a logical 1 to the AND network A25. The flip-flop F1, being supplied with a logical 0, supplies a logical 0 to the AND network A26. Therefore during the interval **7** when conducting signals are supplied to all of the AND networks A25, A26, and A27 only the AND network A25 will conduct and the quantity of $+CC$ will be transferred from the buffer B8A into the buffer B9 as $+|CC|$. If, however, the quantity *CC* is negative the sign bit **15** of sign buffer B8A supplies a logical 0 to the AND network A25 and a logical 1 to the flip-flop F1 which provides a logical 1 at its output terminal S and

to the AND networks A26 and A27 so that during the time interval 7 the quantity $-CC$ would be supplied through the conducting AND networks A26 and A27 and through the twos complement TC3 and supplied as $+|CC|$ to the buffer B9.

The logical 0's or 1's from the flip-flop F2 are supplied to each of the AND networks A17, A18, A28, A29, A30, and A30A, however, only one of these AND networks will be rendered conducting at any one time by this sequencing control (FIGS. 5A and 5B) so that only one of the flip-flops F3–F8 will be supplied with the logical 0 or 1. Therefore to simplify the explanation only the AND network and flip-flop combination effective at that time will be discussed in detail. During the time interval 6, the AND network A29 will be conducting and the logical 0 or 1, as the case may be, will be supplied to and actuate the flip-flop F6. A logical 0 will cause the flip-flop F6 to provide a logical 0 at its output and conversely. The flip-flops F1–F10 may take the form of single bit buffers as compared with the multibit buffers (see FIG. 9).

During the interval 7, the AND network A22 conducts and the quantity $(I_{KP1}-2I_K+I_{KM1})$ stored in the buffer B7 is supplied to the multiply network M1 where it is multiplied by the quantity $2/\omega h$ and the quantity $(I_{KP1}-2BK+I_{KM1})$ $(2/\omega h)$ which is designated DD is supplied to the buffer B8.

At the time interval 9, the quantity DD stored in the buffer B8 is transmitted through the now conducting AND network A23 to the buffer B8A. If the quantity DD is positive the sign output quantity is a logical 0 and flip-flip F1 is actuated to provide a logical 1 to the AND network 25 so that during the next time interval 10, the AND network A25 will conduct and the quantity $\overline{DD}$ will be transferred directly to the buffer B9 as $+|DD|$. If the quantity DD in the buffer B8A is negative, the sign output quantity of buffer B8A is a logical 1 and the flip-flop F1 provides a logical 1 to the AND networks A26 and A27 interval 10 the quantity DD will be transferred through the AND networks A26 and A27 and the twos complement TC3 into the buffer B9 as a positive quantity $+|DD|$. As discussed above with respect to the quantity CC a logical 0 or 1 is supplied to the flip-flop F2 from the sign buffer B8A. During the time interval 9, the AND network A30A will conduct to transmit the logical 0 or 1 to the flip-flop F8 which thereupon maintains at its output a logical 0 or 1 corresponding to the logical output of flip-flop F2.

During the time interval 9, the quantity $+|CC|$ which was stored in the buffer B9 transfers to the buffer B11 through the conducting AND network A36. The quantity $+|DD|$ is transferred to the buffer B9 during the interval 10.

During the time interval 12, the quantity $+|DD|$ is transferred from the buffer 9 through the twos complement TC4 and through the now-conducting AND network A35 into the buffer B10 as $-|DD|$. During this same interval 12, the AND networks A5V and A10 conduct and transmit the quantity V_K from the buffer B2V into the two inputs of the adder network AD2 from hence it is supplied to the twos complement TC2 during the time intervals 12 and 13 and the resulting quantity $-2V_K$ is transmitted through AND network A15 to the buffer B5. Also during the interval 13, the quantity V_{KM1} is transmitted through the AND networks A4V and A7 and through the twos complement TC1 and AND network A13 where it is stored in the buffer B6 as the quantity minus $-V_{KM1}$. Likewise, during the interval 13 the quantity $+|CC|$ from the buffer B11 and the quantity $-|DD|$ from the buffer B10 are transmitted through the conducting AND networks A37A and A37 to the adder AD4. The quantity $CC-DD$ from the adder AD4 flows through the conducting AND network A38 to the buffer B8A. If the quantity $|CC|$ is greater than the quantity $|DD|$, the sign buffer B8A will have a logical 0 at its S output and the flip-flops F1 and F2 will be actuated to provide logical 0's at their outputs. If, however, the quantity $|DD|$ is greater than the quantity $|CC|$, the sign buffer B8A will have a logical 1 at its outputs, which is energized by bit 15, and the flip-flops F1 and F2 will be actuated to supply logical 1 at their S outputs. At the same time the AND network A18 is energized and if the S output of flip-flop F2 is a logical 1 the flip-flop F4 will provide a logical 1 at its output indicating that the quantity $|DD|$ is LGRI and is greater than the quantity $|CC|$ which becomes SMLRI.

If the quantity CC-DD is positive then the quantity $|CC|$ in the buffer B11 becomes LGRI and logical 1's are supplied to the AND networks A40 and A42. During the time interval 14, when the AND network A44 and A46 are conductive, the LGRI quantity is transferred to the buffer B13 through the AND networks A42 and A44. If, however, the quantity $CC-DD$ is negative, then the quantity CC is SMLRI and logical 1's are supplied to the AND networks A39 and A41 so that at time 14 the quantity SMLRI is transferred to the buffer 15 through the AND networks A41 and A46. If the quantity in buffer 11 is LGRI, the quantity in buffer B9 is SMLRI and conversely. During the interval 15 the AND networks 44 and A46 will remain conductive and the quantity $|DD|$ in the buffer B9 will be transferred to the buffer B13 if it is LGRI or to buffer B15 it is is SMLRI because of the logical 0's and 1's supplied to the AND networks A39 and A40.

During the interval 14, the AND networks A6V and A8 will be conducting to transmit the quantities V_{KP1} to one terminal of the adder AD1. The buffer B6 energizes the other terminal of the adder AD1 with the quantity $-V_{KM1}$ whereby the quantity $(V_{KP1}-V_{KM1})$ will be placed in the buffer B4 through the conducting AND network A9 and is the quantity $\overline{AA}$. Further, during the time interval 14, the quantity V_{KP1} will be transmitted from the buffer B3V through the AND networks A6V and A12 to one terminal of the adder AD3. The other terminal of adder AD3 is supplied with $-2V_K$ by the buffer B5 through the AND network A11. The output quantity of the adder AD3 is supplied through the AND network A16 to the buffer B7 as the quantity $(V_{KP1}-2^{V}{}_{K})$.

During the interval 15, the quantity $(V_{VP1}-2V_K)$ is transferred from the buffer B7 through the conducting AND network A21 to the buffer B5.

The AND networks A4V and A12 conduct during time interval 16 to transmit the quantity V_{KM1} from the buffer B1V to one terminal of the adder AD3. At the same time, the AND network A11 conducts to supply the quantity $V_{KP1}-2V_K$ from the buffer B5 to the other input terminal of the adder AD3. The output quantity $(V_{KP1}-2^{V}{}_{K}+{}^{V}{}_{KM1})$ will be transmitted through the con-

ducting AND network A16 to the buffer B7. Also during the interval 16, the quantity, LGRI in the buffer B13 is transmitted through the conducting AND networks A48 and A51 to the denominator or divisor terminal of the divide network D1 and the quantity SMLRI will be transmitted from the buffer B15 through the conducting AND networks A50 and A52 to the numerator or dividend input terminal of the divider D1. The output quantity SMLRI/LGRI will be supplied to the buffer B17 through the conducting AND network A54. This quantity SMLRI/LGRI is the tangent of θ'_I. During the interval 17, the tangent θ'_I quantity is transmitted through the conducting AND network A66 to the look-up table L2 which determines the degree magnitude of the angle θ'_I in degrees and supplies it to the buffer B22.

During the same interval 17, the quantity AA is transmitted from the buffer B4 through the AND network A14 to the buffer B8A for a sign check determination as discussed with respect to the quantity CC during the time interval 6 for actuation of the flip-flop F5. Further, during the interval 17, the quantity LGRI stored in the buffer B13 is transmitted to the buffer B20 through the conducting AND network A48 and A59.

During the time interval 18, the quantity $(V_{KP1}-2V_K+V_{KM1})$ is transmitted to the multiply network M1 through the conducting AND network A22 where it is multiplied by the quantity $2/\omega h$ and deposited in the buffer B8 as the quantity $(V_{KP1}-2V_K+V_{KM1})\ (2/\omega h)$ which quantity is the quantity designated BB. If the quantity AA in the buffer B8A is a positive quantity, it will be transferred from the buffer B8A through the AND network A25 to the buffer B9 as $+|AA|$. If this quantity AA is negative, it is transferred through the AND networks A26 and A27 and through the twos complement TC3 to the buffer B9 as the positive quantity $+|AA|$.

During the time interval 16, the AND networks A20, A32, and A34 conduct to supply the logical 0's and 1's at the outputs of the flip-flops F4, F6, and F8 to the inputs of the AND networks A67–A74. Certain of the input terminals of the AND networks A67, A68, and A70–A74 are negated as indicated by the 0's at their input terminals. The output connections of the AND networks A68, A70, A71, and A73 are connected to the input terminals of an OR network OR. It will be apparent from FIG. 7 that the OR network OR will supply a logical 1 through the AND network A75 to cause the flip-flop F9 to provide a logical 1 at its output solely when the octant of angle θ' is in the even quadrants. Therefore, when during the time interval 19, the AND networks A85 and A92 are actuated by the sequence control 28, the degree magnitude of the angle θ'_I is transmitted to the buffer B27 either directly through the AND network A92 or through the AND networks A85 and A92 and the two's complement TC7 to provide a minus or plus magnitude of θ'_I depending upon the octant of θ'_I. If the OR network has a logical 1 output, the AND network A75 will be energized to cause the flip-flop F9 to place a logical 1 signal on the AND network A85 and because of the negated input a logical 0 signal on the AND network A92. This occurs if the angle θ_I is in the second, fourth, sixth or eighth octant whereby the angle θ'_I is converted to $-\theta'_I$ by the twos complement network TC7. If, however, the angle θ_I is in the first, third, fifth or seventh octant, then the OR network has logical 0 output and will transmit a signal to flip the flip-flop F9 to cause it to have a logical 0 output signal which prevents the AND network A85 from conducting and causes the AND network A92 to conduct under control of the sequencing network 28 so that the angle θ'_I is deposited as $+\theta'_I$ in the buffer B27.

During the time interval 20, the quantity BB is transmitted from the buffer B8 through the AND network A23 to the buffer B8A for a sign check. If the quantity BB is negative, the buffer B8A will cause the flip-flop F1 to have a logical 1 output at its S terminal so that during the next interval 21, the quantity BB will be transmitted through the AND network A26, the twos complement TC3 and the AND network A27 into the buffer B9 as a $+|BB|$. If, however, the quantity BB is positive, the R output of the flip-flop F1 supplies a logical 1 signal to the AND network A25 which will become conductive during the time interval 21 by the sequence network 28 quantity $+BB$ will be deposited directly in the buffer B9 as $+|BB|$. The outputs of the AND networks A67–A74 are connected to and supply logical 0 and 1 quantities to the AND networks A76–A80 so that the proper one of the AND networks A76–A80 will conduct to supply an angle magnitude signal to the buffer B23. All of the AND networks A76–A80 are supplied with signals at the same time from its sequence network 28; however, only the one thereof which is supplied with a logical 1 signal from the AND networks A67–A74 will conduct.

During the interval 21, the $\pm\theta'_I$ quantity stored in buffer B27 will be transmitted to the adder AD5 through the AND network A86. At this same time, the AND network A87 will be conducting to supply the angle quantity in the buffer B23 to the adder AD5. Therefore, depending upon the octant in which the angle of θ_I lies, adder AD5 will add to the quantity $\pm\theta'_I$ (in B27) the proper angle quantity which is in buffer B23 to devise the absolute value of the angle of θ_I which is transmitted through A82 into the buffer B25. During the interval 22, the quantity θ_I is transmitted from the buffer B25 through the twos complement TC8 and the conducting AND network 88 into the buffer B34 as $-\theta_I$ and the quantity $+|BB|$ in buffer B9 is transmitted through the twos complement TC4 and the conducting AND network A35 into buffer B10 as the quantity $-|BB|$.

During the interval 23, the quantity $-|BB|$ from the buffer B10 and the quantity $+|AA|$ from the buffer B11 are supplied to the adder AD4 through the AND networks A37 and A37A and the total AA–BB is supplied through the AND network A38 to the buffer B8A which checks the sign to determine which is the larger, the quantity $|AA|$ or the quantity $|BB|$. If the quantity $|AA|$ is larger, a plus quantity will be in buffer B8A and the flip-flops F1 and F2 will have logical 0 output signals at their S output terminals. If, however, the quantity $|BB|$ is larger than the quantity $|AA|$, the quantity in the buffer B8A will be negative and the flip-flops F1 and F2 will have logical 1 output signals at their S output terminals. As discussed above, the sequence network 28 will render the AND network A17 conductive to supply this logical 1 signal to flip-flop F3. If $|AA|$ is greater than $|BB|$ and consequently the LGRV then AND networks A42 and A43 are con-

ductive (time interval 24) and this signal is transmitted into the buffer B12. If, however, $|BB|$ is larger than $|AA|$, then $|AA|$, is SMLRV and the AND networks A41 and A45 will be conducting and SMLRV will be deposited in the buffer B14.

During the interval 25, the quantity $|BB|$ in buffer B9 will be transmitted to one of the buffers B12 and B14. If the quantity $|BB|$ is SMLRV then the AND networks A40 and A45 will be rendered conducting and it will go into the buffer B14. If, however, the quantity $|BB|$ is greater than the quantity $|AA|$ then it is LGRV and the networks A39 and A43 will be rendered conducting and the quantity LGRV will be deposited in the buffer 12.

During the interval 26, the quantity LGRV from the buffer B12 is transmitted to the denominator or divisor terminal D of the divide network D1 through the conducting AND circuits A47 and A51 and the quantity SMLRV is transmitted from the buffer B14 to the numerator or dividend terminal N of the divide network D1 through the now-conducting AND networks A49 and A52. The output quantity SMLRV/LGRV of the divide network D1 then flows into the buffer B16 through the conducting AND network A53.

During the interval 27, the quantity SMLRV/LGRV, which is the tangent of θ'_V, is transmitted to the two-part look-up table L1 through the conducting AND network A55. The magnitude of the tangent of θ'_V selects a circuit through which the tangent of θ'_I quantity SMLRI/LGRI from the buffer B17 will flow into the second part of the look-up table L1 through the AND network A56. The output of the second part of the two-part look-up table L1 supplies an output quantity (128) $(\text{Cos}\theta'_I\theta'_V)$ to the buffer B18.

During this same interval 27, the quantity SMLRV/LGRV in B16 which is equal to the tangent of the angle θ'_V is supplied through the AND network A65 to the look-up table L2. The output of table L2 is a quantity equal to the magnitude of the angle θ'_V and is stored in buffer B22.

The octant of the angle θ_V is determined by the AND networks A67–A74 under control of the flip-flops F3, F5, and F7 which flip-flops control the AND networks A67–A74 in the manner described in connection with the octant determination of θ_I above. If angle θ_V is in the first, third, fifth, or seventh octant, the output signal of OR will be a logical 0 and the output of flip-flop F9 will be a logical 0, so that the magnitude of the angle θ'_V will be deposited in the buffer B27 as $+\theta'_V$. If the angle is in the second, fourth, sixth, or eighth octant, a logical 1 signal will be supplied by the OR network and a logical 1 signal will be supplied by the flip-flop F9 to the AND networks A85 and A92 whereby the quantity $-\theta'_V$ is stored in the buffer B27.

During the time interval 28 the quantity (128) (Cos θ'_I)/(Cos θ'_V) from the buffer B18 and the quantity LGRV from the buffer B12 are supplied to the input of the multiplier M2 through the conducting AND networks A58, A47 and A57 as absolute numbers. The product output of the multiplier M2 is supplied as a 32 bit number to the 32 bit latch or buffer B19.

During the time interval 29, the 16 bit quantity LGRI stored in the buffer B20 is transmitted to the denominator input D of the dividing network D2, through the conducting AND network A64 and the 32 bit quantity (128) $(\text{Cos}\theta'_I)$ (LGRV)/$\text{COS}\theta'_V$ stored in the buffer B19 is transmitted to the numerator terminal N of the dividing network D2 through the 32 bit AND network A63. The resulting output of network D2 is a 16 bit quantity [(128) $(\text{Cos}\theta'_I)$ (LGRV)/$\text{Cos}\theta'_V$LGRI], equal to the quantity Z and is deposited in the buffer B21. As will be discussed more fully in connection with FIG. 15, the divider D2 includes an overflow indicator whereby the quantity supplied to buffer B21 will be a maximum positive 15 bit quantity should the quotient be a quantity which cannot be expressed in 15 bits.

During the time interval 30, the quantity in buffer B27 which is either $-\theta'_V$ of $+\theta'_V$, depending upon the octant of θ_V is supplied to one terminal of the adder AD5 through the AND network A86 and the angle quantity stored in the buffer B23 is supplied to the other terminal of the adder AD5 through the AND network A87. The output of AD5 is the magnitude of the angle θ_V and flows to buffer B24 through the AND network A81. Also, during the time interval 30, the quantity Z in the buffer B21 flows through the conducting AND network A95 and the twos complement network TC9 and to the buffer B30 as the quantity $-Z$.

During the interval 31, the quantity θ_V from the buffer B24 and the quantity $-\theta_I$ from the buffer B34 is supplied to the adder AD6. The sum quantity $(\theta_V-\theta_I)$ passes through the conducting AND network A93 into the buffer B29 and is equal to angle θ_Z the impedance angle. The magnitude of angle θ_Z is supplied to the sign checking buffer B8A through the AND network A94. If the magnitude of this quantity is negative the flip-flop F1 and F2 will be actuated to render the AND circuit 84 conducting whereby the quantity 360 is supplied to one terminal of the adder AD7. During the time interval 32, the AND network A83 conducts and transmits the magnitude of the angle θ_V to the other terminal of the AD7. The output quantity of the adder AD7 is the value of $+\theta_Z$ which is transmitted to the buffer B28 through the AND network A89.

During the time interval 33, the AND network A97 is rendered conducting to supply the magnitude $+\theta_Z$ to the look-up table L3. The output of the table L3 is the lower limit of the magnitude of Z (Z_{LIMIT}) and is stored in the buffer B31. Z_{LIMIT} is the minimum limit of Z which does not represent a fault within the reach of the relay 10.

During the time interval 34, the AND networks A98 and A96 are rendered conducting to supply the $+Z_{LIMIT}$ quantity from the buffer B31 and the $-Z$ quantity from buffer 30 to the adder AD8. The sum thereof ($+Z_{LIMIT}-$ Z) is supplied through the AND network A99 to the buffer B32 as ΔZ.

If the magnitude of ΔZ is a negative quantity no fault exists within the reach of the relay 10. Conversely, if the magnitude of ΔZ is positive, a fault should exist within the reach of the relay 10. In order to insure the maximum security of the line and not deenergize the line falsely, the first ΔZ which indicates a fault within the reach of the relay 10 will not trip the breaker. To trip, there must be at least two consecutive ΔZ trip signals. Since these ΔZ quantities are supplied each $\frac{1}{2}\omega$ seconds or every 1.3263×10^3 seconds, the use of two successive fault signals will not cause excessive damage to the line even with a close in fault and a stiff bus supply.

In accordance with my invention, I provide a Trip-No-Trip determining network **34** which requires an increasing number of ΔZ trip signals as the location of the fault approaches the reach limit of the relay **10**. The operation of the network **34** will first be described assuming a no-fault line condition in which the ΔZ's are negative or at the most only an occasional positive ΔZ which may be caused by transients or otherwise. The first ΔZ, which is provided as described, will be transmitted by the AND network **A100** to the one input terminal of the adder AD9 during the time interval **35** and will be assumed to be of a magnitude equal to −30. At the same time interval, the quantity in the buffer B33 (assumed to be −200) will be transmitted through the AND network **A101** to the other input terminal of the adder AD9.

Thereafter, during the time interval **36**, the output quantity of the adder AD9 (−230) will be transmitted to the buffer B33 through the AND network **A102**. During the time interval **37**, the −230 quantity is supplied to one terminal of the adder **AD10**. When a negative sign is supplied to the flip-flop **F10** through the AND network **A104** it provides a "clear" signal to the counter CTR which, if it had been energized to a count, will be returned to 0. The −230 quantity supplied to the adder **AD10** will be added to the Z bias signal which has the magnitude +200. The resultant sum output of the adder **AD10** will be negative (−30), and when AND network **A105** conducts the negative sign, will be supplied to the flip-flop **F11**. With a positive input sign, the flip-flop **F11** supplies a logical 0 signal to the AND network **A106**. Conversely with a negative input supplier to the flip-flop **F11** a logical 1 signal is transmitted to the enable input of the AND network **A106**. This logical 1 signal causes the AND network **A106** (internal **38**) to supply a quantity −200 from the −Z bias to reset buffer **B33** to a −200 quantity. This resetting of buffer **B33** occurs each time the quantity supplied thereto from the adder AD9 is greater than −200.

It will be appreciated from the foregoing that whenever a series of +ΔZ signals is supplied, the quantity stored in buffer **B33** will become less and less negative at a rate depending upon the magnitude of these + signals. Since the flip-flop **F11** resets the buffer **B33** only when its quantity decreases below −200, the + quantities will eventually put a + quantity in the buffer **B33**. When this occurs, the next time in which AND network **A104** conducts it will place a + input sign on the input of flip-flop **F10**. This causes the flip-flop **F10** to transmit a count signal to the counter CTR. If thereafter a second + signal is transmitted by the adder AD9 the subsequent conduction of the AND networks **A102** and **A104** will supply a + sign to and actuate the flip-flop **F10** to supply a second signal to the count input CT of the counter CTR. The counter CTR at a second count signal will actuate the trip circuit of the breaker.

It will be appreciated that a close-in fault will cause ΔZ to be a positive quantity approaching Z_{LIMIT} and if such quantity is +201 or greater the counter CTR will actuate the trip circuit at the second ΔZ output. If, however, the fault is closer to the reach or decision making point, the value of + ΔZ will be less and a greater number of ΔZ signals will be required to overcome the −200 quantity which is initially stored in the buffer **B33**. This permits a longer decision making period which is permissible because the fault current will be less at the more remote fault location. An initial −200 quantity can be stored in buffer **B33** by closing the manually operable switch **MS1** to render AND network **A107** conducting. This will prevent any false tripping due to an uncontrolled + quantity in buffer **B33**.

It will be appreciated that if desired the elements of FIG. **4** may be combined and reduced in number. As for example, a single adder, a single multiply network, a single divide network, and a single analog to digital sampler with a plurality of buffer or storage networks which hold the various quantities and provide these quantities to the networks which manipulate them could be used. Such an apparatus could be a general purpose digital computer such as the Prodac-2000 computer sold by Westinghouse Electric Corporation which may be programmed to manipulate the quantities V_{KP1}; V_K; V_{KM1}; I_{KP1}; I_K; and I_{KM1} into the quantities Z, θ_Z, and ΔZ and finally into the decision made output quantity for the trip circuit.

In the form of the invention illustrated in FIG. **8**, analog quantities derived by differentiating the analog current and voltage quantities are utilized. The current in line **100** is sampled by the current transformer **102** and the quantity is filtered in the low pass filter **104** and is supplied as the quantity $(I_X + I_P \sin\omega t)$ to the differentiating and multiplying network **106**. The filter effectively removes any high frequency in the output of the transformer **102**, however, any low of change transient passes through as the quantity I_X. The network **106** includes an operational amplifier **108** having a feedback resistor R_I and an input capacitor C_I and provides an output quantity $-R_1C_1\ (di/dt)$. The values of R_1 and C_1 are chosen to equal $1/\omega$ whereby the output quantity of network **106** equals the quantity $-I_P \cos \omega t$.

This quantity is supplied to a second differentiating and multiplying network **110** wherein the values of R_2 and C_2 are chosen to equal $1/\omega$ whereby the output quantity of network **110** will equal $I_P \sin\omega t$. The quantity $-I_P \cos \omega t$ is supplied to both input terminals of a first multiplier network **112** so that it is effectively squared and becomes $(I_P)^2(\cos^2\omega t)$. Similarly the quantity $(-I_P \sin \omega t)$ is squared by the second multiplier network **114** and becomes $(I_P)^2(\sin^2 \omega t)$. Any suitable analog multiplying network may be used such as the multiplier sold by Intronics Incorporated and designated model **M420**.

The quantities I_P^2 $(\cos^2 \omega t$ and $I_P^2 \sin^2 \omega t)$ are supplied to the two input terminals of an operational amplifier summing network **116** which provides the quantity I_P^2 $(\cos^2\omega t + \sin^2\omega t)$. Since $\cos^2\omega t + \sin^2\omega t$ equals unity the output quantity of network becomes I_P^2.

Similarly as described, the bus or line voltage is sampled by the potential transformer **118** passes AND through the low pass filter **120** so that the quantity $(V_X+V_P \sin \omega t)$ is supplied to the differentiating and multiplying network **122**. This network, like the network **106**, is adjusted to provide a multiplication factor of $1/\omega$ and its output quantity becomes $(-V_P\cos \omega t)$ and is supplied to the differentiating and multiplying network **124**. The network **124** like the network **110** is

adjusted to provide the multiplication factor of $1/\omega$ whereby its output becomes $(+V_P \sin \omega t)$. The quantities $(-V_P \cos \omega t)$ and $(+V_P \sin \omega t)$ are squared by the multipliers **126** and **128** and the squared quantities are added together by the adder **130** to provide the quantity V_P.

The quantities I^2_P and V^2_P are supplied to the denominator and numerator terminals, respectively, of the dividing network **132** to provide an output quantity Z^2. The dividing network **132** may take any of various forms, as for example, the analog divider sold by Intronics Incorporated as model **D401**. The output quantity Z^2 actuates a timer **134** through a NOT network **136** and a zener diode **138**. The network **136** and timer **134** may be similar to the NOT network **68** and timer **62** of Altfather U.S. Pat. No. 3,443,159, dated May 6, 1969 with a time interval of 4/0 milliseconds. The zener diode interrupts the logical 1 signal and supplies a logical 0 signal to the NOT network **136** when the value of Z is less than the critical reach value or Z_{LIMIT} representing the maximum reach of the relay. Therefore, when the value of Z becomes less than Z_{LIMIT} the zener diode **136** supplies an 0 logical signal to network **136** which initiates the 4 millisecond timing of the timer **134**. If the value of Z remains less for the complete 4 ms timing of timer **134**, the timer actuates the trip network **140**. If the value of Z does not remain less than Z_{LIMIT}, then the NOT network **136** resets the timer without intended delay as indicated by the designation 4/0.

FIG. 4 is a block diagram showing AND networks having the prefix A, buffer or storage networks having the prefix B, adder networks having the prefix AD, multiplying networks having the prefix M, dividing networks having the prefix D, twos complement networks having the prefix TC and look-up tables having the prefix L. For purposes of simplicity, single lines interconnect these blocks as if single bit numbers are used. In reality multiple bit numbers are used in the handling of quantities. The number of bits is not important beyond the necessity of having a sufficient number to determine the quantities with a reasonable degree of accuracy. For example, 16 bit quantities may be used except where discussed as being otherwise.

By having the number of bits equal to an even multiple of **4**, standard chips may be utilized to make up the blocks. In some instances the AND network controlling the input to a buffer may be combined with the buffer into a single chip. As for example, the AND network A1V and buffer B1V may take the form of four "Four Bit AND and Latch" chips, as for example, the Texas Instrument chips SN 74175 (see FIG. **9**). Similarly the AND networks which follow a latch or buffer such as network A4V following a latch or buffer B1V may comprise four chips such as Texas Instrument chips SN 7409 (see FIG. **10**). Chips SN **7409** may also be used for AND networks A7, A8, A22, among others. The buffer networks supplied from two or more AND networks may take the form of the combined AND and latch of FIG. **9**. However, in this instance the load latch signal is applied to the combination after the AND gate is opened to permit the new quantity to be supplied thereto and latched in the combination AND and latch.

The adders AD may take the form of four chips such as the Texas Instrument chips SN **7483** (FIG. **11**) wherein the **16A** inputs are connected to receive the 16 output bits of one of the amounts to be added and the **16B** inputs are connected to receive the 16 output bits of the other of the amounts to be added. A logical 0 is supplied to the **C0** input of the chip having the least significant number supplied thereto. The **C4** output of the first chip is supplied to the **C0** input of the second chip, etc.

The twos complement TC may, for example, take the form of four Texas Instrument chips SN **7483** as used in the adder (FIG. **11**) and four chips Texas Instrument SN **7403** (FIG. **12**). The A rather than the A signals are supplied by the chip SN **7403** to the A inputs of the chips SN **7483**. The chips have their input **B1**, **B2**, **B3**, and **B4** supplied with logical 0 signals. A logical 1 signal is supplied the **C0** terminal of the chip having the least significant four bits supplied thereto. The second chip which is supplied with the second least significant four bits has its least significant bit input **C0** connected to the **C4** terminal of the first chip. The remaining third and fourth chips SN **7483** are similarly connected together and to the second chip.

The look-up networks or tables **L1**, **L2**, and **L3** may take the form as illustrated in FIGS. **13A**, **13B**, and **13C**, respectively. The look-up table **L1** (FIG. **13A**) comprises a plural number of decode and memory cells such as the Texas Instrument SN **54/7488** chips. Assuming an eight bit output, 17 SN **54/7488** chips **501–517** will be used to provide an eight bit output which will provide a satisfactory accuracy for lookup table **L1** without necessitating the use of an undue number of chips. The look-up table **L1** is of the two part type which provides 289 addresses. The five binary select input terminals A, B, C, D, and E, respectively, of the chips **510–517** are connected in parallel with each other and selectively to the five least significant bits of the 16 bit output of the buffer **B16** through AND **A55**.

The least significant five of the 16 bit output of buffer **B17**, namely bits $\bar{A}_0$–$\bar{A}_4$ and their complements A_0–A_4 are connected to the five input circuits **1, 2, 3, 4,** and **5** of the memory enable circuits of the chips **501–517**. The complement or bar signals $\bar{A}_3$ and $\bar{A}_4$ of the two most significant of the five utilized bits of buffer **B17** are connected to the input lead **4** of the chips **510–508** and **517** and to the lead five of the chips **501–516**. The status or real signals of the least significant bit of the two most significant bits used A_3 is connected to the enable circuits **4** of the **509–516** chips. The status or real signal of the most significant of the two most significant bits used A_4 is connected to the memory enable circuit **5** of the **517** chip. The memory enable circuit **1** the chips **501, 503, 505, 507, 509, 511, 513, 515,** and **517** are connected to the complement signal $\bar{A}_0$, while the memory enable circuit **1** of the chips **502, 504, 506, 508, 510, 512, 514,** and **516** are connected to the status signal A_0 of the least significant of the five used bits of the buffer **B17**. The memory enable circuit **1** of the chips **501, 502, 505, 506, 509, 510, 513, 514,** and **517** are connected to the complement or bar signal $\bar{A}_1$, while the chips **503, 504, 507, 508, 511, 512, 515** and **516** are connected to the status signals A_1 of the second least significant of the five used bits of buffer **B17**. The memory enable circuits of the chips **501–504, 509–512 & 517** are connected to the

complement or bar signal $\bar{A}_2$ while the chips **505–508** and **513–516** are connected to the status signals A_2 of the third least significant bit of the five used bits of the buffer **B17**. Each of the respective eight outputs F-M of the chips **501–517** are individually connected together to provide an eight bit output to the buffer **B18** which is equal to (128) $Cos\theta'_I/Cos\theta'_V$.

The look-up table **L2**, (FIG. **13B**) is a 17 place table and consequently needs no more than a **5** bit address with a six bit output and as such may utilize a single chip (SN **54/7488**) rather than the plural chips used for the table **L1**. The five bit address which comprises the five least significant output bits of the one of the buffers **B16** or **B17** which happens to be connected thereto by the AND networks **A65** or **A66**. A logical 0 is applied to the memory enable. The output bits will be supplied by the outputs **1–6**.

The look-up table **L3** (FIG. **13C**) is a 361 place table. An address of **8** bits is supplied thereto from buffer **B28** and an eight bit output is provided thereby to buffer **B31**. This table **L3** comprises six chips **520–521** (SN **54/7488**). The like numbered output connections F–M of each chip are respectively connected together as are the binary select connections A–E. These connections A–E are connected respectively to the least significant five bits of the eight bit address with connection A connected to the least and connection E connected to the most significant of the five least significant bits. The status and complement signals of the three most significant bits of the eight bit address are connected to three memory enable circuits **1**, **2**, and **3** of the memory enable in the manner set forth with respect to enable circuits **1–3** of FIG. **13A**.

The analog to digital converter A/D_I and A/D_V are alike and, for example, may be the multiplier digitizer sold by Xerox Data System as type MD 41 and described in their publication No. 901254c, dated July 15, 1968. This device will digitize a ±10 volt input signal to a 15 bit quantity, of which the upper 14 bits are used. The most significant or sign bit **14** is strapped to the top three bits of the current and voltage magnitude storage buffers through the AND's A_1–A_3 in an extended manner so that the most significant bit **15** of the 16 bit signal will be the sign bit. The input signal for the A/D_I is derived from a current transformer through a low pass filter while the input signal for the A/D_V is derived from a potential transformer through a second low pass filter. The converters are each pulsed to digitize the voltage and current signals at time intervals **0**, **20**, and **40**, and multiples thereof by the sequence control **28**.

The flip-flops or flags **F3–F9** are single bit devices and may take any of various forms. They should be devices which will be actuated to provide a logical 1 or 0 output signal in response to the application thereto of a logical 1 or 0 signal at the time a triggering pulse is applied to the respective input controlling AND network associated therewith and to maintain the logical signal until reset by the application of a subsequent triggering pulse. If desired, one of the bit circuits and the latch signal of the chip of FIG. **9** could be utilized. In such event the latch signal input would be energized during the interval that the respective input AND network is enabled to energize the respective flag network. In the case of the flags **F3–F9** the input ANDs could be eliminated and the flags controlled by a trigger signal from the sequence control subsequent to the time that the flag input signal is present (during the interval that the respective input AND is rendered conducting).

Buffer **8A** is similar to the buffer or latch illustrated in FIG. **9**. Its sign checking function is obtained by connecting the input terminal of flip-flop **F1** to the most significant bit **15** of the buffer **B8A**, which is utilized as the sign bit. When the bit **15** is a logical 1 the flip-flop **F1** is set to place a logical 1 at its set output terminal S indicating a negative sign of the quantity in buffer **B8A** and conversely the flip-flop **F1** will be reset to place a logical 1 at its R output when the bit **15** is a logical 0 indicating a positive number in buffer **B8A**.

It will be apparent from FIG. **4** that a positive quantity in buffer **B8A** will result in a first enabling logical 1 signal from flip-flop **F1** into AND **A25** and a disabling logical 0 signal into AND **A26**. Therefore the positive quantity is transferred to buffer **B9** through AND **A25** upon the application of the trigger signal from the sequencing control **28**. Conversely, a negative quantity in buffer **B8A** causes a first enabling logical 1 signal to be applied to ANDs **A26** and **A27**, whereby the negative quantity is transferred into the buffer **B9** as a positive quantity. It will be appreciated that a logical 1 signal can be applied to the flip-flops **F3–F8** only if a negative quantity is in the buffer **B8A** at the time the proper AND network is rendered conducting by the sequencing control **28**.

The flip-flop **F9** is similarly controlled by the OR network OR which supplied a logical 1 signal when a logical 1 signal is supplied to any of its input connections from the AND networks **A68**, **A70**, **A71**, and **A73**. The logical 1, so supplied, causes flip-flop **F9** to supply a logical 1 signal to be supplied to the AND network **A85**, **A81**, and **A92**. Since the AND network **A92** has a NOT input the logical 1 output of **F9** disables the AND **A92** and provides a first enabling signal to the ANDs **A85** and **A91**. Conversely, a logical 0 from flip-flop **F9** disables **A85** and **A91** and provides a first enabling signal to AND **A92**.

The AND network **A104** and flip-flop **F10** combination may take the form described above in connection with the **F3–F8** networks except that a second or complement signal is utilized and which may be derived by the use of a NOT output terminal. The input of **A104** is supplied from the sign bit or 15th bit of the signal in buffer **B33**. The AND network **A105** and flip-flop **F11** combination is likewise similar and its logical 1 output supplies a first enabling signal to the AND network **A106**. The output bit **15** of adder **AD10** which is energized by the sign bit is negated so that when the bit **15** indicates a negative sum quantity it supplies a logical 1 to the **A105–F11** combination to cause a logical 1 enabling quantity to be supplied to the AND network **A106** so that the network **A106** will transmit a −200 quantity to the buffer under control of the sequencing control **28** as described above.

FIG. **14** shows schematically one form of multiplying network **300** which may be used for the multipliers **M1** and **M2**. One of the quantities, which is designated as the multiplier in FIG. **14**, is supplied as a 16 bit quantity by the conductor means **300A** to the shift register **301**. The shift register may, for example, be a Texas Instrument SN **74195** device. The other quantity, which is

designated the multiplicand, is supplied as a 16 bit quantity by the conductor means **302** to the adder **303** which, for example, may be a Texas Instrument SN **7483** device. At the proper time interval (see FIG. **5B**) the sequence control **28** opens the proper ANDs and the quantities to be multiplied are supplied to the multiplying network. At this same time, the sequence control **28** supplies an initiating pulse to the pulse timer **304** through the lead **306**. When initiated, the timer **304** supplies a reset pulse RE to the reset input of shift register **308** and a pulse L to the loading input terminal **314** of register **301**. After the short time interval required to load the quantities, the timer **304** provides an N number square wave spaced main pulses as there are bits in the quantities which in this instance is 16. These N main pulses sequence the N operations required to multiply the input quantities after which the timer **304** will reset itself for its next operation.

Each N main pulse comprises two sequentially occurring pulses ϕ_A and ϕ_B. Assuming the timer **304** has been initiated and the initial loading pulse has been supplied to the N bit multiplier register **301** and the multiplier loaded therein and the resulting pulse RE has been applied to and has reset the 2N bit register **308**, the next ϕ_A pulse will enable the AND **310**. If the LSB bit in register **301** at output terminal **316** is a 1, the AND **310** will conduct and enable the AND **318** to load the N bit sum from adder **303** into the N most significant bits of the register **308**. Since initially the bits in register **308** are all 0's, this N bit sum will be the N bit multiplicand which in the case of **M1** is derived from buffer **B7** and which in the case of **M2** is derived from buffer **B18**. If the LSB at terminal **316** is a logical 0 the sum from the adder **303** will not be loaded into the register **308**.

After the ϕ_A logical 1 pulse is terminated, a logical 1 ϕ_B pulse will occur which is applied to the shift input terminal **312** of register **308** and the shift input terminal **320** of the register **301**. This shifts the least significant bit LSB of the N most significant bits in the register **308** into the most significant of the N least significant bits. The shift in register **301** connects the next least significant bit of the multiplier to the LSB terminal **316** and the operation described is repeated N times, whereby the product will appear in the register **308**.

In the case of multiplier **M2** the desired product loaded into buffer **B19** should be equal to 16 times the actual product of the multiplicand and multiplier supplied thereto. For this purpose the 16 bits loaded into the buffer are bits **5–21** (**4–20** if the least significant bit is numbered 0). The product of **M2** will always be positive because absolute or positive values are supplied as both the multiplicand and multiplier.

In the case of **M1** the product will be plus or minus, depending upon the sign of the quantity in buffer **B7**. The most significant bit is utilized on the sign bit and if a logical 0, the quantity is positive and if a logical 1, the quantity is negative. The sign bits of the multiplicand and multiplier are supplied to the two input terminals of an exclusive OR **322**. The output terminal **324** of OR **322** is supplied to the NOT input **326** of AND **328** and to the real input **330** of AND **332**. If the sign of each the multiplicand and multiplier is the same, a logical 0 signal is supplied by the OR **322** and the AND **328** is effective to transmit the N bit product in the register **308** as a positive number through the output conductors **334** to buffer **B8A**. If the signs of multiplicand and multiplier are different, the OR provides a logical 1 and the negative product in the register is transmitted through a twos complement **336** (see FIG. **13**), the AND **332**, and conductors **334** to the buffer **B8A**.

FIG. **15** shows schematically one form of dividing network **400** which may be used for the dividers **D1** and **D2**. The numerator or dividend input will provide 2N or **32** bits. The least significant bits of the dividend are supplied to the 16 bit parallel input **401** of the shift register **402** which may for example be of the Texas Instrument type (SN **74195**). The 16 most significant bits of the dividend are supplied to the **16** bit parallel input **403** of the shift register **404**. The divisor is a 16 bit quantity and is supplied to one parallel input **406** of the parallel adder **408** through a twos complement **409**. The twos complement may take the form illustrated in FIG. **12**, wherein the adder may take the form illustrated in FIG. **11**.

The most significant bits MSB from the registers **402** and **404** are serially supplied to the least significant bit LSB serial input **410** of the shift register **411**. The 16 bit quantity in the register **411** is supplied to the other parallel input **415** of the adder **408**. The 16 bit output sum from the 16 bit output **417** of the adder **408** is connected to the parallel input **412** of the register **411**, and the output sum may be loaded in the register **411** when a logical 1 signal is supplied to the loading control input **424**.

The most significant bit MSB in the adder output (bit **15** in the instant case of a 16 bit number) is supplied to the output terminal **416** which is connected to the input terminal of an AND circuit **418**. The sign of this bit is tested each ϕ_B pulse and for this purpose the MSB of **408** is supplied through an AND **418** to one input terminal **420** of an AND circuit **422** having its output terminal **423** connected to the parallel loading control terminal **424** of the register **411**. When ϕ_B pulse, to be described in greater detail below, is supplied to the second input terminal **426** of AND **422**, a logical 1 signal is supplied to terminal **424** when the sign of this most significant bit MSB, then at the terminal **416**, is a logical 0 (indicating a plus quantity at output **417**). However, if the sign of MSB is a logical 1 indicating a negative quantity the quantity will not be inserted in the register **411**.

An AND **418** is also connected to the last significant bit LSB serial input terminal **427** of an output shift register **428**. The series of MSB's as they appear at each ϕ_C pulse are sequentially placed in the output register **428**.

The dividend registers will accept a 32 bit input and the divisor register will accept a 16 bit input. Since the desired quotient quantity is a 16 bit quantity, the significant bits supplied to the output register may conceivably be more than 16 resulting in an overflow condition and a meaningless output. In the case of divider **D1** this is not a problem since the dividend or numerator input quantity is always less than 16 times the divisor or denominator quantity and the output quotient will never exceed the **16** bit divisor and the 16 bit capacity of the output register **428**.

In the case of the divider **D2**, however, the input dividend quantity may contain as many as **22** bits while

the input divisor quantity may contain no more than eight bits. This situation, as for example, could occur with full line voltage and low line current. When this occurs, the quotient will be a quantity exceeding 16 bits. When more than 16 bits are serially placed in the register **428**, its 16 bit output quantity is meaningless. For example, suppose the quotient output was a 17 bit quantity in which the most significant bit MSB was a logical 1 followed by 16 logical 0 bits. This would indicate a quotient equal to zero and not an exceptionally large quantity and in the apparatus of FIG. **4** a magnitude of Z less than rather than greater than Z_{LIMIT}.

In order to prevent such a result from an overflow, the divider is provided with an overflow indicator which when an overflow occurs provides at its output, not the quotient, but the maximum possible 16 bit number. In the case of the output quantity Z of the divider D2, it is not necessary to know its exact magnitude; it being satisfactory to know that it is at least the maximum quantity which may be represented by 16 bits which indicates a value of Z in excess of Z_{LIMIT} and no line fault within the reach of the relay. Of course, if such a maximum value would not be satisfactory, the overflow indicator or designator could be arranged to have the output completely ignored.

More specifically, the overflow designator comprises an AND network **432** having three input connections. One of these connections is connected to the "carry output" terminal **433** of the adder **408**, a second is connected to receive the ϕ_B pulses, and the third is connected to receive the ϕ_1—$\phi_{(2N-N)}$ output pulses of a pulse timer **446**. The NOT output terminal **434** of the AND **432** is connected to the operate input terminal **435** of a flip-flop network **436**. The output terminal **435A** of network **436** is connected to the enable input terminal **437** of an AND **438** and to the enable NOT input terminal **439** of an AND **440**. When logical 1 signals are supplied to all of the input connections of AND **432**, a logical 1 signal is supplied to the enable input terminal **436** of AND network **438** and to the enable NOT input terminal **439** of an AND network **440**. The 16 bit output terminals of both ANDs **438** and **440** are connected to the conductors **442** and thereby to the 16 bit input terminals of the buffer **B21**. The 16 bit output of the register **428** is connected to the conductors **442** through the AND **440** and its 16 bit quantity will be supplied to the buffer **B21** at all times when a logical 0 signal is supplied to the enable Not input **439** of AND **440**. In the event the overflow designator AND **432** provides a logical 1 to the input **435**, the flip-flop **436** will flip to provide a logical 1 to the enable input **437** and the enable NOT input whereby the 16 bit circuit through the AND **440** will be interrupted and the AND **438** will be enabled to transmit the maximum 16 bit number from the 16 bit maximum number source **444** through **442** to buffer **B21**.

The operation of the dividing network **400** is initiated by a pulse supplied from the sequence control **28** through conductor **445** to the pulse timer **446** and to the proper ANDs effective to load input bits as indicated in FIG. **4** and at the time intervals indicated in FIG. **5B**. The pulse timer **446**, when initiated, first supplies a resetting pulse RS for transmission to the reset inputs of the registers **411** and **428** and flip-flop **436**, and a loading pulse L to the parallel loading of control terminals of the registers **402** and **404** and to the enable input **409E** of the twos complement **409**. A short time later, which time is sufficient for the bit input signals to be loaded, the pulse timer deenergizes the outputs RS and L and provides a 2N number of sequential square pulses ϕ. During the existence of each pulse the timer **446** provides an ϕ_A, an ϕ_B, and an ϕ_C pulse. The ϕ_A pulses are transmitted to the shift inputs of the registers **404** and **411**, the ϕ_B pulses are transmitted to the ANDs **422** and **432**, and the ϕ_C pulses are transmitted to the shift input **432A** of register **428**. The pulse timer **446** is provided with 2N output terminals for the ϕ pulses as indicated by the designation ϕ_1—ϕ_{2N}. The terminals ϕ_1—$\phi_{(2N-N)}$ are connected together and to the AND **432**.

If during the initial portion of the dividing process, ϕ_1—$\phi_{(2N-N)}$ operations, a logical 1 bit appears at terminal **433** which indicates an zero bit at output **416** it would constitute a significant bit which would be completely shifted out of the register **428** before the end of a dividing step and would render the 16 bit output at the register **428** meaningless. Because only the ϕ_1—$\phi_{(2N-N)}$ pulses are supplied to the AND **432**, only the logical 1 pulses at **433** are effective to actuate the overflow designator. The subsequent logical 1 pulses at **433** which occur each time a MSB at **416** is 0 will not be effective to actuate the overflow designator and the quantity in the register **428** will be the true quotient.

In the case of the divider D1, the output quantity is desired to be 16 times the actual value of the quotient of the quantities supplied thereto. This is accomplished by connecting the 16 bit input signal to input bits **4–19** of the dividend registers **402–404**. The **0–3** bits of register **402** are not used. The **20–31** bits of the register **404** are strapped to bit 19 to provide logical 0 signals thereto. This is possible since only positive quantities are used in D1 as well as D2. The OR network **435** of D1 will be supplied with ϕ_{13} pulses. However, because of the relative values of the input quantities to D1, no overflow is expected and the overflow designator of D1 could be dispensed with. If it is used, the OR network **436** is supplied with the ϕ_1—ϕ_{12} pulses. However, in the case of D1, the maximum number is not to be inserted and the AND **438** and maximum number device **444** should be omitted.

What is claimed and is desired to be secured by United States Letters Patent is as follows:

1. Apparatus of the character comprising, first input terminals adapted to be energized by a first pulsating electrical quantity which has a first sine wave component having a angular frequency ω, mathematical circuitry effective to derive a first derived quantity which is proportional to the first derivative of a varying magnitude electrical quantity supplied thereto, said circuitry further being effective to derive a second derived quantity which is proportional to the second derivative of said varying quantity, connection means connecting said circuitry to said input terminals for supplying said pulsating quantity thereto, said first derived quantity being a cosine function, said second derived quantity being a sine function so that said derived quantities and said maximum magnitude of said sine wave may be represented by the sides of a right triangle in which the two shorter sides are proportional in length to the magnitudes of said derived quantities and in which the length of the longest side is proportional to the max-

imum magnitude of said sine wave component, and trignometric triangle solving means energized by said derived quantities for solving said triangle to determine the length of said longest side of said triangle and thereby said maximum magnitude.

2. The combination of claim 1 in which at least one of said means includes multiplying means which multiplies its said derived quantity by a constant other than unity.

3. The combination of claim 2 in which said constant is a function of ω.

4. The combination of claim 1 in which said first means includes multiplying means which multiplies its said derived quantity by a quantity having the ratio $(1/\omega)$ to provide a third derived quantity and said second means includes multiplying means which multiplies its said derived quantity by a quantity having the ratio $(1/\omega)$ to provide a fourth derived quantity.

5. The combination of claim 4 in which said circuitry includes means squaring said third and fourth derived quantities, and means summing said squared quantities to provide an output quantity proportional to the square of said maximum magnitude of said sine wave component.

6. The combination of claim 1 in which said connecting means connects and disconnects said circuitry to said input terminals for brief intervals at first and second and third instants, said approximation of said first derivative being determined by the difference in magnitude of the pulsating quantity between said first and third instants, said approximation of said second derivative being determined by the difference in the rate of change of the magnitude of said pulsating quantity between said first and second instants and between said second and third instants divided by one half of the time interval between said first and said third instants.

7. The combination of claim 6 in which the first time interval between said first and said second instants is equal to the second time interval between said second and said third instants.

8. The combination of claim 7 in which said first and said second time intervals are equal to $(1/2\omega)$.

9. The combination of claim 8 in which the time of said brief intervals is in the order of magnitude of 10 nano-seconds.

10. The combination of claim 8 in which θ is an angle having an arc tangent determined by the ratio of one of said derived quantities to the other of said derived quantities, said circuitry including first ratioing means energized by said derived quantities and having an output quantity proportional to said ratio to determine said angle θ, and means determining a magnitude proportional to the cosine of said angle θ.

11. The combination of claim 10 in which said one derived quantity is the smaller of said derived quantities and said other derived quantity is the larger of said derived quantities.

12. The combination of claim 10 in which said circuitry provides said derived quantities as algebraic quantities of a plus and minus character, a first selected derived quantity of said derived quantities being plus when θ is in the 180° sector between minus 90° and plus 90° and being negative when θ is in the 180° sector between plus 90° and plus 270°, a second selected quantity of said derived quantities which is not said first selected quantity being plus when θ is in the 180° sector between 0° and 180° and being negative when θ is in the 180° sector between 180° and 360°.

13. The combination of claim 6 in which θ is an angle having an arc tangent determined by the ratio AA/BB and θ' is an angle having an arc tangent determined by the ratio BB/AA, where AA is proportional to said first derived quantity and BB is proportional to said second derived quantity, θ and θ' being the complementary angles of a right triangle, the two shorter sides of which are equal in magnitude to the magnitudes AA and BB and the longer side of which is proportional to the maximum magnitude of said sine wave component, said circuitry being operable to determine the angles θ and θ' by dividing the smaller of AA and BB as a numerator by the larger of AA and BB as the denominator whereby the arc tangent of the determined angle remains between zero and unity.

14. The combination of claim 13, in which said circuitry provides said derived quantities as algebraic quantities of a plus and minus character, a first selected derived quantity of said derived quantities being of plus sign when θ is in the 180° sector between minus 90° and plus 90° and being of negative sign when θ is in the 180° sector between plus 90° and plus 270°, a second selected derived quantity of said derived quantities and which said second selected quantity is not said first selected quantity being of plus sign when θ is in the 180° sector between 0° and 180° and being of negative sign when θ is in the 180° sector between 180° and 360°, said circuitry being effective to provide said ratios as quantities which provide a signal which distinguishes the algebraic quantities AA and BB as to its numerator and denominator location and as to relative signs thereof and as to the location of said signs whereby the arc tangent of θ is determined for the angles 0°–45° and 135°–225° and 315°–260° and the arc of θ' is determined for the angles 45°–135° and 225°–315°.

15. The combination of claim 1 in which there is provided second input terminals adapted to be energized by a second pulsating electrical quantity which has a second sine wave component having an angular frequency ω, said connecting means connecting said circuitry to said second input terminals for supplying said second pulsating quantity thereto, said connecting means being effective to connect said circuitry to said first input terminals at first three separate instants consecutively time spaced by first and second time intervals and to connect said circuitry to said second input terminals at second three separate instants consecutively time spaced by third and fourth time intervals, said circuitry being effective to provide said first derived quantity which is proportional to the difference in magnitude of said first electrical quantity between said first and third of said first three instants divided by the sum of said first and second time intervals and to provide said second derived quantity which is proportional to the change in magnitude of said first electrical quantity between said first and said second of said first three instants divided by said first time interval plus the change in magnitude of said first electrical quantity between said second and said third of said first three instants divided by said second time interval with the sum of the addendum being divided by one half the sum of said first and second time intervals, said circuitry being

effective to provide a third derived quantity which is proportional to the difference in magnitude of said second electrical quantity between said first and third of said second three instants divided by the sum of said third and fourth time intervals and to provide a fourth derived quantity which is proportional to the change in magnitude of said second electrical quantity between said first and second of said second three instants divided by said third time interval plus the change in magnitude of said second electrical quantity between said second and said third of said second three instants divided by said fourth time interval with the sum of the addendum being divided by one half the sum of said third and fourth timer intervals, said triangle solving means including means effective to divide as a numerator the smaller of said first and second derived quantities by the larger of said first and second derived quantities as a denominator to provide the arc tangent of a first angle and to divide as a numerator the smaller of said third and fourth derived quantities by the larger of said third and fourth derived quantities as a denominator to provide the arc tangent of a second angle, said circuitry being effective to provide a fifth quantity which is proportional to the cosine of said first angle and a sixth quantity which is proportional to the cosine of said second angle, said circuitry being effective to divide the product of said cosine of said second angle and the larger of said first and second derived quantities as the numerator by the product of said cosine of said first angle and the larger of said third and fourth derived quantities to provide a quantity proportional to the maximum value of said second sine component.

16. A distance relay for an alternating potential transmission line, said relay having a first pair of input terminals energized by the potential of said line and a second pair of input terminals energized by the current of said line, calculating circuit means, means periodically connecting said calculating means to said pairs of input terminals to sample said voltage and said current at desired time periods, said calculating means being effective to provide cosine ωt quantities which closely approach the first derivative of said voltage and of said current divided by ω where $\omega = 2\pi H_Z$ and t = time in seconds, said calculating means being effective to provide sine (ωt) quantities which closely approach the second derivative of said voltage and of said current divided by ω^2, said calculating means also being effective to divide said sine (ωt) voltage quantity by said cosine (ωt) voltage quantity and thereby determine the magnitude of said tangent (ωt) voltage quantity of a voltage right triangle and to divide said sin (ωt) current quantity by said cosine (ωt) current quantity and thereby determine the magnitude of said tangent (ωt) current quantity of a current right triangle, said calculating means being further effective to solve said right triangles and thereby determine the maximum values of the sinusoidal component of said voltage and of said current in said line, said calculating means still further being effective to determine the magnitude of the angle (ωt) of the voltage and of the current of said voltage and current samples.

17. The combination of claim 16 in which said calculating means is effective to divide said maximum value of said voltage by said maximum value of said current to provide a quantity equal to the apparent impedance of said line, fault determining means comparing the apparent magnitude of said apparent impedance determined from sequential said samples with a predetermined magnitude to determine the presence or absence of a fault within the reach of said relay.

18. The combination of claim 17 in which there is provided a counting means connected for actuation by said fault determining means, said fault determining means being effective to step said counting means each time said predetermined magnitude is greater than said apparent magnitude of said sample and to reset said counting means each time said predetermined magnitude is greater than said apparent magnitude of said sample, breaker trip means connected to said counting means, said counting means being effective to actuate said trip means solely at a count greater than unity.

19. The combination of claim 18 in which said calculating means is effective to determine the magnitude of the phase angle between said voltage and current, and means determining said predetermined magnitude as a function of said phase angle.

20. A controlling network of the character described, said network comprising, a number storage circuit having input and output connections, number supplying means connected to said storage input circuit and including a first gating means, said number supplying means being effective to supply a desired number having a first sign, a number adding circuit having first and second input circuits and an output circuit, second gating means connecting said storage output circuit to said first input circuit of said adding circuit, means for supplying add ends of both + and − signs to said second input circuit of said adding circuit and including a third gating means, fourth gating means connecting said output circuit of said adding circuit to said input connection of said storage circuit, a quantity determining circuit having an input and an output, fifth gating means connecting said output connection of said storage circuit to said input of said quantity determining circuit, and means connecting said output of said quantity determining circuit to said first gating means, said quantity determining means being effective when the number supplied to its said input is of said first sign and is of greater magnitude than said desired number to enable said first gating means to supply said desired number to said storage circuit.

21. The combination of claim 20 in which there is provided a counter, said counter having input and output circuit means, a sign determining means, having an input and an output, means connecting said input of said sign determining means to said storage circuit for energization of said sign means as a function of the sign of the number in said storage circuit, means connecting said output of said sign means to said counter, said sign means being effective each time the number supplied to said storage circuit is of a sign different from said first sign to supply a counting signal to said counter, said sign means being effective each time the number supplied to said storage circuit is of said first sign to supply a signal to reset said counter.

22. The combination of claim 21 in which said means which connects said sign means to said storage circuit includes a sixth gating means, and means opening said gating means in the order of said first gating means, said second gating means, said third gating means, said fourth gating means and said fifth gating means.

23. Apparatus for determining the maximum magnitude of the sine wave component having an angular frequency ω of a complex pulsating electrical quantity, said apparatus comprising, input terminal means adapted to have said electrical quantity applied thereto, sampling means connected to said terminal means for determining the instantaneous magnitude of said quantity during a predetermined desired time interval, conversion apparatus connected to said sampling means, said conversion apparatus including means measuring a first change of magnitude of said signal during a first time period and dividing said changed magnitude by said first time period to provide a first signal approximating the rate of change of said component, said conversion apparatus also including means measuring second and third changes of magnitude of said signal during second and third succeeding time periods and dividing said second changed magnitude by said second time period to provide a second signal and said third changed magnitude by said third time period to provide a third signal and thereafter dividing the difference in magnitude of said third and second signals by the average magnitude of said second and third time periods to provide a fourth signal approximating the rate of change of said first signal, said conversion apparatus further including signal means multiplying said first signal by the magnitude $(1/\omega)$ and said fourth signal by the magnitude $(1/\omega^2)$ and for thereafter adding together said multiplied and squared first and fourth signals to provide an output quantity having a fixed mathematical relationship with respect to the maximum magnitude of said sine wave component.

24. The combination of claim 23 in which each of said time intervals approach zero magnitude whereby said first signal more nearly becomes the first derivative of said component and said fourth signal more nearly becomes the second derivative of said component.

25. The combination of claim 24 in which said first time interval is coextensive with the time interval of said second and said third time interval.

26. The combination of claim 23 in which said first interval is equal to the total interval of said second time interval plus said third time interval and said first interval is coextensive with said second and said third intervals.

27. The combination of claim 26 in which said second time interval is equal to said third time intervals.

28. The combination of claim 27 in which said second and said third time intervals are equal to $(1/2\omega)$ and said first time interval is equal to $(1/\omega)$.

29. Apparatus for determining the maximum magnitude of the sine wave component having an angular frequency comprising input terminal means adapted to arc said electrical quantity applied thereto, first and second electrical conversion means, means connecting said first and second means to said input terminals for obtaining first and second samples of said quantity which occur during at least first and second selected time intervals, said first conversion means being energized by said first sample and being effective to determine an approximation of the first derivative of said first sample and to convert the same to a first output signal corresponding to the product of said approximated first derivative and $(1/\omega)$, said second electrical conversion means being energized by said second sample and being effective to determine an approximation of the second derivative to said second sample and to convert the same to a second output signal corresponding to the product of said approximated second derivative and $(-1/\omega^2)$, third electrical conversion means connected to said first and second conversion means for squaring each of said first and second output signals and thereafter adding said squared products to provide a third output quantity having a fixed mathematical relationship with respect to the maximum magnitude of said sine wave component.

30. The combination of claim 29 in which said first and said second time intervals are coextensive.

31. Apparatus for determining the maximum magnitude of the sine wave component of a complex alternating electrical quantity, having an angular velocity ω, said apparatus comprising input terminal means adapted to have said electrical quantity applied thereto, first electrical conversion means connected to said input terminals for determining an approximation of the first derivative of said quantity and converting same to a first output signal corresponding to the product of said approximated first derivative and $(1/\omega)$ second electrical conversion means connected to said input terminals for determining an approximation the second derivative of said quantity and converting same to a second output signal corresponding to the product of said approximated second derivative and $(-1/\omega^2)$, third electrical conversion means connected to said first and second conversion means for squaring each of said first and second output signals and thereafter adding said squared products to provide a third output quantity, said third output quantity having a fixed mathematical relationship with respect to the maximum magnitude of said sine wave component.

32. Apparatus for determining the impedance of an electrical circuit in which is present an alternating component of current and potential having an angular velocity ω, said apparatus comprising first input terminals adapted to be energized by the current component, second input terminals adapted to be energized by the potential component, mathematic circuitry connected to said first terminals and effective to derive a quantity which approximates the first derivative of said current component multiplied by $(1/\omega)$ and to derive a quantity which approximates the second derivative of said current component multiplied by $(-1/\omega^2)$, second mathematic circuitry connected to said second terminal means effective to derive a quantity which approximates the first derivative of said potential component multiplied by $(1/\omega)$ and to derive a quantity which approximates the second derivative of said potential component multiplied by $(-1/\omega^2)$, third circuitry connected to receive all of said signals and to derive a fifth quantity which approximates the magnitude of the impedance of said electric circuit as derived from said current and potential components.

33. The combination of claim 32 in which said third circuitry comprises first and second and third portions, said first portion being effective to provide a sixth output quantity which is proportional to the ratio of said first and second quantities, said second portions being effective to provide a seventh output quantity which is proportional to the ratio of said third and fourth quanti-

ties, said third portions being actuated by said sixth and seventh quantities to provide said fifth quantity.

34. The combination of claim **33** in which said third circuitry comprises a fourth portion including a plural number of groups of preselected signal generators, one of said output quantities being effective to select a desired one of said groups and the other of said output quantities being effective to select a desired one of said quantities of said selected group, said selected quantity of said selected group being effective to provide said fifth quantity.

35. The combination of claim **32** in which at least one of said mathematic circuitries includes a first switching apparatus and means measuring the magnitude of the quantity supplied thereto and connected to said first input terminals through said switching apparatus, said one circuitry also including timing means actuating said switching apparatus to connect said magnitude measuring means to its said first input terminals at at least first and second instants in the wave of said current component, said first circuitry also including means determining first rate at which said supplied quantity magnitudes changes during the period between said first and second instants and multiplying said first rate by $(1/\omega)$ to thereby provide said quantity which approximates said first derivative, said one circuitry further including means determining a second rate at which its said first rate changes during the period between said first and second instants and multiplying its said second rate by $(-1/\omega^2)$ to provide said quantity which approximates said derivative.

36. The combination of claim **35** in which said timing means actuates said switching to connect and disconnect said magnitude measuring means at said first and second instants and at a third instant intermediate said first and second instants, said first rate being determined by the change in value of said quantity during a first interval which occurs between said first and said third instants and a second interval which occurs between said third and said second instants, said second rate being determined by the change in said first rate between said intervals.

37. The combination of claim **36** in which said intervals are of duration equal to $(1/2\omega)$.

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